A Pulse-Width-Modulation Based Sliding Mode Controller for Buck Converters

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Abstract—This paper presents the design and analysis of a pulse-width-modulation based sliding mode voltage controller for buck converters from a circuit design perspective. A practical design approach which aims at systematizing the procedure for the selection of the control parameters is introduced. Additionally, a simple analog form of the controller for practical realization is provided. It is found that this controller adopts a structure similar to the conventional pulse-width-modulated voltage mode controller. Simulation and experimental results show that the response of the converter agrees with the theoretical design.

I. INTRODUCTION

Sliding mode (SM) controllers are well known for their robustness and stability. Most of the previously proposed SM controllers for switching power converters are hysteresis-modulation (HM) (or delta-modulation) based [1]–[6]. Naturally, they inherit the typical disadvantages of having variable-switching-frequency operation and being highly control sensitive to noise. Possible solutions are to incorporate constant timer circuits into the hysteretic SM controller to ensure constant switching frequency operation [5], or to use adaptive hysteresis band that varies with parameter changes to control and fixate the switching frequency [6]. However, these solutions require additional components and are unattractive for low cost voltage conversion applications.

An alternative solution to this is to change the modulation method of the SM controllers from HM to pulse-width-modulation (PWM). To the authors' knowledge, this concept was first published in [7]. The idea is based on the assumption that at a high switching frequency, the *control action* of a sliding mode controller is equivalent to the *duty cycle control action* of a PWM controller. Hence, the migration of a sliding mode controller from being HM based to PWM based is made possible. This proof was rigourously shown in a companion paper [8] by the same authors. However, the work presented is theoretical, and falls short of a practical consideration on its implementation.

In another paper [9], some possible practical methods of implementing a SM controller on buck type converters are described. Termed as the *indirect implementations of sliding mode control*, it is basically a straightforward circuit representation of the idea provided in [7]. Although the discussion in [9] gives a clear direction as to how such controllers may be developed, it provides only an overview of the PWM based SM controller.

Hence, in this paper, we present the design of a PWM based sliding mode voltage controlled (SMVC) buck converter, with emphasis on its practical and implementation details, from a circuit design perspective, using the theoretical groundwork established in [7] and [8]. In contrast to [7], the design of this controller at circuit level involves a different set of engineering difficulty and consideration. Additionally, we introduce a practical approach to the design and selection of the sliding coefficients of the controller. This approach systematizes the design procedure. It should be noted that it can also be employed for the design of other PWM based SM power converters. Finally, an analog form of the controller that is suitable for practical realization is provided. This controller can be easily implemented from the derived mathematical expressions with only a few operational amplifiers and analog ICs. Simulations and experiments are performed on the proposed converter to validate the theoretical design.

II. THEORETICAL DERIVATION

This section covers the theoretical aspects of the SMVC converter. A practical method of designing the sliding coefficients is also introduced.

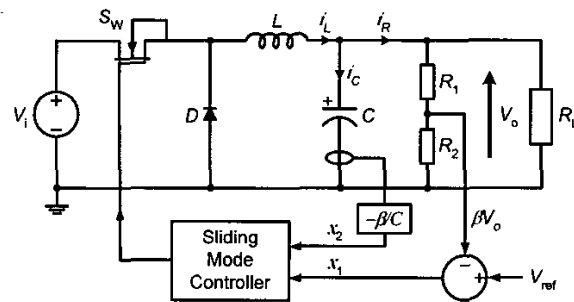### A. Mathematical Model of an Ideal Sliding Mode PID Voltage Controlled Buck Converter

Fig. 1. Basic structure of an SMVC buck converter system.

Fig. 1 shows an SMVC buck converter. Here, the *voltage error* x_1, the *voltage error dynamics* (or the rate of change of voltage error) x_2, and the *integral of voltage error* x_3, can be expressed as

$$
\begin{aligned}
x_1 &= V_{ref} - \beta V_o \\
x_2 &= \dot{x}_1 = \frac{\beta}{C}\left(\frac{V_o}{R_L} - \int \frac{uV_i - V_o}{L}dt\right) \\
x_3 &= \int x_1 dt
\end{aligned}
\tag{1}
$$

where C, L, and R_L are the capacitance, inductance, and load resistance respectively; V_{ref}, V_i, and βV_o are the reference, input, and sensed output voltage respectively; and $u = 1$ or 0 is the switching state of power switch S_W. Then, the state space model of the system can be derived as

$$\dot{x} = Ax + Bu + D \qquad (2)$$

where

$$A = \begin{bmatrix} 0 & 1 & 0 \\ -\frac{1}{LC} & -\frac{1}{R_L C} & 0 \\ 1 & 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ -\frac{\beta V_i}{LC} \\ 0 \end{bmatrix},$$

$$D = \begin{bmatrix} 0 \\ \frac{V_{ref}}{LC} \\ 0 \end{bmatrix}, \quad \text{and} \quad x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}.$$

The basic idea of SM control is to design a certain sliding surface in its control law that will direct the trajectory of the state variables towards a desired origin when coincided. For our system's model, it is appropriate to have a control law that adopts a switching function such as

$$u = \frac{1}{2}(1 + \text{sign}(S)) \qquad (3)$$

where S is the instantaneous state variable's trajectory, and is described as

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 = J^T x, \qquad (4)$$

with $J^T = [\alpha_1 \ \alpha_2 \ \alpha_3]$ and α_1, α_2, and α_3 representing the control parameters termed as sliding coefficients.

B. Stability Analysis in Circuit Terms

As in all other SM control schemes, the determination of the ranges of employable sliding coefficients for the SMVC converter must go through the process of analyzing the stability behavior of the controller/converter system using the Lyapunov's Direct Method [11]. This is performed by firstly combining (2), (3), and the time derivative of (4) to give

$$\dot{S} = J^T A x + \frac{1}{2}J^T B + \frac{1}{2}J^T B \ \text{sign}(S) + J^T D. \qquad (5)$$

Multiplying (5) by (4) gives the Lyapunov function candidate

$$S\dot{S} = S\left[J^T A x + \frac{1}{2}J^T B + \frac{1}{2}J^T B \ \text{sign}(S) + J^T D\right]$$

$$= S\left(J^T A x + \frac{1}{2}J^T B + J^T D\right) + \frac{1}{2}|S|J^T B. \qquad (6)$$

To achieve global reachability and asymptotic stability, the Lyapunov function is evaluated as $S\dot{S} < 0$, which can be written as

$$\begin{cases} \dot{S}_{S>0} = J^T A x + J^T B + J^T D < 0 \\ \dot{S}_{S<0} = J^T A x + J^T D > 0, \end{cases} \qquad (7)$$

i.e.,

$$J^T A x + J^T B + J^T D < 0 < J^T A x + J^T D \qquad (8)$$

or rearranged in scalar representation,

$$0 < LC\frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_o) - \beta L\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{R_L C}\right)i_C + \beta V_o < \beta V_i. \qquad (9)$$

where i_C is the capacitor current.

The above inequalities give the conditions for stability and provide a range of employable sliding coefficients. However, other than stability, no information relating the sliding coefficients to the converter performance is provided.

C. Stability Condition With Design Parameters Consideration

To alleviate the above problem, we propose to first tighten the design constraints by absorbing the actual operating parameters into the inequality. This is done by decomposing (9) into two sections of inequalities and considering them as individual cases with respect to the polarity of the capacitor current flow. Since in practice $\frac{\alpha_1}{\alpha_2} > \frac{1}{R_L C}$, the left inequality of (9) is implied by

$$0 < LC\frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_o) - \beta L\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{R_L C}\right)\left|\hat{i_C}\right| + \beta V_o, \qquad (10)$$

which can be rearranged to give

$$\frac{\alpha_1}{\alpha_2} < \frac{\beta V_o + LC\frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_o)}{\beta L\left|\hat{i_C}\right|} + \frac{1}{R_L C}, \qquad (11)$$

and the right inequality of (9) is implied by

$$LC\frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_o) + \beta L\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{R_L C}\right)\left|\hat{i_C}\right| + \beta V_o < \beta V_i \qquad (12)$$

which can be rearranged to give

$$\frac{\alpha_1}{\alpha_2} < \frac{\beta V_i}{\beta L\left|\hat{i_C}\right|} - \frac{\beta V_o + LC\frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_o)}{\beta L\left|\hat{i_C}\right|} + \frac{1}{R_L C}, \qquad (13)$$

where $\hat{i_C}$ is the peak magnitude of the bidirectional capacitor current flow. Next, equations (11) and (13) can be recombined and further tightened by considering the range of input and loading conditions of the converter to give

$$\begin{cases} \dfrac{\alpha_1}{\alpha_2} < \dfrac{V_o + LC\frac{\alpha_3}{\alpha_2}\left(\frac{V_{ref}}{\beta} - V_o\right)}{L\left|\hat{i_C}\right|} + \dfrac{1}{R_{L(max)}C} \\ \qquad \text{for } V_{i(min)} \geq 2\left[V_o + LC\frac{\alpha_3}{\alpha_2}\left(\frac{V_{ref}}{\beta} - V_o\right)\right] \\ \\ \dfrac{\alpha_1}{\alpha_2} < \dfrac{V_{i(min)}}{L\left|\hat{i_C}\right|} - \dfrac{V_o + LC\frac{\alpha_3}{\alpha_2}\left(\frac{V_{ref}}{\beta} - V_o\right)}{L\left|\hat{i_C}\right|} + \dfrac{1}{R_{L(max)}C} \\ \qquad \text{for } V_{i(min)} < 2\left[V_o + LC\frac{\alpha_3}{\alpha_2}\left(\frac{V_{ref}}{\beta} - V_o\right)\right] \end{cases} \qquad (14)$$

where $R_{L(max)}$ is the maximum load resistance and $V_{i(min)}$ is the minimum input voltage, which the converter is designed for. Additionally, the peak capacitor current $\left|\hat{i_C}\right|$ is the maximum inductor current ripple during steady state operation.

Theoretically, one may assume that at steady state operation, the actual output voltage V_o is ideally a pure DC waveform whose magnitude is equal to the desired output voltage $V_{od} \equiv \frac{V_{ref}}{\beta}$. However, this is not true in practice. Due to the limitation of finite switching frequency, there will always be some steady state DC error between V_o and V_{od}, even with the error-reducing integral controllers (i.e. PI, PID). It is important to take this error into consideration for the design of the

controller since the factor $LC\frac{\alpha_3}{\alpha_2}\left(\frac{V_{ref}}{\beta} - V_o\right)$ is relatively large in comparison to V_o.

Now, considering that

(a) in controllers with integral control function, the difference between V_o and V_{od} is small, and when optimally designed, is normally limited to a range of within ± 5 % of V_{od};

(b) for PWM based SMVC converters, the DC average of V_o is always lower than V_{od}; and

(C) the term $LC\frac{\alpha_3}{\alpha_2}$ is always positive,

we can rewrite the stability condition (14) for PWM based SMVC converter as

$$\begin{cases} \dfrac{\alpha_1}{\alpha_2} < \dfrac{0.95\ V_{od}}{L\left|\hat{i}_C\right|} + \dfrac{1}{R_{L(max)}C} \\ \qquad \text{for } V_{i(min)} \geq \left(1.95 + 0.05\ LC\frac{\alpha_3}{\alpha_2}\right)V_{od} \\ \\ \dfrac{\alpha_1}{\alpha_2} < \dfrac{V_{i(min)}}{L\left|\hat{i}_C\right|} - \dfrac{\left(1 + 0.05\ LC\frac{\alpha_3}{\alpha_2}\right)V_{od}}{L\left|\hat{i}_C\right|} + \dfrac{1}{R_{L(max)}C} \\ \qquad \text{for } V_{i(min)} < \left(1.95 + 0.05\ LC\frac{\alpha_3}{\alpha_2}\right)V_{od} \end{cases}$$

(15)

by substituting $V_o = 0.95\ V_{od}$ or $V_o = V_{od}$ into the appropriate parts. Thus, the control parameters α_1, α_2, and α_3 are now bounded by inequalities that have more stringent stability constraints than in (9).

D. Selection of Sliding Coefficients

Clearly, inequality (15) provides only the general stability information, but give no detail on the selection of the parameters. The equation relating sliding coefficients to the characteristic response of the converter during sliding mode operation can be easily found by substituting $S = 0$ into (4), i.e.,

$$\alpha_1 x_1 + \alpha_2 \frac{dx_1}{dt} + \alpha_3 \int x_1 dt = 0. \tag{16}$$

Rearranging the time differentiation of (16) into a standard second-order system form, we have

$$\frac{d^2 x_1}{dt^2} + 2\zeta\omega_n \frac{dx_1}{dt} + \omega_n^2 x_1 = 0 \tag{17}$$

where $\omega_n = \sqrt{\frac{\alpha_3}{\alpha_2}}$ is the undamped natural frequency and $\zeta = \frac{\alpha_1}{2\sqrt{\alpha_2\alpha_3}}$ is the damping ratio. Recall that there are three possible types of response in a linear second-order system: under-damped ($0 \leq \zeta < 1$), critically-damped ($\zeta = 1$), and over-damped ($\zeta > 1$). For ease of discussion, we choose to design the controller for critically-damped response[1], i.e.,

$$x_1(t) = (A_1 + A_2 t)e^{-\omega_n t}, \quad \text{for } t \geq 0 \tag{18}$$

where A_1 and A_2 are determined by the initial conditions of the system. In a critically-damped system, the bandwidth of the controller's response f_{BW} is

$$f_{BW} = \frac{\omega_n}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{\alpha_3}{\alpha_2}}. \tag{19}$$

[1]The design for an under-damped controller can be performed using a similar procedure as discussed hereafter.

By rearranging (19) and substituting $\zeta = 1$ into the damping ratio, the following design equations are obtained:

$$\frac{\alpha_1}{\alpha_2} = 4\pi f_{BW} \quad \text{and} \quad \frac{\alpha_3}{\alpha_2} = 4\pi^2 f_{BW}^2. \tag{20}$$

Thus, the design of the sliding coefficients is now dependent on the bandwidth of the desired frequency response in conjunction with the stability condition (15). Additionally, it is worth mentioning that the design equations in (20) for the SMVC controller are applicable to all other types of second order converters.

III. IMPLEMENTATION OF PWM BASED SMVC CONTROLLER

This section details the implementation of PWM based SMVC buck converter.

A. Derivation of PWM Control Law

It was previously derived in [8] that the control method [10] in sliding mode control is effectively a duty cycle control. From [10], the equivalent control input u_{eq} can be formulated by setting the time differentiation of (4) as $\dot{S} = 0$, i.e

$$J^T Ax + J^T B u_{eq} + J^T D = 0. \tag{21}$$

Now, solving for u yields

$$\begin{aligned} u_{eq} &= -\left[J^T B\right]^{-1} J^T \left[Ax + D\right] \\ &= \frac{LC}{\beta V_i}\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{R_L C}\right)x_2 + \frac{V_o}{V_i} + \frac{\alpha_3 LC}{\alpha_2 \beta V_i}x_1 \end{aligned} \tag{22}$$

where u_{eq} is continuous and $0 < u_{eq} < 1$. Substituting (22) into the inequality and multiplying by βV_i gives

$$0 < u_{eq}^* < \beta V_i \tag{23}$$

where

$$u_{eq}^* = \beta L\left(\frac{1}{R_L C} - \frac{\alpha_1}{\alpha_2}\right)i_C + \beta V_o + \frac{\alpha_3}{\alpha_2}LC\left(V_{ref} - \beta V_o\right) \tag{24}$$

which will provide the ideal average sliding motion on the manifold $S = 0$.

In terms of PWM based controlled system, the duty cycle D is expressed as

$$D = \frac{V_c}{\hat{V}_{ramp}} \tag{25}$$

where V_c is the control signal to the pulse-width modulator and $\hat{V}_{ramp}$ is the peak magnitude of the constant ramp signal. Since D is also continuous and bounded by $0 < D < 1$, it may also be written in the form

$$0 < V_c < \hat{V}_{ramp}. \tag{26}$$

Comparing the equivalent control and the duty ratio control [8], the following relationships can be established

$$V_c = u_{eq}^* \quad \text{and} \quad \hat{V}_{ramp} = \beta V_i \tag{27}$$

for the practical implementation of PWM based SMVC controller.
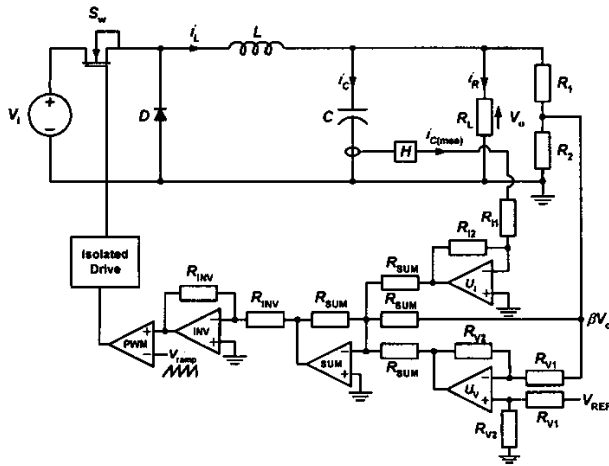
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Fig. 2.   Schematic diagram of the proposed PWM based SMVC buck converter.

B. Implementation of Controller

Fig. 2 shows the schematic diagram of the proposed PWM based SMVC buck converter. The controller design is based on (24) and (27). It basically adopts the structure of a voltage mode PWM controlled converter. Interestingly, this controller also inherits the *input feed-forward voltage control scheme* of conventional PWM voltage mode control in its operation since the input ramp signal $V_{\rm ramp}$ for modulation has peak magnitude that is proportional to the input voltage V_i (refer to (27)).

Briefly, the design of this controller can be summarized as follows: selection of the desired frequency response's bandwidth, calculation of the corresponding sliding coefficients using (20); inspection of the sliding coefficients's appropriateness using stability condition (15); and formulation of the control equations by substituting the calculated parameters into (24) and (27).

IV. SIMULATION AND EXPERIMENTAL RESULTS

TABLE 1
SPECIFICATION OF BUCK CONVERTER

Description	Parameter	Nominal Value
Input voltage	V_i	24 V
Capacitance	C	150 μF
Capacitor ESR	r_C	21 mΩ
Inductance	L	100 μH
Inductor resistance	r_L	0.12 Ω
Switching frequency	f_S	200 kHz
Minimum load resistance	$R_{\rm L(min)}$	3 Ω
Maximum load resistance	$R_{\rm L(max)}$	24 Ω
Desired output voltage	$V_{\rm od}$	12 V

The proposed design approach and analog controller for the PWM based SMVC buck converter are verified through simulation[2] and experiment. The specification of the converter is given in Table 1. The converter is designed to operate in

[2]The simulation is performed using Matlab/Simulink. The step size taken for all simulations is 10 ns.

continuous conduction mode for V_i = 18 V to 30 V and i_R = 0.5 A to 4 A. The calculated critical inductance is $L_{\rm crit}$ = 36 μH. The minimum required capacitance is $C_{\rm min}$ = 9 μF. The maximum allowable peak-to-peak ripple voltage is 50 mV.

To study the compliance of the design equations with the performance and its relationship with the transient response, the controller is designed for two different bandwidths: at one twentieth and at one tenth of the switching frequency f_S, i.e., $f_{\rm BW}$ = 10 kHz (i.e. first order response time constant $\tau_{\rm 10~kHz}$ = 15.915 μs) and $f_{\rm BW}$ = 20 kHz (i.e. $\tau_{\rm 20~kHz}$ = 7.956 μs). The controller is designed for maximum load current (i.e. minimum load resistance $R_{\rm L(min)}$)

A. Steady State Performance

Figs. 3 and 4 show the simulated (left) and experimental (right) waveforms during steady state operation, for the SMVC converter with the 20 kHz bandwidth controller operating at full load (i.e. $R_{\rm L}$ = 3 Ω). It can be seen that except for some ringing noise in the experimentally captured V_c and $\widetilde{V_o}$ waveforms, the simulated and experimental waveforms are in good agreement. The main difference is that for the simulation, output voltage ripple $\widetilde{V_o}$ ≈ ±4 mV (i.e. < 0.035 % of $V_{\rm od}$), and for the experiment, $\widetilde{V_o}$ ≈ ±8 mV (i.e. < 0.07 % of $V_{\rm od}$). This discrepancy is mainly due to the presence of parasitic resistance and equivalent series inductance (ESL) of the capacitor in the practical converter, which are not modeled in the simulation program.

Fig. 5 shows the corresponding set of experimental waveforms for the SMVC converter with the 10 kHz bandwidth controller operating at full load (i.e. $R_{\rm L}$ = 3 Ω). Except for V_c, there is no major difference between these waveforms and the experimental waveforms in Figs. 3 and 4. Due to the higher magnitude of the sliding coefficients, V_c of the 20 kHz bandwidth controller has a higher peak-to-peak value than V_c of the 10 kHz bandwidth controller.

B. Steady State DC Error at Different Loading Conditions

Fig. 6 shows a plot of the measured DC output voltage against the different operating load resistances. At full load operation (i.e. $R_{\rm L}$ = 3 Ω), the converter employing the 20 kHz bandwidth controller has a steady state DC output voltage of 11.661 V, which corresponds to a -2.825 % deviation from $V_{\rm od}$. The plot also shows that even though V_o increases with $R_{\rm L}$, V_o is always less than $V_{\rm od}$. This agrees with the previous assumption that the output voltage of PWM based system is always below the desired voltage. Furthermore, it also shows that the converter has satisfactory load regulation, having only a 0.151 V deviation in V_o for the entire load range of 3 $\Omega \leq R_{\rm L} \leq$ 24 Ω, i.e. the load regulation $\frac{dV_o}{dR_{\rm L}}$ is only 0.72 % from full load to minimum load.

For the converter employing the 10 kHz bandwidth controller, the steady state DC output voltage at full load operation is 11.633 V, which corresponds to a -3.058 % deviation from $V_{\rm od}$. For the entire load range of 3 $\Omega \leq R_{\rm L} \leq$ 24 Ω, V_o has a deviation of 0.189 V, i.e. the load regulation $\frac{dV_o}{dR_{\rm L}}$ is 0.90 % from full load to minimum load. Thus, it can be concluded that the 20 kHz bandwidth controller has better load variation property than the 10 kHz bandwidth controller.
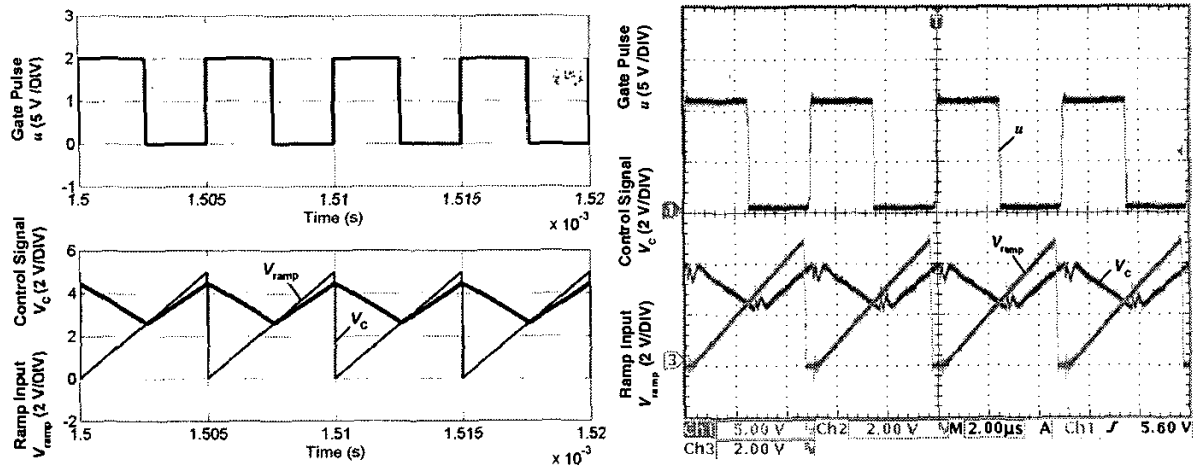
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Fig. 3. Simulated (left) and experimental (right) waveforms of control signal V_c, input ramp V_{ramp}, and generated gate pulse u for SMVC converter with the 20 kHz bandwidth controller operating at constant load resistance $R_L = 3 \ \Omega$.
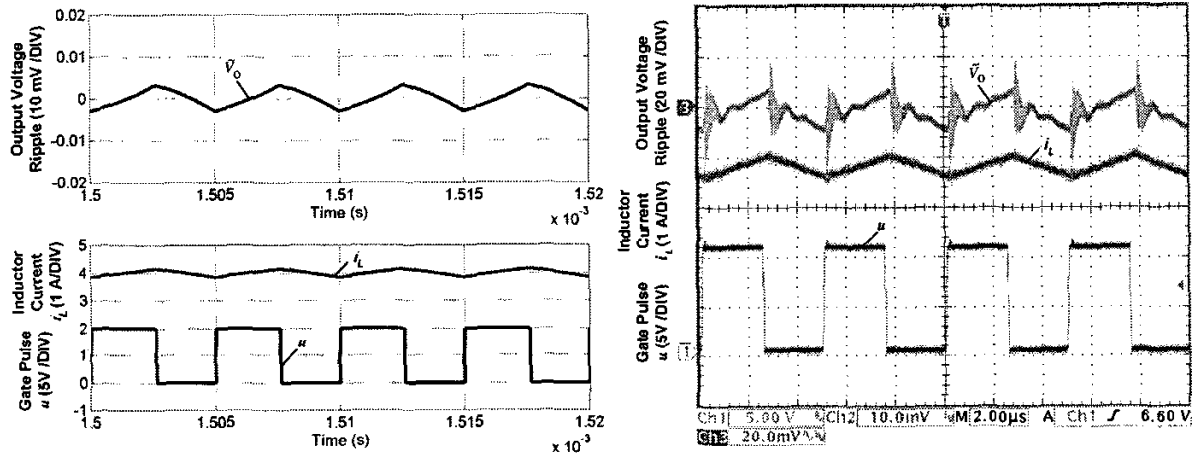

Fig. 4. Simulated (left) and experimental (right) waveforms of gate pulse u, and the corresponding inductor current i_L and output voltage ripple $\widetilde{V_o}$ for SMVC converter with the 20 kHz bandwidth controller operating at constant load resistance $R_L = 3 \ \Omega$.
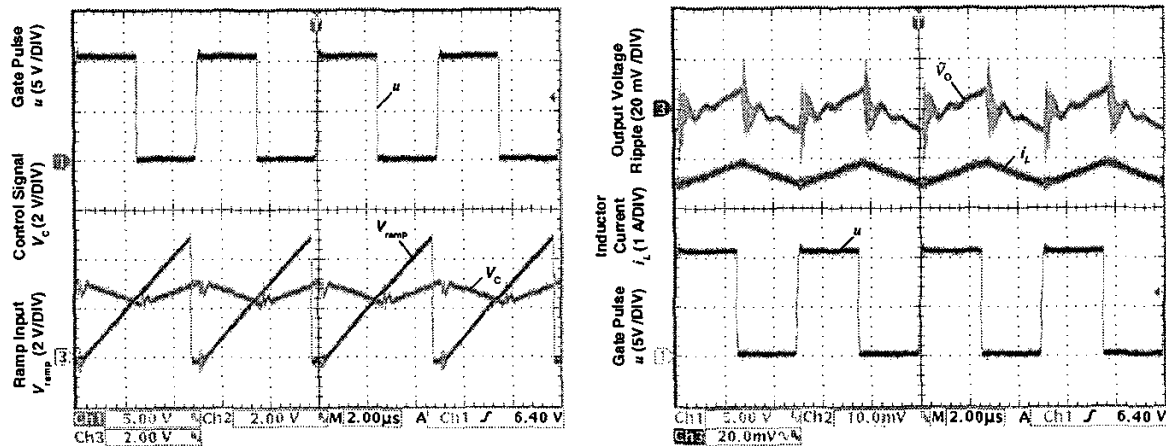

Fig. 5. Experimental waveforms of control signal V_c, input ramp V_{ramp}, and generated gate pulse u (left) and waveforms of gate pulse u, and the corresponding inductor current i_L and output voltage ripple $\widetilde{V_o}$ (right), for the SMVC converter with the 10 kHz bandwidth controller operating at load resistance $R_L = 3 \ \Omega$.
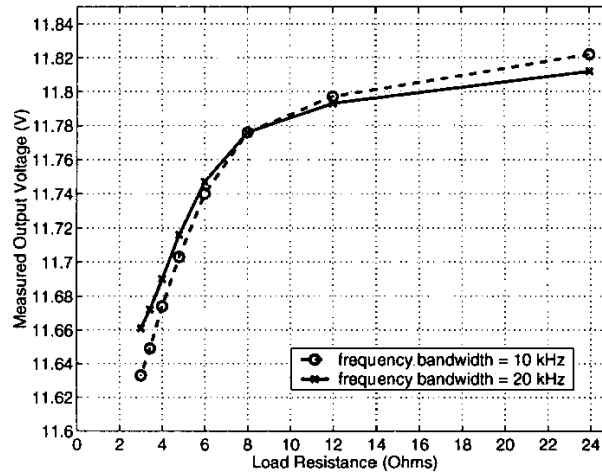
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Fig. 6. Plot of measured DC output voltage V_o against load resistance R_L for SMVC buck converter with both the 10 kHz and 20 kHz bandwidth controllers.
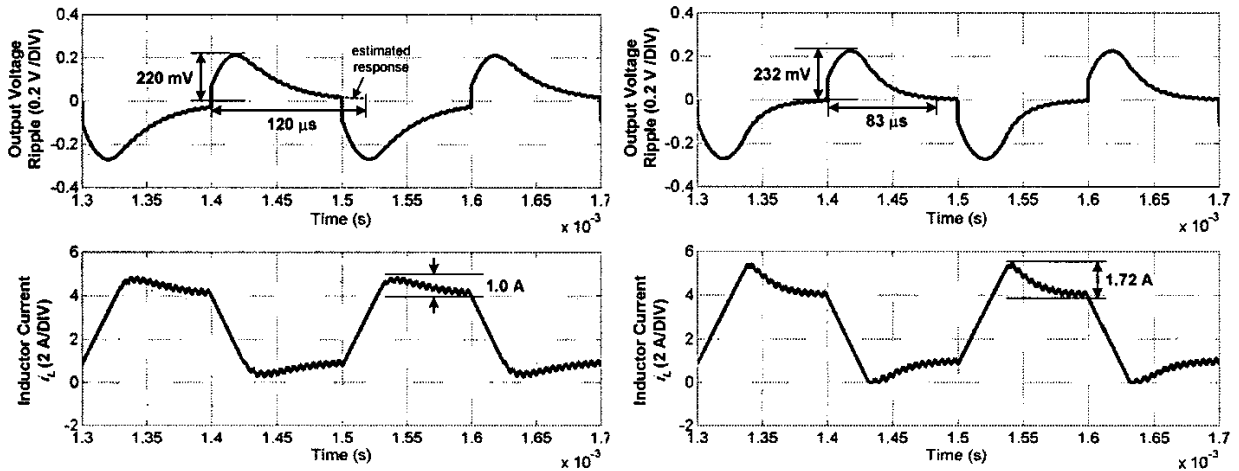

Fig. 7. Simulated waveforms of output voltage ripple $\widetilde{V_o}$ and inductor current i_L of the SMVC converter with the 10 kHz bandwidth controller (left) and the 20 kHz bandwidth controller (right), operating at 5 kHz step load change between $R_L = 3\ \Omega$ and $R_L = 12\ \Omega$.
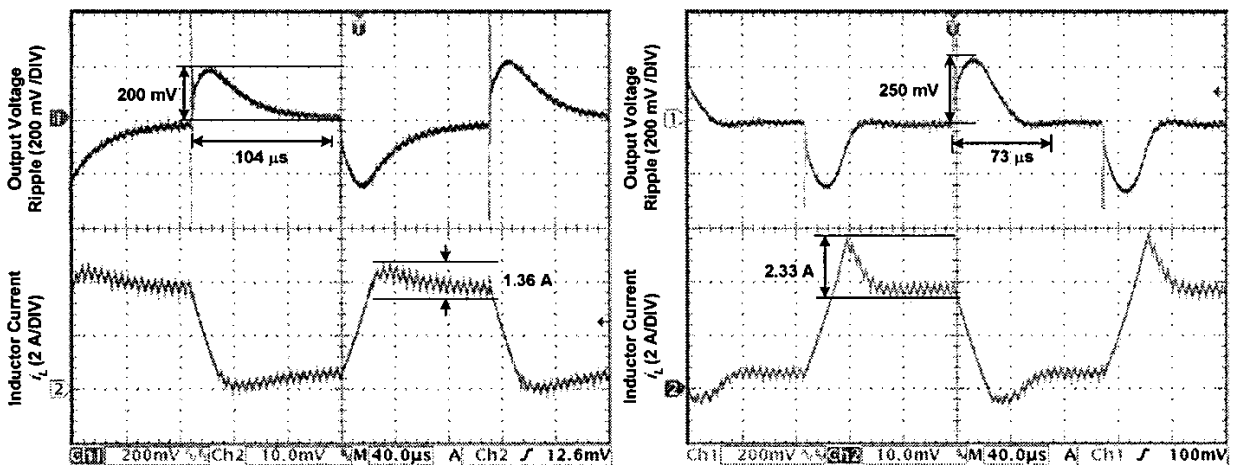

Fig. 8. Experimental waveforms of output voltage ripple $\widetilde{V_o}$ and inductor current i_L of the SMVC converter with the 10 kHz bandwidth controller (left) and the 20 kHz bandwidth controller (right), operating at 5 kHz step load change between $R_L = 3\ \Omega$ and $R_L = 12\ \Omega$.

C. Dynamic Performance

The dynamic performance of the controllers is studied using a load resistance that alternates between quarter load (12 Ω) and full load (3 Ω) at a constant frequency of 5 kHz. Figs. 7 and 8 show respectively the simulated and experimental output voltage ripple (top) and inductor current (bottom) waveforms of the converter for both the 10 kHz bandwidth controller (left) and the 20 kHz bandwidth controller (right). As illustrated in Fig. 7, the simulated output voltage has an overshoot ripple of 220 mV (1.83% of V_{od}) and a steady state settling time of 120 μs for the 10 kHz bandwidth controller, and an overshoot ripple of 232 mV (1.93% of V_{od}) and a steady state settling time of 83 μs for the 20 kHz bandwidth controller, during the load changes. As shown in Fig. 8, the output voltage has an overshoot ripple of 200 mV (1.67% of V_{od}) and a steady state settling time of 104 μs for the 10 kHz bandwidth controller, and an overshoot ripple of 250 mV (2.08% of V_{od}) and a steady state settling time of 73 μs for the 20 kHz bandwidth controller, during the load changes.

Furthermore, consistent with a critically-damped response, there is no ringing or oscillations in transience. However, it should also be mentioned that there are some slight dis-agreements between the experimental and simulation results in terms of the overshoot ripple magnitudes and the settling times. These are mainly due to the modeling imperfection of the simulation program, and the parameters' deviation of the actual experimental circuits from the simulation program due to the variation of the actual components used in the setup.

V. CONCLUSION

A PWM based SMVC buck converter is presented from a circuit design perspective. The description of the design methodology takes into account the different aspects of con-verter's operating conditions. A practical approach to the design of the sliding coefficients is also proposed in this paper. This approach uses an equation that is derived from analyzing the dynamic behavior of the converter during sliding mode operation, in addition to the stability conditions of the system.

An analog form of the controller is also presented. It is found that the PWM based SM controller adopts a similar structure to that of a conventional PWM voltage mode controller. The simulation and experimental results show that the response of the converter agrees with the theoretical design.

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