Hopf-Type Intermediate-Scale Bifurcation in Single-Stage Power-Factor-Correction Power Supplies

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***Abstract*— This paper reports intermediate-scale instability in a single-stage power-factor-correction (PFC) power supply that employs a cascade configuration of a boost stage operating in discontinuous conduction mode (DCM) and a forward stage operating in continuous conduction mode (CCM). The two stages combine into a single stage by sharing one main switch and one control loop to achieve input PFC and tight output regulation. Main results are given by "exact" cycle-by-cycle circuit simulations. The intermediate-scale instability usually manifests itself as local oscillations within a line cycle. Based on the stability analysis of a buck converter operating in CCM, the underlying mechanism of such instability can be attributed to the Hopf bifurcation occurred in CCM forward stage. Finally, experimental results are presented for verification purposes.**

I. Introduction

Nowadays, power factor correction (PFC) techniques have been widely used in switching power supplies to meet the increasingly stringent demand for very low line current harmonics [1], [2]. For low power applications (below 200 W), a preferred choice is the single-stage isolated power-factor-correction power supply (SSIPP), which was first proposed by Redl *et al.* [3]. This circuit consists of a PFC preregulator stage cascaded with an output stage for output voltage regulation. In the past decade [4], [5], much attention has been devoted to the steady-state design and control aspects of the SSIPP. However, the detailed dynamical behavior has seldom been investigated. Recently, the fast-scale period-doubling bifurcation has been observed in the SSIPP operating with DCM boost stage and DCM (or CCM) forward stage [6], [7]. Here, the fast-scale instability refers to instability that is observed in the time scale of switching frequency. On the other hand, bifurcation emerging from line-frequency orbit is also reported in PFC boost converter [8] and is referred to as slow-scale instability in this paper. In practice, the line frequency is much lower than the switching frequency. Thus, these two different time scales can be distinguished easily. In this paper, we report a totally different type of instability observed in the SSIPP with PFC boost preregulator operating in DCM and forward output regulator operating in CCM. The instability reported in this paper usually manifests itself as a local oscillation within a line cycle. Thus, it can also be regarded as the slow-scale instability with respect to switching frequency. To avoid confusion from the instabilities observed in other time scales, we comply with the convention on time scale given in the previous studies, and name the instability observed here as *intermediate-scale instability*. We further find that this instability is essentially caused by Hopf bifurcation of the forward output regulator.

II. System Description

The simplified schematic of the SSIPP under study is shown in its original form in Fig. 1 [3]. The front-end boost converter serves as a PFC converter whose output is connected across the storage capacitor C_1, which in turn serves as the input to a standard forward converter. Moreover, the boost PFC converter and the forward converter share the same active switch S, as shown in Fig. 1. Thus, this circuit can be modelled as a cascade connection of a boost converter and a buck converter, which are *driven synchronously* under one switching pulse-width-modulation (PWM) signal. The control of the circuit takes on the voltage feedback control, in which a control voltage $v_{\rm con}$ is compared with a ramp signal to generate a PWM signal to drive the switch. The ramp signal is given by

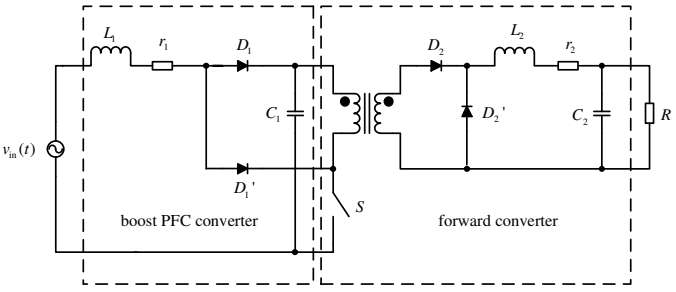

Fig. 1. The single-stage isolated PFC power supply (SSIPP) [3]. This circuit consists of a boost front-end PFC converter and a forward converter. Transformer isolation allows sharing of active switch by the two cascading stages [5]. For the sake of simplicity, the core reset arrangement is not shown in this figure.

$$V_{\rm ramp} = V_L + (V_U - V_L)(\frac{t}{T} \bmod 1) \qquad (1)$$

where V_L and V_U are the lower and upper thresholds of the ramp, and T is the switching period. The output of the comparator is 'high' when $v_{\rm con} > V_{\rm ramp}$, and is 'low' otherwise. Different from the proportional control used in Wu *et al.* [6] and [7], the control voltage $v_{\rm con}$ here is derived from a proportional-integral (PI) feedback control loop, which is more typical in industrial applications.

When the boost stage operates in DCM and the buck stage operates in CCM, three switch states are possible during a switching cycle:

State A : S is on, D_1' and D_2 are on, D_1 and D_2' are off;
State B : S is off, D_1 and D_2' are on, D_1' and D_2 are off;
State C : S is off, D_2' is on, D_1, D_1' and D_2 are off.

Typical current waveforms of the circuit operating with the above switching sequence are illustrated in Fig. 2.

III. Simulation Results

In this section, we will present the observed simulation results of the SSIPP. Our simulation is based on the exact piecewise switched

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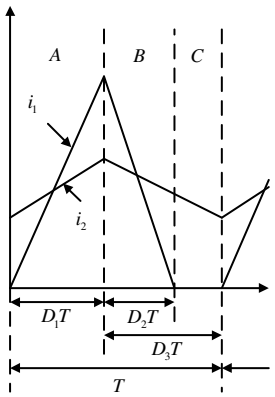


Fig. 2. Typical current waveforms of the SSIPP. The boost stage operates in DCM and the buck stage operates in CCM. The corresponding equivalent circuit presents a sequence of switch states as "ABC" in a switching cycle.

TABLE I

CIRCUIT PARAMETERS USED IN SIMULATIONS

Circuit Component	Values
Input Voltage $v_{\rm in}$	110 V ($V_{\rm in}$, rms), 50 Hz
Inductance L_1, ESR r_1	300 μH, 0.01 Ω
Inductance L_2, ESR r_2	3 mH, 0.01 Ω
Capacitance C_1	470 μF
Capacitance C_2	47 μF
Load Resistance R	15 Ω – 90 Ω
Expected Output Voltage $V_{\rm o}$	30 V
DC Gain of Controller K	0.04
Time Constant of Controller τ_F	1.5 T_0 ($T_0 = \sqrt{L_2C_2}$)
Ramp signal	3 V – 8 V, 20 kHZ

model described in the foregoing section.[1] Since practicing engineers are usually interested in the performance of SSIPP as the output power varies, we will accordingly observe the dynamical behaviors as the output power is changed. In our study, we will only change the load R and keep other circuit parameters fixed.[2] The circuit parameters used in our simulations are shown in Table I, in which the DC gain and time constant of PI controller are also included.

A. Stable operation

When the output power is high, e. g., 60 W, the SSIPP can work in stable operation. Fig. 3 (a) shows the time-domain waveforms of i_1 and $v_{\rm con}$. In order to see the change in dynamical behavior clearly, we collect the sampled peak values for i_1 and the corresponding values for v_C during each switching period in the steady state. Fig. 3 (b) shows the peak values of i_1 and Fig. 3 (c) shows the phase portrait of the peak values of i_1 and v_C.

B. Intermediate-scale instability

We now gradually increase the load resistance to obtain a lower output power. When the output power is adjusted below 48.1 W, we can clearly observe the occurrence of the intermediate-scale instability. Figs. 4 (a) to (c) show the corresponding waveforms and phase portraits at 45 W, from which the local oscillations of i_1 and $v_{\rm con}$ with about 7 period within one half line cycle can be readily recognized.

[1]The detailed expression of As and Bs corresponding to different switch state are not given for the limit of paper length.

[2]The output power equals $V_{\rm o}^2/R$, where $V_{\rm o}$ is the expected regulated output voltage in the steady state.

IV. ANALYSIS OF HOPF BIFURCATION

As shown in Fig. 4, the intermediate-scale instability usually manifests itself as local oscillations within a line cycle. Moreover, we can see that it is the oscillation of $v_{\rm con}$ that gives rise to the distortion in i_1. Thus, it is natural to pay specific attention to the underlying mechanism for the oscillation of $v_{\rm con}$. In this section, we will give some analytical results and study the relationship of the intermediate-scale instability with Hopf bifurcation.

In our study, the forward output regulator is designed to operate in CCM. As shown in Fig. 1, the input of the forward output regulator is the voltage v_C across the storage capacitor C_1. Usually, v_C is only crudely regulated by the boost PFC preregulator. If the capacitance of C_1 is sufficiently large, v_C at steady state can be approximately considered as the DC component V_C of v_C. An equation for V_C, which can be solved numerically, was given in [3] for the case of DCM regulating stage. For the system considered in our study, the equation regarding V_C can also be obtained in a similar way, and is given by

$$\int_0^{T_{\rm L}/2} \frac{v_{\rm in}^2}{V_C - v_{\rm in}} dt = \frac{L_1 T_{\rm L} V_C}{RT} \tag{2}$$

where $T_{\rm L}$ is the line period.

Moreover, as shown in Fig. 5, we can get an equivalent model of the regulating stage. For simplicity of analysis, we will neglect r_2, i.e., the ESR of L_2. Then, this model is essentially a voltage-mode controlled buck converter operating in CCM with input voltage V_C which can be obtained by numerically solving (2). Now, suppose that the intermediate-scale instability takes place in the overall SSIPP system. In this case, the corresponding buck model must also lose its stability, and the control voltage $v_{\rm con}$ will exhibit the similar oscillating waveforms shown in Fig. 4 (a).[3] Thus, we can conclude that the critical condition for the intermediate-scale instability of the overall SSIPP system is equivalent to that for Hopf bifurcation for the equivalent buck converter model of the regulating stage model shown in Fig. 5. Obviously, this conclusion reduces our study model from the complicated "SSIPP" form to a more simple "buck" form, which greatly simplifies the analysis process. To study the "low-frequency" Hopf bifurcation in the PI voltage-mode controlled buck converter, we can utilize the averaged model of the corresponding circuit, which has been successfully used to analyze Hopf bifurcation in Ćuk converter and parallel-connected boost converters [9], [10].

For the buck converter shown in Fig. 5, the averaged model can be represented by the averaged equations

$$\frac{di_2}{dt} = \frac{-v_{\rm o}}{L_2} + \frac{dV_C}{L_2} \tag{3}$$

$$\frac{dv_{\rm o}}{dt} = \frac{i_2}{C_2} - \frac{v_{\rm o}}{\tau} \tag{4}$$

$$\frac{dv_{\rm con}}{dt} = \frac{-Ki_2}{C_2} + (\frac{1}{\tau} - \frac{1}{\tau_F})Kv_{\rm o} + \frac{KV_{\rm ref}}{\tau_F}(1 + \frac{R_1}{R_2}) \tag{5}$$

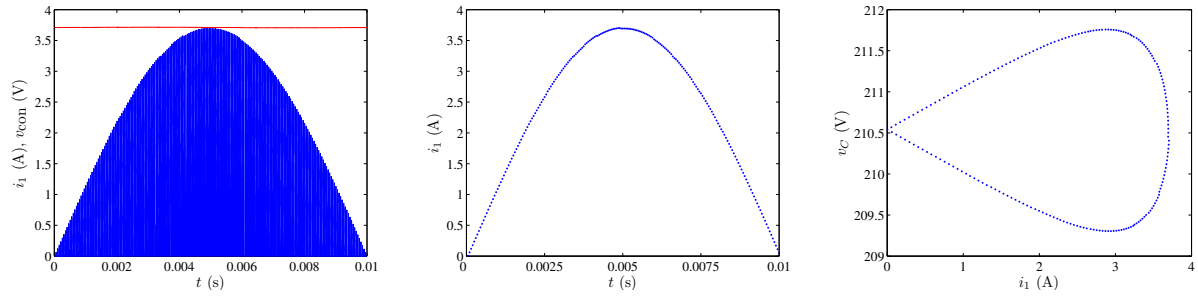
where $K = R_F/R_1$ and $\tau_F = R_F C_F$ are the DC gain and the time constant of the PI controller respectively, $\tau = RC_2$ and d is the duty cycle which is given by

$$d = \frac{v_{\rm con} - V_L}{V_U - V_L}. \tag{6}$$

The equilibrium point of the averaged equations can be calculated by setting all time-derivatives of (3)–(5) to zero and solving for i_2, $v_{\rm o}$ and $v_{\rm con}$. This gives the equilibrium point X_0 to be

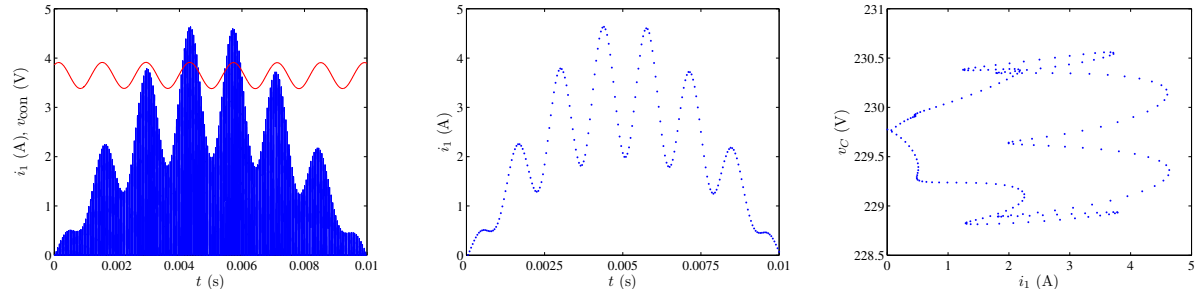
$$\begin{bmatrix} \frac{D_0 V_C}{R} \\ D_0 V_C \\ V_L + D_0(V_U - V_L) \end{bmatrix} \tag{7}$$

[3]Here, "the corresponding buck model" means that all parameters including V_C of the buck model are the same as those of the SSIPP system.



(a) (b) (c)

Fig. 3. Simulations at 60 W power. (a) Waveforms of i_1 and $v_{\rm con}$; (b) peak values of i_1 and (c) phase portrait of peak values of i_1 and v_C.



(a) (b) (c)

Fig. 4. Simulations at 45 W power. (a) Waveforms of i_1 and $v_{\rm con}$; (b) peak values of i_1 and (c) phase portrait of peak values of i_1 and v_C.

where

$$D_0 = \frac{V_{\rm ref}}{V_C}\left(1+\frac{R_1}{R_2}\right). \tag{8}$$

It is well-known that the stability of this equilibrium point is determined by the eigenvalues of the system's Jacobian at the equilibrium point. The standard procedure is to solve the following equation for λ:

$$\det[\lambda I - J(X_0)] = 0. \tag{9}$$

Upon expanding, we get

$$a_0\lambda^3 + a_1\lambda^2 + a_2\lambda + a_3 = 0 \tag{10}$$

where

$$a_0 = 1 \tag{11}$$

$$a_1 = \frac{1}{\tau} \tag{12}$$

$$a_2 = \frac{1}{L_2C_2} + \frac{KV_C}{L_2C_2(V_U - V_L)} \tag{13}$$

$$a_3 = \frac{KV_C}{L_2C_2\tau_F(V_U - V_L)}. \tag{14}$$

Then, the so-called *Routh Table* associated with the polynomial (10) can be constructed as

$$\begin{matrix} a_0 & a_2 \\ a_1 & a_3 \\ a_2 - \frac{a_0a_3}{a_1} & \\ a_3 & \end{matrix}. \tag{15}$$

Since $a_0 = 1$ in our case, (15) can be reduced to

$$\begin{matrix} 1 & a_2 \\ a_1 & a_3 \\ a_2 - \frac{a_3}{a_1} & \\ a_3 & \end{matrix}. \tag{16}$$

The Routh-Hurwitz criterion states that all of the roots of the polynomial (10) have real parts strictly less than zero if and only if all elements in the first column of the *Routh Table* are nonzero and have the same sign [11]. Since $a_i > 0$ $(i = 0, 1, 2, 3)$ here, applying the Routh-Hurwitz criterion, we can easily get the critical condition $a_1a_2 = a_3$ for the equilibrium point of the averaged equations. Substituting (12)–(14) into it, we can get the ultimate form of this critical condition as

$$K_C = \frac{\tau_F(V_U - V_L)}{V_C(\tau - \tau_F)} \tag{17}$$

The buck converter will lose its stability when $K > K_C$.

Strictly speaking, (17) does not give a formal condition for the occurrence of Hopf bifurcation. Hence, a further numerical check of the eigenvalues is required in order to confirm the occurrence of Hopf bifurcation. In our study, however, the analysis is based on the averaged model which will exclude any fast-scale bifurcation, e.g., period-doubling bifurcation. Therefore, we can assert that Hopf bifurcation must occur if the system loses stability when $K > K_C$. On the other hand, it implies that the critical condition is only valid when no other bifurcation has occurred prior to this predicted Hopf bifurcation.

Furthermore, we can also utilize (2) and (17) to obtain the operation boundary within which Hopf bifurcation does not occur. Fig. 6 shows such a stability boundary in the parameter space of output power versus K. For the purpose of comparison, we also present the stability boundary from circuit simulations, which clearly verifies the validity of (2) and (17) in locating the normal operating region.

V. Experimental Verifications

To verify the intermediate-scale instability observed in the simulations , an experimental circuit prototype of the SSIPP under study has been built. It should be noted that our emphasis here is the

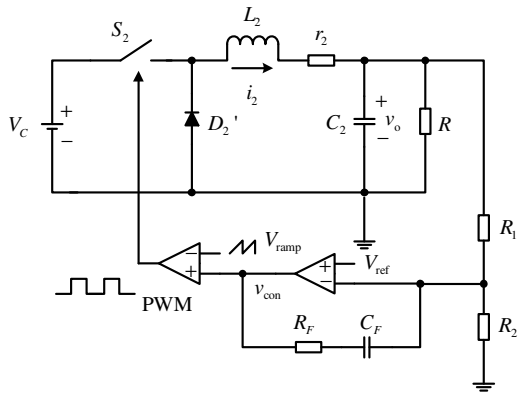


Fig. 5. Equivalent model of regulating stage.

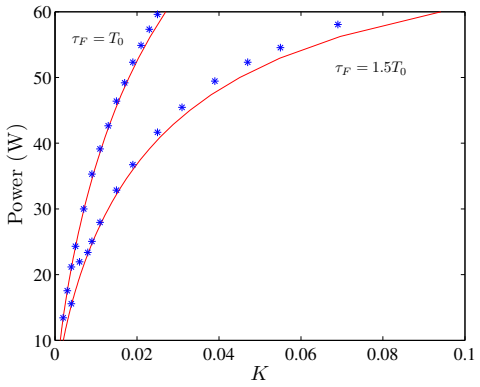


Fig. 6. Stability boundary in the parameter space of output power versus K. Here, $T_0 = \sqrt{L_2 C_2}$. The stable region is located above the boundary curve. The simulation results are indicated with $*$ and the analytical results are plotted with solid curves.

qualitative behavior of the intermediate-scale instability caused by Hopf bifurcation. Thus, the absolute verification of the specific set of simulation results given in the foregoing section is not mandatory. As a result, the parameters used in the experiment are different from those in simulations. Nonetheless, the experimental results clearly verify the phenomena observed from simulations.

Fig. 7 shows the measured waveforms of control voltage and the current of L_1, where the system works in stable operation. Fig. 8 presents the measured waveforms of control voltage and the current of L_1 when Hopf bifurcation take places. In this case, the seriously oscillating waveforms of the control voltage and the current of L_1 clearly shows the occurrence of Hopf bifurcation.

VI. Conclusion

In this paper, the intermediate-scale instability has been reported in an SSIPP operating with DCM boost stage and CCM forward stage. We have reported the results from "exact" cycle-by-cycle circuit simulations. Furthermore, we find that the instability reported here is essentially caused by Hopf bifurcation of the regulating forward stage. Finally, experimental results are also given to verify our observations made from simulations.

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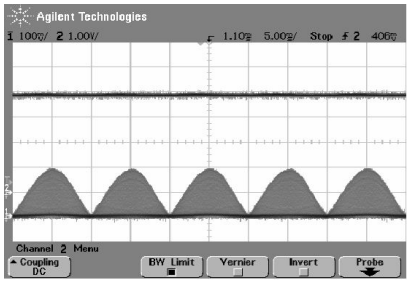

Fig. 7. Measured waveforms with current probe (10 mV/A) at time scale 5 ms/div. Upper trace: control voltage (1 V/div); lower trace: current of L_1 (100 mV/div).

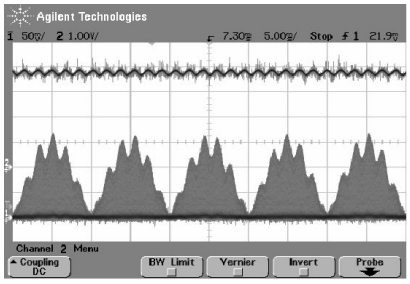

Fig. 8. Measured waveforms with current probe (10 mV/A) at time scale 5 ms/div. Upper trace: control voltage (1 V/div); lower trace: current of L_1 (50 mV/div).

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