Single-Stage Single-Switch Isolated PFC Regulator with Unity Power Factor, Fast Transient Response, and Low-Voltage Stress

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***Abstract*—In this paper, a simple control method is presented for a single-stage single-switch isolated power-factor-correction (PFC) regulator that can simultaneously achieve unity power factor and fast output voltage regulation while keeping the voltage stress of the storage capacitor low. The converter topology comprises essentially a cascade combination of a discontinuous-mode boost converter and a continuous-mode forward converter. The proposed control utilizes variation of both duty cycle and frequency. The role of varying the duty cycle is mainly to regulate the output voltage. Changing the frequency, moreover, can achieve unity power factor as well as low-voltage stress. Basically, the switching frequency is controlled such that it has a time periodic component superposed on top of a static value. While the time periodic component removes the harmonic contents of the input current, the static value is adjusted according to the load condition so as to maintain a sufficiently low-voltage stress across the storage capacitor. The theory is first presented which shows the possibility of meeting all three requirements using a combined duty cycle and frequency control. An experimental prototype circuit is presented to verify the controller's functions.**

***Index Terms*—Analog integrated circuits, power conversion harmonics, switched mode power supplies.**

I. Introduction

SINGLE-STAGE single-switch power-factor-correction (PFC) regulators typically take the form of a cascade combination of a discontinuous-mode PFC converter and a dc/dc converter, with the two converters sharing one single switch. The PFC converter relies on the discontinuous-mode (DCM) operation to provide high power factor, while the dc/dc converter can operate in either mode. Operating the dc/dc converter in DCM at constant frequency enjoys constant voltage stress of the storage capacitor irrespective of the magnitude of the output load [1], [2], but is generally less efficient due to higher current stress on the active switch. Moreover, harmonic distortions are still significant. On the other hand, operating the dc/dc converter in continuous mode (CCM), at the expense of a larger inductor, is usually more efficient at full load where the current stress is at its maximum and allows the use of frequency modulation to eliminate harmonic distortion of the PFC converter because the CCM dc/dc converter is insensitive to frequency variation [3]. However, in this case, the voltage stress in the storage capacitor varies with the load, and can take a rather high value under low-load conditions. To control the voltage stress, Jovanović *et al.* [4] proposed a frequency variation scheme which, however, made no attempt to reduce harmonic distortions. In this paper, we reexamine the single-stage single-switch isolated PFC converter, composing of a DCM boost converter and a CCM forward converter. Our purpose is to derive a combined duty cycle and frequency control method that can achieve "near" harmonic-free input current, fast transient response, as well as low-voltage stress.

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II. Overview of Circuit and Operation

A. Circuit Overview

The schematic diagram of a single-stage PFC regulator, consisting a cascade connection of a boost converter and a forward converter, is shown in Fig. 1. As in any PFC regulator, a storage element is required to buffer the difference between the instantaneous input power and the instantaneous output power. Capacitor C_s serves the purpose, presenting itself as the load of the boost converter and the source of the forward converter. The two converters share the same active switch S_1. The additional diode D_1 in the boost converter prevents the primary current of transformer T_1 from circulating through diode D_2. In this particular single-stage PFC regulator, it is assumed that the boost converter is operating in DCM, whereas the forward converter is operating in CCM. The charging current i_{D_2} of capacitor C_s is a rectified sinusoid which causes a ripple voltage to appear on the output voltage v_{C_s} of the boost converter. The amplitude of the ripple voltage would depend on the value of C_s and the input current of the forward converter. With a sufficiently large C_s, the ripple voltage can be kept to a small value compared to the dc component of v_{C_s}.

B. Output Voltage Regulation

In the steady state, v_{C_s} is essentially a dc voltage, denoted by V_{C_s}, by virtue of C_s being sufficiently large. The forward converter is designed to operate in CCM and, hence, is insensitive to frequency variation. The output voltage u can be expressed as

$$u = \frac{dV_{C_s}}{N}. \tag{1}$$

As a result, the output voltage regulation can be easily achieved by means of voltage-mode feedback which varies the duty cycle d of switch S_1 at either constant or variable

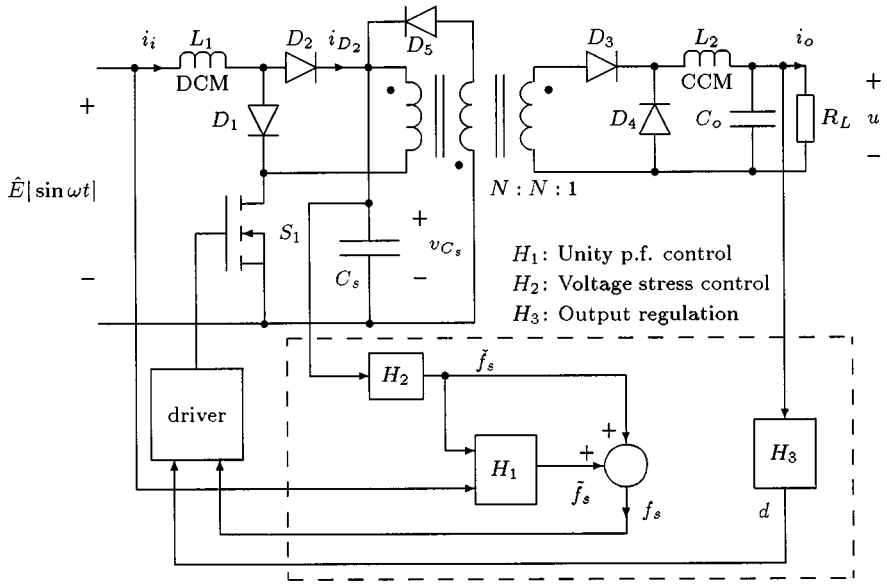

Fig. 1. Single-stage single-switch PFC regulator and the proposed control.

frequency. In addition, dynamics of the feedback control loop governs the load transient performance.

C. Unity Power Factor

Within a switching cycle, the waveforms of input current i_i of the boost converter and charging current i_{D_2} of C_s are shown in Fig. 2, where $1/f_s$ denotes the switching period, d/f_s denotes the on-time of switch S_1 and d'/f_s denotes the on-time of diode D_2. For the boost converter operating in discontinuous mode, we have

$$d' = \frac{\hat{E}|\sin\omega t|}{V_{C_s} - \hat{E}|\sin\omega t|}\, d < (1-d). \tag{2}$$

The averaged input current of the DCM boost converter is

$$\bar{i}_i = \frac{d^2}{2f_sL_1}\,\frac{1}{1-\dfrac{\hat{E}|\sin\omega t|}{V_{C_s}}}\,\hat{E}\sin\omega t. \tag{3}$$

Note that overbar (–) denotes averaged values over one switching cycle.

If the switching frequency f_s is adjusted according to [3]

$$f_s = \check{f}_s \frac{1}{1-\dfrac{\hat{E}|\sin\omega t|}{V_{C_s}}} \tag{4}$$

then the averaged input current becomes

$$\bar{i}_i = \frac{d^2}{2\check{f}_sL_1}\hat{E}|\sin\omega t|. \tag{5}$$

Since the duty cycle d is nearly constant within each half cycle of the ac mains, (5) indicates that the DCM boost converter is operating with unity power factor. In other words, provided the duty cycle is nearly constant, harmonic-free input current can be obtained by properly adjusting the switching frequency periodically with respect to the input-voltage-to-storage-capacitor-voltage ratio [6]. Usually, if the input voltage is varying at twice the mains frequency, so is the required switching frequency modulation.

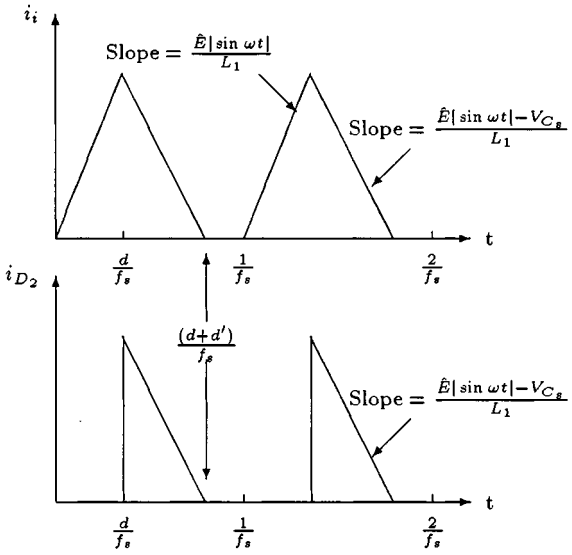

Fig. 2. Waveforms of i_i and i_{D_2}.

D. Capacitor Voltage Stress

With the output forward converter operating in continuous mode, a complete low-frequency averaged model for the single-stage PFC regulator can be obtained as shown in Fig. 3.

From Fig. 2, the averaged output current of the DCM boost converter is

$$\overline{i_{D_s}} = \frac{d^2}{2f_sL_1}\,\frac{\dfrac{\hat{E}|\sin\omega t|}{V_{C_s}}}{\dfrac{\hat{E}|\sin\omega t|}{V_{C_s}} - 1} \tag{6}$$

which is equal to the averaged charging current of capacitor C_s. The averaged discharging current of capacitor C_s is equal to the

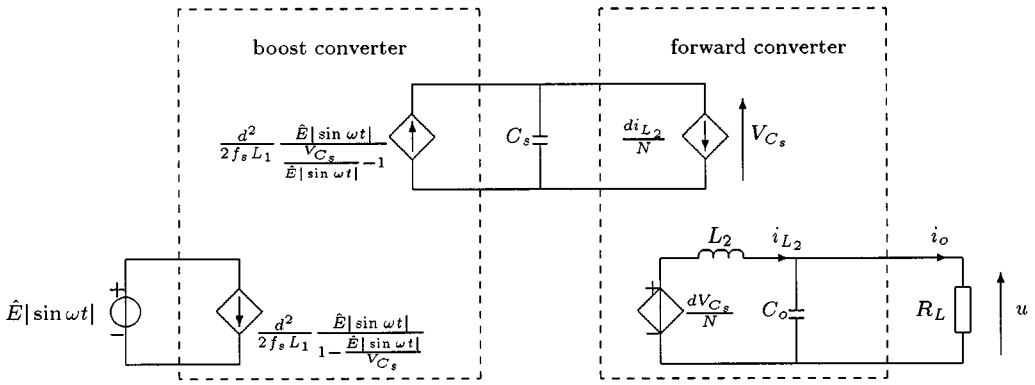

Fig. 3. Averaged behavior model of the PFC regulator.

averaged input current of the CCM forward converter which is di_o/N in the steady state.

The voltage stress V_{C_s} across C_s can be derived by equating the average values between the output current of the DCM boost converter and the input current of the CCM forward converter within a half cycle of the ac mains

$$\frac{\omega}{\pi}\int_0^{\pi/\omega}\frac{d^2}{2f_sL_1}\frac{\hat{E}|\sin\omega t|}{\frac{V_{C_s}}{\hat{E}|\sin\omega t|}-1}\,dt=\frac{\omega}{\pi}\int_0^{\pi/\omega}\frac{di_o}{N}\,dt. \quad (7)$$

The output current i_o of the CCM forward converter can be replaced by

$$i_o=\frac{dV_{C_s}}{NR_{L_{\text{eff}}}} \quad (8)$$

where $R_{L_{\text{eff}}}$ denotes the effective load resistance which includes various losses in the converters. In fact, $R_{L_{\text{eff}}}$ can be estimated as ηR_L where η is the efficiency of the converters with a specific output power level feeding a load resistance of R_L.

If f_s is adjusted according to (4), then the steady-state equation for V_{C_s} can be obtained as

$$V_{C_s}=\hat{E}\sqrt{\frac{N^2R_{L_{\text{eff}}}}{4\check{f}_sL_1}}. \quad (9)$$

From (9), the static voltage stress V_{C_s} varies with the loading condition and switching frequency. For different loading conditions, the voltage stress can be maintained at a constant value by adjusting the value of switching frequency $\check{f}_s$ via feedback [4].

E. Proposed Frequency Control

In order to achieve both low-voltage stress and harmonic-free input current operation, the frequency used to drive the switch should have a static load-dependent component which is varied only when load changes, and also a periodic, time dependent, component which is continuously generated to shape the input current. In short, denoting the static and periodic components by $\check{f}_s$ and $\tilde{f}_s$, respectively, we may write

$$f_s=\check{f}_s+\tilde{f}_s. \quad (10)$$

Moreover, for a DCM boost converter, it has been shown, according to (4), that in order to yield harmonic-free input current, the periodic component should be controlled in the following form:

$$\tilde{f}_s=H_1(t)\times\check{f}_s. \quad (11)$$

III. Controller Design

Referring to Fig. 4, the controller circuit is very similar to that of a pulsewidth modulation (PWM) controller using voltage-mode feedback control except that the oscillation frequency of the sawtooth oscillator is under feedback control for maintaining a more or less constant voltage stress on capacitor C_s and at the same time the oscillation frequency is also modulated under feedforward control with the input voltage for unity-power-factor operation. Hence, the switching frequency control can be divided into two units—unity-power-factor control unit and voltage stress control unit. At full load, the driver operates at the lowest switching frequency which is determined by I_0 feeding from the voltage stress control unit. Moreover, I_0 is modulated according to (4) by the unity-power-factor control unit which is essentially a current-mode product–quotient circuit based on the translinear circuit principle. At low load, V_{C_s} remains constant by feedback control on I_0 using the transconductance amplifier in the voltage stress control unit. The limit of the highest switching frequency, which occurs at low load, is determined by R_{limit}.

In practical implementation, the product–quotient, the transconductance amplifier, and the associated current mirror circuits can be fabricated as part of a PWM controller chip, and the required voltage rating of the controller is not affected by high values of $\hat{E}|\sin\omega t|$ and V_{C_s} since the corresponding inputs to the controller are clamped below V_+. Also the accuracy of the translinear circuit depends merely on the degree of matching between the transistors used. This matching

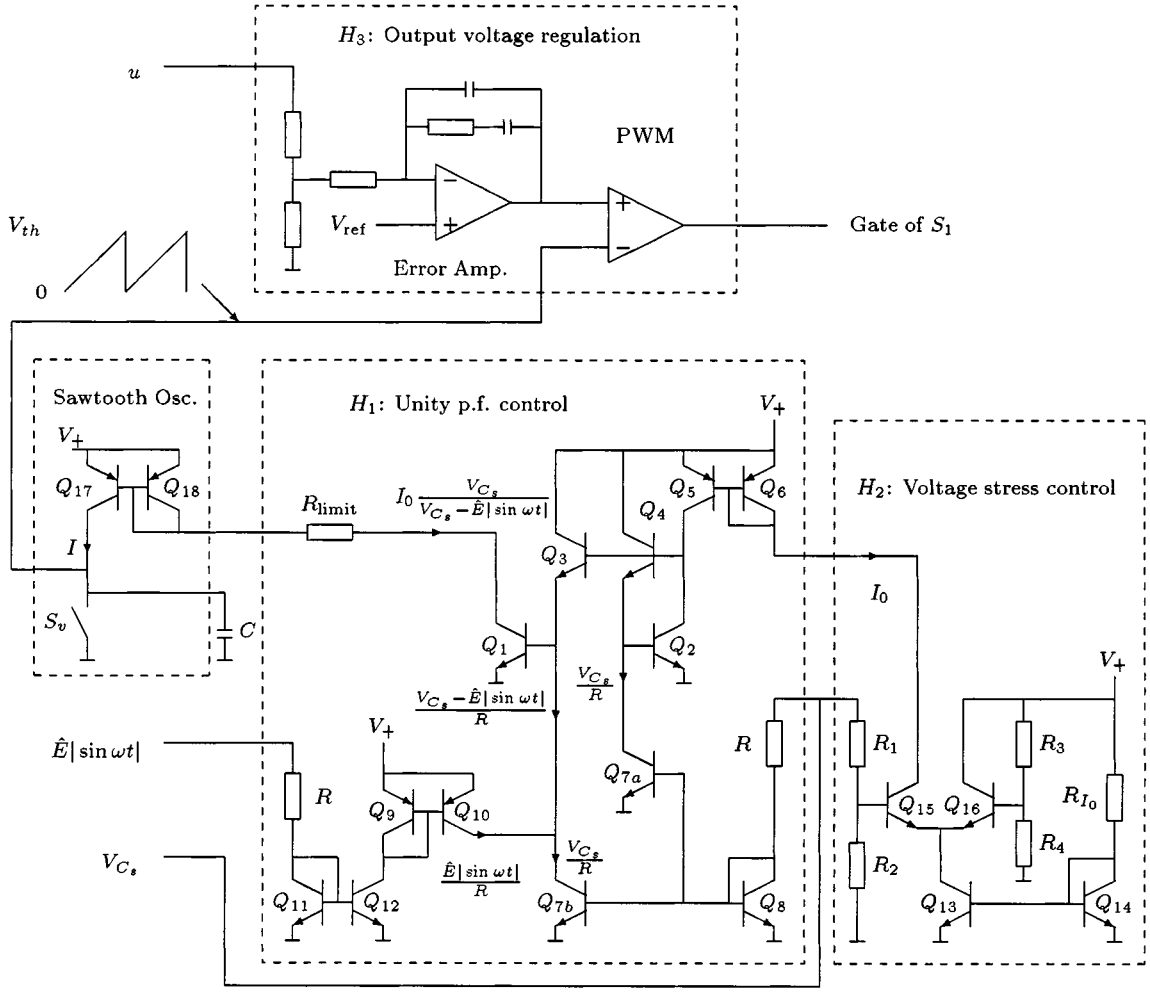

Fig. 4. Controller circuit for the proposed frequency control scheme.

requirement can be easily satisfied with currently available integrated circuit techniques.

A. Output Voltage Regulation

Referring to dashed box H_3 in Fig. 4, the output voltage regulation is achieved by generating suitable PWM waveform, i.e., duty-cycle control, by comparing the sawtooth waveform with the amplified feedback error voltage.

B. Sawtooth Oscillator

Referring to the dashed box marked with sawtooth osc. in Fig. 4, the current mirror formed by Q_{17} and Q_{18} provides a current I to charge up capacitor C. The value of I is usually adjusted with an external resistor by connecting the resistor between the collector of Q_{18} and the ground. When the capacitor voltage is equal to a threshold voltage, say V_{th}, switch S_v turns on and capacitor C is discharged. Immediately after the discharge, switch S_v turns off and capacitor C is charged up by current I again. The circuit oscillates with a frequency determined by the duration of the charging interval. Specifically

$$f_s = \frac{I}{CV_{th}}. \tag{12}$$

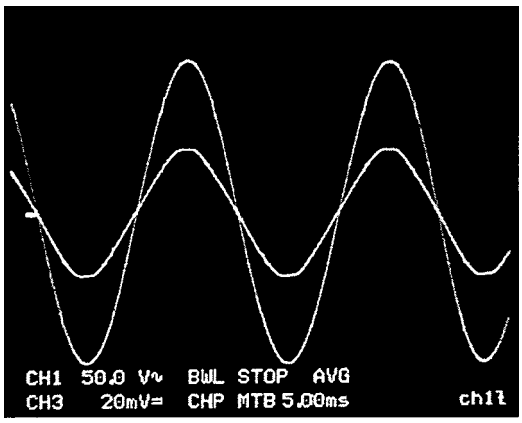

Fig. 5. Larger trace: input line-voltage waveform at 50 V/div. Smaller trace: input line-current waveform at 1 A/div with an output load of 6 A at 12 V.

If current I is controlled according to

$$I = I_0 \frac{V_{C_s}}{V_{C_s} - \hat{E}|\sin \omega t|} \tag{13}$$

TABLE I
SPECIFICATIONS AND COMPONENTS FOR THE SINGLE-STAGE PFC SWITCHING REGULATOR

Parameters	Components/Values
u	12 V
$\hat{E}$	110 $\times\sqrt{2}$ V
i_o	0.7 – 7.0 A
f_s	80 – 320 kHz
L_1	65 μH
L_2	71 μH
C_s	270 μF
C_o	1000 μF
D_1, D_2, D_5	MUR1560
D_3, D_4	MBR10100
S_1	IRF840
L_1 Core	Kool Mμ 77894-A7
L_1 Winding	29 T of 64×ϕ0.13 mm
L_2 Core	Kool Mμ 77930-A7
L_2 Winding	21 T of 64×ϕ0.13 mm
Transformer Core	TDK PC40
Transformer L_m	2 mH
Primary Winding	20 T of 48×ϕ0.13 mm
Reset Winding	20 T of 16×ϕ0.13 mm
Secondary Winding	4 T of 64×ϕ0.13 mm

then the condition of (4) is satisfied with

$$\check{f}_s = \frac{I_0}{CV_{th}}. \tag{14}$$

C. Translinear Circuit

Referring to dashed block H_1 in Fig. 4, the circuit is a translinear circuit which consists of a product–quotient circuit and five current mirrors. All transistors used are identical and have a high current gain such that their base currents are negligible compared to their collector currents. Furthermore, if two transistors have the same V_{BE} voltage, then their collector currents are equal in magnitude.

Referring to Fig. 4, Q_5 and Q_6 are connected as a current mirror to provide Q_2 a collector current of I_0. The value of I_0 is controlled by the voltage stress control unit shown as dash block marked with H_2 in Fig. 4.

In addition, Q_{7a} and Q_8 are connected as a current mirror to provide Q_4 with a collector current of V_{C_s}/R. Similarly, Q_{11} and Q_{12}, Q_9 and Q_{10}, and, Q_{7b} and Q_8 are connected as current mirrors to provide Q_3 with a collector current of $(V_{C_s} - \hat{E}|\sin \omega t|)/R$.

The product–quotient circuit is constructed with Q_1, Q_2, Q_3, and Q_4 in such a way that

$$V_{BE_1} + V_{BE_3} = V_{BE_2} + V_{BE_4}. \tag{15}$$

Based on the translinear circuit principle [5]

$$I_{C_1} I_{C_3} = I_{C_2} I_{C_4} \tag{16}$$

or

$$I_{C_1} = \frac{I_{C_2} I_{C_4}}{I_{C_3}}. \tag{17}$$

Hence, putting $I_{C_2} = I_0$, $I_{C_4} = V_{C_s}/R$, and $I_{C_3} = (V_{C_s} - \hat{E}|\sin \omega t|)/R$, we have

$$I_{C_1} = I_0 \frac{V_{C_s}}{V_{C_s} - \hat{E}|\sin \omega t|} \tag{18}$$

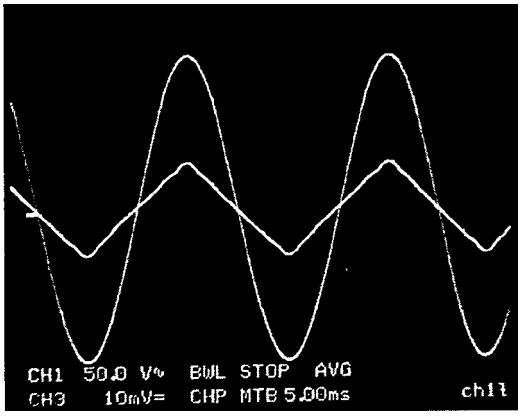

Fig. 6. Larger trace: input line-voltage waveform at 50 V/div. Smaller trace: input line-current waveform at 0.5 A/div with an output load of 2 A at 12 V.

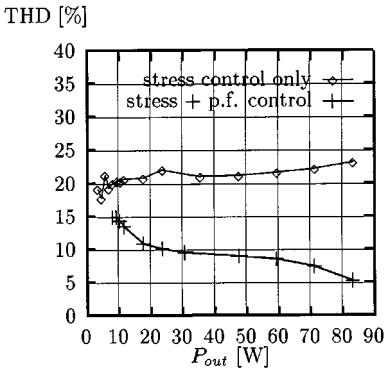

Fig. 7. Measured THD of the input line current with and without unity power factor control.

which exactly realizes (13). Finally, the required frequency control of (4) can be realized easily by mirroring I_{C_1} to the charging current I in the sawtooth oscillator block, as shown in Fig. 4. The maximum switching frequency $f_{s_{\max.}}$ occurs when I_{C_1} has its maximum value which can be easily set by resistor R_{limit}.

D. Transconductance Amplifier

Referring to dashed block H_2 in Fig. 4, the circuit is a transconductance amplifier which consists of a differential pair and a constant current source for biasing. Q_{15} and Q_{16} are connected as the differential pair and Q_{13} and Q_{14} are connected in a current mirror to act as the constant current source. The bias current for the differential pair is controlled by collector current $I_{C_{14}}$ which is given by

$$I_{C_{14}} \approx \frac{V_+}{R_{I_0}}. \tag{19}$$

The transconductance amplifier produces an output current I_0 feeding the unity-power-factor control unit. The magnitude of I_0 depends on the difference between the base voltages of the differential pair, the bias current is steered between the emitters of Q_{15} and Q_{16}. The value of capacitor voltage V_{C_s} is sampled through resistors R_1 and R_2 to the base of Q_{15} for feedback comparison, i.e.,

$$V_{B_{15}} = \frac{R_2}{R_1 + R_2} V_{C_s}. \tag{20}$$

TABLE II
MEASURED HARMONIC CURRENTS VERSUS EN REQUIREMENTS

Harmonic order n	Measured harmonic current[mA] @ $I_{\text{line}} = 0.9193$A	Extrapolated harmonic current [mA] @ $I_{\text{line}} = 16$ A	Maximum permissible current [mA] of EN 61000-3-2
3	59.1	1028	2300
5	12.8	223	1140
7	14.1	245	770
9	12.1	211	400
11	11.3	197	330
13	7.70	134	210
15	6.46	112	150
17	5.12	89	132
19	2.70	47	118
$21 \leq n \leq 39$	≤ 1.00	≤ 17.4	$150 \times \frac{15}{n}$

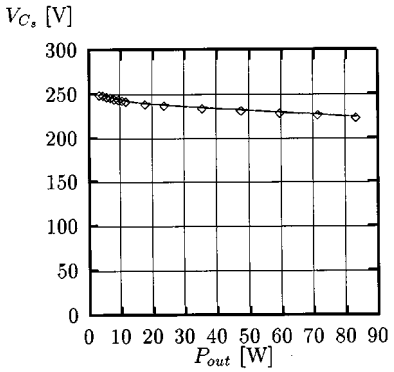

Fig. 8. Measured voltage stress on the storage capacitor against output power.

The base voltage of Q_{16} is biased with resistors R_3 and R_4

$$V_{B_{16}} = \frac{R_4}{R_3 + R_4} V_+ \tag{21}$$

which is fixed so that it can be used as the reference for comparing the change in V_{C_s}.

Under low-load condition, there is an increase in capacitor voltage V_{C_s} which reflects on the base voltage of Q_{15} according to (20). The change in base voltage of Q_{15} is converted into a corresponding change of current in I_0 according to the transconductance of the differential pair. Eventually, the load-dependent component of the switching frequency $\tilde{f}_s$ varies according to (14). Then the voltage stress can be kept at a constant value according to (9) if the amount of change in switching frequency $\tilde{f}_s$ can match with the amount of change in load $R_{L_{\text{eff}}}$. The maximum voltage stress V_{C_s} on the storage capacitor can be estimated by

$$V_{C_{s_{\text{maxi.}}}} \approx \frac{R_1 + R_2}{R_2} \left(\frac{R_4}{R_3 + R_3} V_+ + V_{BE} \right). \tag{22}$$

When the base voltage of Q_{15} is higher than that of Q_{16} by a V_{BE}, all the bias current is steered into the collector of Q_{14}. Therefore, $I_{C_{14}}$ sets the maximum collector current of Q_{15} feeding to the unity-power-factor control unit. In other words, resistor R_{I_0} is used to set the maximum value of I_0.

IV. EXPERIMENTAL VERIFICATION

A. Design Considerations

For maximum output power at full load, the regulator operates at lowest switching frequency. In order to achieve undistorted input current for unity-power-factor operation, the proposed power factor control scheme requires a threefold frequency variation in $\tilde{f}_s$ when $V_{C_s} = 234$ V and $\hat{E} = 110 \times \sqrt{2}$ V. At one-tenth load, the switching frequency must be increased to maintain a constant voltage stress. Assuming a full-load efficiency and one-tenth load efficiency of 85% and 34%, respectively, the proposed voltage stress control requires a fourfold frequency variation in $\tilde{f}_s$. Hence, if perfect unity power factor is also required at one-tenth load, an overall frequency variation of up to twelvefold is needed. Therefore, in practice, it is imperative to limit the extent of the power factor control at low-load condition in order to avoid excessive frequency variation. In other words, near-perfect unity power factor can be easily achieved near full load, while some degradation in the attainable power factor is expected at low load. In addition, a further increase in the range of frequency excursion is expected if the line input voltage varies from its nominal value. Therefore, this method may require an impractically large frequency variation if the regulator operates under a universal input voltage range.

B. Implementation

An 84-W experimental prototype has been built with the specifications and the components shown in Table I. The driver employed is UC3825 which provides output voltage regulation using voltage-mode feedback. The oscillation frequency of the sawtooth oscillator circuit in the driver is controlled by an external circuit which consists of the current-mode product–quotient circuit and the transconductance amplifier as shown in Fig. 4. The current-mode product–quotient circuit and the transconductance amplifier are implemented by transistors array CA3096 in the experiment.

C. Experimental Results

The input line-current waveforms at high load and low load are shown in Figs. 5 and 6. At full load, operating with lowest

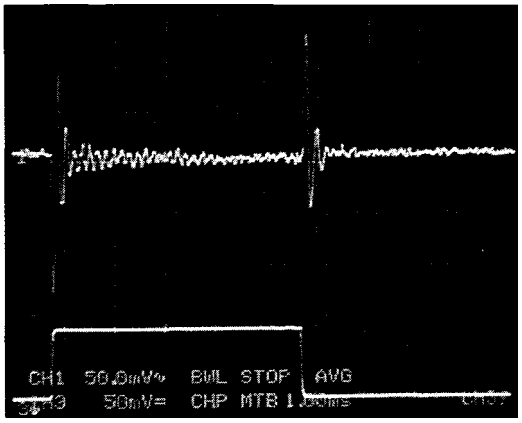

Fig. 9. Load transient performance from 2 to 6 A. Upper trace: output voltage waveform at 50 mV/div. Lower trace: output current waveform at 2.5 A/div. Time base: 1 ms/div.

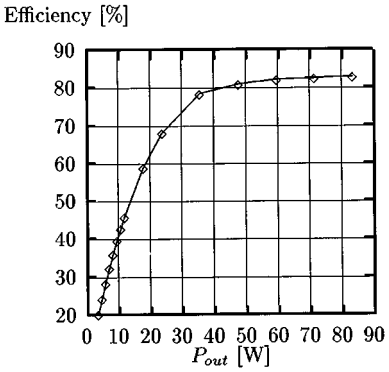

Fig. 10. The measured overall efficiency.

switching frequency, 80 kHz, the input line current is practically harmonic-free with a measured THD of 5.2% and power factor of 0.997. Distortion appears at low load due to the limit imposed on the maximum switching frequency, 320 kHz, by R_{limit} in the current-mode product–quotient circuit. THD performances with and without power factor control against output power are shown in Fig. 7. It is clear that the proposed periodic frequency modulation $\tilde{f}_s$ can provide a significant reduction, from 22.7% to 5.2%, in THD at full load, and, to a lesser extent, also at low load, e.g., at 1/3 load, from 21.9% to 10.0%.

We note that the European standard EN 61000-3-2 [7] specifies the maximum permissible harmonic current individually for each harmonic frequency and applies to equipment operated from 230 Vac with a maximum line current of 16 A. For evaluating the harmonic performance of the prototype, we tabulate the measured current harmonics and their extrapolated values at a line current of 16 A against the European standard in Table II. Under the proposed control scheme, the input line-current waveform remains the same for different input voltages provided that the input-voltage-to-storage-capacitor-voltage ratio is unchanged. Therefore, the extrapolation can be easily made by scaling the harmonic currents with the input line current. The results in Table II show that the proposed periodic frequency modulation $\tilde{f}_s$ can provide a sufficient margin in harmonics current reduction for complying the European standard even if the power level of the prototype is scaled up for a line current of 16 A.

The voltage stress on the storage capacitor against output power is shown in Fig. 8 which confirms the effectiveness of the stress control. The proposed load-dependent frequency variation $\check{f}_s$ can keep the capacitor voltage stress between 227–240 V for a change of loading from full load to one-tenth load. Hence, the maximum voltage stress across the active switch is kept under 480 V. It is clear that the voltage stress has to be scaled up accordingly if the regulator is designed to operate at a line voltage of 230 Vac. The load transient performance is shown in Fig. 9. The settling time of the output voltage is less than 0.5 ms for a change of load current from 2 to 6 A. The corresponding transient overshoot voltage is less than 1%. Finally, the measured overall efficiency is shown in Fig. 10. The efficiency of the regulator decreases rapidly when the regulator is operated at low-load condition. The low-efficiency performance is the price to pay for maintaining a low-voltage stress at low-load condition where the regulator is controlled to operate at highest switching frequency that generates higher switching loss.

V. Conclusion

This paper derives a practical control approach for achieving unity power factor, low-voltage stress and fast regulation, in a single-stage single-switch PFC regulator. The converter consists of a DCM boost converter cascaded with a CCM buck converter. Fast regulation is achieved by the usual duty-cycle modulation of the CCM buck converter which is insensitive to frequency variation. The control also utilizes frequency variation to eliminate harmonic distortions and to keep voltage stress low. The proposed control functions have been implemented with an external circuit incorporated with a conventional PWM driver with voltage-mode feedback regulation. The performance of the converter with the proposed control functions has been verified with experimental tests. The external circuit consisting of a current-mode product–quotient circuit and a transconductance amplifier could be easily incorporated into existing PWM circuit with custom analog integrated circuit (IC) technology.

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