Fast-Scale Instability of Single-Stage Power-Factor-Correction Power Supplies

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***Abstract*—This paper describes the fast-scale bifurcation phenomena of a single-stage power-factor-correction (PFC) power supply which is a cost effective design for low-power applications. The circuit employs a cascade configuration of a boost converter and a forward converter, which share an active switch and operate in discontinuous conduction mode, to provide input PFC and tight output regulation. Main results are illustrated by "exact" circuit simulations as well as theoretical analysis based on the use of Jacobians. This work provides a convenient means of predicting stability boundaries which can facilitate the selection of practical parameter values for maintaining stable operation.**

***Index Terms*—Bifurcation, dc–dc converter, instability, power factor correction (PFC), single-stage converter.**

I. Introduction

THE single-stage isolated power-factor-correction (PFC) power supply (SSIPP) proposed by Redl *et al.* [1] is a cost effective design solution for power supplies that are required to provide PFC and tight output regulation in the low-power range. The circuit basically employs a cascade structure consisting of a boost PFC converter and a forward converter for output regulation [1]. Being a single-stage converter, the SSIPP uses one active switch, as shown in Fig. 1, and hence mandatorily operates the PFC stage in discontinuous conduction mode (DCM) in order to allow the duty cycle control to be solely deployed for output regulation since the DCM boost converter can automatically achieve a good power factor without additional control [2], [3]. Furthermore, such an operating mode, as pointed in the Redl *et al.* proposal [1], avoids a variable voltage stress for the storage capacitor which sits between the two stages. Due to its practical versatility for low-power applications, this circuit has received a great deal of attention in the past decade [4]–[6]. However, previous studies have mainly focused on its steady-state design and control aspects, the detailed dynamical behavior and the stability boundaries have not been thoroughly pursued.

Recently, studies of the dynamical behavior of switching power converter circuits have revealed the possibilities of various kinds of bifurcation behavior, e.g., in pulsewidth-modulated (PWM) dc–dc converters [7]–[12], current-mode controlled dc–dc converters [13]–[15], thyristor and diode circuits [16], [17], free-running dc–dc converters [18], parallel-connected dc–dc converters [19], [20], general switching circuits [21], [22], etc. For the boost PFC preregulators operating in continuous conduction mode (CCM), it has been found that both fast-scale and slow-scale instabilities are possible [23]–[25]. However, similar problems in the DCM counterparts are known by practitioners but are not systematically explained and studied. Clearly, the slow-scale instability problem may worsen the harmonic distortion of the input current, whereas the fast-scale instability problem may impose higher current stresses on the switching devices. It has been observed that the peak current can increase by 10%–20% when fast-scale instabilities occur in some intervals of the mains cycle [24], [25]. Thus, the study of such instability problems has a practical motivation. See also Banerjee and Verghese [26] and Tse [27] for some surveys of the recent research in this area.

In this paper, we report fast-scale period-doubling bifurcation observed in the complete single-stage PFC power supply, in which both the PFC boost preregulator and the forward output regulator are designed to operate in DCM. In this paper, we will show that, with improper choice of system parameters, the converter can suffer from fast-scale instability for some intervals of time during the line cycle. This is important because line current distortions are often resulted from occasional instabilities that occur in some parts of the line cycle. Computer simulations based upon exact cycle-by-cycle system equations are presented in this paper. The extents to which fast-scale instability may occur are quantitatively measured and the parameters that affect fast-scale instability are identified. Analytical equations and design curves are derived from discrete-time models to facilitate the design of this type of power supplies to avoid fast-scale instability for all times.

II. System Description

The SSIP converter under study is shown in its original form in Fig. 1 [1]. The front-end boost converter serves as a PFC converter whose output is connected across the storage capacitor C_1, which in turn serves as the input to a standard forward converter. Moreover, the boost PFC converter and the forward converter share the same active switch S, as shown in Fig. 1. Thus, this circuit can be modeled as a cascade connection of a boost converter and a buck converter, which are *driven synchronously* under one switching PWM signal, as shown in Fig. 2 [3]. The control uses a simple PWM scheme, in which a control voltage

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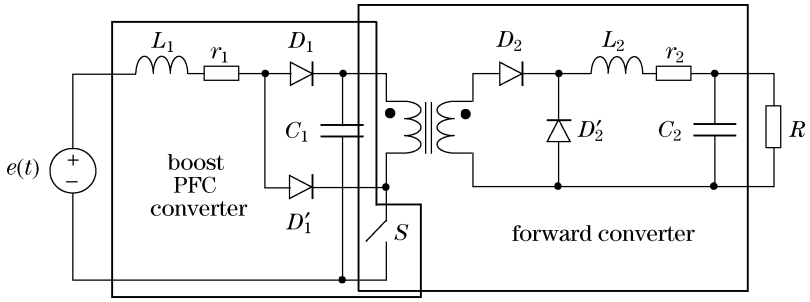

Fig. 1. The SSIPP [1]. This circuit consists of a boost front-end PFC converter and a forward converter. Transformer isolation allows sharing of active switch by the two cascading stages [5], [6]. For brevity, the core reset arrangement is omitted.

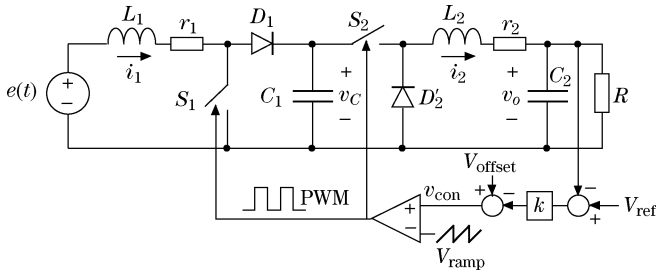

Fig. 2. Equivalent circuit model of the single-stage PFC power supply.

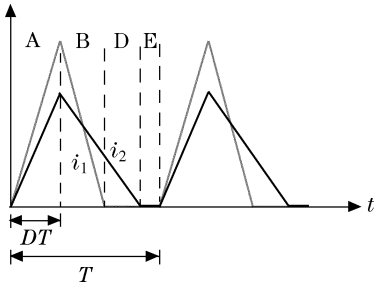

Fig. 3. Typical current waveforms of the single-stage PFC power supply. Both the boost and the buck stages operate in DCM.

v_{con} is compared with a sawtooth signal to generate a PWM signal to drive the switches. The sawtooth signal is given by

$$V_{\text{ramp}} = V_L + (V_U - V_L)\frac{t \bmod T}{T} \tag{1}$$

where V_L and V_U are the lower and upper voltage limits of V_{ramp}, and T is the switching period. The PWM signal is "high" when $v_{\text{con}} > V_{\text{ramp}}$, and is 'low' otherwise. The control voltage v_{con} is derived from a voltage feedback loop, i.e.,

$$v_{\text{con}} = V_{\text{offset}} - k(v_o - V_{\text{ref}}) \tag{2}$$

where V_{ref} is the reference output voltage, k is the feedback gain, and V_{offset} is a dc voltage that gives the required steady-state duty cycle, i.e., $V_{\text{offset}} = V_L + D(V_U - V_L)$.

When both the boost and the buck stages are working in DCM, five switch states are possible during a switching cycle:

State A: S_1 and S_2 are on, D_1 and D_2 are off;
State B: S_1 and S_2 are off, D_1 and D_2 are on;
State C: S_1 and S_2 are off, D_1 is on and D_2 is off;
State D: S_1 and S_2 are off, D_1 is off and D_2 is on;
State E: S_1 and S_2 are off, D_1 and D_2 are off.

It is worth noting that the sequence of switch states, in general, takes the order as written above. However, either State C or State D (not both) goes in the middle because exact synchronous switching of the diodes is not possible in practice. For simplicity in our study, we will omit State C, assuming that the buck stage has a relatively larger inductance. Typical current waveforms are illustrated in Fig. 3. Note that the choice between omitting State C or D must be consistent with the choice of parameters, which can be easily verified by simulations. Nonetheless, such a choice is arbitrary and does not affect the analysis.

During the off-time of each diode, the circuit state is constrained to lie in the space defined by the zero value of the corresponding current. Thus, i_1 can be ignored for State D, and both i_1 and i_2 can be ignored for State E. Then, according to the circuit topology in each switch state, we can write the state equations as follows:

$$\begin{cases} \dot{x} = A_1 x + Be(t), & \text{for State A} \\ \dot{x} = A_2 x + Be(t), & \text{for State B} \\ \dot{y} = A_3 y, & \text{for State D} \\ \dot{v} = A_4 v, & \text{for State E} \end{cases} \tag{3}$$

where $e(t)$ is the input voltage, the state vectors are defined as $x = [i_1\ v_C\ i_2\ v_o]^T$, $y = [v_C\ i_2\ v_o]^T$, and $v = [v_C\ v_o]^T$, and the system matrices for this converter are

$$A_1 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1} & 0 \\ 0 & \frac{1}{L_2} & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \tag{4}$$

$$A_2 = \begin{bmatrix} -\frac{r_1}{L_1} & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \tag{5}$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \tag{6}$$

$$A_4 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C_2 R} \end{bmatrix} \tag{7}$$

$$B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{8}$$

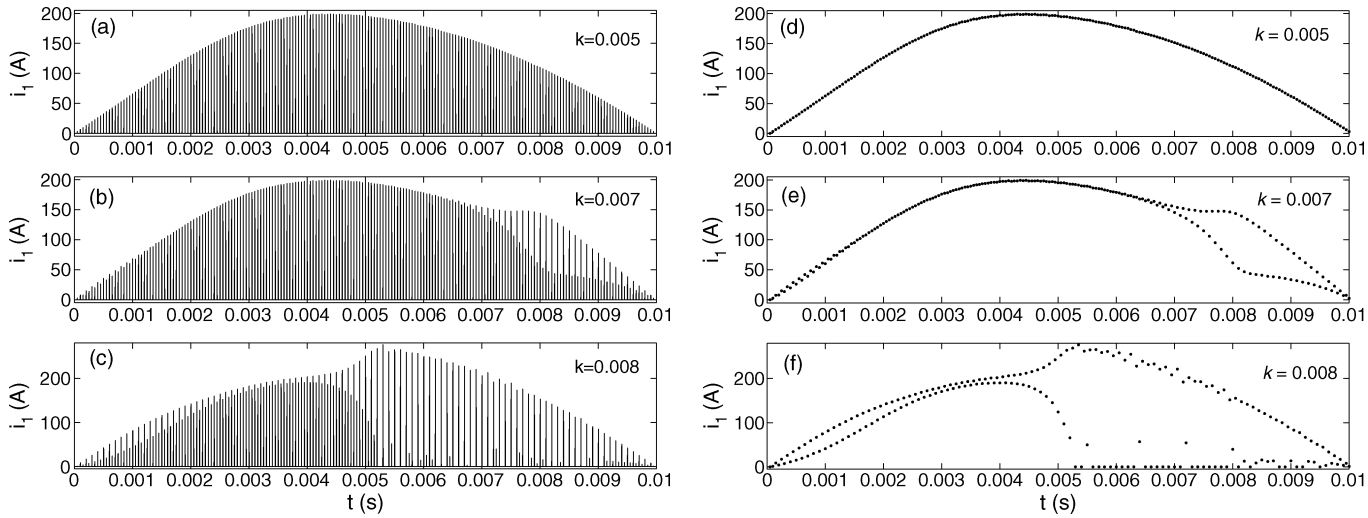

Fig. 4. (a)–(c) Time-domain waveforms and (d)–(f) sampled-data waveforms of i_1 for $C_1 = 100$ μF, $V_C = 349$ V and $V_{\rm ref} = 80$ V. The sampled-data waveforms are obtained by sampling the peak values of the waveforms and hence indicate the instantaneous current stress.

TABLE I
COMPONENT VALUES USED IN SIMULATIONS

Circuit Components	Values
Switching Period T	50 μs
Input Voltage	110 V rms, 50 Hz
Inductance L_1, ESR r_1	2 μH, 0.01 Ω
Inductance L_2, ESR r_2	10 μH, 0.01 Ω
Capacitance C_1	10-100 μF
Capacitance C_2	34 μF
Load Resistance R	10 Ω

where all component symbols are as defined in the circuit diagram shown in Fig. 2.

III. COMPUTER SIMULATION STUDY

In this section, we begin with a series of computer simulations to identify possible bifurcation phenomena. Since we are primarily concerned with system stability in relation to the reference output voltage $V_{\rm ref}$ and the feedback gain k, we will focus on variation of these two parameters. Our simulation is based on the state equations derived in the foregoing section. Essentially, for each set of parameter values, time-domain cycle-by-cycle waveforms are generated by solving the appropriate linear equation in a sub-interval of time, according to different switching states. After the transient period, we capture the steady-state time-domain waveforms. The circuit component values used are listed in Table I.

For a certain range of parameters, fast-scale instability may occur within a line cycle. Such instability manifests itself as a period-doubling bifurcation at the switching frequency.

A. Simulation Results for Relatively Large Storage Capacitance

We begin with a relatively large value of capacitance for C_1. We generally observe that fast-scale instability occurs near the two ends of a half line cycle, as shown in Fig. 4 for different values of the feedback gain k for $C_1 = 100$ μF. Fig. 4(a) shows the stable operation with $k = 0.005$. Fig. 4(b) shows bifurcation in some intervals of the line cycle with $k = 0.007$. Fig. 4(c) shows fast-scale instability in the whole line cycle with $k = 0.008$. Specifically, period doublings at the switching period occurs at some phase angle of the line cycle and instability grows toward the zero-crossings of the line cycle. In order to observe the change in dynamical behavior clearly, we collect the sampled peak values for i_1 and i_2 during each switching period in the steady state, and the corresponding sampled values for v_C and v_o. Fig. 4(d)–(f) shows the corresponding sampled-data waveforms of Fig. 4(a)–(c). Period-doubling bifurcations are clearly observed. Fig. 5 shows the corresponding phase portraits of the sampled input current i_1 and voltage v_C.

Of engineering importance is the existence (and location) of the critical bifurcation points along the line cycle as it affects the peak current value of the input current and hence the current stress on the switch. We denote the two critical points in terms of phase angle $\theta_{c1} = \omega t_1$ and $\theta_{c2} = \omega t_2$, where ω is the line angular frequency. Fig. 6 plots the two critical phase angles θ_{c1} and θ_{c2} as functions of the feedback gain k and $V_{\rm ref}$. Here, we observe that the converter fails to maintain the expected stability operation in intervals corresponding to $\theta < \theta_{c1}$ and $\theta > \theta_{c2}$.

Furthermore, for a certain reference output voltage $V_{\rm ref}$, there is a critical value of feedback gain k_c, above which the operation has regions of fast-scale instability. Likewise, for a given feedback gain k, there is a critical reference output voltage $V_{\rm ref_c}$, below which the operation has regions of fast-scale instability. Consequently, these critical parameter values define a stability boundary dividing the parameter space of the feedback gain and the reference output voltage, as shown in Fig. 7.

B. Simulation Results for Relatively Small Storage Capacitance

We now examine the system when the capacitance C_1 is relatively small. We observe that, unlike in the case for large C_1, fast-scale instability grows in the middle of a half line cycle,

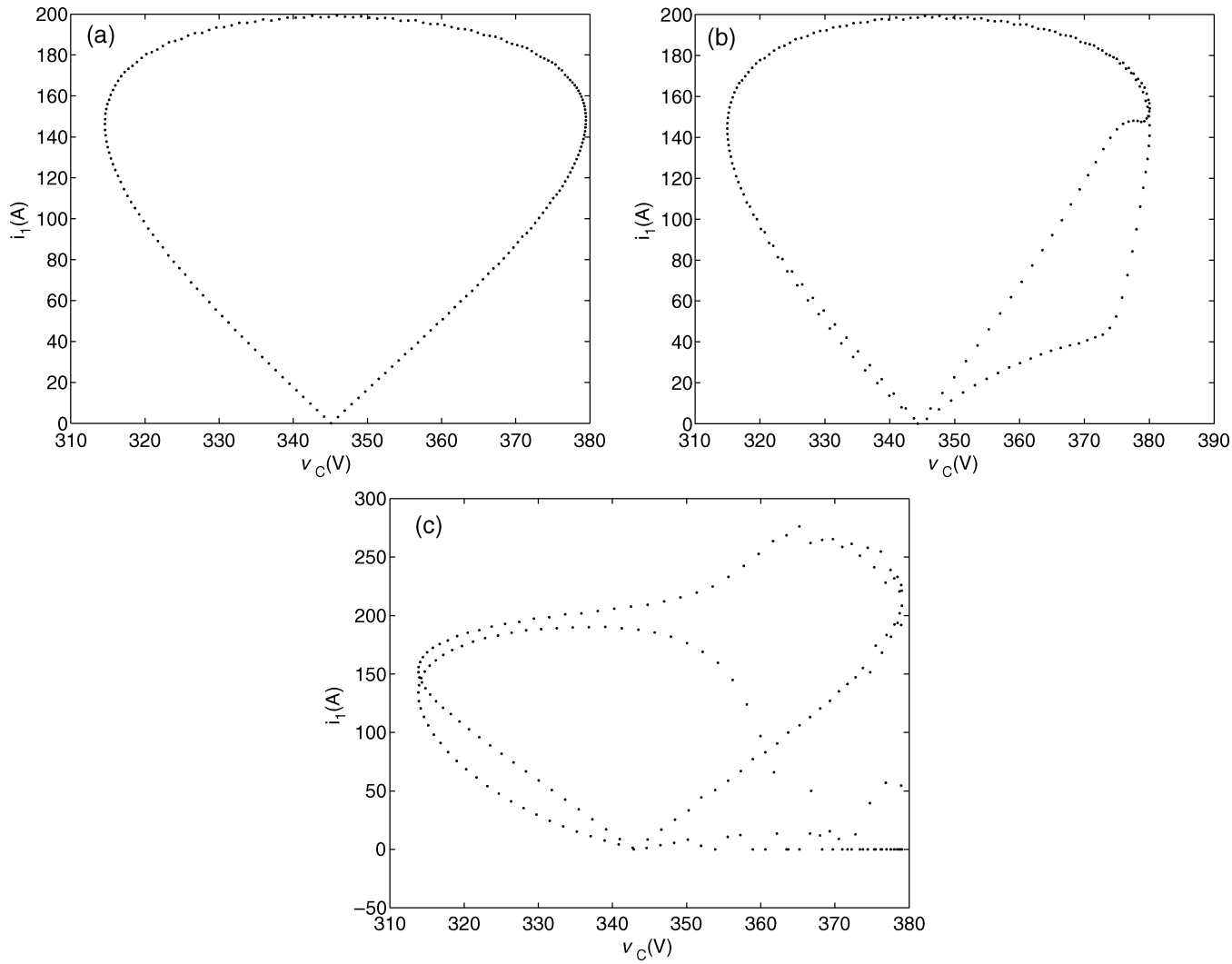

Fig. 5. Phase portraits of sampled i_1 versus v_C for $C_1 = 100\ \mu$F, $V_C = 349$ V and $V_{\rm ref} = 80$ V.

i.e., the regions near the zero-crossings being fast-scale stable. Fig. 8 shows various scenarios with different values of the feedback gain k for $C_1 = 10\ \mu$F. Fig. 8(a) shows fast-scale instability in some interval of the line cycle for $k = 0.006$. Fig. 8(b) shows the fast-scale period-2 and period-4 (with respect to the switching period) operations in some interval of the line cycle for $k = 0.007$. Fig. 8(c) shows fast-scale instability in some intervals of the line cycle for $k = 0.01$. Fig. 8(d)–(f) shows the corresponding sampled-data waveforms.

Similarly, we denote the two critical points in terms of phase angle as θ_{c1} and θ_{c2}. Fig. 9 plots the two critical phase angles θ_{c1} and θ_{c2} as functions of the feedback gain k. Here, we observe that the converter fails to maintain the desired stable operation in the interval $\theta_{c1} < \theta < \theta_{c2}$.

C. Effects of Storage Capacitance on Fast-Scale Instability

Here, we observe two apparently different instability manifestations. Specifically, for relatively large storage capacitance, the growth of fast-scale instability takes place near zero-crossings of the line cycle, whereas for relatively small storage capacitance, such fast-scale instability occurs near the high input-voltage regions of the line cycle. In this subsection, we present a detailed inspection of the effect of the size of the storage capacitance. Extensive simulations have been performed to track the values of the critical phase angles as C_1 increases. The results are shown in Fig. 10. There is no sudden jump of the critical phase angles as the storage capacitance varies. Instead, a continuous transition has taken place, as clearly illustrated in Fig. 10. This general transition, giving rise to the different locations of stability regions observed for large and small storage capacitance, are due to the phase shift of the storage capacitor voltage. Such a trend is general observed for different values of feedback gain k. Furthermore, the width of the stable region decreases as k increases.

IV. Theoretical Analysis of Fast-Scale Bifurcation Behavior

From the foregoing simulation study, we have identified period-doubling bifurcation in certain parameter ranges. In this section, we try to analyze the bifurcation in terms of suitable discrete-time model. Since the input voltage $e(t)$ is a rectified sine wave, whose frequency is much lower than the switching frequency (200 times less in this case), we can assume that the input voltage is a constant value equal to $e(nT)$ during a

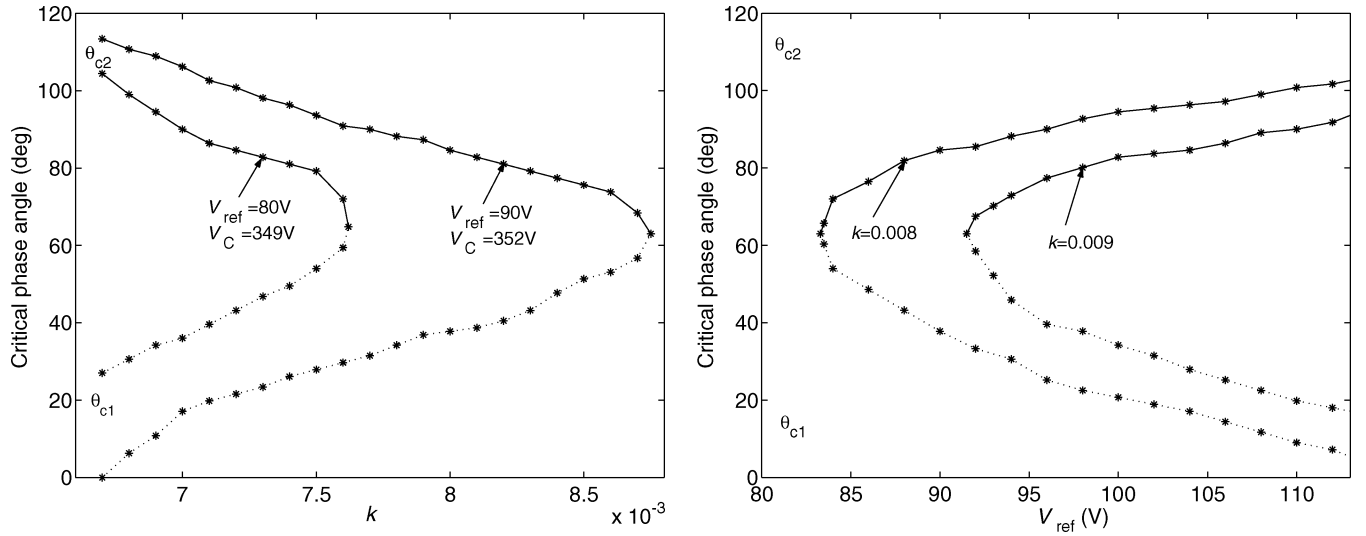

Fig. 6. Left: critical phase angles in line cycle versus feedback gain k; right: critical phase angles in line cycle versus $V_{\rm ref}$, both for $C_1 = 100\ \mu$F. θ_{c1} and θ_{c2} are the critical phase angles at which period-doubling bifurcation begins to occur. Fast-scale stable regions correspond to $\theta_{c1} < \theta < \theta_{c2}$.

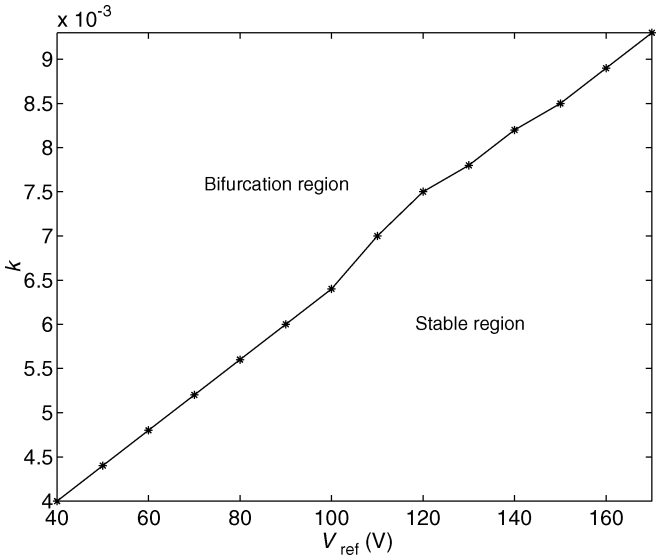

Fig. 7. Stability boundary in the parameter space of feedback gain versus output reference voltage for $C_1 = 100\ \mu$F.

switching period. The aim of the analytical study is to derive the discrete-time map describing the dynamics of the system. Then, by examining the Jacobian of this map, the stability can be assessed.

A. Derivation of Discrete-Time Map

Our purpose in this subsection is to derive a discrete-time map that describes the dynamics of the single-stage PFC converter operating in DCM. As mentioned before, due to the DCM, currents i_1 and i_2 do not act as state variables in this discrete-time model since $i_1(t_n) = 0$ and $i_2(t_n) = 0$ for all n. Thus, the iterative map we aim to find takes the following form

$$v_{n+1} = f(v_n, d_n, h_{1,n}, h_{2,n}) \tag{9}$$

where $v_n = v(nT)$ denotes the value at the beginning of the nth cycle, d_n is the duty cycle in the nth cycle, $h_{1,n}$ is the fraction of the switching period during which S_1 is off and i_1 is nonzero, and $h_{2,n}$ is the fraction of the switching period during which S_2 is off and i_2 is nonzero.

It is necessary to correctly model the change in state-space dimension when the diodes switch off in order to obtain correct stability results. With D_1 switched off, the matrix projecting the four-dimensional state x to the three-dimensional state y is

$$M = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}. \tag{10}$$

With D_2 switched off, the matrix projecting the three-dimensional state y to the two-dimensional state v is

$$N = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{11}$$

With the switches turned on, the matrix augmenting the state-space dimension from two (v) to four (x) is

$$Q = M^T N^T = \begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix}. \tag{12}$$

The state is unchanged in dimension and continuous at instants when the switches are turned off.

The state equations are given in (3) for different states. Here, without loss of generality, we omit state C. Thus, there are four consecutive subintervals in one switching cycle.

1) For $nT \le t < nT + d_nT$, S_1 and S_2 are on, D_1 and D_2 are off;
2) For $nT + d_nT \le t < nT + d_nT + h_{1,n}T$, S_1 and S_2 are off, D_1 and D_2 are on;
3) For $nT + d_nT + h_{1,n}T \le t < nT + d_nT + h_{2,n}T$, S_1 and S_2 are off, D_1 is off and D_2 is on;
4) For $nT + d_nT + h_{2,n}T \le t < (n+1)T$, S_1 and S_2 are off, D_1 and D_2 are off.

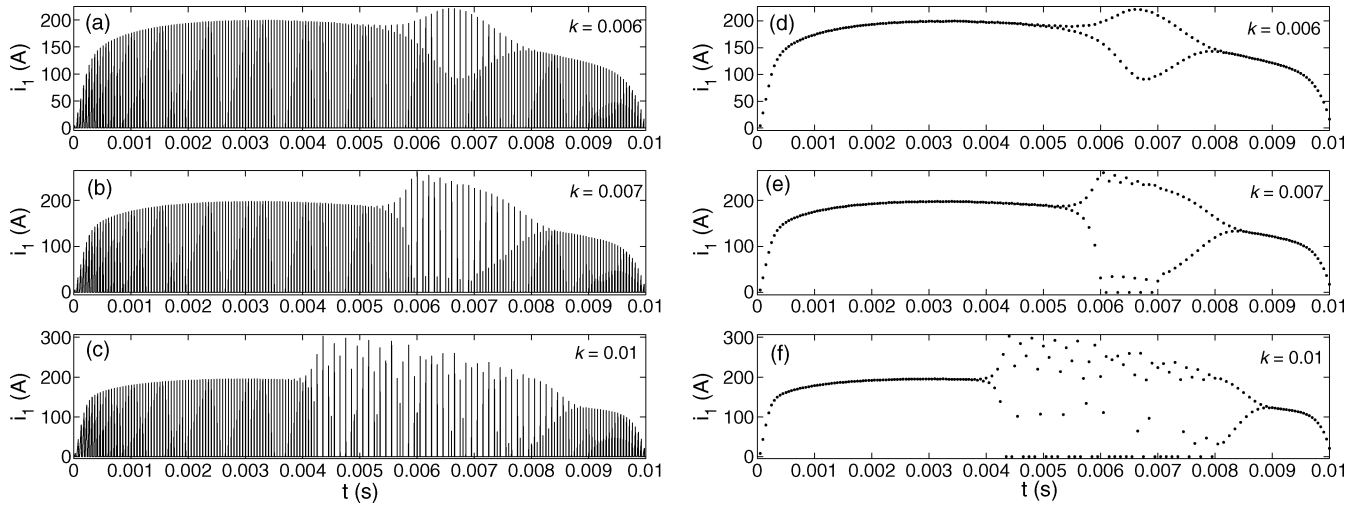

Fig. 8. (a)–(c) Time-domain waveforms and (d)–(f) sampled-data waveforms of i_1 for $C_1 = 10\ \mu$F, $V_C = 321$ V and $V_{\rm ref} = 90$ V.

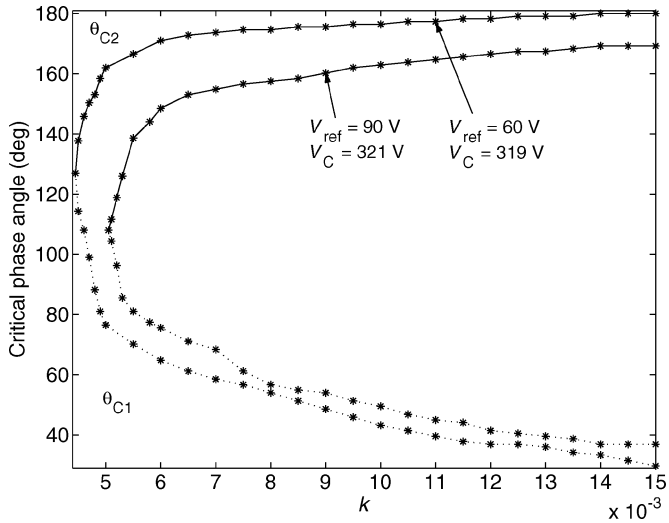

Fig. 9. Critical phase angles in line cycle versus feedback gain k for $C_1 = 10\ \mu$F. Fast-scale unstable regions correspond to $\theta_{c1} < \theta < \theta_{c2}$.

For the state equation in each subinterval, we can derive the solution, and by stacking up the solutions, v_{n+1} can be expressed in terms of v_n, d_n, $h_{1,n}$, and $h_{2,n}$, as represented in (13), i.e.,

$$\begin{aligned} v_{n+1} &= \Phi_4(\bar{d}_n T) N \Phi_3(\bar{h}_n T) M \\ &\quad \times \left\{ \Phi_2(h_{1,n}T)\Phi_1(d_n T) M^T N^T v_n \right. \\ &\qquad + \left[\Phi_2(h_{1,n}T) \left(\Phi_1(d_n T) - \mathbf{1}\right) A_1^{-1} \right. \\ &\qquad\quad \left. \left. + \left(\Phi_2(h_{1,n}T) - \mathbf{1}\right) A_2^{-1} \right] B e_n \right\} \end{aligned} \quad (13)$$

where $\bar{d}_n = 1 - h_{2,n} - d_n$, $\bar{h}_n = h_{2,n} - h_{1,n}$, $\mathbf{1}$ is the unit matrix, e_n is the input voltage at the beginning of the nth cycle, and

$$\Phi_j(\xi) = e^{A_j \xi} = \mathbf{1} + \sum_{n=1}^{\infty} \frac{1}{n!} A_j^n \xi^n, \quad \text{for} \quad j = 1, 2, 3, 4. \quad (14)$$

Our next step is to find the feedback equations that connect d_n, $h_{1,n}$ and $h_{2,n}$ to v_n. To find the defining equation for the duty cycle d_n, we first note that both switches are turned off when $v_{\rm con} = V_{\rm ramp}$. For brevity, we define

$$\begin{aligned} s(v_n, d_n) &= v_{\rm con} - V_{\rm ramp} \\ &= (V_{\rm offset} + k V_{\rm ref} - V_L) - (V_U - V_L) d_n \\ &\quad - k v_o(d_n T) \\ &= (V_{\rm offset} + k V_{\rm ref} - V_L) - (V_U - V_L) d_n \\ &\quad - k_1^T \left[\Phi_1(d_n T) M^T N^T v_n \right. \\ &\qquad \left. + \left(\Phi_1(d_n T) - \mathbf{1}\right) A_1^{-1} B e_n \right] \end{aligned} \quad (15)$$

where $k_1^T = [0\ 0\ 0\ k]$. Thus, S_1 and S_2 are turned off simultaneously when

$$s(v_n, d_n) = 0. \quad (16)$$

Also, d_n, $h_{1,n}$ and $h_{2,n}$ are related by enforcing continuity of the inductor currents at the switching instants [27], i.e.,

$$h_{1,n} = \frac{e_n}{v_{C,n} - e_n} d_n = \frac{e_n}{k_2^T v_n - e_n} d_n \quad (17)$$

$$h_{2,n} = \frac{v_{C,n} - v_{o,n}}{v_{o,n}} d_n = \frac{k_2^T v_n - k_3^T v_n}{k_3^T v_n} d_n \quad (18)$$

where $k_2^T = [1\ 0]$ and $k_3^T = [0\ 1]$. Combining (16), (17), and (18) with (13) yields the discrete-time iterative map for the closed-loop system.

B. Derivation of the Jacobian

The Jacobian plays an important role in the study of dynamical systems. The essence of using a Jacobian in the analysis of the dynamical systems lies in the capture of the dynamics in the small neighborhood of an equilibrium point or orbit. We will make use of this conventional method to examine the bifurcation phenomena observed earlier in Section III.

Suppose the equilibrium point is given by $v(nT) = V_Q$. The Jacobian of the discrete-time map evaluated at the equilibrium point can be written as follows:

$$\begin{aligned} J(V_Q) &= \frac{\partial f}{\partial v_n} + \frac{\partial f}{\partial d_n}\frac{dd_n}{dv_n} + \frac{\partial f}{\partial h_{1,n}}\left(\frac{\partial h_{1,n}}{\partial v_n} + \frac{\partial h_{1,n}}{\partial d_n}\frac{dd_n}{dv_n}\right) \\ &\quad + \frac{\partial f}{\partial h_{2,n}}\left(\frac{\partial h_{2,n}}{\partial v_n} + \frac{\partial h_{2,n}}{\partial d_n}\frac{dd_n}{dv_n}\right)\Bigg|_{v_n = V_Q}. \end{aligned} \quad (19)$$

Using (13), (16) and (18), we can find all the derivatives in (19). First, $\partial f / \partial v_n$ can be found from (13), i.e.,

$$\frac{\partial f}{\partial v_n} = \Phi_4(\bar{d}_n T) N \Phi_3(\bar{h}_n T) M \Phi_2(h_{1,n}T) \Phi_1(d_n T) M^T N^T. \quad (20)$$

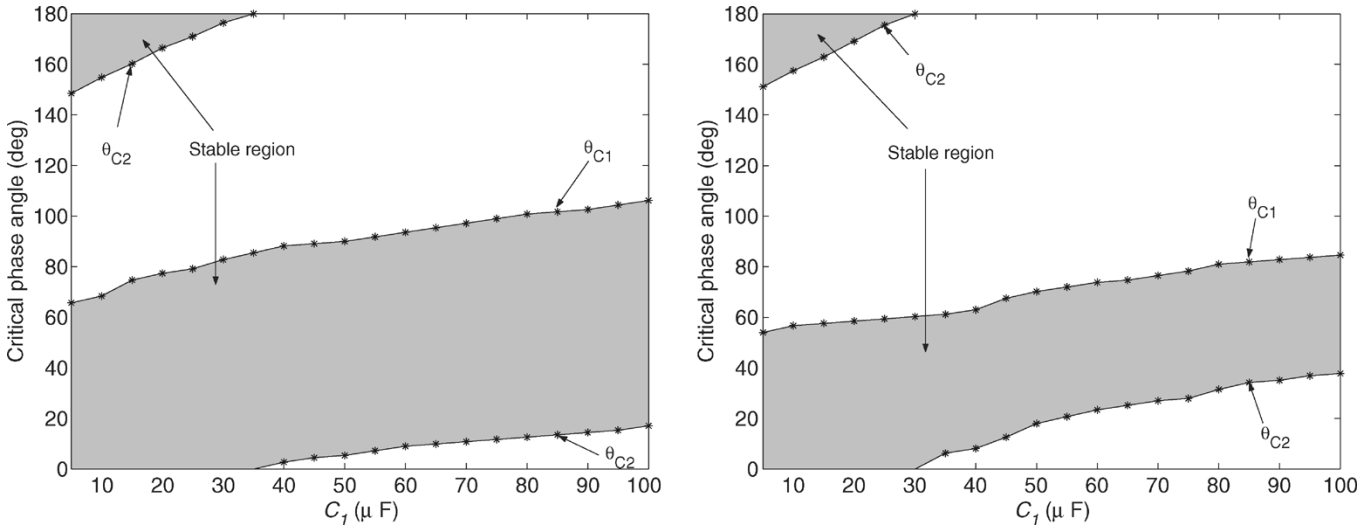

Fig. 10. Left: critical phase angles versus C_1, with $V_{\rm ref} = 90$ V and $k = 0.007$; right: critical phase angles versus C_1, with $V_{\rm ref} = 90$ V and $k = 0.008$.

Also, $\partial f/\partial d_n$ can be obtained as

$$\begin{aligned}\frac{\partial f}{\partial d_n} =& \Phi_4(\bar{d}_nT)(-A_4T)N\Phi_3(\bar{h}_nT)M\\ &\times\left[\Phi_2(h_{1,n}T)\Phi_1(d_nT)M^TN^Tv_n\right.\\ &\quad+\left(\Phi_2(h_{1,n}T)\left(\Phi_1(d_nT)-\mathbf{1}\right)A_1^{-1}\right.\\ &\qquad\left.\left.+\left(\Phi_2(h_{1,n}T)-\mathbf{1}\right)A_2^{-1}\right)Be_n\right]\\ &+\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)M\\ &\times\left[\Phi_2(h_{1,n}T)\Phi_1(d_nT)A_1TM^TN^Tv_n\right.\\ &\quad\left.+\Phi_2(h_{1,n}T)\Phi_1(d_nT)Be_n\right]\\ =&-TA_4\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)Mx(nT+d_nT+h_{1,n}T)\\ &+T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)M\Phi_2(h_{1,n}T)\\ &\times\Phi_1(d_nT)\dot{x}(nT)_+ \end{aligned}\tag{21}$$

where $\dot{x}(t)_+$ denotes the right-hand side time derivative of state vector x at time t. In (21), the first term corresponds to cascading the solutions of the state equations given in (3) and, therefore, equals $-TA_4v_{n+1}$. By applying the appropriate transition matrices and (10), (11), and

$$MA_2M^T = A_3;\quad MB = 0;\quad NA_3N^T = A_4 \tag{22}$$

we can put the second term of (21) as

$$\begin{aligned}&T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)M\Phi_2(h_{1,n}T)[A_1x(nT+d_nT)+Be_n)]\\ &\quad=T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)M\Phi_2(h_{1,n}T)\\ &\qquad\times[\dot{x}(nT+d_nT)_+ +(A_1-A_2)x(nT+d_nT)]\\ &\quad=T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)\\ &\qquad\times[\dot{y}(nT+d_nT+h_{1,n}T)_+\\ &\qquad\quad+M\Phi_2(h_{1,n}T)(A_1-A_2)x(nT+d_nT)]\\ &\quad=T\Phi_4(\bar{d}_nT)N\\ &\qquad\times\left[A_3y(nT+d_nT+h_{2,n}T)\right.\\ &\qquad\quad\left.+\Phi_3(\bar{h}_nT)M\Phi_2(h_{1,n}T)(A_1-A_2)x(nT+d_nT)\right]\\ &\quad=T\Phi_4(\bar{d}_nT)\\ &\qquad\times\left[NA_3N^Tv(nT+d_nT+h_{2,n}T)\right.\\ &\qquad\quad\left.+N\Phi_3(\bar{h}_nT)M\Phi_2(h_{1,n}T)(A_1-A_2)x(nT+d_nT)\right]\\ &\quad=TA_4v_{n+1}+T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)\\ &\qquad\times M\Phi_2(h_{1,n}T)(A_1-A_2)x(nT+d_nT).\end{aligned}\tag{23}$$

Hence, $\partial f/\partial d_n$ can be expressed as

$$\begin{aligned}\frac{\partial f}{\partial d_n} =& T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)M\Phi_2(h_{1,n}T)\\ &\times(A_1-A_2)x(nT+d_nT).\end{aligned}\tag{24}$$

Likewise, we obtain

$$\begin{aligned}\frac{\partial f}{\partial h_{1,n}} =& \Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)(-A_3T)M\\ &\times\left\{\Phi_2(h_{1,n}T)\Phi_1(d_nT)M^TN^Tv_n\right.\\ &\quad+\left[\Phi_2(h_{1,n}T)\left(\Phi_1(d_nT)-\mathbf{1}\right)A_1^{-1}\right.\\ &\qquad\left.\left.+\left(\Phi_2(h_{1,n}T)-\mathbf{1}\right)A_2^{-1}\right]Be_n\right\}\\ &+\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)M\\ &\times\left\{\Phi_2(h_{1,n}T)A_2T\Phi_1(d_nT)M^TN^Tv_n\right.\\ &\quad+\left[\Phi_2(h_{1,n}T)A_2T\left(\Phi_1(d_nT)-\mathbf{1}\right)A_1^{-1}\right.\\ &\qquad\left.\left.+\Phi_2(h_{1,n}T)T\right]Be_n\right\}\\ =&T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)\\ &\times\{-A_3Mx(nT+d_nT+h_{1,n}T)+M\Phi_2(h_{1,n}T)\\ &\quad\times\left[A_2\left(\Phi_1(d_nT)M^TN^Tv_n\right.\right.\\ &\qquad\left.\left.+\left(\Phi_1(d_nT)-\mathbf{1}\right)A_1^{-1}Be_n\right)+Be_n\right]\}\\ =&T\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)\\ &\times[-\dot{y}(nT+d_nT+h_{1,n}T)_+\\ &\quad+MA_2M^Ty(nT+d_nT+h_{1,n}T)]\\ =&0.\end{aligned}\tag{25}$$

Furthermore

$$\begin{aligned}\frac{\partial f}{\partial h_{2,n}} =& T\Phi_4(\bar{d}_nT)(-A_4N+NA_3)\Phi_3(\bar{h}_nT)M\\ &\times\left\{\Phi_2(h_{1,n}T)\Phi_1(d_nT)M^TN^Tv_n\right.\\ &\quad+\left[\Phi_2(h_{1,n}T)\left(\Phi_1(d_nT)-\mathbf{1}\right)A_1^{-1}\right.\\ &\qquad\left.\left.+\left(\Phi_2(h_{1,n}T)-\mathbf{1}\right)A_2^{-1}\right]Be_n\right\}\\ =&T\Phi_4(\bar{d}_nT)NA_3k_4k_4^Ty(nT+d_nT+h_{2,n}T)\\ =&0\end{aligned}\tag{26}$$

since $-N^TN+\mathbf{1}=k_4k_4^T$, $k_4^T=[0\ 1\ 0]$, and the condition for diode D_2 to switch off is

$$i_2(nT+d_nT+h_{2,n}T) = k_4^Ty(nT+d_nT+h_{2,n}T) = 0. \tag{27}$$

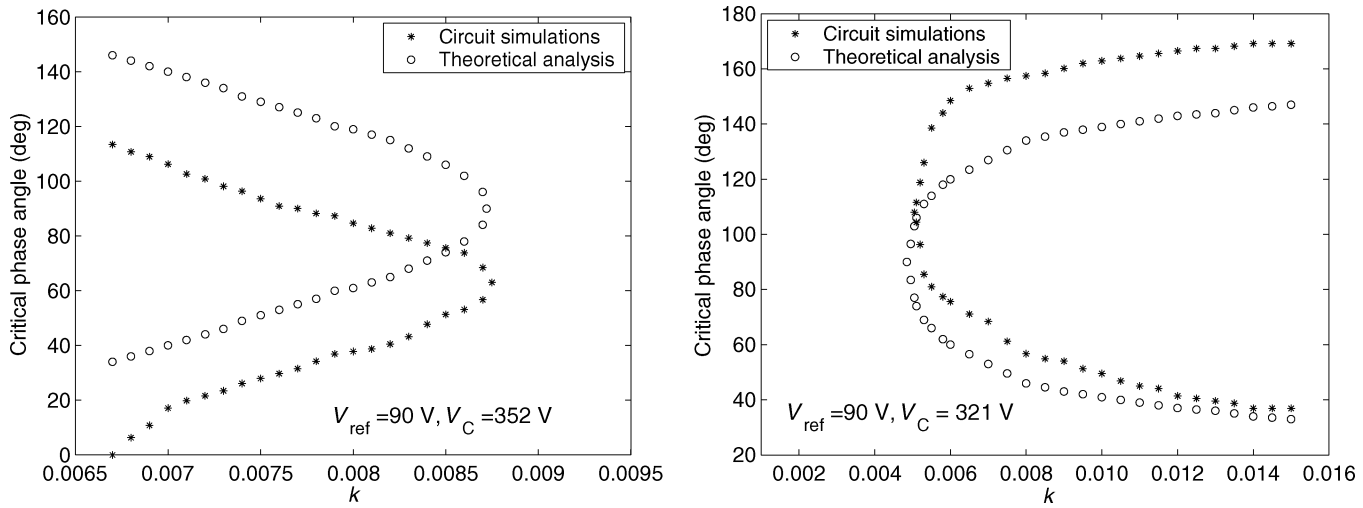

Fig. 11. Left: comparison of critical phase angles obtained from analysis and simulations for $C_1 = 100\ \mu$F; right: comparison of critical phase angles obtained from analysis and simulations for $C_1 = 10\ \mu$F. The difference between theoretical and simulation data can be attributed to the fact that analytical computation of the Jacobian assumes a steady-state operating point for each value of the input voltage, but such a steady state is never reached in the simulations in which time-varying input voltage has been used.

Now, from (25) and (26), the final state v_{n+1} is first-order independent of the switch-off times of the diodes. Thus, dd_n/dv_n is the last derivative needed to compute (19). From (15), we have

$$\frac{dd_n}{dv_n} = -\left(\frac{\partial s}{\partial d_n}\right)^{-1}\frac{\partial s}{\partial v_n} = -\frac{k_1^T\Phi_1(d_nT)M^TN^T}{(V_U-V_L)+Tk_1^T\Phi_1(d_nT)(A_1M^TN^Tv_n+Be_n)}. \tag{28}$$

Finally, substituting the derivatives obtained above in (19), the Jacobian is obtained as shown in (29) at the bottom of the page.

C. Computation of Critical Phase Angles

The Jacobian derived here can be used to evaluate the dynamics of the system. We study the loci of the characteristic multipliers, the aim being to identify possible bifurcation scenarios as the input voltage varies with time. To find the characteristic multipliers, we solve the following polynomial equation in λ:

$$\det\left[\lambda\mathbf{1} - J(V_Q)\right] = 0. \tag{30}$$

In a line cycle, the input voltage is $\hat{e}\left|\sin\theta\right|$, where $0 < \theta = \omega t < \pi$. We track the movement of the characteristic multipliers as we vary the phase angle θ. For a stable operation, all characteristic multipliers should stay inside the unit cycle. Any crossing from the interior of the unit cycle to the exterior indicates a bifurcation. For any set of parameters, we can compute the discrete-time map (13) and the corresponding Jacobian given in (29) for every $V_Q = v(nT)$, and record the values of $\theta = \omega t_n$ when one of the characteristic multipliers of the Jacobian reaches -1. These are the critical phase angles at which period-doubling occurs. A comparison of these results with those obtained by computer simulations is shown in Fig. 11. The theoretical results generally match with the simulations. The discrepancies can be attributed to the fact that the computation of the Jacobian assumes a steady-state operating point for each value of the input voltage, but such a steady-state is never reached in the circuit simulations in which actual time-varying input voltage has been used. Thus, the simulation data should more realistically locate the stability boundaries, while the theoretical results produced from the analytical expressions provide quick and reasonably close numerical estimates.

V. Conclusion

Power factor correction has become an important design consideration for switching power supplies. For low-power applications (below 200 W), a cost effective solution is to use a single-stage design in which the PFC stage is integrated with the dc–dc power stage. The specific solution proposed by Redl *et al.* [1] has proven to be versatile for low-power applications in terms of ease of control and containment of voltage stresses. Such a design utilizes DCM of operation to simplify the control and to maintain a fixed (load independent) voltage stress in the storage capacitor. In this paper we have performed a detailed study of the fast-scale bifurcation behavior of this converter and we have investigated into the effects of various parameters on the stability of the system. Such fast-scale stability problems are important as they affect the peak current stresses imposed on the switching devices. The results obtained here can be used to facilitate parameter selection for guaranteeing stable operation.

$$J(V_Q)=\Phi_4(\bar{d}_nT)N\Phi_3(\bar{h}_nT)M\Phi_2(h_{1,n}T)\left[\mathbf{1}-\frac{(A_1-A_2)\left(\Phi_1(d_nT)M^TN^Tv_n+(\Phi_1(d_nT)-\mathbf{1})\,A_1^{-1}Be_n\right)k_1^T}{\frac{(V_U-V_L)}{T}+k_1^T\Phi_1(d_nT)(A_1M^TN^Tv_n+Be_n)}\right]\cdot\Phi_1(d_nT)M^TN^T. \tag{29}$$

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