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Self-organized Ge nanocrystals embedded in HfAlO fabricated by pulsed-laser deposition and application to floating gate memory

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A trilayer metal-oxide-semiconductor structure containing a HfAlO tunnel layer, isolated Ge nanocrystals, and a HfAlO control layer, was obtained using pulsed-laser deposition (PLD). Self-organized Ge nanocrystals were formed by PLD at 600 °C, suggesting a useful low-temperature process for fabricating Ge nanocrystals embedded in dielectric materials. The self-organized Ge nanocrystals so formed were uniform in size and distribution with a density approaching 10^{12} cm^{-2}. The effects of deposition temperature and growth rate in forming Ge nanocrystals were investigated and it was revealed that a relatively low temperature and growth rate are favorable for the formation of Ge nanocrystals. The memory effect of the Ge nanocrystals with storage charge density of up to 10^{12} cm^{-2} has been demonstrated by the presence of hysteresis in the capacitance-voltage curves. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1846154]

The nanocrystal floating gate embedded in dielectrics has attracted a great deal of attention recently because it can potentially be applied in nonvolatile, high-speed, high-density, and low-power consuming memory.[1–15] Compared to conventional floating gate memories such as flash, a device composed of nanocrystals isolated by dielectrics benefits from a relatively low operating voltage, high endurance, fast write-erase speeds, and better immunity to soft errors.[1] For the first nano-floating-gate memory, the materials of nanocrystals and dielectrics were Si and SiO_2, respectively.[1] In recent years, several new memory nodes such as Ge, SiGe, Au, TiN, and Ag have been investigated, and some of them were incorporated with high-*k* dielectrics.[3–14] The Ge nanocrystal is considered to be an ideal memory node due to its relatively small band gap compared to Si and compatibility with current complementary metal-oxide-semiconductor (CMOS) technology. However, it is still difficult to fabricate uniform and self-organized Ge nanocrystals. Most of the methods, including the thermal annealing of Ge and dielectric mixture layer,[13–15] Ge ion implantation,[5] and the oxidation of SiGe,[6,7] require annealing at high temperatures. Baron *et al.*[16] has fabricated Ge nanodots on the SiO_2 matrix by low-pressure chemical vapor deposition. However, silicon nuclei are needed in this method. Pulsed-laser deposition (PLD) is a good method for growing high-quality structures at low temperatures. Hassan *et al.*[17] employed it to fabricate Ge nanocrystals embedded in an AlN matrix for optical application. In this Letter, we report on the formation of self-organized Ge nanocrystals at relatively low substrate temperatures using PLD, and the memory effect of the metal-oxide-semiconductor (MOS) structure composed of Pt electrode, a HfAlO control gate, Ge nanocrystals, and a HfAlO tunnel layer on Si substrate. The motivation for integrating the Ge nanocrystals with HfAlO is its potential for implementation in the new generation CMOS technology. In fact, recent studies have shown that high-*k* dielectrics, instead of SiO_2, for the tunnel layer in nanocrystal floating gate memory can also improve the tradeoff between the data retention and program efficiency due to the unique band asymmetry of high-*k* dielectrics in the programming and retention modes.[9] In addition, our earlier works have shown that HfAlO is a promising high-*k* material because of its thermal stability.[18]

A pulsed excimer laser with multiple targets was used to deposit HfAlO films and Ge nanocrystals, where the atomic ratio of HfO_2 to Al_2O_3 in the composite target was 1:2. The laser fluence and frequency used were 5 J/cm^2 and 2 Hz, respectively. A 7-nm-thick tunnel HfAlO layer was first grown on a *P*-type (100) Si substrate at 550 °C. Subsequently, the Ge nanocrystals were deposited on the surface of the HfAlO at 600 °C. Different deposition time and substrate temperatures were implemented in order to study their effects on the formation of Ge nanocrystals. The memory structure used in this study is a MOS capacitor with a dielectric stack made up of Ge nanocrystals sandwiched between the tunnel and control HfAlO layers. The control HfAlO layer, with a thickness of 10 nm, was deposited at 550 °C. The samples were finally annealed at 800 °C for 30 min in N_2 ambient, and Pt dot electrodes with a diameter of 0.2 mm were subsequently deposited by PLD.

Ge nanocrystals were characterized by atomic force microscopy (AFM) and scanning electron microscopy (SEM) before the deposition of the control layer. Trilayer structures

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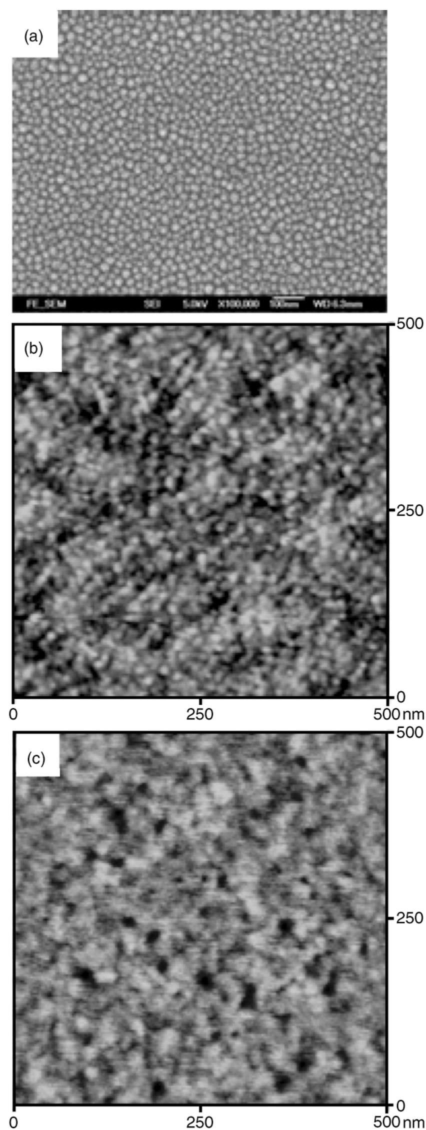

FIG. 1. SEM picture of high-density self-organized Ge nanocrystals deposited on (a) HfAlO matrix by PLD for 1 min at 600 °C, and AFM images of Ge nanocrystals on HfAlO matrix by PLD for 30 s at (b) 600 °C and (c) 700 °C.

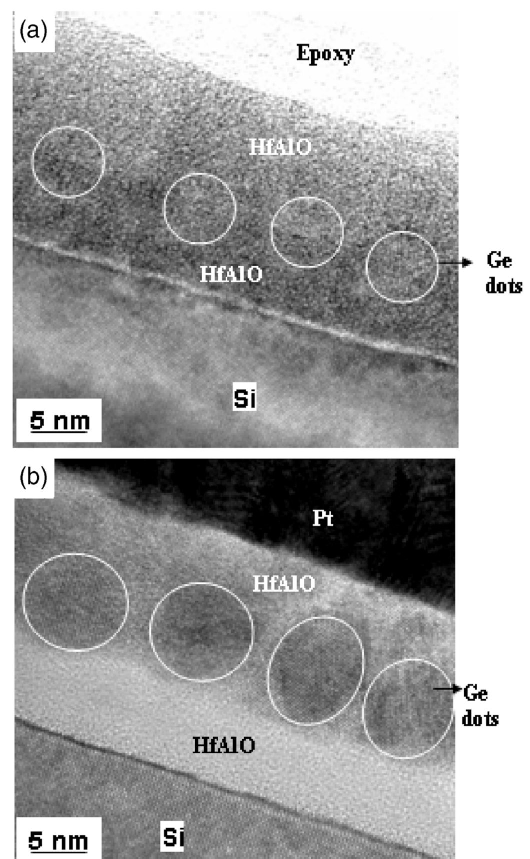

FIG. 2. High-resolution TEM images of samples composed of HfAlO control gate, Ge nanocrystals, and HfAlO tunnel layer on Si substrate: (a) as-grown and (b) annealed at 800 °C.

were investigated by high-resolution transmission electron microscopy (TEM). The memory effect in Ge nanocrystal-embedded capacitors fabricated by PLD was characterized by measurements of capacitance voltage (*C-V*) and current voltage (*I-V*).

Figure 1(a) shows a typical SEM image of Ge nanocrystals grown at 600 °C. It can be seen that Ge nanocrystals are well self-organized and distribute uniformly. The density and mean size of the dots are about 8×10^{11} cm^{-2} and 25 nm, respectively. The island structure of the Ge suggests that the growth is based on the Volmer-Webber mode, where Ge atoms can easily combine with each other but not with HfAlO on Si in our experimental conditions. The most remarkable difference between PLD and other vapor deposition methods is the high energy of the plasma generated by the laser ablation of the desired target material. Therefore, during PLD the Ge plasma has a relatively high forward velocity, which leads to the relatively uniform distribution of Ge nanocrystals. According to the observation by cross-sectional TEM (not shown here), the height of these nanocrystals is about 25 nm, resulting in an increased surface roughness on the top dielectric that hinders the application of nanocrystal floating gate memory. Therefore, the deposition time of Ge has been reduced accordingly in the following experiments.

The substrate temperature was found to be an important parameter for the growth of Ge nanocrystals. Figures 1(b) and 1(c) show AFM images of the Ge nanocrystals grown at the temperatures of 600 and 700 °C, respectively. From Fig. 1(b), it can be seen that the Ge nanocrystals are well self-organized and their diameter is about 10 nm. By contrast, the diameter of the Ge nanocrystals deposited at 700 °C, as shown in Fig. 1(c), is larger and their height becomes smaller. This suggests that when the substrate temperature increases, the diffusion coefficient of Ge atoms also increases, and the Ge atoms are relatively easier to combine with the HfAlO atoms. Therefore, the substrate temperature of 600 °C for the growth of Ge nanocrystals has been used to fabricate memory capacitors.

The structure of the memory capacitor was investigated by cross-sectional TEM. Figure 2(a) shows the structure of the as-grown samples containing three obvious layers on silicon substrate, i.e., the HfAlO control layer, the Ge nanocrystals layer, and the HfAlO tunnel layer. The Ge nanocrystals indicated by white circles are uniformly distributed between the HfAlO control layer and the tunnel layer. The thicknesses of the tunnel layer and the control layer are about 7 and 14 nm, respectively. From the high-resolution TEM image, as shown in Fig. 2(a), it can be seen that the HfAlO layers have an amorphous structure and the Ge nanocrystals are single crystalline. The lattice fringes that were observed are identified as {111} planes of Ge. Our experimental results showed that the growth rate can also affect the crystallinity of the Ge nanocrystals. When the growth rate is higher, the

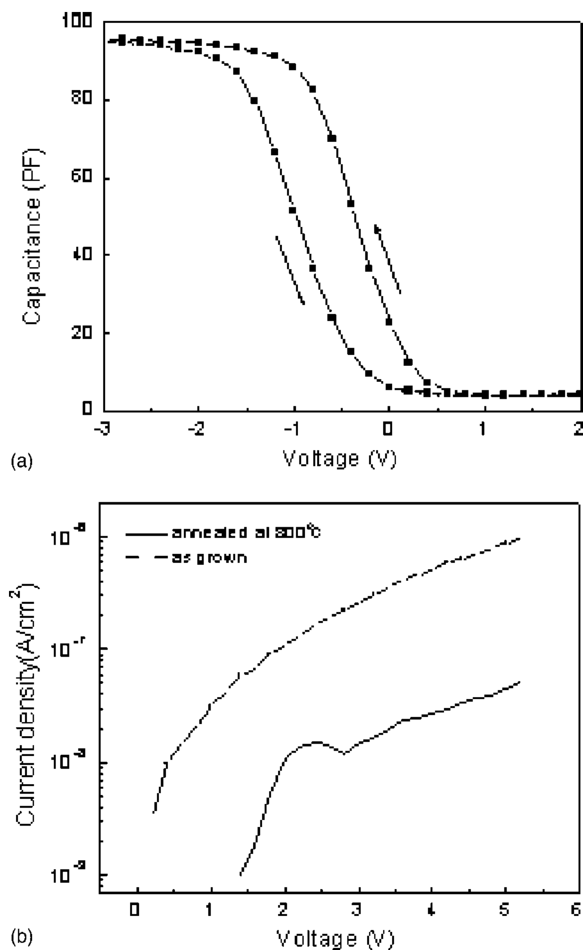

FIG. 3. (a) High-frequency (1-MHz) *C-V* curves and (b) *I-V* curves of as-grown and 800 °C annealed MOS capacitors.

Ge nanocrystals are amorphous. It can also be seen from Fig. 2(a) that the Ge nanocrystals are spherical in shape and their diameter is about 10 nm, which is consistent with the AFM result shown in Fig. 1(b). The interface between the HfAlO tunnel layer and the silicon substrate is almost free from any interfacial layer. Figure 2(b) is the high-resolution TEM image of the MOS structure annealed at 800 °C. It can be clearly seen that even after annealing at 800 °C, the interface between the HfAlO tunnel layer and the silicon substrate is still sharp and is free from any interfacial layer. It can also be seen that after annealing at 800 °C, the Ge nanocrystals increased in size. Some crystal lattices in the control layer may be due to the diffusion of Ge. It is also worth noting that the existence of Ge and Ge diffusion may decrease the crystallization temperature of HfAlO and lead to localized crystallization. The detailed mechanism should be studied further.

The *C-V* measurement of the as-grown and 800 °C annealed MOS capacitors incorporating the Ge nanocrystals revealed that the as-grown sample exhibits abnormal *C-V* characteristics (not shown) and the sample annealed at 800 °C presents a significant hysteresis, indicating successful charge storage. Figure 3(a) shows the high-frequency (1-MHz) *C-V* curve of the sample annealed at 800 °C. Anti-clockwise hysteresis indicates electron trapping in the capacitor. The effect of the mobile ions on the charge trapping can be ruled out, since no hysteresis was observed in the control sample without Ge nanocrystals under our experimental conditions and no obvious deformation can be observed in the *C-V* curves as shown in Fig. 3(b). The flatband voltage shift is about 0.6 V. Calculated by the formula in Refs. 1 and 19, the stored charge density is up to 10^{12} cm^{-2}.

The different *C-V* characteristics between the as-grown and the annealed samples can be understood by measuring their leakage currents. Figure 3(b) shows the leakage currents of the two samples with and without annealing. It can be seen that the leakage current of the memory structure annealed at 800 °C is very small and it is much smaller than that of the sample without annealing. The relatively large leakage current of the sample without annealing is due to the presence of a large amount of oxygen vacancies in the as-grown HfAlO films. Annealing at 800 °C in a quartz tube reduced the oxygen vacancies and the leakage current.

In summary, we have fabricated at relatively low temperature by PLD method a memory structure containing a HfAlO control gate, well self-organized Ge nanocrystals, and a HfAlO tunnel layer. The substrate temperature and growth rate were found to be the key factors influencing the size and distribution of the Ge nanocrystals. The obvious memory effect of the trilayer structure was demonstrated by the presence of hysteresis in the *C-V* curves with a storage charge density of up to 10^{12} cm^{-2}.

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