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DOI (link to publication from Publisher):
10.5278/vbn.phd.engsci.00098

Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

AN ELECTRICAL METHOD FOR JUNCTION TEMPERATURE MEASUREMENT OF POWER SEMICONDUCTOR SWITCHES

BY
NICK BAKER

DISSERTATION SUBMITTED 2016

AALBORG UNIVERSITY
DENMARK

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by

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Dissertation submitted: April 6th 2016

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PhD Series: Faculty of Engineering and Science, Aalborg University

ISSN (online): 2246-1248
ISBN (online): 978-87-7112-548-1

Published by:
Aalborg University Press
Skjernvej 4A, 2nd floor
DK – 9220 Aalborg Ø
Phone: +45 99407140
aauf@forlag.aau.dk
forlag.aau.dk

Printed in Denmark by Rosendahls, 2016

Copyright Statement

This thesis has been submitted for assessment in partial fulfillment of the PhD degree. The thesis is based on the submitted or published scientific papers which are listed below. Parts of the papers are used directly or indirectly in the extended summary of the thesis. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty.

Thesis Title: An Electrical Method for Junction Temperature Measurement in Power Semiconductor Switches

Name of PhD Student: Nick Baker

Name of Supervisors: Professor Stig Munk-Nielsen and Professor Francesco Iannuzzo

List of Publications:

1. N. Baker, M. Liserre, L. Dupont, Y. Avenas, "**Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters,**" in 39th Annual Conference of the IEEE Industrial Electronics Society (IECON 2013), pp. 942-948, 10-13 Nov. 2013.

2. N. Baker, M. Liserre, L. Dupont, Y. Avenas, "**Improved Reliability of Power Modules: A Review of Online Junction Temperature Measurement Methods,**" in IEEE Industrial Electronics Magazine, vol.8, no.3, pp. 17-27, Sept. 2014.

3. N. Baker, L. Dupont, Y. Avenas, F. Iannuzzo, S. Munk-Nielsen, "**Experimental Evaluation of IGBT Junction Temperature Measurement via a Modified VCE Method with Series Resistance Removal,**" in 9th International Conference on Integrated Power Systems (CIPS 2016), to be published, March 2016.

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6. N. Baker, S. Munk-Nielsen, F. Iannuzzo, M. Liserre, "**IGBT Junction Temperature Measurement via Peak Gate Current,**" in IEEE Transactions on Power Electronics, vol.31, no.5, pp. 3784-3793, May 2016.

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8. N. Baker, S. Munk-Nielsen, F. Iannuzzo, M. Liserre, " **IR Camera Validation of IGBT Junction Temperature Measurement via Peak Gate Current,**" in review for IEEE Transactions on Power Electronics.

Acknowledgements

Firstly, I am eternally grateful to Professor Stig Munk-Nielsen for giving me the chance to work at Aalborg University. Thank you to Professor Marco Liserre for allowing me the opportunity to work on this PhD in Power Semiconductor Devices, and to Professor Stig Munk-Nielsen and Professor Francesco Iannuzzo for agreeing to continue supervision of the project.

I must also extend my sincerest gratitude to Dr. Laurent Dupont and Associate Professor Yvan Avenas for their incredibly helpful advice throughout the PhD period. In particular, their knowledge in the topic of junction temperature measurements was invaluable in the beginning stages of this research.

Furthermore, I would like to make a special thank you to Dr. Laurent Dupont for inviting me for a 6 month research visit at the SATIE Laboratory in Versailles, France. His meticulous approach and detailed planning ensures that experimental quality under his supervision is second to none.

I would also like to thank Iain Russell and Alan James for the many great debates in The Wharf. Finally, I thank my family and my girlfriend for their support during this period.

I wish all my colleagues and friends from the CORPE and IEPE projects at Aalborg University all the best for the future.

Abstract

Power semiconductor switches are critical components in power electronic converters and operate in thermally stressful environments. The junction temperature of a power semiconductor directly influences its power loss and is intrinsically linked to numerous failure mechanisms. Knowledge of this temperature is therefore important for optimal operation and for reliability reasons. If the junction temperature is known during the operation of a converter, real-time condition monitoring and active thermal control systems could be developed to improve system reliability.

Performing direct measurements of junction temperature is difficult since the power semiconductor is generally encapsulated inside an array of packaging materials. Alternatively, the electrical behaviour of a semiconductor largely depends on temperature. If this relationship is known, the electrical parameters of the device can be monitored and used to estimate the junction temperature. These are known as Temperature Sensitive Electrical Parameters (TSEPs) and are one way to carry out non-invasive, real-time junction temperature measurements on fully packaged devices.

Nevertheless, successful implementation of these techniques during the normal operation of a power semiconductor is thus far limited. Often holding back their use is the need to compensate for inherent fluctuations caused by a constantly changing electrical environment (or alternatively requiring interruption to normal operation to force fixed electrical conditions), and significant uncertainty over accuracy. As a result, this PhD aims to develop new methods, or improvements to existing methods, for junction temperature measurement via TSEPs during the operation of power semiconductor switches.

In Chapter 1, the state-of-the-art in the topic of junction temperature measurement is introduced. A literature review of TSEPs investigated for use in operating power semiconductor switches is then provided. From this, several implementation issues are identified and used to formulate technical objectives for the PhD thesis.

Chapter 2 introduces the first original contribution of the thesis. Two TSEP-based methods for junction temperature measurement, unpublished in scientific literature before the commencement of the PhD, are presented. The measurement principles are explained, and experimental validation is provided on Insulated-Gate-Bipolar-Transistors (IGBTs). The foremost advantages in the presented TSEPs are that they are measured without interruption to normal IGBT operation, and do not require compensation for varying load current conditions. The primary method presented is referred to as the Peak Gate Current (I_{GPeak}) method, which is selected for further examination in Chapter 3.

In Chapter 3, the second scientific contribution of the thesis is provided. Here, the accuracy of the I_{GPeak} method on IGBTs is extensively examined using direct measurements of junction temperature from an Infra-Red camera. The validation is performed on IGBT dies with differing geometry, as well as IGBTs in both healthy and degraded conditions. Finally, IGBTs in a paralleled configuration are investigated. These results in terms of accuracy are compared with a traditional TSEP method commonly found in prior art.

Finally, Chapter 4 provides a summary of the work, along with the main scientific contributions and limitations of the PhD.

Thesis Structure

This thesis is presented as a collection of papers, however an extended summary is provided comprising of 4 chapters. The relevant papers for each chapter are listed as follows, and are included in Appendix C of the extended summary.

Chapter 1:

A. **N. Baker**, M. Liserre, L. Dupont, Y. Avenas, "Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters," in 39th Annual Conference of the IEEE Industrial Electronics Society (IECON 2013), pp. 942-948, 10-13 Nov. 2013.

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C. **N. Baker**, L. Dupont, Y. Avenas, F. Iannuzzo, S. Munk-Nielsen, "Experimental Evaluation of IGBT Junction Temperature Measurement via a Modified VCE Method with Series Resistance Removal," in 9th International Conference on Integrated Power Systems (CIPS 2016), to be published, March 2016.

Chapter 2:

D. **N. Baker**, S. Munk-Nielsen, M. Liserre, F. Iannuzzo, "Online junction temperature measurement via internal gate resistance during turn-on," in 2014 16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe), pp. 1-10, 26-28 Aug. 2014.

E. **N. Baker**, S. Munk-Nielsen, F. Iannuzzo, M. Liserre, "Online junction temperature measurement using peak gate current," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1270-1275, 15-19 March 2015.

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Chapter 3:

G. **N. Baker**, L. Dupont, S. Munk-Nielsen, F. Iannuzzo, M. Liserre, "Experimental evaluation of IGBT junction temperature measurement via peak gate current," in 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), pp. 1-11, 8-10 Sept. 2015.

H. **N. Baker**, S. Munk-Nielsen, F. Iannuzzo, M. Liserre, " IR Camera Validation of IGBT Junction Temperature Measurement via Peak Gate Current," in review for IEEE Transactions on Power Electronics.

Chapter 4:

N/A

Contents

I. Introduction

This section will outline the background and motivation for junction temperature measurements in power semiconductors. A literature review of the state-of-the-art for junction temperature measurements will be provided. In particular, problems and challenges associated with using Temperature Sensitive Electrical Parameters will be identified and described. From this, objectives for the PhD Thesis are formulated.

1.1. Reliability Challenges in Power Electronics

1.1.1. Power Converter Failures

Power electronic converters are used to provide high efficiency power conversion in a variety of industries and can be found in many renewable, automotive, aerospace and railroad systems. These applications are often safety critical and place stringent demands on reliability. For example, unexpected failures may lead to severe accidents in automotive or aerospace applications, while unscheduled maintenance or downtime can induce high economic costs for renewable power plants. In numerous cases, power electronic converters are also required to operate in thermally stressful environments, such as in electric vehicles where ambient operating temperatures may exceed 150°C.

The anticipation of failures in power electronic converters is difficult, but is of great interest so that the operation of a system can be halted before a breakdown occurs and prompt maintenance scheduled. Taking the case of a photovoltaic (PV) power plant, the system can be simplified into two distinct units: the solar panels/modules, and the power inverter. A complete breakdown in either of these units can cause significant downtime in the system. Nevertheless, multiple solar module failures can often be tolerated and not lead to a breakdown of the entire array, whereas a component failure in the inverter can lead to downtime in the entire system.

The relevance of inverter reliability is further heightened with solar panel/module manufacturers frequently offering warranties of up to 20-years (perhaps covering the life of the power plant), while warranties for solar inverters rarely reach the 10-year mark [1]. Although the market competition between PV inverter manufacturers has traditionally focused on the efficiency of their product, a failure that induces a downtime of just a few days can easily negate the yield attained through a 1% efficiency improvement. Oversizing the inverter, or introducing redundancy into the inverter system is one option to improve reliability, however this is often not economical.

1.1.2. Failures in Power Semiconductor Devices

Power semiconductors are a key element in converter systems. In a 2011 industry-based survey [2], 93% of respondents placed reliability as a primary issue in the field of power electronic converters. Power semiconductors were ranked as one of the most fragile components, with 31% of respondents considering them as the weakest link. This was followed by capacitors and gate drivers at under 20% and 15% respectively.

The junction temperature (T_j) and temperature cycling conditions form a considerable influence on power semiconductor reliability and performance. Failure mechanisms are generally separated into two categories: semiconductor-related failure mechanisms and package-related failure mechanisms. Wu *et al.* [3] define semiconductor-related failure mechanisms with two further groupings: short-circuit and open-circuit failures. Many of these failures are due to abnormal conditions rather than longer term wear-out fatigue induced by temperature cycling. Nevertheless, some semiconductor failure mechanisms such as latch-up (loss of control of an IGBT/MOSFET from the gate), leading to a short circuit, can be provoked through the accumulation of thermal fatigue [4].

The silicon semiconductor die is usually housed in a structure to form what is known as a power module. It is in these packaging materials that failures are most frequently observed. Figure 1-1 displays a typical structure of a traditional wire-bonded power module along with some of the common failure locations. These failures are primarily attributed to the differences in the coefficients of thermal expansion (CTE) of the various materials of the semiconductor die and package construction, combined with the temperature swings they experience [5].

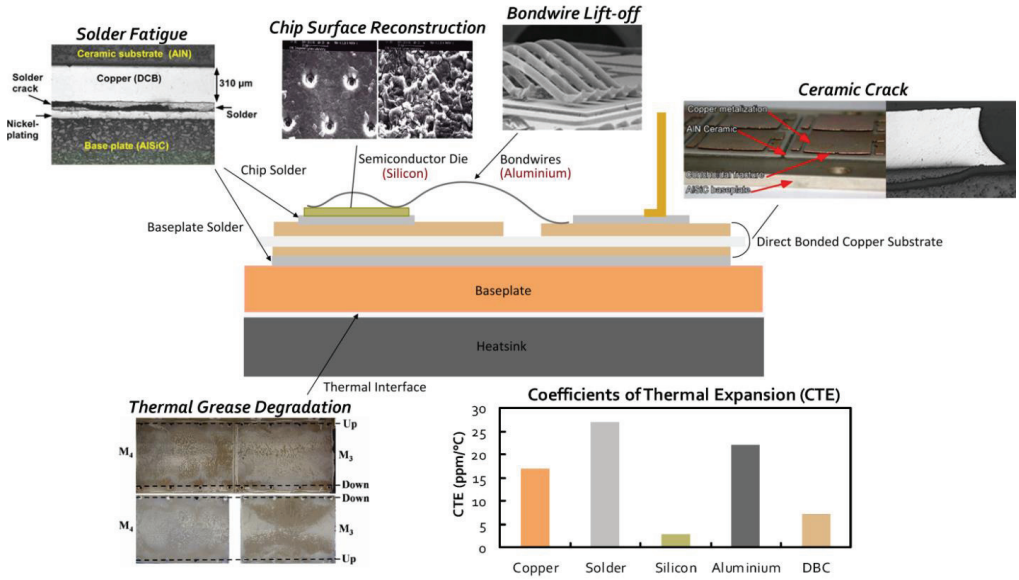


Fig. 1-1: Cross-section and common degradation locations of a traditional wire-bonded power module [6][7][8][9]

One of the largest mismatches in CTE is between the semiconductor die (silicon), and the bondwires and surface metallisation (aluminium) [5]. This mismatch is exacerbated due to the bondwire being bonded directly onto the surface of the die. Therefore, the power dissipation in the semiconductor, along with the ohmic self-heating of the bondwire, induce large temperature swings in the materials. Repeated thermal cycling then leads to stress that results in degradation of the bondwires and eventual lift-off from the semiconductor die itself.

The failure of a single or small number of bondwires can alter the current distribution in the module and increase ohmic resistances. If operation of the device is not halted before a suitable threshold, catastrophic failure can occur that can manifest itself in a number of ways. This could include melting of the remaining bondwires, thermal runaway in paralleled semiconductors, or triggering of parasitic events that lead to device destruction.

Outside of these categories, some system level degradations can also have a large impact on power semiconductor health. For example, Perpina *et al.* show how thermal grease displacement occurs during thermal cycling tests – leading to a deteriorated thermal conductivity between the heatsink and the power module [9]. Intermittent misfiring of the gate driver can also lead to catastrophic failures or repeated short periods of overstress [10].

1.1.3. Benefits of Accurate T_j Knowledge for Power Module Reliability

An active area of research in power module reliability is the development of condition monitoring systems. Much research has focused on monitoring electrical parameters that indicate degradation. In particular, the collector-emitter voltage (V_{CE}) at high current in IGBTs [11][12][13], and the evolution a module's thermal resistance (R_{th}) [8][14][15][16] have been studied since the 1990s.

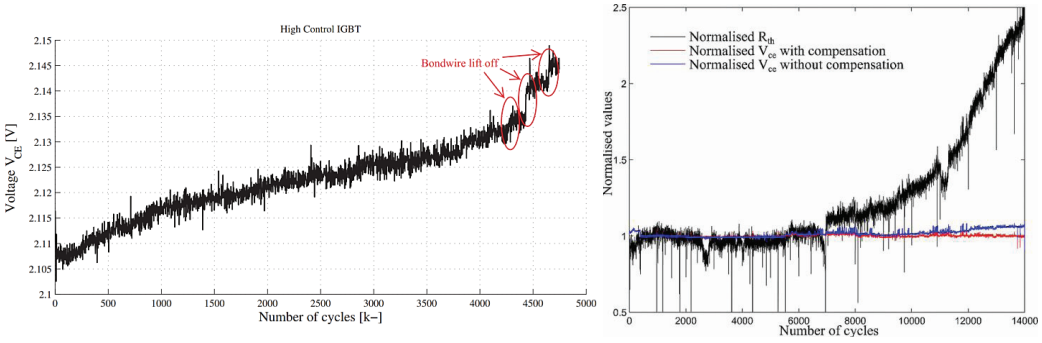
While these parameters readily observe degradation in laboratory conditions, they are ultimately influenced by numerous failure mechanisms. As such, they are difficult to use as a standalone parameter to monitor device degradation. This is especially the case for the V_{CE} at high current, which can be effected by junction temperature, gate oxide integrity, bond-wire fatigue, quality of electrical connections, and surface metallisation reconstruction. This manifests in aging trends for V_{CE} that are not consistent: increases of 5%, 7% and 20% before module failure have been reported in literature [11][13][17], while decreases of up to 25% were present in other studies [18][19].

As a result, interpreting parameters of this nature requires a thorough understanding of the relationship between the parameter, health condition, and operational profile. As a first principle, accurate real-time junction temperature knowledge can help identify which failure mechanism is dominant in the device, or more precisely determine when a degradation parameter signals a critical level of degradation.

Illustrating this point, Fig. 1-2a displays a commonly reported trend in the V_{CE} as an IGBT is subject to an accelerated aging test. The gradual increase of V_{CE} could be due to aluminium reconstruction increasing the ohmic sheet resistance, or degradation in the thermal path contributing to a gradual increase in T_j. On the other hand, sharp step increases in the V_{CE} can often be seen when a bond wire lifts off from the IGBT. Therefore, knowledge of T_j is necessary to reliably assess which failure mechanism is causing the increase in V_{CE}. In fact, some aging studies that monitor the V_{CE} attempt to compensate for T_j using electrothermal models (shown in Fig. 1-2b) [20], while others include a temperature sensitive parameter for T_j measurement in laboratory accelerated aging test benches [16][17][21][12].

Outside of the traditional V_{CE}, several alternative approaches have been proposed for damage evaluation in power modules. Principally, these indicators involve switching transients or

parasitic ringing variations in the device [4][23][24][25][26]. Nevertheless, these parameters are also intrinsically linked to junction temperature.



(a) *(b)*

Fig. 1-2:
(a) Increase of V_{CE} during accelerated aging test: step change indicates bondwire lift-off [22]
(b) V_{CE} increase during aging test with junction temperature compensation (red) and without (blue) [20]

Finally, precise knowledge of the amplitude and frequency of junction temperature swings could lead to better utilisation of model based prognostic systems that predict the remaining life of a power module [27]. This information could also be used to develop thermal control algorithms that regulate power losses to reduce thermal stress, and prolong module lifetime, when operating in a degraded condition [28].

1.1.4. Junction Temperature Estimation in Power Electronic Converter Design

The junction temperature is therefore a necessary consideration in the design of a converter system to ensure optimal reliability and operation. At a minimum, it must be guaranteed that T_j does not exceed the specified maximum limits under all operating conditions. Traditionally, T_j estimation has been performed using analytical calculations; in fact, some semiconductor manufacturers provide software tools for this purpose [29]. These calculations are usually based on datasheet values for both the electrical and thermal characteristics of the power module.

The junction temperature variation of a power semiconductor is generally a result of the power losses resulting from the application mission profile, in addition to changes in environmental conditions. Fig. 1-3 demonstrates an idealised evolution of T_j in a power module over time. The smaller and faster T_j cycles may be caused by the demands of the application, while the larger and slower cycles are a result of the environmental conditions.

An average junction temperature could be determined using one-dimensional stationary thermal models and neglecting thermal capacitances. If non-stationary phenomena are accounted for, it is possible to estimate the junction temperature swing, ΔT_j, and then the maximum junction temperature, $T_{j(max)}$, which must be respected for safe operation. Otherwise, a safety margin for the maximum junction temperature ripple must be included in the design of the cooling system. As a result, there is interest in developing more complex models for real-time T_j estimation [30].

Although these modelling techniques are widely used, there are several questions regarding their accuracy. Bruckner and Bernet [31] attempt to experimentally verify the accuracy of these estimations on IGBTs in a three-level voltage source inverter. They find that the estimated T_j is typically higher than the measured temperature via an infra-red camera – with realistic errors in the region of ±11%. This uncertainty can lead to an oversizing of cooling systems to ensure a proper level of reliability, at the expense of increased volume, weight and cost. Furthermore, the thermal and electrical characteristics of a power module alter over the lifetime of a converter [9] [32]; consequently, these calculations are not valid during the entire lifecycle of the module.

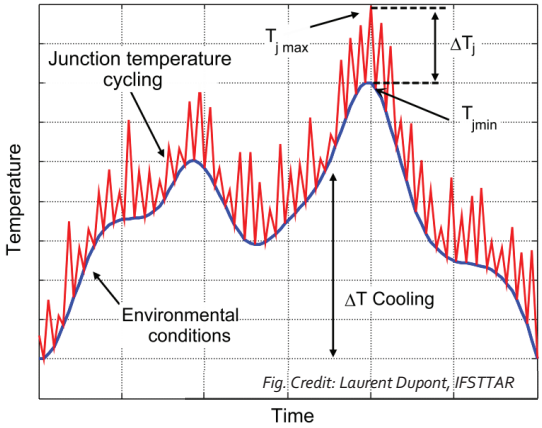


Fig. 1-3: Typical idealised evolution of junction temperature in a power module over time

1.1.5. Thesis Scope

Since model based junction temperature estimation is prone to error, an accurate method for real-time junction temperature measurement would be beneficial. Nevertheless, direct measurements of junction temperature in power semiconductors are problematic: access to the semiconductor die is blocked by the packaging materials.

Consequently, this thesis focuses on a group of indirect measurements known as Temperature Sensitive Electrical Parameters (TSEPs). Here, the temperature dependent electrical behaviour of the semiconductor is used as the temperature sensor. The measurements are therefore non-invasive. This work focuses on developing TSEP-based methods for power semiconductor switches, which encompasses both IGBTs and MOSFETs.

1.2. Main methods of real time junction temperature measurement

Sensing junction temperature during converter operation is difficult, and the selection of a measurement method should be made with respect to the application. The main dilemmas in the selection or design of a temperature measurement system are displayed in Fig. 1-4 and entail:

- Accuracy:
  - ↳ The desired accuracy vs. actual T_j: a measurement of baseplate temperature may be sufficient to indicate a fault in the heatsink or cooling

system, while measurements of actual die or bondwire temperatures may be required for thermal control algorithms.

- Time resolution:
  - ↳ Some measurement methods are unable to track short temperature cycles induced by load current and can only provide an averaged value over a number of seconds.
- Cost-benefit trade-off
  - ↳ Aside from the initial implementation cost, methods of junction temperature measurement may disrupt power module operation in a number of ways.

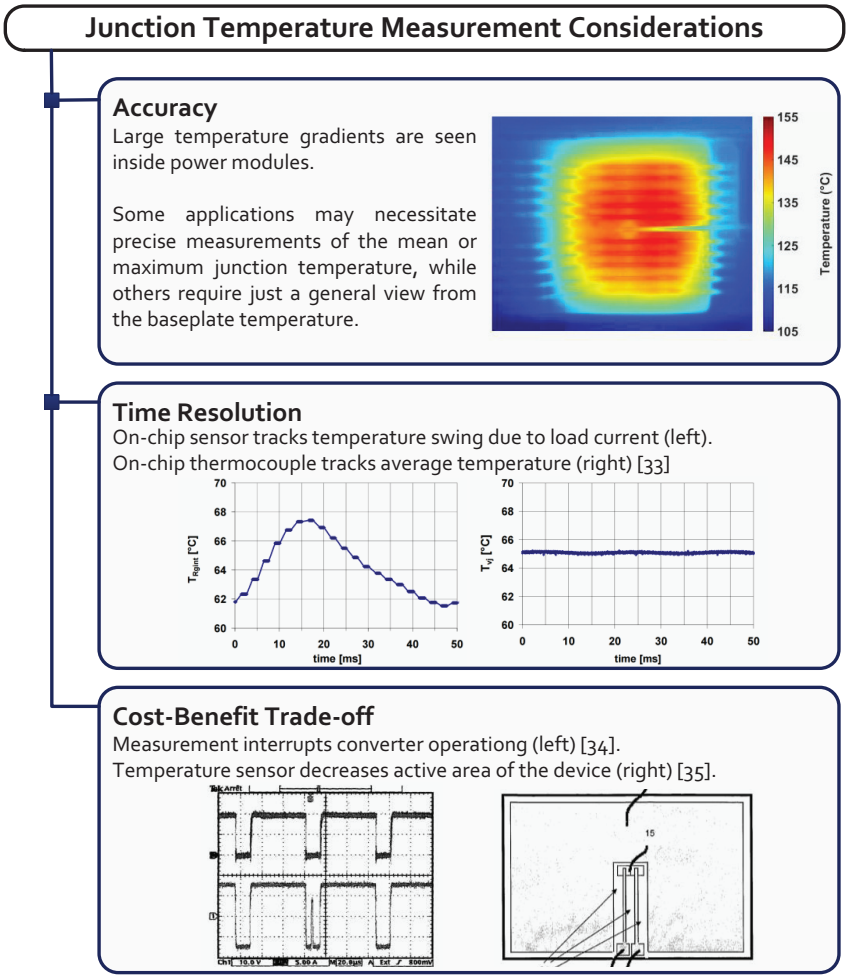


Fig. 1-4: Considerations for designing or selecting a junction temperature measurement method

1.2.1. Direct Temperature Measurement Methods

In laboratory settings, a variety of T_j measurement methods are available. If direct access to the semiconductor die is possible, optical and physical contact methods such as infra-red (IR) cameras or optical fibres can be used to map temperature inside the power module. Fig. 1-5 displays an open IGBT module with optical fibre thermal sensors in direct contact to several of the dies, allowing temperature measurements at high voltage during IGBT operation [36]. Nevertheless, this solution is limited by the response time of the sensor (25ms). Multiple optical fibres can also be used on the same die to map the temperature distribution across the die surface [37].

For IR camera measurements, the removal of the dielectric insulating gel is required. Additionally, both the die and bondwires must be painted to create a uniform emissivity across the surface [38]. If care is not taken, an excessively thick layer of paint can have an impact on the thermal operating environment, and high voltage operation may be unsafe due to the absence of dielectric gel.

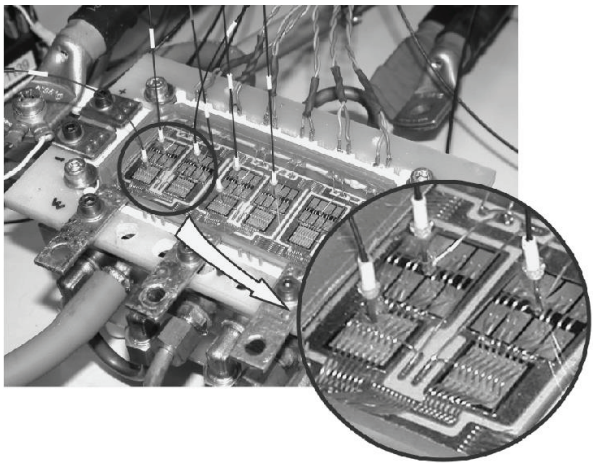


Fig. 1-5: Power module with integrated optical fibre thermal sensors [36]

Since direct access to the semiconductor is usually prevented by the module packaging, electrical methods are often preferred for temperature measurements in power modules. Two families are outlined in scientific literature: firstly, the use of supplementary electrical sensors located on the chip surface; and secondly, the use of the semiconductor's electrical behaviour.

In the category of supplementary sensors, a common approach is to use a diode, or string of diodes, fabricated on the chip surface. Because the forward voltage drop of a diode has a linear relationship with temperature, it is possible to use it as a temperature indicator. An example of this is displayed in Fig. 1-6; in fact, commercial examples already exist [39][40]. These sensors provide accurate measurements and fast response times, but the increased complexity of the power module is a drawback: a temperature sensing diode decreases the active area of the die, and requires additional contact pads and packaging terminals.

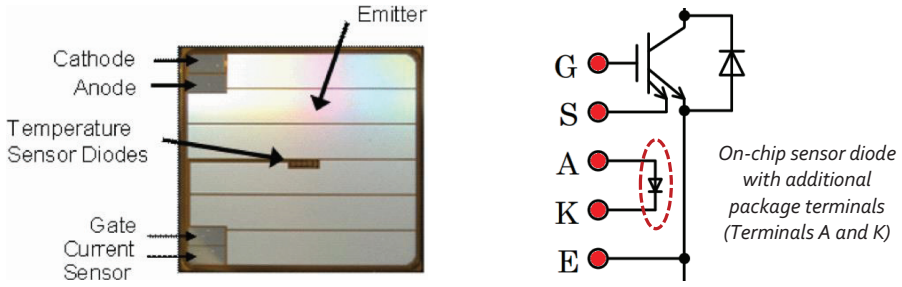


Fig. 1-6: On-chip supplementary temperature sensors [39][40]

These sensors also provide local temperature measurements, which can present some issues. For instance, Fig. 1-7 displays a map of the temperature distribution in two IGBTs, in which the peak temperature results from a solder void located in the backside of the chip. Unless a sensor is situated in the immediate vicinity, a local measurement is unable to detect the presence of peaks such as this. In fact, if the sensor is not optimally placed, the measured temperature could be more than 20°C below the maximum.

In order to have a good representation of the global surface temperature, Thollin *et al.* [41] present a functional power semiconductor die containing an array of 13 temperature and voltage sensors. They are made with a deposition of a thin thermo-sensitive polysilicon layer and located inside the top metallisation. In this case, multiple external wires are needed to obtain the temperature value given by each sensor; therefore, the setup becomes increasingly complex.

Another sensor solution requiring power module modification is outlined by Brekel *et al.* [33]. A modified IGBT substrate layout, including a gate connection with dual contact pads, is used to provide room for sensing equipment that facilitates the measurement of the internal gate resistance. The temperature dependence of this resistance is then used to evaluate the semiconductor temperature.

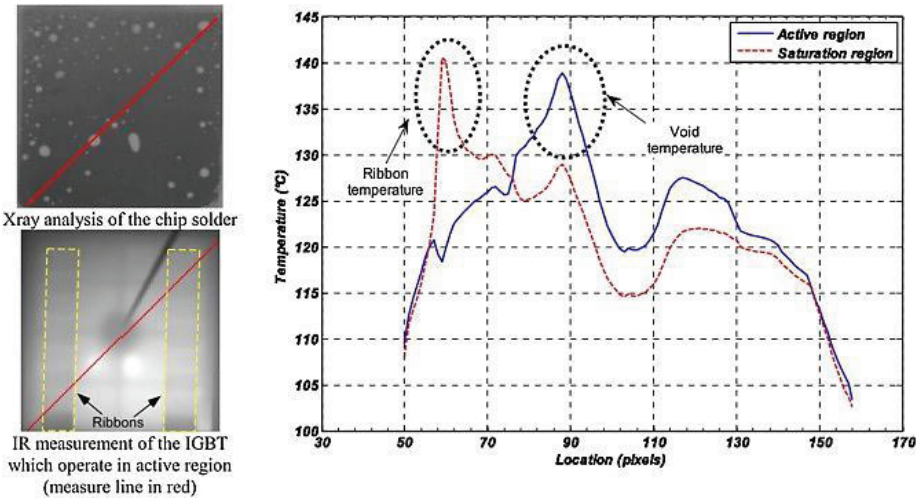


Fig. 1-7a: Temperature distribution in an IGBT chip with peak temperature caused by a solder void [42]

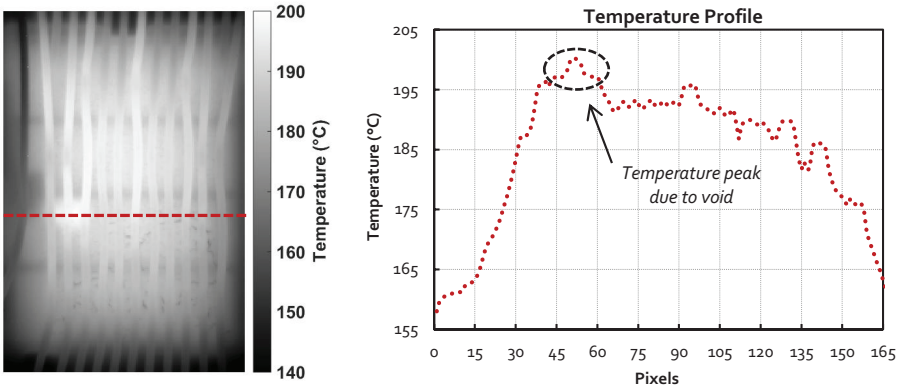


Fig. 1-7b: Temperature distribution in an IGBT chip with peak temperature caused by a solder void

1.2.2. Temperature Sensitive Electrical Parameters (TSEPs)

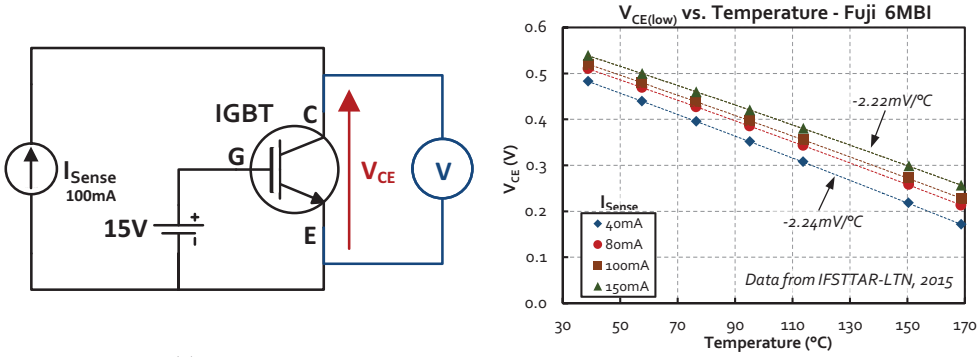
The observation of junction temperature without modification to the die or packaging can be achieved through the use of temperature-sensitive electrical parameters (TSEPs). These approaches directly use the electrical behaviour of the semiconductor as the temperature sensor, which theoretically allows for instantaneous junction temperature measurements. The electrical parameter that is selected for use is usually calibrated with respect to temperature by setting the power module to a series of known temperatures and recording the electrical parameter to create a look-up table. Typically, just one representative temperature can be extracted and is assumed to be influence by the entire active area of the die – multiple measurements cannot be extracted to create a temperature distribution profile.

TSEPs have been used to perform thermal characterisation of semiconductors for a number of years. Reviews of the variety of TSEPs are provided by Blackburn [43] in 1988, and more recently in 2012 by Avenas, Dupont and Khatir [44].

The most commonly used TSEP is the voltage drop under a low current injection ($V_{CE(low)}$). This TSEP has been used for thermal measurements in bipolar transistors for many decades [43][45][46], and takes advantage of the temperature dependence of the voltage drop across a PN junction.

The measurement process is very simple and demonstrated in Fig. 1-8 for an IGBT: a constant sensing current generally in the range of 1mA – 100mA (or approximately 1/1000th of the device current rating) is fed into the power device and the subsequent voltage drop is measured. In silicon devices, this parameter generally exhibits a negative temperature dependence of approximately -2mV/°C. The $V_{CE(low)}$ vs. temperature on a Fuji 1200V/100A IGBT module for a variety of sensing currents is shown in Fig. 1-8, where a temperature sensitivity of between -2.22mV/°C and -2.24mV/°C is apparent. The $V_{CE(low)}$ can also be seen to depend highly on the value of the sensing current. Therefore, the sensing current must be strictly controlled and a measurement of $V_{CE(low)}$ is not possible during normal load current commutation.

Typically, the $V_{CE(low)}$ has been used for offline characterisation or in current cycling setups [12], where the sensing current is injected into the device after a short delay (perhaps a few hundred μs) once the load current has been removed. The $V_{CE(low)}$ can then be recorded as the device is cooling, and a linear regression vs. the square root of time can be used to estimate the temperature value at the moment the load current is switched off [43][46].



(a) *(b)*

Fig. 1-8: (a) Electrical circuit for measurement of the most common TSEP, $V_{CE(low)}$ (b) $V_{CE(low)}$ on a Fuji 6MBI100VA-120-50 IGBT measured with a variety of sensing currents

The $V_{CE(low)}$ is widely used since most power semiconductors contain a PN junction in their structure (e.g. diodes, IGBTs, base-emitter in bipolar transistors). For MOSFET devices, the $V_{CE(low)}$ can also be used by applying the method to the intrinsic body-diode; however, the threshold voltage (V_{TH}) has been traditionally used with more accurate results [47].

Nevertheless, temperature measurements using TSEPs in power semiconductors during normal operation are not well developed. Issues surrounding their use range from the need to separate of the effects of temperature from inherent electrical variations, to significant errors in accuracy of the measurements.

In the past three years, a significant amount of research has been disseminated on this topic. Table I displays a synthesis of publications where a TSEP has been investigated for use in online junction temperature measurement (i.e. during normal semiconductor operation). Some of the key concepts will be outlined in the following subsections. In order to ease this process, the TSEPs have been divided into three main categories:

- **Classical TSEPs:** This includes the use of traditional TSEPs such as $V_{CE(low)}$, V_{TH} and the saturation current (I_{sat})
- **Static characteristic:** Principally, this involves the on-state voltage drop at high current
- **Dynamic characteristics:** These measurements generally consist of using the transient switching parameters of the device

The main implementation issues and barriers to using TSEPs in operating power semiconductors will be summarised. From this, technical objectives for the PhD are formulated.

1.3. Literature Review of Online TSEP Proposals

1.3.1. Classical TSEPs

Classically used TSEPs are attractive since significant knowledge on these measurement techniques is already available and the methods are well characterised. For example, the $V_{CE(low)}$ has been repeatedly demonstrated to provide accurate results close the mean junction temperature of the chip [48][49]. This is also true for V_{TH} [44][47].

The main drawback in the use of classical TSEPs is that they typically have to be performed in specific electrical conditions, and thus many attempts to incorporate the measurements in converter setups have required significant modification to the converter or control strategy. This can include the addition of supplementary components, momentary disconnection of power devices from the power circuit, and interruption to normal load current control.

Regarding the most common TSEP, $V_{CE(low)}$, temperature measurement can be conducted in inverters when the output current crosses close to zero [21][50]. An accompanying delay is consequently necessary in order to have enough time to complete the measurement [21]. Alternatively, some authors propose to include supplementary switches in order to momentarily interrupt the load current and isolate the characterised devices while the temperature measurement takes place [51][52]. This is displayed in Fig. 1-9, where Forest *et al.* place additional MOSFETs and IGBTs in the load line of an H-bridge inverter, allowing the load current to be diverted in under 1µs. A 100mA sensing current can then be injected into the desired IGBT and a measurement of $V_{CE(low)}$ performed. The total delay for this procedure amounts to a few hundred microseconds.

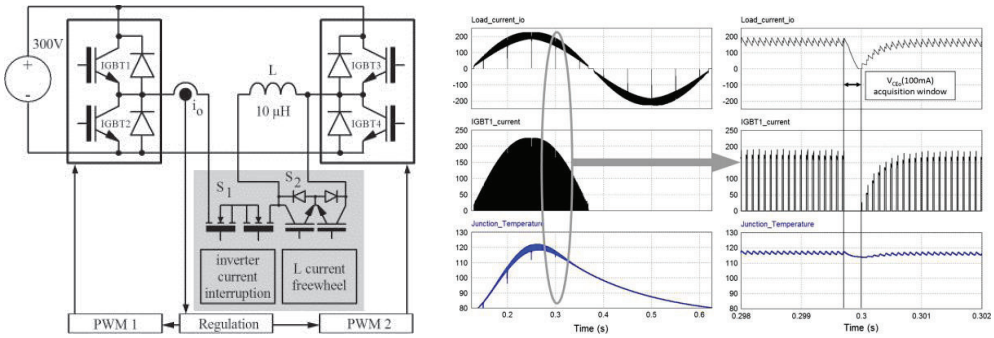


Fig. 1-9: $V_{CE(low)}$ measurement during inverter operation using supplementary switches [52]

The $V_{CE(low)}$ has also been proposed for online measurements in MOSFET devices by applying the method to the body-diode [53]. Likewise, this application required momentary disconnection of the MOSFET from the power circuit.

For $V_{TH,}$ measurement in both IGBTs and MOSFETs has been proposed in several publications. In the case of MOSFETs, measurement circuits included an additional gate resistor of several kΩ which could be used to slow down the turn-on transition when a measurement is desired [54]. A disconnection of the MOSFET from the main power circuit was also required in order to force the drain current to a fixed, low value of several mA.

TABLE I. LITERATURE REVIEW OF TSEPS INVESTIGATED FOR ONLINE USE

Method		Comments						
		Device	***Dependents***	***Additional Comments***	***Potential Measurement Frequency***	***Linearity***	***Required Sensing Resolution***	***Reference***
Classical TSEPs	Short Circuit Current	IGBT	T, V	Induces a Hard Switching Fault to create short circuit.	Very Low	Good Linearity	Depends on device (0.15% of max I_{short} per °C)	[59]
	Saturation Current	MOS Transistors	T, V	Partially turns on the device with a low gate voltage during the off-state	Unknown	Non-Linear (Exponential)	Varies depending on temperature range	[34]
	$V_{CE(low)}$	Transistors and Diodes MOSFET Body-diode	T	Requires specific current low current level. Requires interruption to normal load current.	Low (when load current comes close to 0A or interrupting operation)	Good Linearity	2mV/°C in silicon devices	[21] [50] [51] [52] [53]
	V_{TH}	IGBTs, MOSFETs	T	Possible disconnection of the device from power circuit May require increased gate resistor Dependence on load current according to extraction method	Dependent on measurement circuit	Good Linearity	4 - 10mV°/C May require measurement synchronisation accuracy in nanoseconds	[54] [55] [56] [57]
Static characteristic	$V_{CE(high)}$	IGBTs, Diodes, MOSFETs	T, I, V_{GE}	Requires very accurate current sensors Generally inaccurate temperature measurements	High (each on-state)	Good Linearity	±2-3mV/°C Sensitivity depends on current level and device type	[62] [63] [64] [65] [66] [67] [68]
Dynamic characteristics	IGBT Turn-Off	IGBT	T, I, V, V_{GE}	Dependent on a high number of inherent electrical variations	High (Each Switching Cycle)	Good Linearity	ns/ps per °C	[72] [73] [74] [69] [75] [76] [78]
	Turn-On Delay	MOS Transistors	T, V, V_{GE}	Closely related to V_{TH}	High (Each Switching Cycle)	Good Linearity	ns/ps per °C	[69] [70] [71]
	Rise-Time	MOS Transistors	T, I, V, V_{GE}	Dependent on a high number of inherent electrical variations	High (Each Switching Cycle)	Good Linearity	ns/ps per °C	[69] [71]

For V_{TH} in IGBTs, several authors use the induced voltages over the parasitic inductances of the packaging to trigger a measurement of the gate voltage as the IGBT turns on [55][56][57]. This gate voltage value is then assumed to be V_{TH}. Since the IGBT is not disconnected from the power circuit (and in particular the collector current is not controlled), this V_{TH} extraction may be influenced by collector current variation [56][58]. Furthermore, unless the external gate

resistance is significantly larger than the internal gate resistance, the sensitivity of the method is impaired. Low values of gate resistor can also mean that measurement synchronisation jitter in the region of 10ns can induce significant errors [55].

Another known TSEP for power-MOS devices is the saturation current (I_{sat}) under a given gate-emitter (gate-source) and a given collector-emitter (drain-source) voltages. Bergogne *et al.* [34] use this technique when the semiconductor is in off-state by partially turning on the device for 2µs with a gate voltage of around 6V. As with the $V_{CE(low)}$, interruption to normal converter operation is a primary drawback (shown in Fig. 1-4). In addition, I_{sat} has an exponential relationship with temperature which could present difficult calibration procedures [34][49].

A similar method is presented by Xu *et al.* [59], who study the short circuit current as a TSEP in a 2-level inverter. Here, a hard switching fault is induced during inverter operation with the use of supplementary switches, and the peak short circuit current measured. The foremost problem here is a very high thermal dissipation during the short circuit which can cause fast thermal runaway. Logically, the measurement frequency is very limited since repetitive short circuits could cumulatively degrade the device. Another facet of this method is ensuring that negligible self-heating is present before a measurement of the peak short circuit current can performed. Consequently, a very low stray inductance in the current loop is a likely requirement.

As a conclusion, it appears that temperature measurements are possible during the operation of a converter using classical TSEPs. However, the modification to the structure of the converter and/or its operation can be seen as a serious drawback. It is therefore important to find TSEPs that are electrically suited to online temperature measurements: static and dynamic characteristics are both potential solutions.

1.3.2. Static Characteristic

Because the IV characteristic of all power devices depends on the temperature, an obvious way to estimate the junction temperature of a device would be to simultaneously measure its forward voltage and current ($V_{CE(high)}$). This is an attractive option since opportunity to measure this TSEP occurs naturally in every switching cycle. Moreover, current sensors are generally already included in converter setups, and several measurement circuits have recently been presented that allow measurement of the forward voltage in real operating conditions [60][61]. This method has been used by several different authors in recent years [62][63][64][65][66][67].

Issues with the $V_{CE(high)}$ approach stem from the fact that power modules do not permit electrical measurements on solely the semiconductor die – individual dies are connected to the 'outside' (and thus any measurement system) through a series of interconnections, bond-wires and packaging materials. The ohmic voltage drop of these materials becomes significant at higher current and significantly impacts the measurement. Therefore, the layout of the module has a large influence on the method. Typically, the interconnection and packaging materials will be at different temperatures to the die during operation and introduce large errors in the temperature measurement. These errors have been documented in a number of publications and can exceed ±30°C [62][67]. The inaccuracy also exists in MOSFET devices when similarly using $R_{DS(on)}$ as a TSEP [47].

To counteract this problem, Choi [65] and Ghimire [66] propose the use of a correction factor. Although providing accurate results, this correction factor is generated directly from measuring the module resistance, coupled with measurements made via an IR camera or through FEM simulations. A thorough knowledge of the exact layout inside the module, or indeed an open module to perform measurements on, is consequently required to formulate the corrections. Additionally, due to the natural variation of V_{CE} through bondwire lift-off or aluminium surface reconstruction, this correction factor needs constant recalibration as the device ages.

An alternative correction method is proposed by Dupont and Avenas [67], which mathematically reduces the resistance contribution to zero. Here, the V_{CE} is measured at two different gate voltages (15V and 13V), and the difference between the two measurements is used as the TSEP. This method is reported to reduce measurement errors to usually within -5°C, as well as being reasonably unaffected by bond-wire lift-off. Nevertheless, an advanced gate driver providing fast transition between two different stable turn-on voltages, along with a high degree of post-processing of measurement data, would be required to perform the measurement.

This leads to another fundamental issue with $V_{CE(high)}$: the dependence on gate voltage (V_{GE}) as well as load current. If the gate driver turn-on voltage is not stable with performance demands or ambient temperature, a method to compensate for these fluctuations may be necessary. Finally, the sensitivity of the TSEP is particularly dependent on the current level, and can range from a negative dependency at low current, to a positive dependency at high current. A crossover point is also present where the temperature dependence of $V_{CE(high)}$ is negligible. Both of these issues are displayed in Fig. 1-10 on a Fuji 6MBI100VA-120-50 IGBT module.

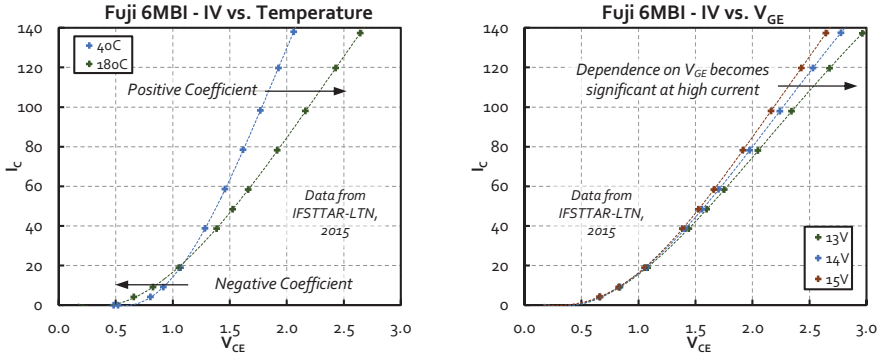


Fig. 1-10: IV Characteristic ($V_{CE(high)}$) vs. Temperature and V_{GE} for a Fuji1200V/100A IGBT Module

Lastly, the accuracy of the current sensors can present an issue. Table II shows the results of temperature measurement using $V_{CE(high)}$ on an Infineon SIGC100T60R3 IGBT while lightly varying the current measurement. It can be seen that a current variation of only 0.5% introduces a temperature measurement discrepancy of close to 4°C. Therefore, the current sensor requires excellent accuracy and synchronisation with voltage measurement in order obtain reliable temperature values.

TABLE II. EFFECT OF THE CURRENT LEVEL ON $V_{CE(HIGH)}$ TSEP

	Current close to 80A		Current close to 100A	
Current (A)	79.8	80.2	99.8	100.2
Estimated temperature (°C)	111.2	116	150.5	154

Data from IFSTTAR, LTN

1.3.3. Dynamic Characteristics

The dynamic (or switching) characteristics of a power module are another attractive group of TSEPs since a measurement opportunity presents itself in each switching cycle. In the case of IGBTs and MOSFETs, several different TSEPs are available: the turn-on delay [69][70][71], the turn-off delay [69][72][73][74][75][76][78], and the current slope during turn-on [69][71].

These measurements are constrained by the need for very fast sensors as the sensitivity of the TSEPs can be in the range of several ns/°C or even ps/°C in smaller devices. A particularly developed TSEP in this category appears to be the use of the length of the miller plateau during turn-off in an IGBT. A similar approach is presented in two publications [75][78]. In both cases, authors show the possibility to generate two automatic pulses that signify the start and the end of the miller plateau; these two pulses could then be used to trigger a time-to-digital converter. The sensitivity here appears to be in the region of 1-5ns/°C for medium-high power devices.

Dynamic characteristics however are particularly susceptible to inherent electrical variations induced by the operating conditions. For example, the turn-off time in the TSEP described above may be influenced by: temperature, DC voltage, load current, control strategy, and fluctuations in gate driver performance. A high number of dependents would seemingly suggest increased complexity in both the calibration process, as well as in actual use in a converter setup.

Anyhow, Sundaramoorthy *et al.* [76] demonstrate a technique to simultaneously measure both temperature and current by using the voltage over the parasitic emitter inductance during turn-off. The peak value of this voltage is dictated by the current slope (which is temperature dependent), while the integral of the voltage is determined by the total current being switched.

Validation of the accuracy of TSEPs based on switching times appears to be scarce in scientific literature. Sundaramoorthy *et al.* [77] provide a validation of the previously mentioned junction temperature measurement via the miller plateau length, but the validation does not include comparisons with infra-red measurements and is performed on a closed module. Therefore, temperature measurements made using these methods should be made with caution, especially given the influence of numerous electrical parameters.

1.4. Additional TSEP Implementation Issues

In addition to those highlighted above, some other general implementation issues also surround the use of TSEPs during normal operation of power semiconductors. These general issues are briefly outlined in the following paragraphs and principally include: calibration requirements, and the accuracy of TSEP measurements.

1.4.1. Calibration Requirements

Before using a TSEP, it is necessary to obtain its relationship with temperature. This procedure can be more or less complex depending on the properties of the TSEP in question.

First of all, the linearity of the TSEP and number of electrical dependents can be a good indicator of the time and post processing requirements. The amount of time consumed in the calibration process depends upon the number of calibration points desired, and the time required to heat the power module to the desired series of temperatures. If the TSEP is linear with no electrical dependents, only a few calibration points are needed. In this category, the $V_{CE(low)}$ appears to be the most ideal TSEP, since it has a linear dependency on temperature and calibration is only required at one low current level (around $1/1000^{th}$ of the rated current).

For a large number of devices of the same batch and part number, the variability of the TSEP between each device is of great interest. Ideally, all devices would have an identical calibration curve, so that one set of data could be used across the entire batch. If the temperature sensitivity does not vary from device to device, then a single calibration point may be adequate in order to adjust for the variance of the absolute value of the TSEP parameter. Again, the $V_{CE(low)}$ demonstrates the most ideal properties in this category, for which most silicon devices will display a temperature sensitivity of around -2mV/°C. Most TSEPs however generally display some variation between devices. In particular, V_{TH} demonstrates a non-negligible variation between chips of the same type [21][47][49]; while TSEPs that are influenced by module layout, such as $V_{CE(high)}$, will also require individual calibration. This is displayed in Fig. 1-11a, where the $V_{CE(high)}$ for two IGBTs from inside the same module are shown, and a clear offset can be seen.

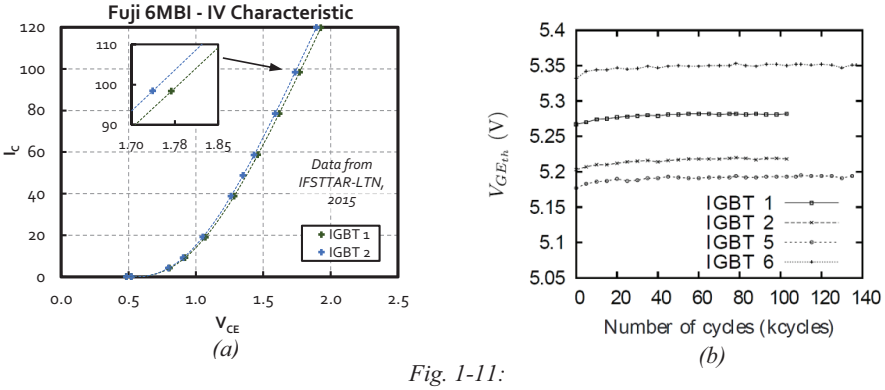


Fig. 1-11:
(a) IV characteristic for two IGBTs inside a Fuji 6MBI100VA-120-50 module – an offset in the TSEP can be seen between the two IGBTs
(b) V_{TH} during power cycling on four IGBTs from the same module [21]

Another pressing issue for calibration is the stability of TSEPs as the power module ages. Fig. 1-11b shows the V_{TH} for four IGBTs inside a power module throughout a power cycling test. A clear offset between the V_{TH} of each IGBT can be seen, as well as a variation as the power cycling test progresses. If the TSEP changes significantly during a power module's lifetime, periodic TSEP recalibration may therefore be required.

Finally, it is usually assumed that the entirety of the power module, including the die and packaging materials, is at a uniform temperature set by the oven or hot-plate used in the calibration procedure. However, this is not valid for TSEPs that require calibration at high current levels, since non-negligible self-heating is induced in the device. As a result, calibration has to be performed with short current pulses (from 10 to 100 microseconds) in order to keep self-heating to a minimum.

Alternatively, Dupont and Avenas present a compensation technique that uses the $V_{CE(low)}$ to adjust for the self-heating during the high current calibration pulses of $V_{CE(high)}$ [67]. This technique involves measuring the junction temperature of an IGBT via $V_{CE(low)}$ directly before, and after, the high current calibration pulse. To estimate self-heating, $V_{CE(low)}$ is recorded after the calibration pulse for a period of a few hundred microseconds and extrapolated back to the point at which the calibration current is removed. The measurement is then compared to the junction temperature via $V_{CE(low)}$ from directly before the calibration. Using this technique, an estimation of the self-heating in an Infineon FS200R12PT4 IGBT module is shown in Fig. 1-12. It can be seen that, for a high starting temperature of 150°C and a 120A calibration pulse lasting 300µs (IGBT is rated for 200A), the self-heating induced can close to 2°C.

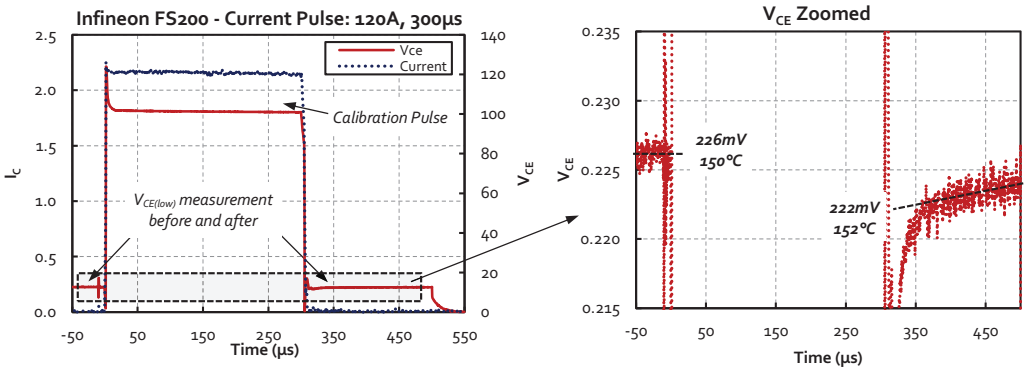


Fig. 1-12: Self-heating during high current pulse, estimated using $V_{CE(low)}$

1.4.2. Accuracy of TSEP Measurements

The term 'junction temperature' is ambiguous, since the temperature of a power semiconductor cannot be described using a single temperature value. Instead, the junction is made up of a distribution of temperatures. A clear demonstration of this is in Fig. 1-7, where the surface temperature of the IGBT dies can span up to 30°C when measured via an IR camera. In some conditions, a non-negligible temperature gradient may also be apparent with respect to depth [79]; nevertheless, direct measurements of the die surface (such as via IR camera) are usually taken as representative of the junction. As a result of this ambiguity, the 'accuracy' of a TSEP measurement depends on the desired temperature to be measured: whether this is the mean, maximum, or some other pertinent temperature of the device.

Inconsistencies between TSEP measurements have in fact been found as far back as 1966, where researchers placed the maximum temperature of the junction with most importance [45]. Since then, there is ample research to back up the assertion that TSEPs deliver different temperature

measurements on the same device. These discrepancies may also change depending on the device and dissipation conditions [42][47][49]. An example of this is shown in Table III, which displays the results of a study where three different TSEPs are used on a variety of power MOSFETs. It can be seen that on MOSFETs 3 and 5, the temperature measurements via TSEPs can diverge over 10°C. On the other hand, the TSEPs used on MOSFETs 2 and 4 show a divergence of only 3°C.

TABLE III. TEMPERATURE MEUSUREMENTS ON POWER MOSFETS USING DIFFERENT TSEPS [47]

	Measured Temperature (°C)			
MOSFET Type	IR Radiometer (Max)	V_{TH}	$V_{CE(low)}$ (body-diode)	$R_{DS(on)}$
1	33.5	31.0	28.8	25.7
2	38.0	35.0	36.5	33.4
3	80.0	80.3	70.7	69.2
4	37.0	36.8	36.1	33.0
5	73.0	69.0	62.0	56.0

As a result, any new TSEP proposal should undergo experimental validation and comparison with a direct measurement method, in order to specify what temperature of the device is being measured. Additionally, since TSEP concepts are generally substantiated on new power modules, it is not clear whether all TSEPs provide repeatable measurements throughout the entire module lifetime. The accuracy should therefore also be assessed on power modules that are in a degraded condition.

A particular source of inaccuracy can come when using TSEPs on modules with paralleled semiconductors dies. For example, both V_{TH} and I_{sat} have been demonstrated to give inconsistent errors depending on which particular die is most thermally stressed in the case of two IGBTs in parallel [49].

A further limitation encountered with several paralleled dies is that a TSEP typically only provides a single temperature, but large temperature distributions may be seen inside power modules with multiple dies. To map the temperatures of each chip, some authors have proposed methods which involve taking several TSEP measurements in different electrical conditions, and then using numerical techniques to extract individual temperatures [80].

1.5. PhD Objectives

1.5.1. Research Questions

From the literature review of TSEP studies, several research questions emerge:

- Can a TSEP be implemented in a converter without undue disruption to power module operation?
- Is there a simple way to separate the effects of temperature from inherent electrical fluctuations? Alternatively, is a TSEP available that is solely dependent on temperature?
- What is the level of accuracy of the TSEP?
- What would be the level of complexity of the TSEP calibration procedure?

- Can a TSEP be robust and reliable throughout the lifespan of the device and withstand the effects of power module degradation?

1.5.2. Technical Objectives

As a result, the PhD has several technical objectives. In short, the PhD should develop a new TSEP, or an improvement to an existing TSEP, that has the following features:

- Measured in the normal operating cycle of a power semiconductor switch (MOSFET or IGBT) without disruption to operation or control strategy
- Does not require a calibration procedure with complex post-processing
- Is independent from inherent electrical variations outside of temperature, or allows easy separation of the effects of temperature

In addition, the PhD should also:

- Validate the temperature measurement provided by the new TSEP via direct measurements such as optical fibres or an IR camera.
- Perform this validation on multiple types of semiconductor (MOSFET or IGBT), and on paralleled semiconductor dies
- Assess the effect that common power module degradation mechanisms have on the accuracy of the TSEP

II. Proposed TSEP Measurement Methods

In this chapter, electrical methods for junction temperature measurement in IGBTs and MOSFETs are presented. Predominantly, a measurement method called the 'Peak Gate Current' is focused on, which involves detecting the peak voltage over the external gate resistor during the turn-on delay. This voltage is then used to calculate the internal gate resistance, which is a temperature dependent electrical parameter. The theoretical background for the temperature measurement is explained, along with experimental verification provided on IGBTs. Primary advantages of the method include an immunity to load current variation, a good linear relationship with temperature, and an autonomous measurement circuit that can be integrated into a gate driver without disruption to operation. Both the advantages and disadvantages of the method will be discussed.

An additional electrical method considered during the PhD period will also be briefly outlined. However, this was not extensively studied. Both envisioned methods do not require compensation for load current, as this was seen to be a major contributor to some of the implementation issues outlined in Chapter 1.

2.1. Internal Gate Resistance - R_{Gint}

To achieve the technical objectives stipulated in section 1.5.2, developing a TSEP that would be uninfluenced by load current variation was a key focus. Such a TSEP would hold multiple advantages. Firstly, the calibration procedure would comprise of few measurement points; secondly, accurate and synchronised load current measurements would not be required.

The internal gate resistance (R_{Gint}) of an IGBT or MOSFET is one electrical parameter that is not influenced by load current. The R_{Gint} of an IGBT or MOSFET has conventionally been a distributed resistance of the gate that influences the propagation delay of the gate signal across the die [81]. In power modules that include paralleled power MOS transistors, manufacturers often increase the size of R_{Gint}, or include additional integrated resistors in the die, in order to prevent high frequency oscillations and to improve current sharing [82][83]. The temperature dependence of R_{Gint} is a consequence of the temperature coefficient of resistivity for poly-silicon, which is often the material of manufacture.

Using R_{Gint} as a TSEP is particularly appealing since a review of academic literature reveals previous investigations using R_{Gint} for temperature measurement in both MOSFETs and IGBTs [33][84]. Nevertheless, both of these investigations required a modified substrate layout to facilitate the measurement. By modifying the substrate to include a gate connection with dual contact pads, a four-point probing technique could be used to measure the ohmic resistance of the gate. This measurement principle is depicted in Fig. 2-1. Taking Fig. 2-1b on an IGBT, a constant sense current of 500mA is applied at the connections F1 and F2, which creates a voltage drop over R_{Gint}. This voltage is then measured through connections S1 and S2. Because the resistance depends on temperature, the measured voltage drop varies and is used as the temperature indicator.

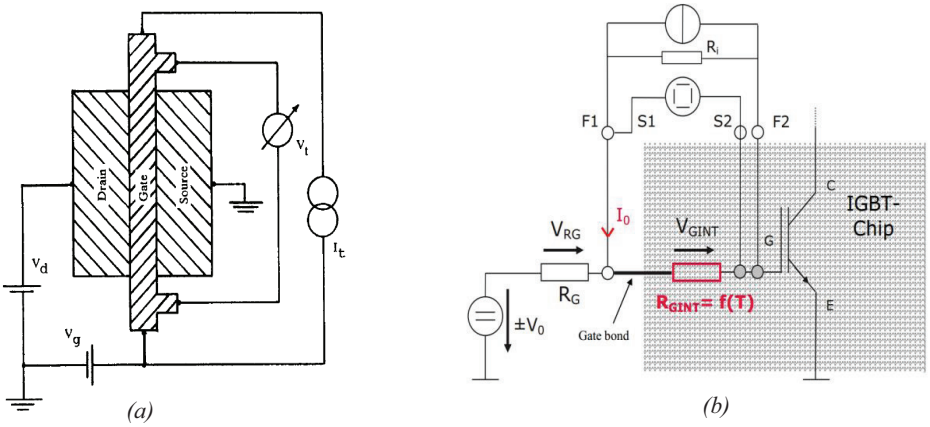


Fig. 2-1: R_{Gint} measurement principle using modified substrate for (a) MOSFETs [84] and (b) IGBTs [33]

The modification of the substrate layout and the need for additional measurement equipment inside the power module can be seen as a drawback to this approach. Consequently, the following subsections will identify measurement principles that allow the temperature variation of R_{Gint} to be viewed on any standard power MOSFET or IGBT module – without modification to the device substrate or packaging.

2.1.1. R_{Gint} Measurement on Standard Power Modules

For the purpose of temperature measurement in standard power modules, R_{Gint} is considered to be the equivalent series resistance (ESR) of both the gate-emitter and gate-collector capacitance (gate-source and gate-drain capacitance in MOSFETs), as shown in Fig. 2-2.

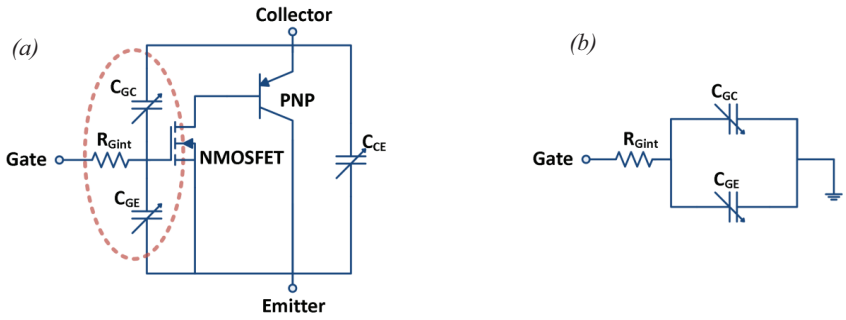
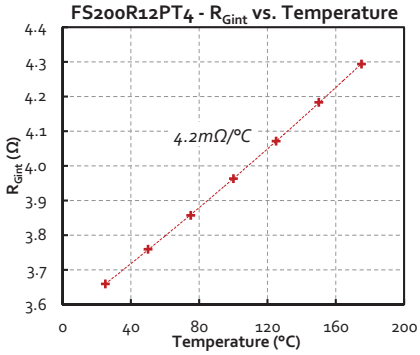
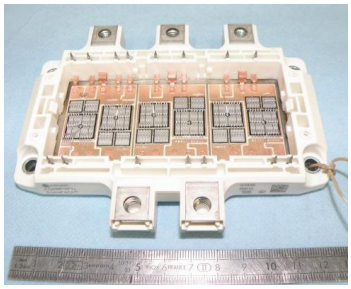


Fig. 2-2: (a) IGBT Parasitic Capacitances: R_{Gint} and input capacitances circled (b) Equivalent circuit with R_{Gint} as the ESR of the paralleled C_{GC} and C_{GE} capacitances.

For a standalone measurement, the ESR (or R_{Gint}) of a MOSFET or IGBT can be measured using an LCR meter. This involves shorting the collector and emitter, applying a high frequency sinusoidal voltage to the gate, and measuring the resultant magnitude and phase. The frequency of the sinusoidal voltage must be high enough to ensure that the reactance of the gate capacitance is negligible, and is therefore typically in the region of 1MHz or more. Fig. 2-3 displays R_{Gint} vs. temperature for one IGBT inside an Infineon FS200R12PT4 module, measured using a Keysight E4990A impedance analyser. A temperature sensitivity of +4.2mΩ/°C can be observed, with a nominal R_{Gint} at 25°C of approximately 3.65Ω.





Infineon FS200R12PT4 IGBT Module

Fig. 2-3: R_{Gint} vs. Temperature for an IGBT from an Infineon FS200R12PT4 module. Measured using a Keysight E4990A impedance analyser

Some high-end LCR meters are able to perform measurements in around 20ms, which is too long for direct application during the operation of most converters where switching frequencies usually exceed 1 kHz.

Nevertheless, this sinusoidal voltage method has very recently been proposed for use in operating IGBTs through the use of a specialised gate driver [85][86]. Here, a high frequency sinusoidal signal, at the resonant frequency of the gate capacitance, is superimposed on the gate voltage during the off-state. In this approach, the drawbacks appear to be that the gate driver requires substantial modification, along with additional external control to safely feed in the high frequency sinusoidal voltage. The resonant frequency of each device may also vary and thus the measurement circuit could require tailoring to each individual device. In some cases, an additional inductance may be added to the sinusoidal voltage feed-in path in order to lower the resonant frequency of the gate [85].

The following section will present the first original contribution of the thesis: a method to measure R_{Gint} that does not require any modification to the gate driver, or additional external control. To achieve this, the peak gate current during turn-on and the voltage swing of the gate driver are used to calculate the internal gate resistance. A description of the measurement principle, followed by experimental verification on IGBTs is provided. However, the measurement principle should be applicable to all MOSFETs and IGBTs containing an internal gate resistance. Advantages and disadvantages of the method are also discussed, along with some implementation considerations.

2.2. Peak Gate Current (I_{GPeak}) Measurement Principle

The peak gate current (I_{GPeak}) method for junction temperature measurement uses the normal charging cycles of the gate terminal during a hard switching turn-on. Simplified waveforms of an IGBT turn-on process are shown in Fig. 2-4. The turn-on process of an IGBT is well documented [87][88]; therefore, only the beginning of the process (between T0 and T1) will be discussed here, since this is where the peak gate current occurs.

The turn-on process begins at T0 when the gate driver output voltage swings from 0V, to a positive value above the threshold voltage of the transistor. At this point, the gate current begins

charging the capacitances C_{GE} (C_{GS} in MOSFETs) and C_{GC} (C_{GD} in MOSFETs), while the device remains in an off-state. This period is known as the turn-on delay and continues until T1, when the charge on C_{GE} reaches the threshold voltage and the transistor turns on. The length of this period can range from just a few nanoseconds for small discrete transistors, to up to a microsecond for large IGBT modules.

During T0-T1, both C_{GE} and C_{GC} remain stable for the following reasons. Firstly, the V_{CE} remains at a high and constant value (perhaps at the DC-link for that particular application). In these conditions, C_{GC} remains small and independent of V_{GE} [89][90]. C_{GE} also remains stable with a high V_{CE}, and is independent of V_{GE} while the charge remains below V_{TH} [89].

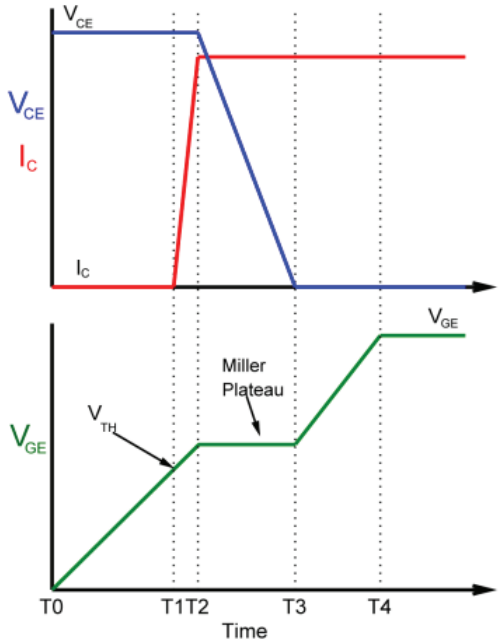


Fig. 2-4: Simplified gate voltage, collector current, and collector-emitter voltage waveforms during IGBT turn-on process

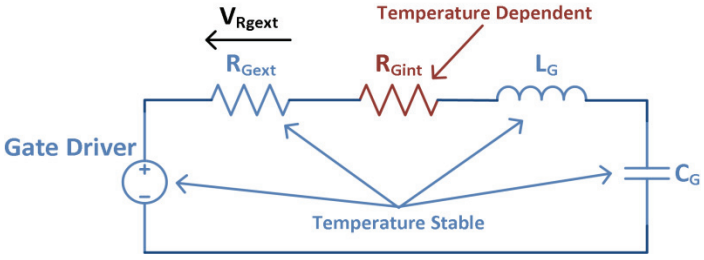


Fig. 2-5: Gate Driver RLC Circuit during turn-on delay

Subsequently, the gate current during the turn-on delay can be viewed as a step response of a second order RLC circuit [91]. This supposition is displayed in Fig. 2-5 and includes: the gate driver as a step voltage source, the parasitic gate inductance, the gate resistance (both internal

and external), and the gate capacitance (the combined paralleled capacitances C_{GC} and C_{GE}). Essentially, the gate is seen to be a fixed capacitor being charged through a resistor by a step voltage source.

If the parasitic gate inductance is kept sufficiently low, so that the RLC circuit is overdamped (i.e. $R^2 > 4L/C$), its behaviour will shift closer towards that of a first order RC circuit where the initial (and peak) charging current into the capacitor can be calculated using:

$$I = \frac{V}{R} e^{-t/RC} \qquad (1)$$

In this scenario, I_{GPeak} can be approximated through Ohm's Law, $I \approx V/R$, where V is the voltage swing of the gate driver, and R is the total gate resistance.

From Fig. 2-5, the external gate resistance is assumed to have insignificant temperature dependence; the gate capacitance is stable until V_{th} is reached; and the gate inductance has little influence on the behaviour of the circuit in an overdamped condition (and is anyhow also independent of temperature). On the condition that the gate driver delivers a fixed step voltage, the variation of R_{Gint} with temperature can be the only cause of fluctuation in the initial peak in-rush current into the gate. An increase of this resistance due to temperature will reduce the magnitude of I_{GPeak}. Therefore, I_{GPeak} provides a suitable observation point for the temperature-dependent variation of R_{Gint}.

2.2.1. I_{GPeak} Measurement – Peak Detector Circuit

Using a peak detector circuit, it is possible to monitor I_{GPeak} by measuring the peak value of the voltage across the external gate resistor (V_{Rgext}), since this voltage is directly proportional to the peak gate current. The peak detector circuit consists of a differential amplifier, a peak detector, and a reset switch that is controlled by the gate voltage signal, as seen from the schematic in Fig. 2-6. The output of the peak detector is held on a memory capacitor. At the device turn-off transition, the memory capacitor is discharged via the reset switch controlled by the gate voltage.

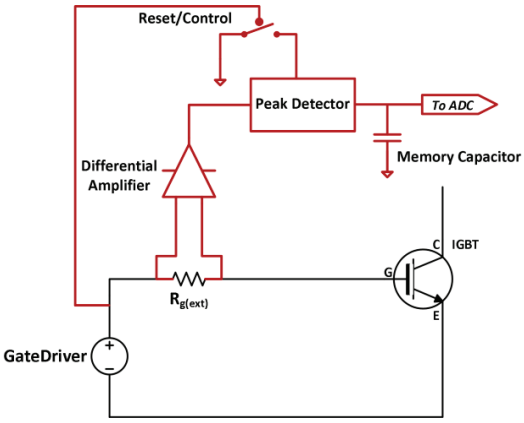


Fig. 2-6: Peak Detector Schematic to detect peak voltage over the external gate resistor

A prototype peak detector circuit was built and mounted on an off-the-shelf Concept2 gate driver [92]. The gate driver has an external gate resistor of 1.25Ω. Fig. 2-7 displays a sample of the output of the peak detector from the turn-on of an Infineon FF1000R17IE4 IGBT module (1700V/1000A), together with the gate voltage and V_{Rgext}. The peak detector detects the peak of V_{Rgext} while the gate voltage is still below V_{TH}. The measurement is then held on the memory capacitor while V_{Rgext} reduces to zero.

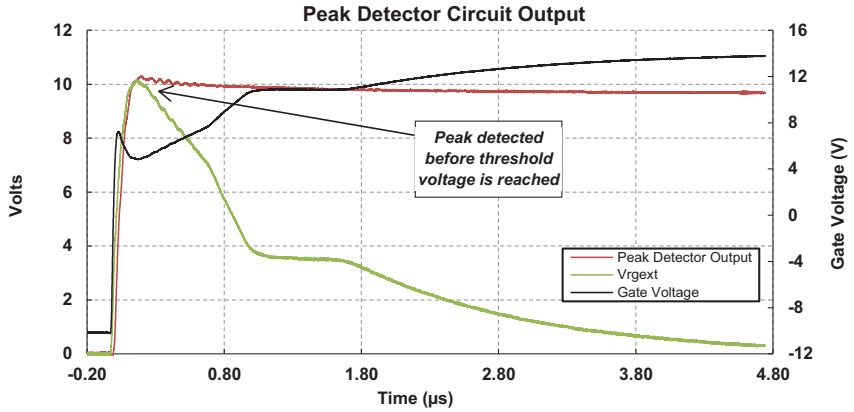
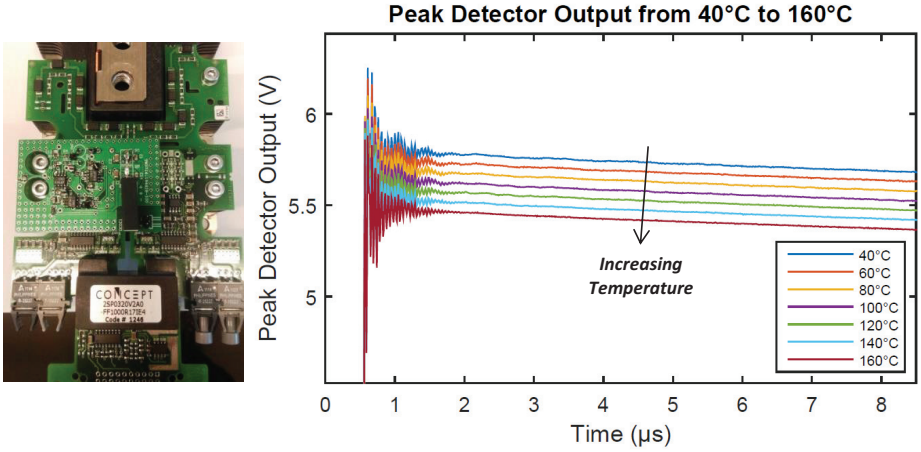


Fig. 2-7: Peak detector output and gate voltage during turn-on in an Infineon FF1000R17IE4 – peak is detected before threshold voltage is reached



(a) *(b)*

Fig. 2-8: (a) Peak Detector Prototype and gate driver (b) Sample Peak Detector Output from 40°C to 160°C on an Infineon FS200R12PT4

Fig. 2-8 displays a photo of the prototype and the output of the peak detector on an Infineon FF200R12PT4 module from 40°C to 160°C. A linear sensitivity of around 3mV/°C can be observed. In this figure, a non-negligible voltage droop in comparison to the temperature sensitivity is apparent. Therefore, it is imperative that the voltage on the memory capacitor is sampled early and after the same delay for each measurement. In the following experiments, this measurement delay is always under 1µs after turn-on.

Care has also been taken to eliminate the effects of component fluctuation with ambient temperature. This primarily entailed removing the inherent inaccuracy caused by the voltage drop of the diode used in ordinary peak detector circuits [93]. Future prototypes could improve on both of the above aspects. Nevertheless, the subsequent experiments are all performed using the prototype and gate driver shown in Fig. 2-8.

2.2.2. Gate Driver Performance Compensation

R_{Gint} is not the only parameter that can influence the value of I_{GPeak}. A fundamental source of error in the I_{GPeak} measurement may stem from fluctuations in gate driver performance, which can result from ambient temperature conditions as well as application demands [17]. In short, the gate driver cannot be viewed as an ideal step voltage source. This issue is depicted in Fig. 2-9, which shows the turn-on voltage of a Concept2 gate driver while an IGBT is being switched with a baseplate temperature from 40°C to 160°C. The ambient temperature around the gate driver is also recorded during this procedure and found to fluctuate from 25°C to 34°C. Two issues can be identified from the figure. The first is that the gate driver source voltage has a transient fluctuation of over 100mV, coinciding with the switching of the IGBT. Secondly, the static value of gate driver source voltage also varies around 40mV as the ambient temperature increases during the procedure from 25°C to 34°C.

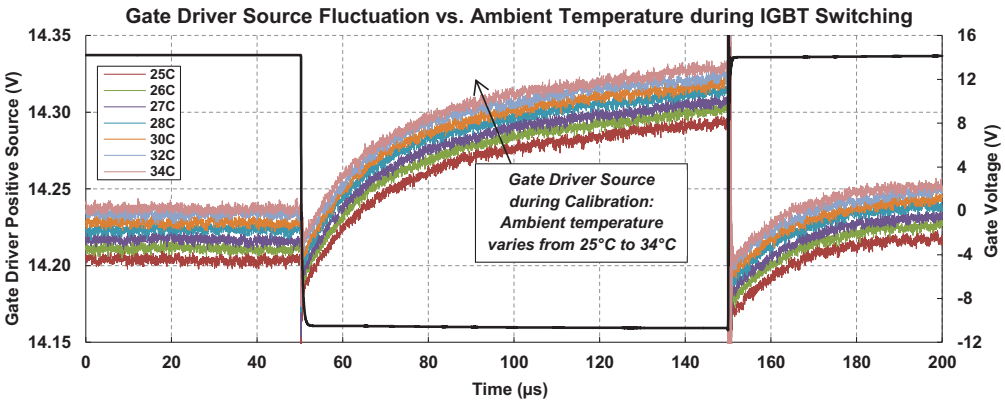


Fig. 2-9: Gate Driver turn-on voltage during IGBT switching

Using an LTSpice simulation of the peak detector circuit on the gate of an Infineon FS200R12PT4 (modelled as an LCR circuit as in Fig. 2-5, with L=100nH, R_{Gext}=1.25Ω, R_{Gint}=3.5Ω, C_G=80nF), it is estimated that each 10mV fluctuation in gate voltage swing can induce a 2.2mV discrepancy in the output value of the peak detector. This is shown in Fig. 2-10. With a sensitivity of 3mV/°C, a 100mV change in the gate voltage could lead to a measurement error of close to 7°C.

To counteract this, the gate voltage is sampled just before turn-on (V_{Gneg}), along with the positive source for the turn-on voltage from the gate driver (V_{Gpos}). These values provide the step voltage swing to the gate (V_{Gpos} - V_{Gneg}). I_{GPeak} is then calculated by dividing the output of the peak detector ($V_{peakdetector}$) by the value of R_{Gext}.

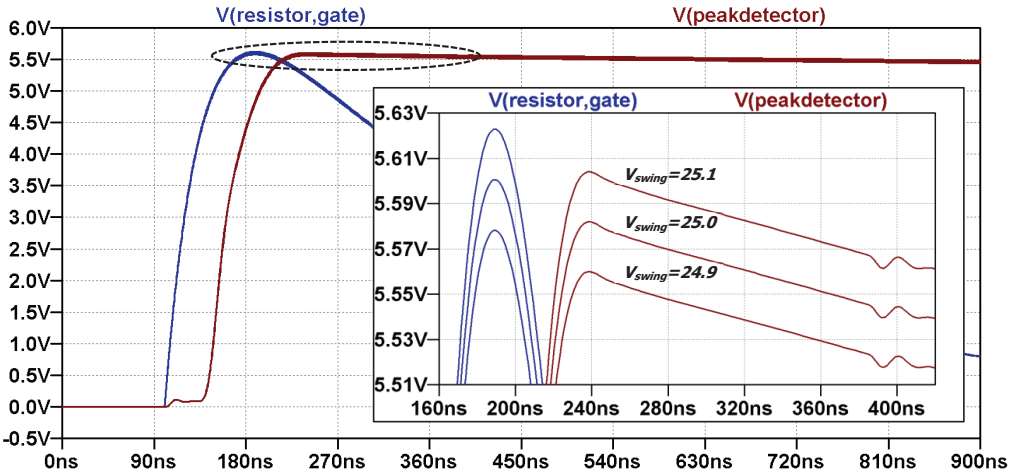


Fig. 2-10: LTSpice simulation example of the influence of gate voltage swing (V_{Swing}) on the output of peak detector. Gate voltage swing is varied from 24.9V to 25.1V. V(resistor,gate) is the voltage over the external gate resistor. V(peakdetector) is the output of the peak detector circuit.

According to the assumptions described in section 2.2, the peak gate current can be approximated using Ohm's law. Therefore, with the exact voltage swing and peak gate current known, Ohm's law can be rearranged to provide an approximation of R_{Gint}:

$$R_{Gint} = \frac{V_{Gpos} - V_{Gneg}}{\left(V_{peakdetector}/R_{Gext}\right)} - R_{Gext} \qquad (2)$$

In other words, the peak gate current and the voltage swing of the gate driver are used to calculate R_{Gint}. Because R_{Gint} is the temperature dependent property of the device, it is the result of the above calculation that is used for junction temperature measurement.

2.2.3. High Power Verification of Measurement Concept

The aim of this section is to verify the I_{GPeak} measurement concept in high power conditions, and to experimentally confirm that the method is immune to electrical fluctuations caused by load current.

A. Setup

A modified double pulse test is used to verify the I_{GPeak} measurement concept under high power conditions. The setup is adapted from a non-destructive testing system described in [94]. A schematic of the test setup is shown in Fig. 2-11 and includes two IGBT legs: a DUT IGBT, and an auxiliary IGBT. A visualisation of the control of these IGBTs is also included in Fig. 2-11.

The operation of the test setup is as follows. The Aux. IGBT is first turned on for a period of a few hundred microseconds in order to ramp up the current through the inductor (exact pulse length depends on the desired current level). The Aux. IGBT is then turned off, and the current freewheels in the diode of the Aux. IGBT for a 70µs dead-time. The DUT IGBT is subsequently turned on with the inductor current at the predetermined level. During this turn-on phase, an

I_{GPeak} measurement is taken, along with measurements of the gate voltage required to calculate a value of R_{Gint}.

This routine allows a load current to be set in the DUT IGBT without self-heating of the DUT itself. The IGBTs used are 1700V/1000A Infineon FF1000R17IE4 modules, and the DC-link voltage is 450V. A photo of the setup is included in Fig. 2-12.

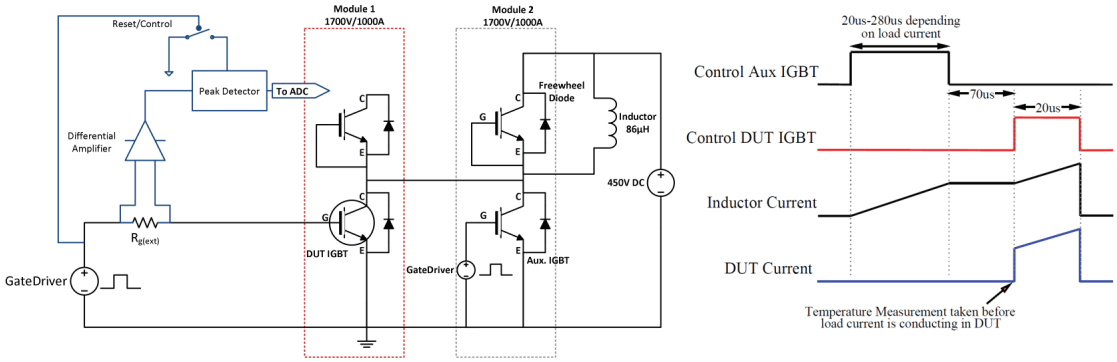


Fig. 2-11: (a) High Power Test Setup Schematic (b) Test synchronisation

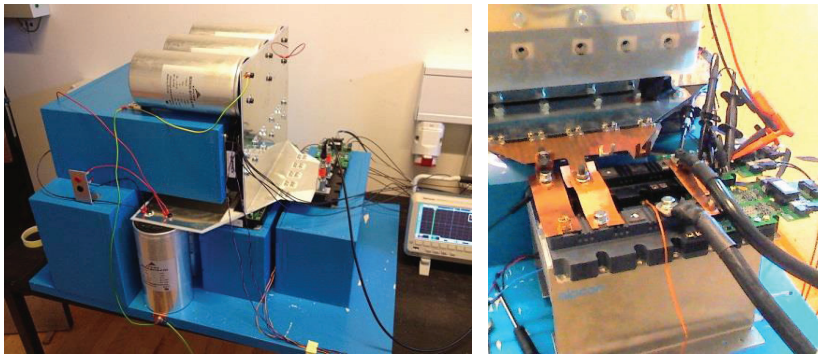


Fig. 2-12: (a) Non-Destructive Testing System for Primepack3 IGBT modules [94] (b) With both Aux and DUT IGBT modules connected for double pulse test

B. Calibration

To calibrate the I_{GPeak} method with temperature, the DUT IGBT is screwed onto a peltier cooler and the above procedure is conducted with zero load current from 20°C to 125°C. I_{GPeak} is used to approximate R_{Gint} in accordance with (2), and the results are shown in Fig. 2-13. For each temperature value, 10 samples are taken and the mean is calculated. A 12-bit oscilloscope is used to sample the outputs of the peak detector and gate driver.

The specified datasheet value for R_{Gint} in the Infineon FF1000R17IE4 is 1.5Ω. It can be seen from Fig. 2-13, that using I_{GPeak} to calculate R_{Gint} gives a similar nominal value of approximately 1.6Ω at 25°C. The temperature sensitivity is around 0.9mΩ/°C and the relationship is strongly linear.

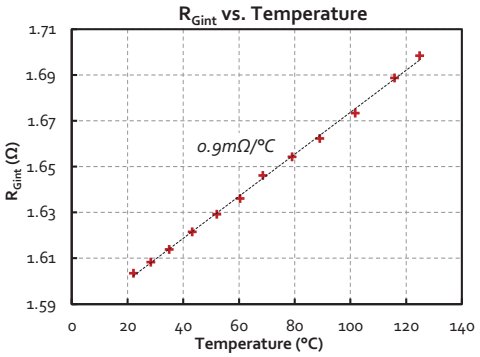


Fig. 2-13: R_{Gint} vs. Temperature for an Infineon FF1000R17IE4 – I_{GPeak} is used to calculate R_{Gint}

C. Load Current Variation

After calibration is completed, the procedure is repeated at room temperature with load currents of up to 1400A. I_{GPeak} is again used to calculate R_{Gint} in accordance with (2).

Fig. 2-14 displays the results of R_{Gint} vs. load current. A dependence on load current appears to be absent: the mean R_{Gint} is 1.604Ω and the standard deviation is 7mΩ. These results match theoretical expectations, since the measurement of I_{GPeak} takes place before the gate voltage has reached the threshold voltage of the IGBT. Therefore, the IGBT is still in an off-state and no load current is flowing.

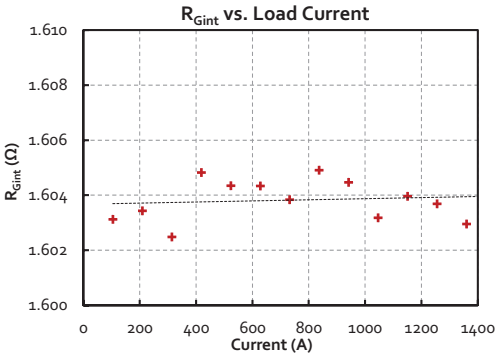


Fig. 2-14: R_{Gint} vs. Load Current for an Infineon FF1000R17IE4

2.2.4. Sensitivity Variation between Modules

The above results show a good linear relationship with temperature and an immunity to load current variation, which are advantageous characteristics for a simple TSEP calibration procedure. For further assessing the potential ease of use, the variability of the calibration curves for R_{Gint} from device to device is of interest.

The Infineon FF1000R17IE4 module tested above is constructed with 6 IGBT dies in parallel (Infineon SIGC186T170R3E), each with an internal gate resistor of 5Ω, totalling a combined R_{Gint} of 0.83Ω. The temperature sensitivity of 0.9mΩ/°C, as displayed in Fig. 2-13, represents a relative change of around 0.10%/°C.

It should be noted that the Infineon FF1000R17IE4 also contains an additional 4Ω gate resistor in series to the gate of each of the six IGBTs inside the module, which are shown in Fig. 2-15. The resistors are clearly separate from the die, but increase the overall R_{Gint} to 1.5Ω (as specified in the datasheet). Nevertheless, these resistors are typically Metal Electrode Leadless Face (MELF) resistors which can be manufactured with temperature tolerances as low as ±5ppm/K [95]. Therefore, negligible temperature dependence is assumed for these resistors in the above calculations.

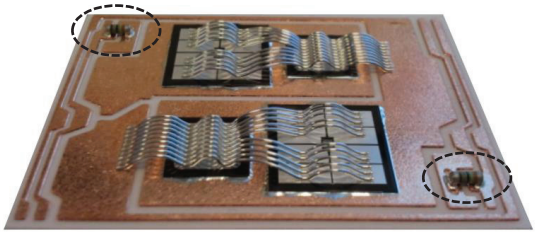


Fig. 2-15: Additional gate resistors on the copper substrate in one section of an Infineon FF1000R17IE4 [96]

Several more IGBTs were characterised from a six-pack Infineon FS200R12PT4 module, which have an R_{Gint} of 3.5Ω. In fact, Fig. 2-3 already showed a 4.1mΩ/°C temperature sensitivity of R_{Gint} in one of these IGBTs when measured using an impedance analyser. The calibration results for R_{Gint} calculated using the I_{GPeak} method are shown in Fig. 2-16. For the three IGBTs calibrated, the temperature sensitivity ranges from 2.74mΩ/°C to 2.82mΩ/°C – markedly lower than when measured using the impedance analyser. This decreased sensitivity could be due to the influence of the gate inductance, and will be explained in Section 2.2.5. Nonetheless, the three IGBTs displayed almost uniform temperature sensitivity. However, a clear offset in the calibration curves for each chip that spans close to 80mΩ can be seen.

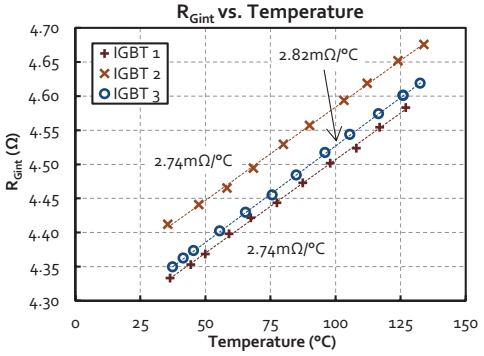


Fig. 2-16: R_{Gint} vs. temperature for 3 lower side IGBTs in an Infineon FS200R12PT4. I_{GPeak} is used to calculate R_{Gint}

Calibration results for IGBTs from the Infineon FS200R12PT4 in a 2x and 3x paralleled configuration are shown in Fig. 2-17. The temperature sensitivity here is lowered to 1.56mΩ/°C and 1.12mΩ/°C respectively. Even so, the relative sensitivity of R_{Gint} remains reasonably similar across all IGBT configurations – between 0.08%/°C and 0.10%/°C. These results are summarised in Table IV.

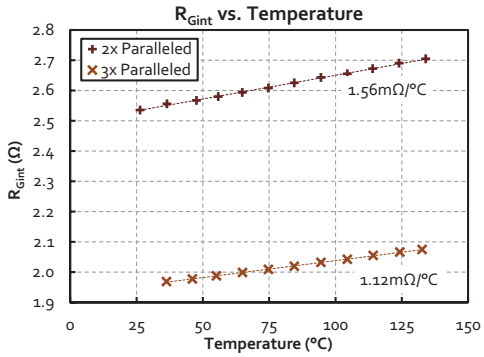


Fig. 2-17: R_{Gint} vs. temperature for paralleled IGBTs in an Infineon FS200R12PT4

TABLE IV

R_{GINT} AND TEMPERATURE SENSITIVITY FOR SEVERAL CHIPS

Chip(s)	Total R_{Gint}	Absolute Sensitivity	Relative Sensitivity
1x *IGC189T120T8RL (Single Chip)*	3.5Ω	2.8mΩ/°C	0.08%/°C
2x *IGC189T120T8RL (Paralleled)*	1.75Ω	1.6mΩ/°C	0.09%/°C
3x *IGC189T120T8RL (Paralleled)*	1.17Ω	1.1mΩ/°C	0.09%/°C
6x *SIGC186T170R3E (Paralleled)*	0.83Ω	0.9mΩ/°C	0.10%/°C

The tested samples (all IGBTs manufactured by Infineon) suggest that R_{Gint} has a low sensitivity in comparison to other TSEPs. Avenas *et al.* propose the use of a ratio in order to compare the sensitivity of various TSEPs [44]:

$$S = \frac{|s|}{|val_{max}|}$$

where s is the sensitivity of the TSEP per °C and val_{max} is the maximum measured value of the TSEP in the required temperature range. Using this criterion, R_{Gint} has a sensitivity ratio of less than 0.001. V_{CElow} and V_{TH} on the other hand can have sensitivity ratios of between 0.004 and 0.010, while the saturation current is shown to have a ratio of close to 0.020 [44].

Nevertheless, it may be possible for the IGBT manufacturer to increase the temperature sensitivity with through adjusting the doping of the Polysilicon used to create R_{Gint} [82][97]. Due to this, it is difficult to make a universal assumption on the expected sensitivity of the measurement method across all types of devices and manufacturers.

2.2.5. Gate Driver Requirements for Implementation

The I_{GPeak} method for junction temperature measurement has a number of characteristics that could simplify real-world use. However, a successful implementation of the method may place

stringent demands on the design of the gate driver.

Firstly, as described in Section 2.2, the gate path inductance must be kept to a minimum in order for (1) to be valid. In fact, the inductance in the gate path can have a direct impact on the sensitivity of the method. This is displayed in Fig. 2-18, which shows an LTSpice simulation of the peak detector output on the RLC gate network of Fig. 2-5. In this simulation, R_{Gint} is given a temperature sensitivity of 4.1mΩ/°C, and the gate inductance is stepped between 100nH, 700nH, and 2µH. It can be seen that the peak detector output varies around 360mV across a 100°C span when the inductance set to 100nH. Conversely, with the inductance at 2µH, the sensitivity decreases by over 60%: only a 130mV span is present across the 100°C range.

Even so, simply reducing the gate inductance to an absolute minimum will not always lead to an increased sensitivity. This is shown in Fig. 2-18b, where the gate inductance is set to just 1nH. In this condition, the peak detector output reaches a maximum value around 100ns after turn-on, even though the peak voltage across the external gate resistor occurs considerably earlier. This is due to a number of limitations with the operational amplifiers used in the measurement circuit, which can include the propagation delay, bandwidth, and ability to source output current to rapidly charge the memory capacitor. As a result, the peak detector is unable to correctly track the peak voltage and delivers an attenuated sensitivity.

As a result of these issues, the sensitivity of the I_{GPeak} method is intrinsically linked to the IGBT die, as well as the module layout and gate driver. Explicitly, an identical IGBT die could present a different temperature sensitivity if tested in two different modules (with different parasitic gate inductances) and with two different gate drivers.

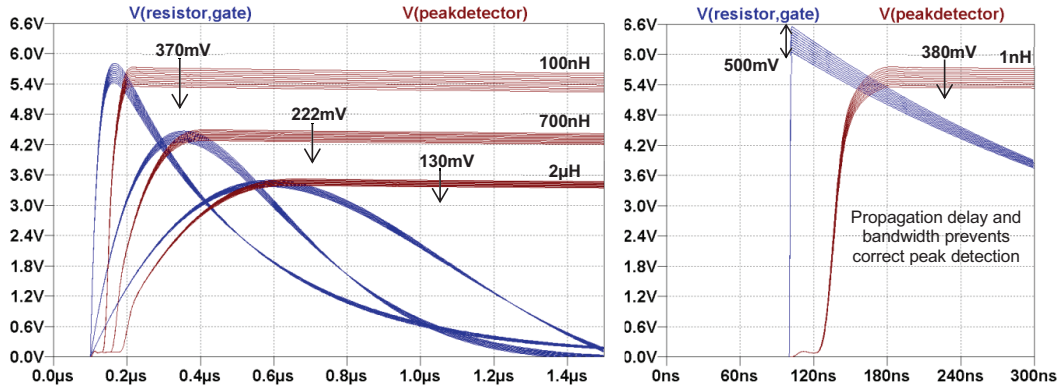


Fig. 2-18:

(a) Simulated influence of inductance on temperature sensitivity. V(resistor,gate) is the voltage across the external gate resistor. V(peakdetector) is the output of the peak detector circuit. Temperature is swept from 0-100°C. R_{Gext}=1.25Ω, C_G=80nF, R_{Gint}=3.5Ω(+4.1mΩ/°C), rise time of step voltage=1ns.

(b) Propagation delay and op-amp bandwidth prevent correct detection of peak voltage over the external gate resistor

Another requirement for (1) to be valid is for the gate RLC network to be sufficiently damped ($R^2 > 4L/C$). To achieve this, it is advisable to use a gate driver with a negative turn-off voltage. This will ensure that the MOS-gate capacitor of the IGBT will comprise of the single oxide capacitance (C_{oxide}), rather than the series sum of C_{oxide} and the depletion capacitance ($C_{depletion}$).

As a result, the total gate capacitance will be considerably larger. Fig. 2-19 displays a C_{GE}-V_{GE} profile of the previously characterised Infineon FS200R12PT4. While the gate voltage is below approximately -1.5V, the gate capacitance is close to 80nF. If a unipolar gate driver is used (i.e. the turn-off voltage is 0V), the gate capacitance would be just 13nF. In this case, the overall gate resistance would have to be increased to compensate for this, or the gate RLC network could easily shift into an under-damped condition.

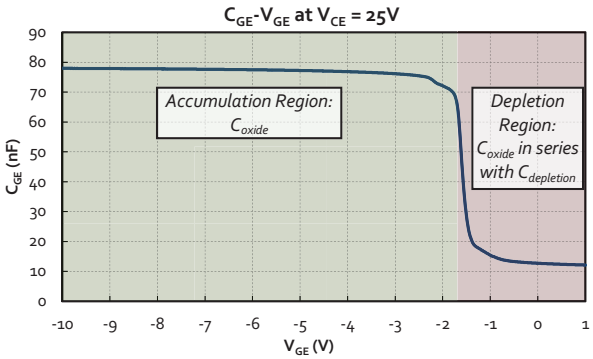


Fig. 2-19: Gate Capacitance-Voltage Profile for a single IGBT inside an Infineon FS200R12PT4

Other issues surrounding the gate driver include the fluctuation of source voltages with ambient temperature and performance, as demonstrated in Fig. 2-9. Furthermore, an ideal step voltage would also produce an instantaneous rise time; however this is not the case in real world gate drivers. The presented prototype in Fig. 2-8 uses a gate driver with Infineon BSO220N03MS MOSFETs forming the push-pull stage, with a rise time of 2.8ns. Conversely, some gate drivers have output rise times of over 100ns [98] and can also have a limited maximum output current. Gate drivers with slow rise times or output current limits could hinder the viability of temperature measurement via I_{GPeak}.

An additional issue results from using the voltage over the external gate resistor to measure the peak gate current. The external gate resistor requires a high stability with ambient temperature, as well as low parameter drift over its lifetime. MELF resistors could be one solution for this, which for example can be manufactured with temperature coefficients of ±5ppm/K, and maximum resistance deviations of 0.05% [95].

As a conclusion, the gate driver capacity must be considered carefully before attempting to implement temperature measurement via the I_{GPeak} method. In summary, five main criteria are required for designing a gate driver suitable to implement temperature measurement via I_{GPeak}:

1) Low parasitic gate inductance
2) Negative turn-off voltage
3) Stable gate driver turn-on and turn-off voltages (temperature stable and stable with performance demands)
4) Low output voltage rise time (<10ns) and high peak output current capability
5) Low temperature coefficient and parameter drift of external gate resistor (including any additional gate resistors included inside the module structure, i.e. Fig. 2-15)

2.3. *Temperature Measurement using Gate Voltage Integration*

2.3.1. *Gate Charging Constant*

Aside from using the Peak Gate Current, an alternative method for viewing the temperature variation of R_{Gint} was also investigated. This method again uses the same assumptions for the turn-on delay as described in Fig. 2-5; however, the RC time constant is used rather than a measurement of the peak current.

The time constant for the charging of the gate capacitor in a MOSFET or IGBT before the threshold voltage is reached (i.e. during the turn-on delay) can be written as [87]:

$$R_G[C_{GS} + C_{GD}(V_{DS})] \qquad (3)$$

where R_G is the gate resistance, C_{GS} is the gate-source capacitance (gate-emitter in IGBTs), C_{GD} is the gate-drain capacitance (gate-collector in IGBTs) and V_{DS} is the drain-source voltage (collector-emitter in IGBTs). Because the gate capacitances and the external gate resistor are stable, the time required to charge the gate capacitor to a specified level of charge will alter only depending on fluctuations of R_{Gint} due to temperature.

As a result, the temperature variation of R_{Gint} should be detectable in an assessment of the gate charge over a short period during the turn on delay. Two possible measurement principles could be employed to achieve this, which are shown in Fig. 2-20. The first is an integration of the gate current during the turn-on delay; the second is an integration of the gate voltage.

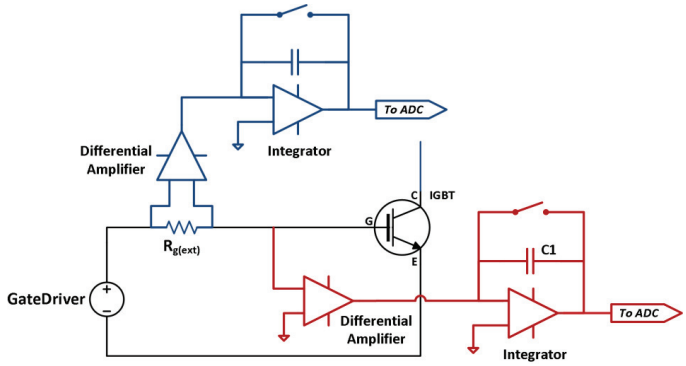


Fig. 2-20: Potential measurement topologies for evaluating R_{Gint} based on the charging constant of the gate capacitor

For experimental confirmation of the measurement concept, an integration of the gate voltage (shown in red in Fig. 2-20) was investigated. Fig. 2-21 displays the gate voltage at varying temperatures during turn-on of an Infineon FF1400R17IP4 IGBT module. The figure is zoomed in during the turn-on delay so that the temperature variation can clearly be seen. At the most sensitive point, the sensitivity is around 3-4mV/°C and decreases as the gate charges.

An integration circuit was constructed and mounted on a Concept2 gate driver. The main components of the circuit are a differential amplifier with one input connected to the gate voltage, followed by an op-amp integrator controlled though a fibre optic terminal. A photo of the circuit, along with an oscilloscope screen-cap of the circuit output during turn-on of an

Infineon FF1400R17IP4 from 25°C to 125°C, is shown in Fig. 2-22. The integration period begins 200ns after turn-on is initiated, and lasts for 350ns. Since the turn-on delay time is over 800ns for this module, this integration period finishes well before V_{TH} is reached.

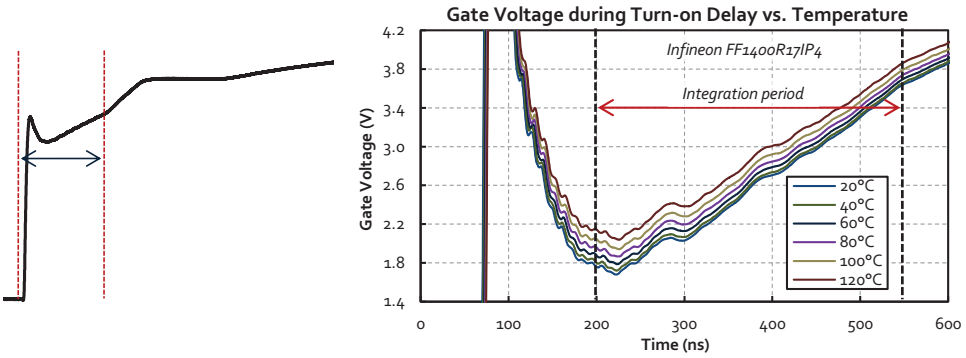


Fig. 2-21: Gate Voltage during the turn-on delay vs. temperature on an Infineon FF1400R17IP4 IGBT module

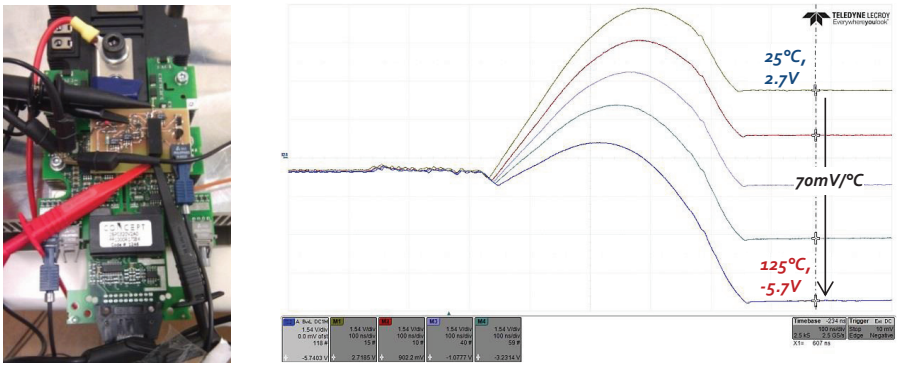


Fig. 2-22: Photo of gate voltage integration circuit and output during turn-on on an Infineon FF1400R17IP4 from 25°C to 125°C – gate voltage is integrated for 350ns during turn-on delay

2.3.2. Reasons for discontinuing research

The most attractive feature of the integration circuit is the level of sensitivity that can be achieved. In Fig. 2-22, a sensitivity of 70mV/°C is seen, with the integrator output around 2.7V at 25°C and -5.7V at 125°C. Nevertheless, this sensitivity can be artificially altered by increasing or decreasing the length of the integration period. In fact, the integration period of 350ns in length was chosen through trial and error in order to attain good sensitivity while keeping the integrator output within a range that would be easily sampled by an analogue-to-digital converter. Furthermore, the sensitivity of the integrator output can also be varied by increasing or decreasing the size of the capacitor, C1, from Fig. 2-20. In this test, a very low capacitance of 56pF was used. As a consequence, the sensitivity of the method is highly dependent on measurement circuit parameters, and would require tailoring to each individual device.

Further issues with the measurement concept include the additional control signals required to operate the integrator reset switch. Finally, there is no obvious or simple method to compensate for fluctuation in gate driver performance.

The above issues are in contrast to the previously described I_{GPeak} method, where sensitivity is mostly independent of measurement circuit parameters, no external control is required, and compensation for gate voltage fluctuation is uncomplicated. As a result, the I_{GPeak} method was selected for further experimental investigation, which will be detailed in Chapter 3.

2.4. Chapter Summary

An electrical method for junction temperature measurement of IGBTs or MOSFETs is presented. In accordance with the objectives outlined in Section 1.5.2, a focus was placed on developing a method immune from inherent electrical fluctuation caused by load current, and which could be measured in the normal operating cycle of the IGBT or MOSFET without interruption to operation.

To achieve this, a method utilising the temperature dependence of the internal gate resistance is presented. This change in resistance causes a variation in the peak gate current during the turn-on delay of an IGBT or MOSFET. The peak gate current is measured via a peak detector circuit that detects the peak voltage over the external gate resistor. A prototype measurement circuit is mounted on an off-the-shelf gate driver, and does not cause disruption to normal operation or require additional external control signals.

Experimental verification is provided on IGBTs. The measurement concept is shown to be independent of load current; however, some compensation is required for gate voltage fluctuation.

A variety of IGBTs are calibrated with the method. The temperature sensitivity is shown to be linear, and reasonably uniform between IGBTs of the same type. Nevertheless, this sensitivity appears to be noticeably lower than some traditional TSEP-based methods.

Several additional demands on the gate driver to implement the method are described. In particular, the parasitic inductance in the gate path can have a direct influence on the sensitivity.

Additionally, an alternative method based on the internal gate resistance is briefly presented. Here, an integration of the gate voltage during turn-on delay is used. Although providing greater sensitivity, this method has a large dependence on components in the measurement circuit, as well as requiring additional control and with no obvious approach to compensate for gate voltage fluctuation.

As a result, further experimental investigation in the following chapter is performed solely on the Peak Gate Current (I_{GPeak}) method.

III. Experimental Validation of I_{GPeak}

This chapter focuses on validating the accuracy of the I_{GPeak} method for IGBT junction temperature measurement. Two types of IGBT with the gate pad in the centre and the edge are investigated, along with paralleled IGBTs, and IGBTs suffering partial bond-wire lift-off. To perform validation, infra-red measurements are used, and I_{GPeak} is simultaneously compared with the traditional $V_{CE(low)}$ method.

In short, the I_{GPeak} method is found to provide measurements that are related to temperature of the gate pad. Consequently, both the gate pad position and the temperature distribution in the IGBT have an influence on whether I_{GPeak} adequately represents the mean junction temperature. This is in contrast to $V_{CE(low)}$, which consistently provides a temperature close to the mean regardless of the IGBT type.

The results also remain consistent after IGBTs are degraded through bondwire lift-off. In a paralleled IGBT configuration, the I_{GPeak} method delivers a measurement based on the average temperature of the gate pads.

The chapter will provide details on the IGBT chips studied, and the methodology behind the infra-red thermal measurements. The electrical test bench will be described, which allowed thermal measurements to be conducted on IGBTs operating under constant current injection. The results of each temperature measurement on the variety of IGBT configurations are then presented.

All experiments in this chapter are performed in collaboration with Dr. Laurent Dupont, (IFSTTAR, Versailles, France).

3.1. Motivation for Temperature Measurement Validation

Chapter 1 highlights the issue that the level of accuracy for different TSEP-based junction temperature measurement methods is highly inconsistent. Nevertheless, many recent TSEP proposals come with little or no validation (perhaps limited to one single chip) of the temperature provided. This is a pressing issue since the 'junction temperature' can span a wide temperature distribution, and the accuracy of a TSEP can depend on what temperature of the device is most desired. Therefore, for the I_{GPeak} method to be realistically considered for use, the temperature provided must be validated with direct measurements.

This chapter focuses considerably on this area and attempts to validate I_{GPeak} on multiple IGBTs and configurations. First of all, infra-red measurements are used to validate I_{GPeak} on two identically rated IGBTs with differing geometry (shape and gate pad position). Where possible, the IGBTs are also investigated in a paralleled configuration – both with and without large temperature disequilibrium between the paralleled IGBTs. Finally, since the electrical parameters of a device are prone to alter throughout its lifetime, a pertinent question is whether the accuracy of a TSEP method is resistant to these effects. To begin a preliminary assessment on this question, an IGBT is investigated both before and after several bondwires are disconnected from the die, which mimics one of the most common degradation mechanisms reported in prior literature.

Additionally, all results obtained using the I_{GPeak} method are compared to measurements made using the conventional TSEP method for IGBTs, the $V_{CE(low)}$. Although the $V_{CE(low)}$ requires interruption to load current in order to use the measurement during power dissipation [21][52], it is selected for comparison with I_{GPeak} due to its widespread use and repeated evidence of correlation with mean junction temperature [48][49].

3.2. IGBTs under test

Two Infineon IGBTs are chosen for investigation, which are both rated at 1200V/200A. Additionally, each IGBT contains an R_{Gint} of 3.5Ω. Although these dies have identical specifications, the geometry of the chips is dissimilar and is the primary reason for their selection. The first IGBT (Die: *IGC189T120T8RL [99]*, Module: *FS200R12PT4*) is square in profile with the gate pad in the centre, while the second IGBT (Die: *IGC193T120T8RM [100]*, Module: *FF600R12ME4*) has a rectangular profile with the gate pad at the side. These IGBTs will subsequently be referred to as Type A and Type B respectively. The geometry and dimensions of the dies are shown in Figs. 3-1 and 3-2. The datasheets for each IGBT are included in Appendix A.

Because functional dies complete with bondwires and packaging could not be obtained individually, the experiments are performed on individual dies isolated from inside commercial multi-chip power modules. The module layout for IGBT A (square, gate pad centre) also allowed investigation of two IGBTs in parallel. In addition, IGBT A is investigated both with and without bond-wire removal.

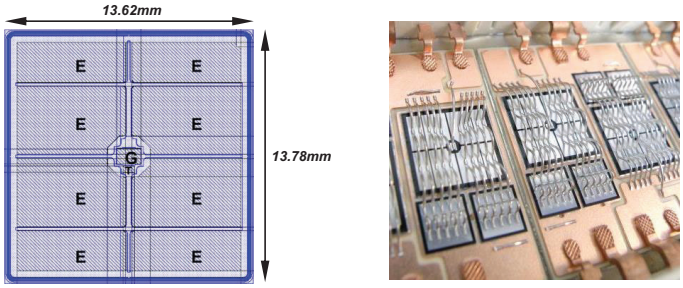
3.3. Infra-Red Thermal Measurements

To prepare the power modules for IR measurements, the dielectric gel was first removed by soaking for several hours in Ardrox 2312 at 75°C. The modules were then cleaned with Acetone and deionised water.

The chips were painted with PYROMARK 1200 high temperature paint. Care was taken in the painting process to achieve as consistent emissivity as possible across the chip surface: the paint was filtered to attain a uniform particle size, and micro-spraying equipment was used that allowed tight control over the paint thickness. A still frame from a video of the micro-spraying robot painting a power module is shown in Fig. 3-3, while before and after photos of IGBT B are shown in Fig. 3-4.

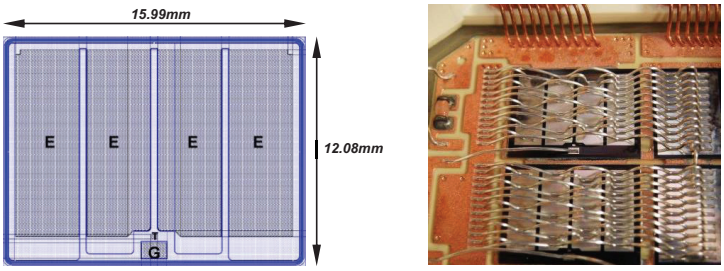
The thickness of the paint was selected as a trade-off between achieving uniform emissivity while minimising the impact on the thermal behaviour of the IGBTs. The paint thickness in all cases was between 10-16µm, compared to the 115-120µm thickness of the IGBT dies.

The IR camera used is a CEDIP-FLIR SC7500. For each measurement, 100 IR frames (100Hz frequency) are acquired while the IGBTs are conducting a constant current and in a thermal steady-state. The position of the camera is controlled by a 3-axis positioning system in order to fix identical positioning for each image acquisition.



(a) (b)

Fig. 3-1: ***IGBT A***
(a) Geometry of Infineon IGC189T120T8RL bare die
(b) Dies inside FS200R12PT4 module after dielectric gel is removed



(a) (b)

Fig. 3-2: ***IGBT B***
(a) Geometry of Infineon IGC193T120T8RM bare die
(b) Dies inside FF600R12ME4 module after dielectric gel is removed

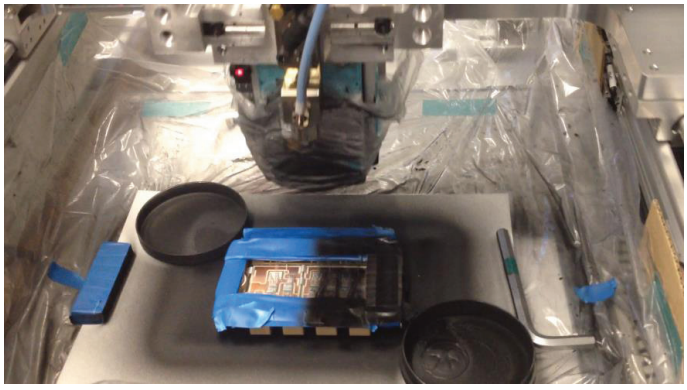


Fig. 3-3: Still frame from video of micro-spraying robot painting an open power module

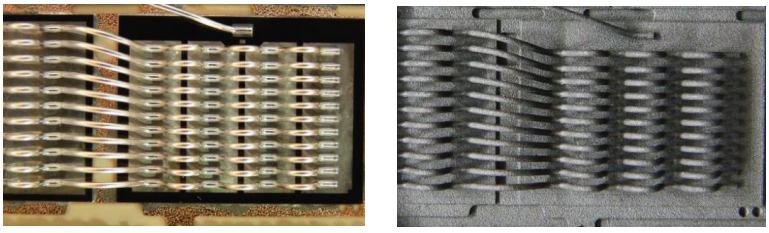
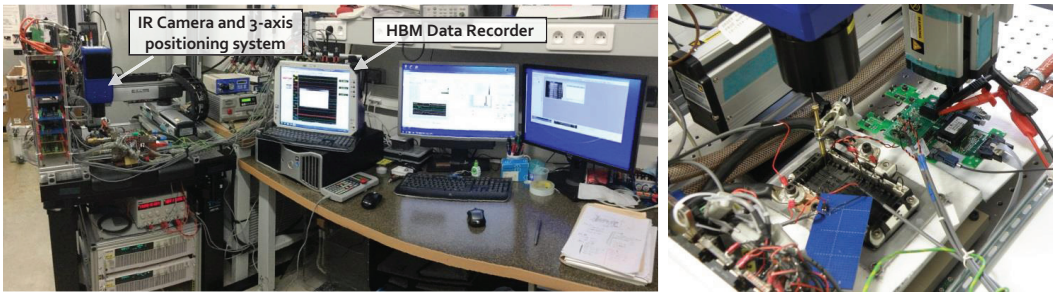


Fig. 3-4: IGBT B before painting (left) and after painting (right)



(a) (b)

Fig. 3-5: (a) Panoramic view of test bench (b) Close up of power module, IR Camera, and gate driver with peak detector measurement circuit

3.4. Test Bench Operation

A panoramic view of the test bench, along with a close up of the IR camera, power module and gate driver with peak detector circuit (as presented in Chapter 2) is shown in Fig. 3-5.

The test bench allows the TSEPs to be evaluated with IGBTs operating under constant current injection. A schematic of the test setup is displayed in Fig. 3-6, and the operating principle is described below. The basic premise is a two stage operation: a heating phase and a measurement phase.

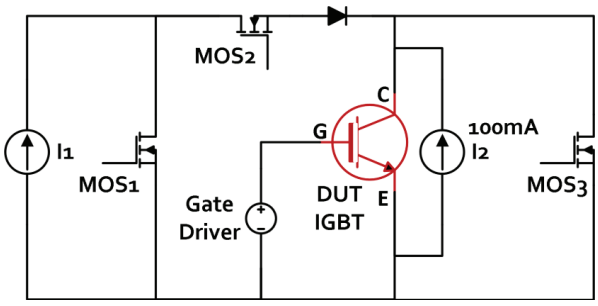


Fig. 3-6: Test Bench Schematic

The first step is the heating step, where a high current is fed into the DUT IGBT from the current source I1. This induces self-heating in the device, which can last for several minutes until a thermal steady-state is reached. The second step is the measurement step. At this point, the IGBT temperature is measured using the three presented measurement methods: IR camera, $V_{CE(low)}$ and I_{GPeak}.

All electrical measurements are performed using a HBM Gen3i data recorder. To measure I_{GPeak}, the peak detector prototype described in Chapter 2 is used, and the circuit output along with the gate voltage is sampled at 100MS/s (14-bit resolution). The V_{CE} of the DUT IGBT is recorded at 2MS/s (16-bit resolution).

It is clear that $V_{CE(low)}$ and I_{GPeak} cannot be performed while conducting the full dissipation current: $V_{CE(low)}$ requires a low sensing current of 100mA and I_{GPeak} must be recorded during an

IGBT turn-on. Therefore, synchronisation of MOSFETs MOS1, MOS2, MOS3, and current source I2 are used in order to facilitate these measurements.

Current source I2 is fixed at 100mA and provides the sensing current to perform a temperature measurement using $V_{CE(low)}$. MOS1 and MOS2 on the other hand are used to control the injection of the high heating current into the IGBT. MOS3 is used to force a zero collector-emitter voltage during measurement of I_{GPeak}.

The general procedure is as follows and depicted in Fig. 3-7. First of all, t_0 depicts the end of the heating phase which may have been ongoing for several minutes previously, with the DUT IGBT conducting a high current. In this phase, the temperature evolution of the chip is monitored using the IR camera. Once a thermal steady-state is reached, 100 IR images are sampled. Following this, t_1 commences with I_{DUT} redirected into MOS1, and the DUT IGBT switched off – a transition that lasts 100µs in total. In t_2, MOS3 is closed to short the collector and emitter of the DUT IGBT. This fixes the V_{CE} at 0V and is vital to ensure a stable C_G for the I_{GPeak} measurement, as described in Chapter 2. The IGBT is turned on again and a measurement of I_{GPeak} occurs using the peak detector circuit. In total, I_{GPeak} is measured 200µs after the heating current is removed. The negative gate voltage and the positive voltage supply of the gate driver are sampled 500ns before turn-on, while the output of the peak detector is recorded 1µs after turn-on.

Now that the I_{GPeak} measurement is completed, MOS3 is opened and a 100mA sensing current (I2) is injected into the DUT IGBT during t_3. The $V_{CE(low)}$ is recorded for a period of 250µs, and a linear regression vs. the square root of time is used to estimate the $V_{CE(low)}$ at the instant the load current is removed the DUT IGBT [43]. Finally, the original I_{DUT} is returned to the DUT IGBT in t_4.

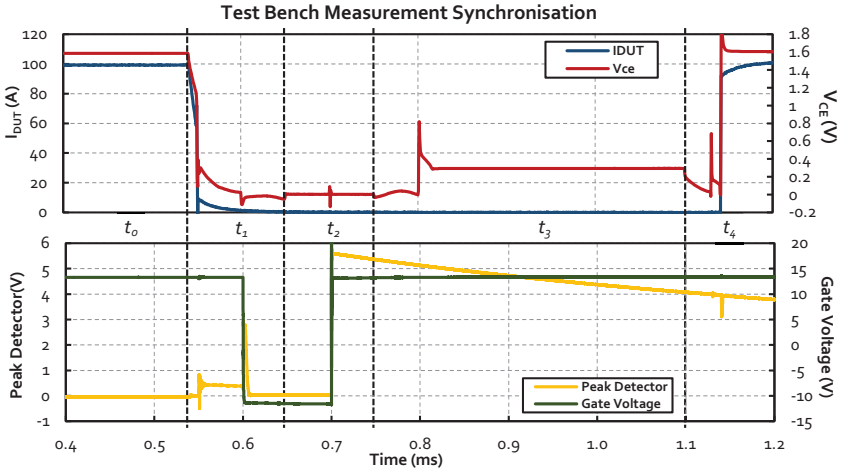


Fig. 3-7: Synchronisation of Electrical Measurements

This procedure is repeated 10 times and the mean value of these measurements is used for analysis. For calibration of $V_{CE(low)}$ and I_{GPeak}, the cooling fluid to the IGBT heatsink is varied from 40°C to 180°C, and the procedure described above is performed with I_{DUT} set to 0A. A

type-K open thermocouple is placed on the copper base of the power module and used as the reference temperature during the calibration procedure, as shown in Fig. 3-8.

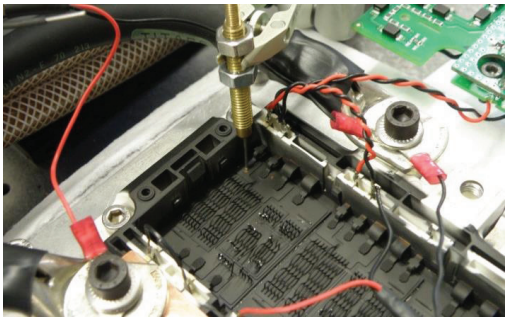


Fig. 3-8: Thermocouple on copper substrate of power module used for temperature reference

3.5. Gate Capacitance Stability at V_{CE} = 0V

Although the measurement of I_{GPeak} is conducted at a constant V_{CE}, previous assumptions have stipulated that a *high* V_{CE} is also required for C_G to be stable. Since I_{GPeak} is measured at a V_{CE} of 0V in these experiments, a short validation of the stability of C_G in this condition was conducted. Fig. 3-9 displays a C_{GE}-V_{GE} profile vs. temperature on IGBT A with the collector-emitter shorted (i.e. the same conditions for I_{GPeak} measurement in the test bench).

The profile shows that C_{GE} is around 80nF and stable with temperature while V_{GE} remains below approximately -1V. Given that the Concept2 gate driver used in the peak detector prototype has a negative turn-off voltage of -10V [92], I_{GPeak} should be detected well before the voltage on the gate capacitor reaches -1V. Therefore, the fluctuation of C_{GE} with temperature at a V_{GE} beyond -1V should not impact the measurement of I_{Gpeak}. In this experimental format, a unipolar gate driver with a turn-off voltage of 0V would yield fallacious results.

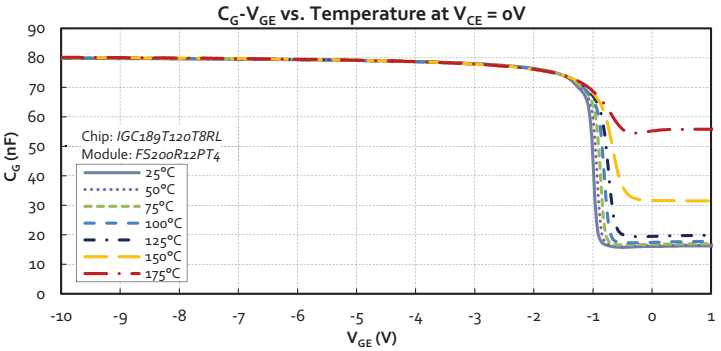


Fig. 3-9: C_G-V_{GE} vs. temperature profile for IGBT A (Infineon FS200R12PT4)

3.6. Results

In the following sections, all raw data values for the dissipation results are included in the tables in Appendix B.

3.6.1. *Definition of 'Junction Temperature'*

In prior literature concerning the evaluation of TSEP accuracy, the mean surface temperature and absolute maximum temperature of the chip are the two most common measurements chosen for comparison with the TSEP.

In this work, the 'junction temperature' is assumed to be the mean surface temperature of the emitter metallisation on the IGBT die. These emitter pads can be seen in the die datasheets and in Figs. 3-1 and 3-2. As a result, the 'junction temperature' does not include the entirety of die area, or any of the attached bondwires.

To extract the mean surface temperature of the emitter pads, IR images are processed using image masks in MATLAB to remove the undesired pixels. This process is depicted in Fig. 3-10.

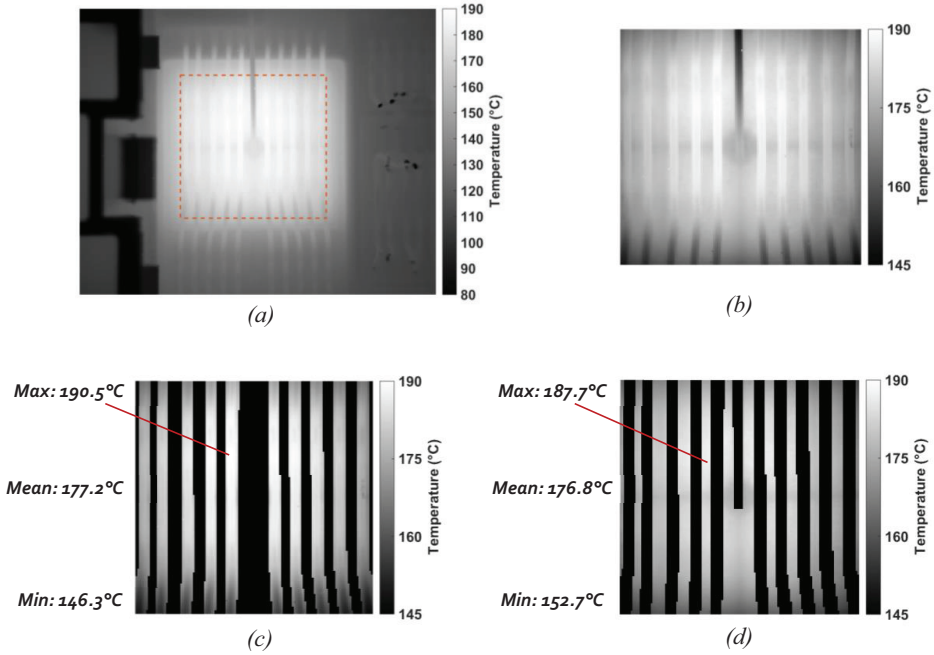


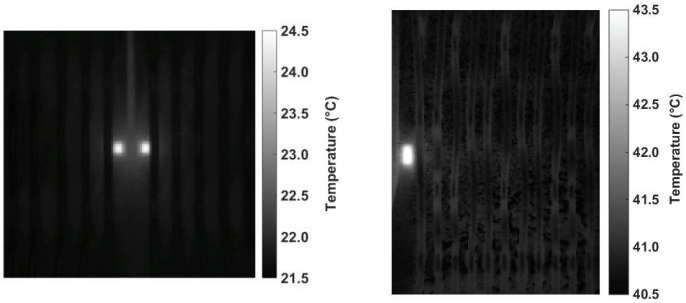
Fig. 3-10: Processing of IR images to extract the junction temperature
(a) Unedited IR image of IGBT A during dissipation at 140A
(b) Cropped IR image to the emitter active area of the die
(c) IR image of bondwires with die surface removed
(d) IR image of die surface with bondwires removed. This image is used to calculate the mean junction temperature

A noteworthy observation from this process is that the bondwires experience a wider temperature distribution than the die. From Fig. 3-10, it can be seen that the temperatures in the bondwires have both a lesser minimum and a higher maximum. The maximum temperature of the bondwires is close to 3°C higher than the die, while the minimum is more than 6°C lower. Nonetheless, the overall mean temperature of both structures is similar, with the mean temperature of the bondwires just 0.4°C higher than the die surface.

3.6.2. Location of R_{Gint}

The IR camera was used to perform a preliminary assessment on the location of the internal gate resistor for each IGBT. To do this, IGBTs were shorted between the collector and emitter, and switched using a gate driver at a frequency of 30kHz. Fig. 3-11 displays thermal images of the chip surface during this procedure. Clear heating in the gate pad of around 3°C can be seen on both IGBTs, which is assumed to be the result of the self-heating of the internal gate resistor.

As a result, post processing of IR images involved creating image masks in MATLAB to extract both the mean surface temperature of the emitter metallisation on the IGBT die (IR_{Mean}), as well as the mean temperature of the gate pad (IR_{Gate}).



(a) *(b)*

Fig. 3-11: Self-heating of R_{Gint}: (a) IGBT A (b) IGBT B

3.6.3. Calibration

Two chips are characterised from each module. In addition, the layout of the *FS200R12PT4* module allowed IGBT A to be calibrated with two IGBTs in parallel. In this case, the sensing current for $V_{CE(low)}$ was accordingly doubled from 100mA to 200mA.

Calibration curves for the two TSEP measurement methods are shown in Figs. 3-12 and 3-13. I_{GPeak} is used in conjunction with the gate voltage swing to calculate R_{Gint}, as specified in Chapter 2. Although both R_{Gint} and $V_{CE(low)}$ display a near linear relationship with temperature, a 2nd order polynomial fit is in fact used to calculate their respective relationships for when the TSEPs are used during dissipation.

For the traditional $V_{CE(low)}$, the calibration reveals very little variance between the chips. The temperature sensitivity is approximately -2.4mV/°C, with only a small offset between IGBT A and B of around 6mV. Furthermore, the paralleled chips of IGBT A displayed precisely the same $V_{CE(low)}$ as when they were calibrated individually.

On the other hand, R_{Gint} has significant variation between IGBTs in spite of each chip having a specified datasheet value of 3.5Ω. Within chips from the same module, sensitivity was fairly uniform: 3.2mΩ/°C for IGBT A, and 2.9mΩ/°C for IGBT B. However, an offset of approximately 20-30mΩ is present between T1 and T2 for both IGBT types. Furthermore, there is a discrepancy of around 50mΩ between IGBT A and B. For the paralleled chips of IGBT A, the sensitivity was halved to 1.6mΩ/°C.

These observations could be due to manufacturing tolerances in the production of R_{Gint}. It should be noted that a number of IGBTs from a separate module of IGBT Type A were previously calibrated in Chapter 2, where a similar pattern of consistent temperature sensitivity with an offset between IGBTs was observed. Nevertheless, in Chapter 2 the sensitivity of IGBT Type A was approximately 2.8mΩ/°C (from Fig. 2-16), as opposed to 3.2mΩ/°C from this calibration procedure. This discrepancy may be due to differences in the measurement system or the inductance in the gate path, since each module was calibrated with a non-identical connection between the gate driver and gate-emitter terminals.

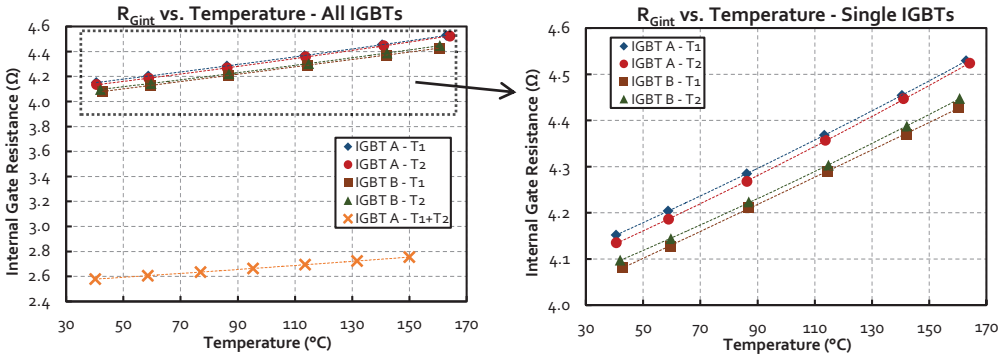


Fig. 3-12: R_{Gint} vs. Temperature from calibration data for IGBT A and B (I_{GPeak} used to calculate R_{Gint})

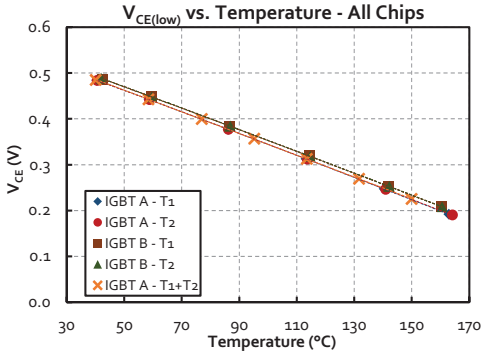


Fig. 3-13: Calibration Results – $V_{CE(low)}$ vs. Temperature for IGBT A and B

3.6.4. Dissipation Results: Single IGBTs

Temperature measurements during dissipation were conducted at a range of current values from 40-160A. The heating current was limited to below the 200A rating of each IGBT in order to maintain a safe maximum junction temperature of below 200°C. The input fluid to the heatsink was maintained at 40°C during all tests.

Fig. 3-14 displays the temperature measurement results during dissipation on a single IGBT of both Type A and B. Temperature measurements via I_{GPeak} and $V_{CE(low)}$ are displayed, along with IR measurements regarding the surface temperature of the die and gate pad.

For IGBT A (square, gate pad centre), all temperature measurements appear to match closely. On the other hand, the 4 temperature measurement methods show clear divergence on IGBT B – particularly at high current levels. In IGBT B, I_{GPeak} clearly underestimates the mean surface temperature and provides a temperature that is lower than measured via $V_{CE(low)}$.

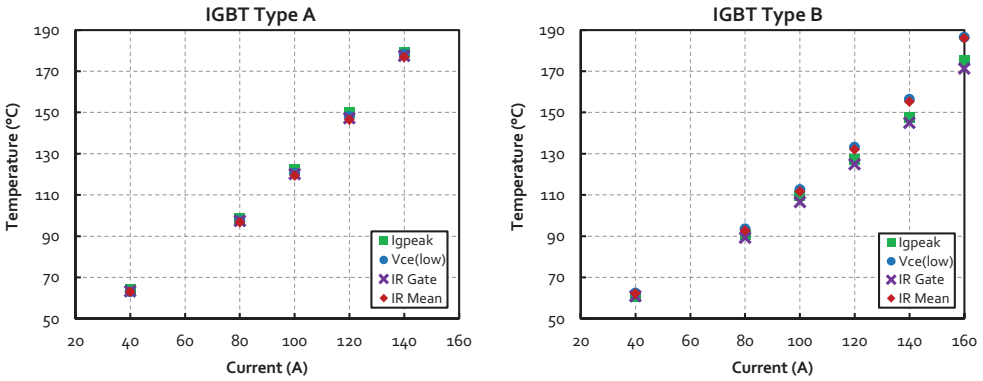


Fig. 3-14: Temperature measurement results during dissipation in single IGBTs from 40A to 160A

To demonstrate these trends more precisely, Fig. 3-15 compares both TSEP measurements in relation to IR_{Mean} for both IGBTs. It can be observed that in all cases, $V_{CE(low)}$ provides a temperature that slightly overestimates the mean surface temperature of the active area. The difference between the V_{CElow} and IR_{Mean} remains strictly lower than +2°C. These results are in accordance with several previous studies [48][49]. The slight overestimation of the mean temperature may be a consequence of the temperature gradient across the chip during dissipation, which is a contrast to the homogenous temperature during calibration. Due to the negative temperature coefficient of $V_{CE(low)}$, the central and hotter parts of the chip experience an increased current density compared to the colder outer parts of the chip. As the entire current in the chip must equal the total sense current of 100mA, these hotter areas subsequently contribute a larger weighting in the composition of $V_{CE(low)}$.

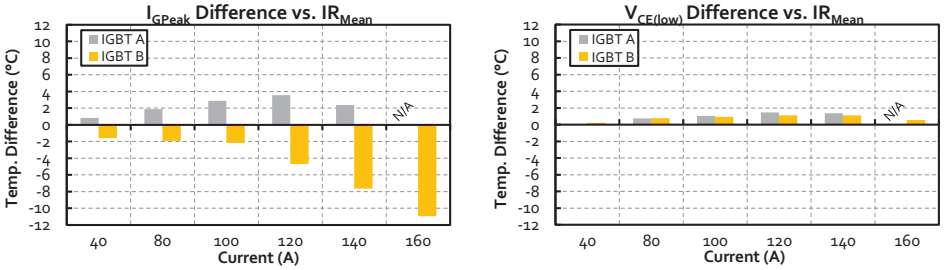


Fig. 3-15: Temperature measurement via I_{GPeak} and $V_{CE(low)}$: difference vs. mean surface temperature

Meanwhile, I_{GPeak} provided a temperature that differed in comparison to IR_{Mean} depending on the chip type. In IGBT A, with a centrally located gate pad, I_{GPeak} obtained a temperature that was higher than the mean surface temperature by between 1 and 4°C. These results are comparable to those obtained via $V_{CE(low)}$.

Conversely, for IGBT B, I_{GPeak} always delivered a temperature lower than IR_{Mean}. At lower current levels, this underestimation was not severe at around -2°C. However, this increased to -7.6°C and -10.9°C at higher current (and temperature) levels.

These trends could perhaps be anticipated due to the respective locations of the gate pad. In fact, Fig. 3-16 shows the correlation of temperature measurement via I_{GPeak} to the temperature of the gate pad measured via IR camera. In almost all cases on both chip types, I_{GPeak} provided a temperature within +1°C and +3°C of the gate pad.

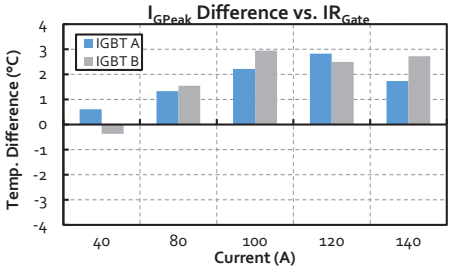


Fig. 3-16: Temperature measurement via I_{GPeak}: difference vs. gate pad temperature

A gate pad at the side experiences a comparatively lower temperature than one in the centre due to the temperature gradient across the chip during dissipation. These temperature gradients generally become more significant at higher mean temperatures. This is shown in Fig. 3-17, which displays the temperature profile across IGBT B at all investigated current levels. This is therefore an explanation of why I_{GPeak} still delivered a reasonable approximation of IR_{Mean} (within -2°C) on IGBT B up to 100A dissipation current, while severely underestimating IR_{Mean} as the current and temperature increased.

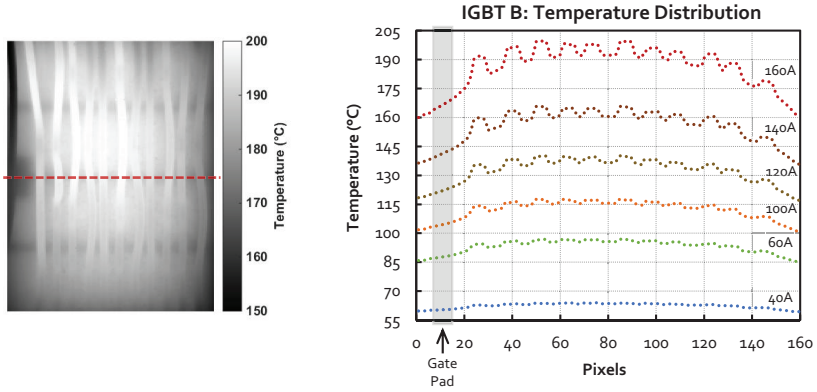


Fig. 3-17: Temperature profile across IGBT B from 40A to 160A. Temperature is plotted along the red line

These results infer that use of I_{GPeak} for junction temperature measurement on single IGBTs would require consideration of the gate pad position, as well as the expected operating temperatures and temperature distribution throughout the chip.

The fact that the I_{GPeak} method consistently measures a slight overestimation of the gate pad temperature could indicate a systematic error in the measurement. This may be due to a suboptimal design of the peak detector circuit, or a systematic error in the measurement principle. For example, the gate connection in the IGBTs studied is not a kelvin connection. Therefore, the collector current and the gate current must share the same path (including bondwires), which could produce a discrepancy between the calibration conditions with 0A load current, and the dissipation conditions with a high heating current.

3.6.5. Dissipation Results: Degraded IGBTs – Partial Bondwire Removal

To begin an assessment on the robustness of the I_{GPeak} method, temperature measurements were performed on a degraded IGBT suffering bondwire lift-off. The bondwire lift-off mechanism was selected for two reasons. Firstly, it is one of the most common degradation mechanisms written about in academic literature, and secondly it is easy to emulate without requiring removal of the power modules from the test setup. In this manner, the I_{GPeak} method can be assessed in precisely the same conditions for both the healthy and degraded states.

To achieve the degraded condition, 3 bondwires on IGBT A were cut with wire clippers, resulting in the complete disconnection of a central emitter pad on the IGBT. An IR image of this condition at 140A is displayed in Fig. 3-18, from which, clear distortion of the temperature distribution can be seen in comparison to the healthy IGBT. Mean and maximum temperatures of the IGBT are around 5-10°C higher after bondwire removal.

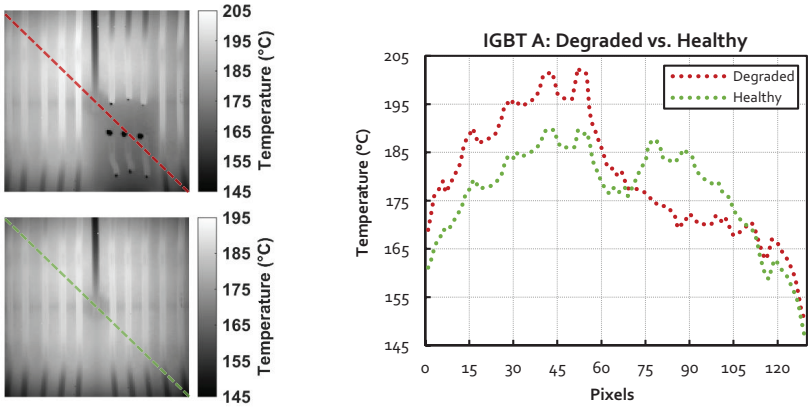


Fig. 3-18: Comparison of IGBT A temperature profile at 140A before and after bondwire removal. Temperature is displayed along diagonal lines

Temperature measurements on the degraded IGBT A are shown in Fig. 3-19. These results appear similar to the findings of IGBT A in a healthy condition (Fig. 3-14) – all temperature measurements match closely.

For further analysis, Fig. 3-20 is presented and displays a comparison of I_{GPeak} in relation to IR_{Mean} and IR_{Gate}, both before and after degradation. The correlation between I_{GPeak} and IR_{Gate} remains almost unchanged between healthy and degraded conditions. However, a non-negligible shift can be seen when comparing I_{GPeak} to IR_{Mean}. In a healthy state, I_{GPeak} typically delivered a temperature between 2-3°C larger than the mean junction temperature. After bondwire removal,

this overestimation reduced by 1-2°C. In fact, a -0.4°C underestimation of IR_{Mean} was observed at the highest heating current of 140A. Although this adjustment may seem small, it is in clear contrast to $V_{CE(low)}$, whose correlation with IR_{Mean} altered less than ±0.2°C in all cases, as shown in Fig. 3-21.

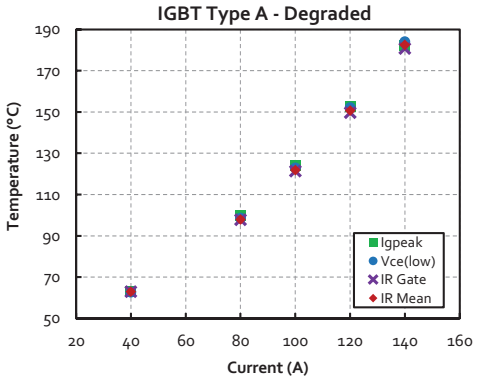


Fig. 3-19: Temperature measurement results during dissipation on IGBT A with partial bondwire removal

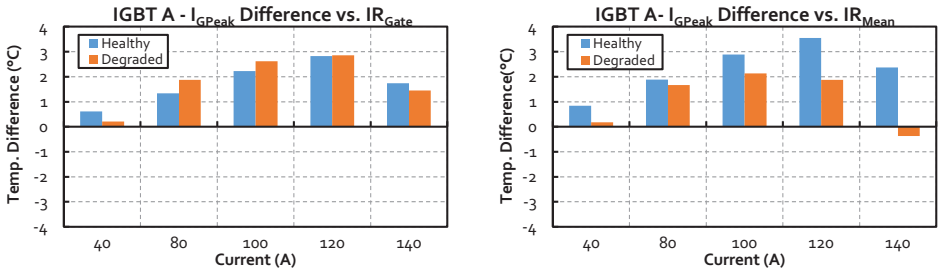


Fig. 3-20: Temperature measurement via I_{GPeak} in degraded and healthy conditions:
(left) Difference vs. gate pad temperature
(right) Difference vs. mean surface temperature

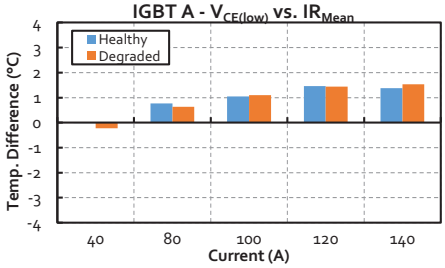


Fig. 3-21: Temperature measurement via $V_{CE(low)}$: Difference vs. mean surface temperature in healthy and degraded condition

These results again infer that I_{GPeak} is primarily influenced by local conditions in the vicinity of the gate pad, rather than the overall active area of the die as is the case with the traditional $V_{CE(low)}$.

Although I_{GPeak} was found to be largely unaffected by bondwire lift-off, this is perhaps a logical observation since the emitter bondwires may contribute a total resistance of just a few mΩ, opposed to the 3.5Ω of R_{Gint}. Additionally, since the parasitic gate inductance mainly comes from the terminal leads, the lift-off of just a few bondwires cannot significantly change the total inductance in the circuit [91].

To further assess the robustness of I_{GPeak}, an investigation on IGBTs with a degraded gate oxide or gate capacitance would be relevant, especially as there is some data to suggest that the gate capacitances can vary as an IGBT is subject to accelerated aging [101][102].

3.6.6. Dissipation Results: Paralleled IGBTs

The module structure for IGBT A allowed investigation of two IGBTs in parallel. For paralleled IGBTs, the heating current ranged from 120A to 240A, and the sense current for $V_{CE(low)}$ was accordingly doubled from 100mA to 200mA. The gate driver and peak detector was unchanged from previous investigations.

Firstly, the paralleled IGBTs were assessed without inducing temperature disequilibrium. In this condition, the temperature difference between the mean surface temperatures of the IGBTs was a maximum of 2°C. Temperature measurements in this paralleled state are displayed in Fig. 3-22. Since the temperature difference between the two IGBTs is minimal, single IR measurements are displayed which is the cumulative mean of both IGBTs (i.e. $\frac{IR_{Mean-T1}+IR_{Mean-T2}}{2}$).

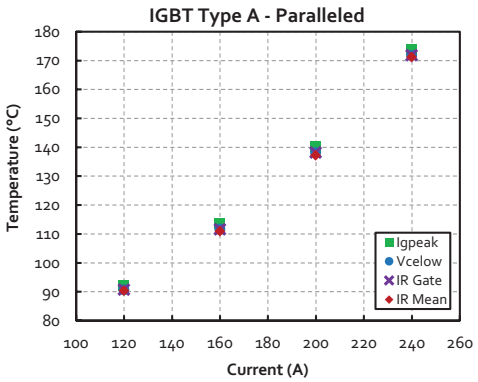


Fig. 3-22: Temperature measurement results during dissipation for 2x paralleled IGBT A at 120A – 240A

The results on IGBT A in a paralleled configuration follow the same trends as with single IGBTs. It can be seen from Fig. 3-23 that I_{GPeak} delivers a temperature within +2°C of the gate pad temperature. This leads to an overestimation of IR_{Mean} by between +1°C and +3°C. Additionally, $V_{CE(low)}$ again provides a temperature closely correlated with the mean surface temperature, with measurements at all current levels showing a difference of less than +1°C.

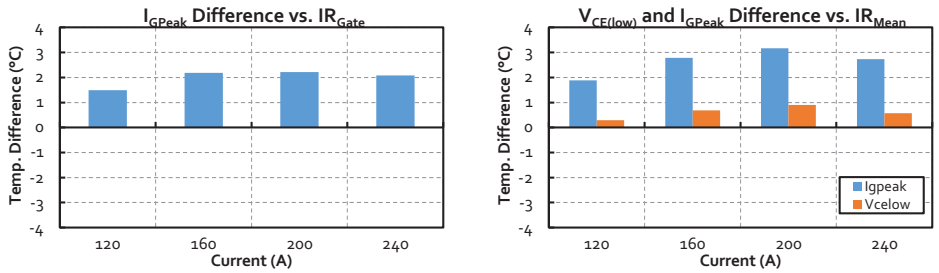


Fig. 3-23: Temperature measurement via I_{GPeak} for 2x paralleled IGBT A:
(left) I_{GPeak} Difference vs. gate pad temperature
(right) I_{GPeak} and $V_{CE(low)}$ Difference vs. mean surface temperature

3.6.7. Dissipation Results: Paralleled IGBTs with Temperature Disequilibrium

A more interesting scenario is to examine the TSEP methods on paralleled IGBTs that have a large temperature imbalance. To achieve this, the connection from the heatsink to the baseplate was loosened on one side of the power module so that one IGBT suffered a deteriorated thermal contact. The IGBTs were then examined with a heating current of up to 200A, where the temperature disequilibrium between the two IGBTs reached up to 20°C.

Fig. 3-24 displays the temperature measurement results with this thermal imbalance. In this figure, the mean surface temperature measured via IR camera is included for both IGBTs. It can be seen that both I_{GPeak} and $V_{CE(low)}$ provide a temperature in between the IR_{Mean} of each IGBT.

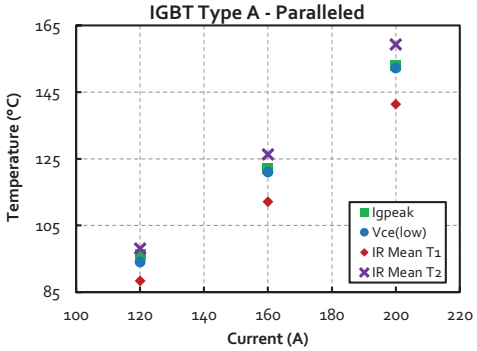


Fig. 3-24: Temperature measurements during dissipation on 2x paralleled IGBT A with temperature disequilibrium

I_{GPeak} delivers a temperature within +2°C of the cumulative mean temperature of the gate pad, which is shown in Fig. 3-25. Fig. 3-26 demonstrates the temperature profile of the two IGBTs with a 200A heating current. Here, the I_{GPeak} and $V_{CE(low)}$ measurements are within 1°C of each other and appear to correspond closely with the combined mean temperature profile of the two IGBTs. In fact, both TSEP measurements overestimate the cumulative mean surface temperature by between +1°C and +3°C, as shown in Fig. 3-27.

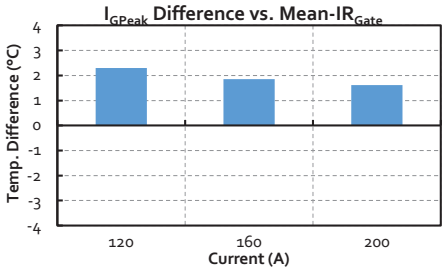


Fig. 3-25: Temperature measurement via I_{GPeak} on 2x paralleled IGBT A with temperature disequilibrium: Difference vs. cumulative mean of gate pads

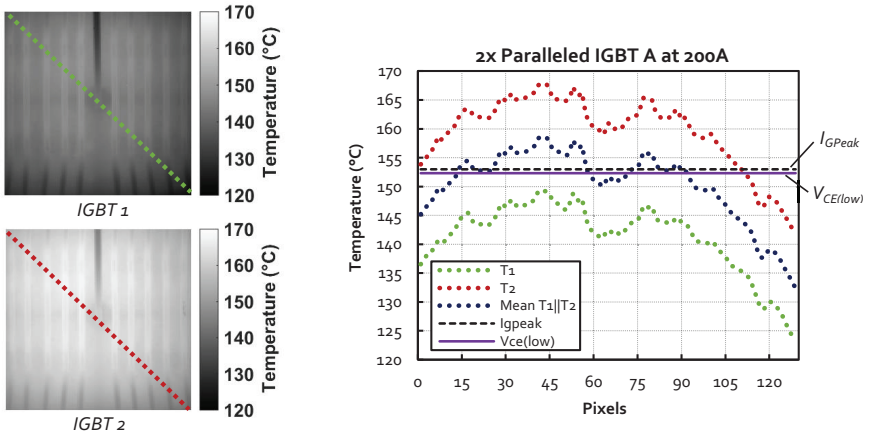


Fig. 3-26: Temperature profile of 2x IGBT A with 200A heating current. Temperature is plotted along diagonal coloured lines.

These results suggest that I_{GPeak} can provide an adequate assessment of the mean temperature of IGBT chips in a paralleled condition, at the least in line with results provided by the traditionally used $V_{CE(low)}$. This is providing that the IGBTs contain a centrally located gate pad.

For a more detailed assessment on the performance of I_{GPeak} with paralleled chips, a number of additional studies could be carried out. Clearly, immediate steps would be to assess I_{GPeak} on a greater number than two IGBTs in parallel, as well as on paralleled IGBTs with the gate pad at the edge of the die. Other relevant studies would be to investigate the impact of additional gate resistors sometimes placed inside power modules (shown in Fig. 2-15), as well as the use of non-standard paralleling techniques such as grouping IGBTs into 'cells' [103]. Finally, investigating the feasibility of extracting multiple temperatures to form a temperature map, by making multiple measurements in different electrical conditions [80], is a possible research area.

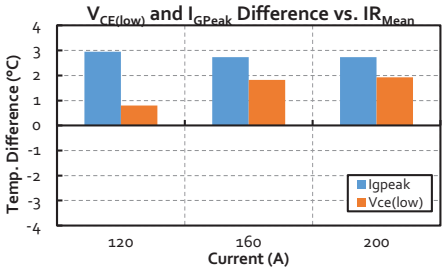


Fig. 3-27: Temperature measurement via I_{GPeak} and $V_{CE(low)}$: difference vs. cumulative mean temperature in 2x paralleled IGBT A with temperature disequilibrium

3.7. Chapter Summary

This chapter uses infra-red measurements to experimentally validate the temperature provided by I_{GPeak} when used on IGBTs. The accuracy of I_{GPeak} is compared to a traditional electrical temperature measurement method, the $V_{CE(low)}$. To perform validation, IGBTs are operated under constant current injection and temperature measurements are taken while the IGBT is in a thermal steady-state.

The I_{GPeak} method is found to correlate closely with the temperature conditions in the vicinity of the gate pad. This is in contrast to $V_{CE(low)}$, which is influenced by the entire area of the die. As a result, I_{GPeak} provided a slight overestimation of the mean surface temperature of the die in IGBTs with a centrally located gate pad, while underestimating the mean surface temperature in IGBTs with a gate pad located at the side. These trends became more pronounced as the overall temperature of the dies increased, which in turn induced more pronounced temperature gradients.

The I_{GPeak} method is found to be unaffected by partial bondwire lift-off, which is a common degradation mechanism in IGBTs. In this respect, the I_{GPeak} method continued to provide a temperature associated with the gate pad temperature with the IGBT in a degraded condition. However, since the temperature distribution in the die was modified due to this degradation, the correlation with the mean surface temperature was altered slightly.

In paralleled IGBTs where the gate pad is centrally located, I_{GPeak} was found to have similar averaging properties as the traditional $V_{CE(low)}$ method, and provided a temperature slightly overestimating the cumulative mean temperature when a large temperature disequilibrium is present between the IGBTs.

As a general conclusion, using and interpreting measurement results provided by I_{GPeak} requires a good knowledge of the gate pad position, as well as likely operating temperatures and the temperature gradient in the chip.

Several areas for future research in assessing of the validity of I_{GPeak} are suggested. These include investigations on IGBTs with gate oxide degradation, investigations on large numbers of IGBTs in parallel (greater than two), as well as the impact that module internal layout and non-standard IGBT paralleling techniques can have on the measurement.

IV. Conclusion

This chapter will summarise the scientific contributions of the thesis. Limitations of the work will also be outlined, along with suggestions for future research.

4.1. Contributions

The general purpose of the thesis is to expand the breadth of research concerning the use of temperature sensitive electrical parameters for junction temperature measurement of power semiconductor devices in operating power electronic converters.

The main scientific contributions of the thesis are as follows:

1) An electrical method for IGBT junction temperature measurement is proposed, which is referred to as 'the I_{GPeak} method' throughout the thesis. To be specific, the Peak Gate Current is measured during the normal turn-on process of the IGBT, and is used to calculate a value for the Internal Gate Resistor located in the semiconductor die. This is performed without interruption to operation, and without additional control signals. Additionally, the method is immune to inherent electrical fluctuations caused by a changing load current. These features are seen as advantageous for using an electrical method for junction temperature measurement during normal IGBT operation.

2) The experimental validation of the accuracy of the proposed I_{GPeak} method is subject to a level of scrutiny generally not present in prior art: the method is examined on multiple IGBT types, IGBTs in paralleled configuration, and IGBTs in degraded conditions.

A general contrast between the work conducted in the thesis vs. prior art is found in the Table V.

4.2. Limitations

There are several limitations in the work which prevent the I_{GPeak} method from being considered a comprehensive solution for junction temperature measurement during converter operation:

1) In Chapter 2, a rudimentary prototype is built and the method is verified under high voltage conditions. Nevertheless, the measurement circuit has yet to be implemented in a real converter setup. Chapter 3 also performs validation of the accuracy under low voltage conditions (current cycling). As a result, there may be alternative approaches to the measurement circuit design that are more suited to conditions in a real power electronic converter.

2) The calibration process is not extensively studied. Data is presented in both Chapter 2 and 3 that suggests that IGBTs of the same type have a consistent linear sensitivity curve, however with an offset in absolute value between the IGBTs. Nevertheless, these IGBTs represent a small data sample, and methods to transfer the calibration procedure to large numbers of IGBTs are not investigated.

3) Although experimental validation of the accuracy of the I_{GPeak} method was significantly focused on, there are still several weaknesses in this research area. Firstly, experiments are performed on IGBTs from just one manufacturer (Infineon). The conclusions drawn

from these experiments are that the type of IGBT can have a large impact on the accuracy of the method. Therefore, use of the I_{GPeak} method on IGBT dies from another manufacturer may yield different results to those found in Chapter 3. Secondly, it cannot be certain that module structure does not have an impact on the method. For example, no comparison was performed between a kelvin and non-kelvin gate-emitter connection, and no comparison was performed between alternative module layouts with paralleled IGBTs. Finally, an assessment of the impact of gate oxide degradation is absent.

TABLE V

THESIS CONTRIBUTION VS. PRIOR ART

	Proposed Method	**Prior Art**
Measurement Principle	Does not require load current compensation Does not require external control or supplementary components Measured during normal turn-on without interruption to operation	Methods require at least one of the following: 1) Load current compensation 2) Additional control signals 3) Supplementary components 4) Brief interruption to operation
Accuracy Validation	Validated via direct Infra-Red thermal measurements Compared with a traditional and accurate TSEP Evaluated on IGBTs with differing geometry Evaluated on IGBTs in paralleled condition (both with and without temperature disequilibrium) Evaluated before and after bondwire lift-off	Little or no validation of TSEPs proposed for online implementation Validation usually limited to a single chip

4.3. Future Work

From the limitations of the thesis, there are several avenues for future research:

- Implement the I_{GPeak} method in a real converter setup and investigate favourable measurement circuit designs to achieve this.
- Validate the I_{GPeak} method on a statistically significant number of IGBTs, including multiple manufacturers.
- Investigate the feasibility of a 'one point calibration' procedure.
- Investigate whether it is possible to use multiple I_{GPeak} measurements under different electrical conditions (i.e. different gate voltage swing), combined with numerical techniques to extract a temperature map across paralleled devices
- Assess the impact of gate oxide degradation on the accuracy of the I_{GPeak} method
- Feasibility assessment of use in Power MOSFETs, or wide-bandgap devices.

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VI. Appendix A – IGBT Die Datasheets

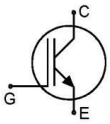
IGC189T120T8RL

IGBT4 Low Power Chip

Features:
- 1200V Trench & Field stop technology
- low switching losses
- positive temperature coefficient
- easy paralleling
- Qualified according to JEDEC for target applications

Recommended for:
- low / medium power modules

Applications:
- low / medium power drives



Chip Type	V_{CE}	I_{Cn} [1)]	Die Size	Package
IGC189T120T8RL	1200V	200A	13.62 x 13.87 mm^2	sawn on foil

[1)] nominal collector current at Tc = 100°C, not subject to production test - verified by design/characterization

Mechanical Parameters

Die size		13.62 x 13.87	mm^2
Emitter pad size (incl. gate pad)		See chip drawing	
Gate pad size		1.31 x 0.811	
Area total		188.9	
Thickness		115	µm
Wafer size		200	mm
Max.possible chips per wafer		125	
Passivation frontside		Photoimide	
Pad metal		3200 nm AlSiCu	
Backside metal		Ni Ag –system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond		Electrically conductive epoxy glue and soft solder	
Wire bond		Al, <500µm	
Reject ink dot size		∅ 0.65mm ; max 1.2mm	
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, Temperature 17°C – 25°C, < 6 month	
	for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C, < 6 month	

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Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, T_{vj} =25 °C	V_{CE}	1200	V
DC collector current, limited by $T_{vj\,max}$	I_C	1)	A
Pulsed collector current, t_p limited by $T_{vj\,max}$ 2)	$I_{c,puls}$	600	A
Gate emitter voltage	V_{GE}	±20	V
Operating junction temperature	T_{vj}	-40 ... +175	°C
Short circuit data 2)3) V_{GE} = 15V, V_{CC} = 800V, T_{vj} = 150°C	t_{SC}	10	µs

1) depending on thermal properties of assembly

2) not subject to production test - verified by design/characterization

3) allowed number of short circuits: <1000; time between short circuits: >1s.

Static Characteristics (tested on wafer), T_{vj} =25 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V , I_C=1 mA	1200			V
Collector-Emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=60A	tbd	tbd	tbd	
Gate-Emitter threshold voltage	$V_{GE(th)}$	I_C=7.4mA , V_{GE}=V_{CE}	5.3	5.8	6.3	
Zero gate voltage collector current	I_{CES}	V_{CE}=1200V , V_{GE}=0V			2.6	µA
Gate-Emitter leakage current	I_{GES}	V_{CE}=0V , V_{GE}=20V			120	nA
Integrated gate resistor	r_G			3.5		Ω

Electrical Characteristics (not subject to production test - verified by design / characterization)

Parameter		Symbol	Conditions	Value			Unit
				min.	typ.	max.	
Collector-Emitter saturation voltage	T_{vj} =25 °C	V_{CEsat}	V_{GE}=15V, I_C=200A	1.55	1.8	2.05	V
	T_{vj} =150 °C				2.1		
Input capacitance		C_{ies}	V_{CE}=25V, V_{GE}=0V, f=1MHz T_{vj} =25 °C		14000		pF
Reverse transfer capacitance		C_{res}			500		

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Further Electrical Characteristic

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

This chip data sheet refers to the device data sheet	FS200R12PT4	Rev 2.1

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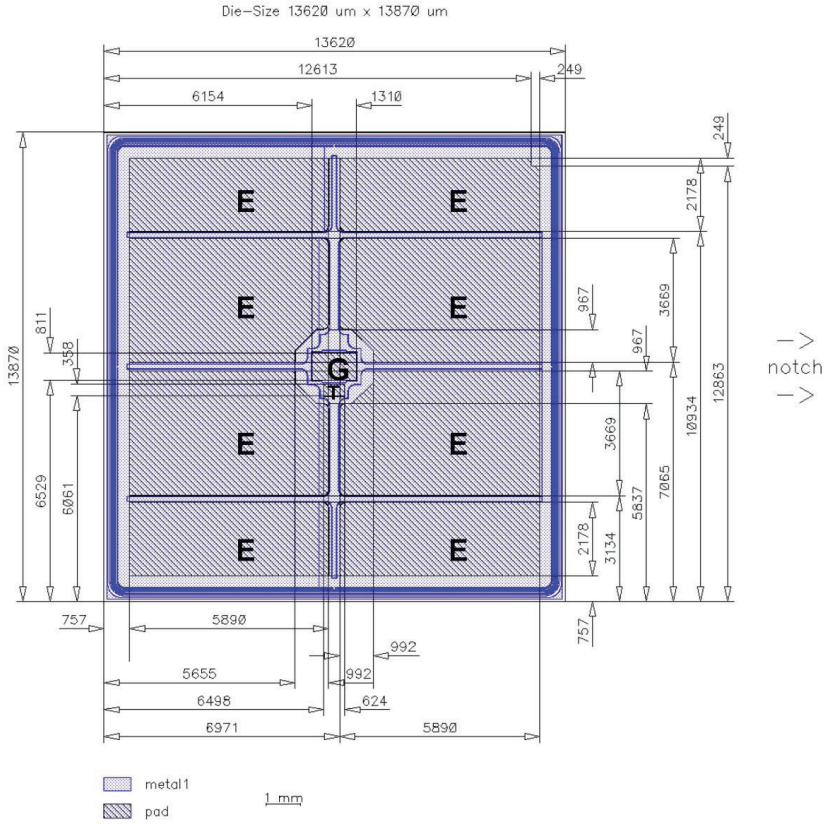
Chip Drawing



E = Emitter
G = Gate
T = Test pad do not contact

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Description

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Version	Subjects (major changes since last revision)	Date

Published by
Infineon Technologies AG
81726 Munich, Germany

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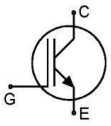
IGC193T120T8RM

IGBT4 Medium Power Chip

Features:
- 1200V Trench & Field stop technology
- low switching losses
- soft turn off
- positive temperature coefficient
- easy paralleling
- Qualified according to JEDEC for target applications

Recommended for:
- medium power modules

Applications:
- medium power drives



Chip Type	V_{CE}	I_{Cn}	Die Size	Package
IGC193T120T8RM	1200V	200A	15.99 x 12.08 mm^2	sawn on foil

Mechanical Parameters

Die size		15.99 x 12.08	mm^2
Emitter pad size (incl. gate pad)		See chip drawing	
Gate pad size		1.31 x 0.811	
Area total		193.2	
Thickness		120	µm
Wafer size		200	mm
Max.possible chips per wafer		121	
Passivation frontside		Photoimide	
Pad metal		3200 nm AlSiCu	
Backside metal		Ni Ag –system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond		Electrically conductive epoxy glue and soft solder	
Wire bond		Al, <500µm	
Reject ink dot size		∅ 0.65mm ; max 1.2mm	
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, Temperature 17°C – 25°C, < 6 month	
	for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C, < 6 month	

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Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, T_{vj} =25 °C	V_{CE}	1200	V
DC collector current, limited by $T_{vj\,max}$	I_C	1)	A
Pulsed collector current, t_p limited by $T_{vj\,max}$ 2)	$I_{c,puls}$	600	A
Gate emitter voltage	V_{GE}	±20	V
Operating junction temperature	T_{vj}	-40 ... +175	°C
Short circuit data 2)3) V_{GE} = 15V, V_{CC} = 800V, T_{vj} = 150°C	t_{SC}	10	µs

1) depending on thermal properties of assembly

2) not subject to production test - verified by design/characterization

3) allowed number of short circuits: <1000; time between short circuits: >1s.

Static Characteristics (tested on wafer), T_{vj} =25 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V , I_C=5.7 mA	1200			V
Collector-Emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=60A	0.97	1.15	1.32	
Gate-Emitter threshold voltage	$V_{GE(th)}$	I_C=7.4mA , V_{GE}=V_{CE}	5.3	5.8	6.3	
Zero gate voltage collector current	I_{CES}	V_{CE}=1200V , V_{GE}=0V			2.6	µA
Gate-Emitter leakage current	I_{GES}	V_{CE}=0V , V_{GE}=20V			120	nA
Integrated gate resistor	r_G			3.5		Ω

Electrical Characteristics (not subject to production test - verified by design / characterization)

Parameter		Symbol	Conditions	Value			Unit
				min.	typ.	max.	
Collector-Emitter saturation voltage	T_{vj} =25 °C	V_{CEsat}	V_{GE}=15V, I_C=200A	1.55	1.8	2.05	V
	T_{vj} =150 °C				2.05		
Input capacitance		C_{ies}	V_{CE}=25V, V_{GE}=0V, f=1MHz T_{vj} =25 °C		12500		pF
Reverse transfer capacitance		C_{res}			680		

Further Electrical Characteristic

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

This chip data sheet refers to the device data sheet	FF600R12ME4_B11	Rev 2.0

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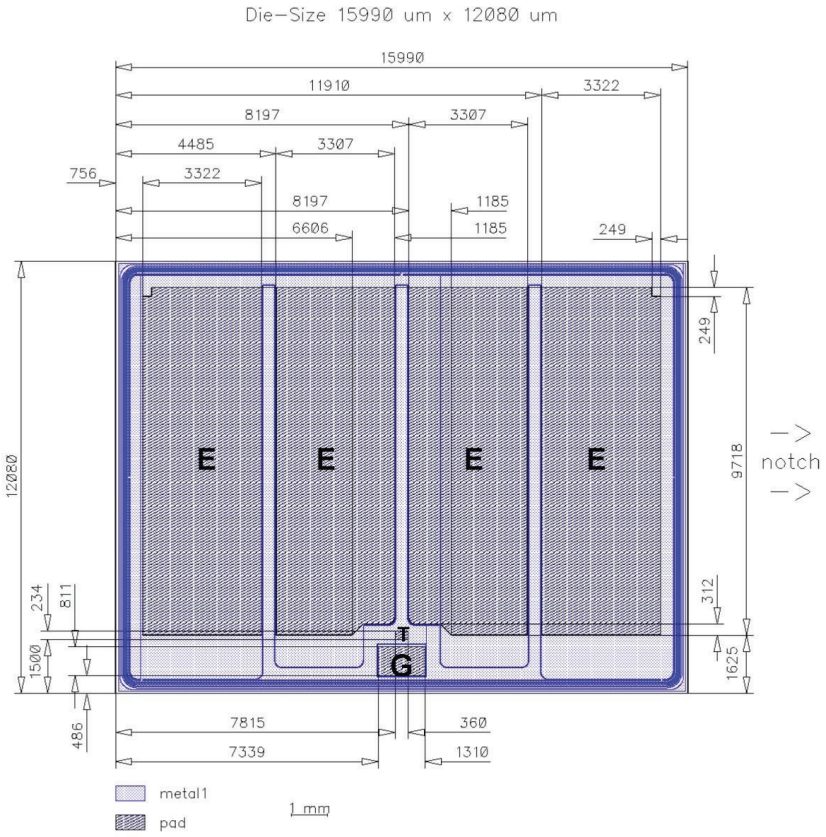
Chip Drawing



E = Emitter
G = Gate
T = Test pad do not contact

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Description

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Version	Subjects (major changes since last revision)	Date

Published by
Infineon Technologies AG
81726 Munich, Germany

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VII. Appendix B – Dissipation Results Table

Complete table of temperature measurement results from experiments performed in Chapter 3.

IGBT A - Healthy					
Current (A)	**I_{GPeak} (°C)**	**$V_{CE(low)}$ (°C)**	**IR_{Gate} (°C)**	**IR_{Mean} (°C)**	**IR_{Max} (°C)**
0	42.1	42.0	41.7	41.8	42.1
40	63.9	63.0	63.3	63.1	65.3
80	98.7	97.6	97.4	96.8	102.1
100	122.3	120.5	120.1	119.4	126.7
120	150.1	148.0	147.2	146.5	156.5
140	179.2	178.2	177.5	176.9	190.5

IGBT A - Degraded					
Current (A)	**I_{GPeak} (°C)**	**$V_{CE(low)}$ (°C)**	**IR_{Gate} (°C)**	**IR_{Mean} (°C)**	**IR_{Max} (°C)**
0	40.9	40.5	40.8	40.9	41.3
40	63.1	62.7	62.9	63.0	65.8
80	99.6	98.6	97.7	98.0	105.1
100	123.9	122.9	121.3	121.8	132.2
120	152.5	152.1	149.6	150.6	165.3
140	182.1	184.0	180.7	182.5	203.1

IGBT B					
Current (A)	**I_{GPeak} (°C)**	**$V_{CE(low)}$ (°C)**	**IR_{Gate} (°C)**	**IR_{Mean} (°C)**	**IR_{Max} (°C)**
0	41.8	41.6	41.5	41.6	41.8
40	60.6	62.4	60.9	62.2	64.3
80	90.8	93.5	89.2	92.7	97.6
100	109.5	112.7	106.6	111.7	118.4
120	127.4	133.2	124.9	132.1	140.7
140	147.6	156.4	144.9	155.3	166.5
160	175.0	186.5	171.3	186.0	201.5

IGBT A - 2x Paralleled without Temperature Disequilibrium						
Current (A)	**I_{GPeak} (°C)**	**$V_{CE(low)}$ (°C)**	**IR_{Gate} T1 (°C)**	**IR_{Gate} T2 (°C)**	**IR_{Mean} T1 (°C)**	**IR_{Mean} T2 (°C)**
120	92.2	90.6	90.7	90.8	90.3	90.4
160	113.7	111.6	110.5	112.6	110.0	111.9
200	140.3	138.1	136.7	139.5	135.7	138.6
240	173.9	171.7	171.0	172.6	170.1	172.2

IGBT A - 2x Paralleled with Temperature Disequilibrium						
Current (A)	**I_{GPeak} (°C)**	**$V_{CE(low)}$ (°C)**	**IR_{Gate} T1 (°C)**	**IR_{Gate} T2 (°C)**	**IR_{Mean} T1 (°C)**	**IR_{Mean} T2 (°C)**
120	96.2	94.1	89.2	98.6	88.4	98.1
160	122.0	121.1	113.1	127.1	112.2	126.3
200	153.1	152.3	142.5	160.5	141.4	159.4

VIII. Appendix C – Attached Collection of Papers

ISSN (online): 2246-1248
ISBN (online): 978-87-7112-548-1

AALBORG UNIVERSITY PRESS