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Five-Level Active-Neutral-Point-Clamped DC/DC Converter for Medium Voltage DC Grids

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***Abstract*—This paper proposes a five-level active-neutral-point-clamped (5L-ANPC) dc/dc converter for applications in medium voltage dc (MVDC) grids. A modulation strategy is proposed for the 5L-ANPC dc/dc converter to generate multi-level voltage waveforms, which can effectively reduce voltage change rate *dv/dt*, reduce voltage stress on the transformer, and thus reduce the electromagnetic interference (EMI) and increase reliability. An elimination method for the dead time effect is also proposed along with the proposed modulation strategy by employing a switch in series with the flying capacitor, which can effectively eliminate high voltage leaps caused by the dead time effect. In addition, a capacitor voltage control strategy is proposed for the 5L-ANPC dc/dc converter to ensure the balanced flying capacitor voltage and desired five-level voltage waveforms. Finally, simulation and experimental studies are conducted, and the results have verified the proposed converter and control strategies.**

***Index Terms*—Dc/dc converter, five-level active-neutral-point-clamped (5L-ANPC), medium voltage dc (MVDC) grids.**

I. Introduction

DC-based distributions and dc-based micro-grids have been proposed as promising solutions for future smart-grid systems because of their clear merits, such as no reactive power, no frequency stability, high conversion efficiency, and easy system control [1-3]. Furthermore, dc-based data centers and residential systems have also been increasingly developed recently [4], [5]. The performance of dc-based systems highly depends on dc/dc converters because these converters are responsible for delivering power and changing voltage levels among dc-based systems. Accordingly, a dc/dc converter with high performances and high reliability is desired for the dc grids.

So far, a number of dc/dc converters for dc grids have been reported in literature and these dc/dc converters can be classified into two types, namely non-isolated converters and isolated converters. The isolated converters can gain galvanic isolation and a high ratio of voltage conversion by utilizing the high frequency transformer in comparison with the non-isolated converters [6], [7], and thus increase the reliability and safety of whole dc-based systems [8], [9], which makes them normally applied into the medium voltage dc-based systems [10-13]. Generally, there are mainly three types of isolated dc/dc converters including two-level based isolated converters, three-level (TL) based isolated converters, and modular multilevel converters (MMC). The two-level based isolated dc/dc converters require least quantity of power switches in medium voltage applications [11-13]. However, the power switches in them have to withstand the full dc bus voltage, which results in high conduction losses, high voltage change rate *dv*/*dt*, and large electromagnetic interference (EMI) [14-16]. The MMC distinguish themselves from others due to their low switches' voltage stress, low EMI, and good power quality arising from the increasing amount of voltage levels [17-19]. However, it would require more power switches, voltage transducers with increased cost [20], and complicated control algorithm for capacitor voltage balancing [21], [22]. Normally, the two-level based converters and MMC are more suitable for power transmission in low voltage and high voltage dc-based distributions [23], [24] respectively.

The TL based isolated dc/dc converters were presented in [25-35] with the advantage of low switch voltage stress, good EMI, improved power quality, and small filter size in comparison with the two-level based isolated dc/dc converter, simpler circuit structure, easier control strategy, and more reliability in comparison with MMC. Therefore, TL based converters are regarded as a favorable choice for high power converters applied to the medium voltage dc (MVDC) grids [25] with dc bus voltage of several thousand volts [36-38]. In 1992, a novel TL dc/dc converter was first proposed to lower the switch voltage stress for high voltage applications [26]. A zero voltage and zero current switching TL dc/dc converter was proposed in [27], in which a flying capacitor in primary side and an auxiliary circuit in the secondary side are added to achieve zero voltage switching of the leading switches and zero current switching of the lagging switches for improving the converter's efficiency. The soft switching technique for the TL dc/dc converter was systematically discussed in [28]. An isolated full bridge TL (FBTL) dc/dc converter and a hybrid isolated FBTL dc/dc converter were presented in [29] and [30] respectively, in which a double phase-shift control strategy and a chopping phase-shift control strategy were proposed respectively to achieve soft switching in FBTL converter. Other research works about the TL based dc/dc converters have also been conducted on the topics of topology and control strategy [31-34]. The major contributions of above works are mainly

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focused on soft switching techniques and power density to increase the converter's efficiency. When it comes to the applications of MVDC grids, the voltage stress on the transformer in TL based converters should be taken into consideration since MVDC grids have a high dc bus voltage and such high dc bus voltage would increase the voltage stress on the transformer, thus increases EMI and decreases the system reliability. However, little attention has been put on this topic in literatures so far. An improved FBTL dc/dc converter with a voltage balance control strategy was proposed in [35] for wind turbines in medium voltage dc-based system, which can reduce the *dv/dt* and voltage stress on the transformer. However, a passive filter is added into the primary side of the transformer, which reduces the step-up rate and converter's efficiency.

In this paper, a 5L-ANPC dc/dc converter with the corresponding modulation strategy is proposed to step down the medium voltage about several thousands volts to the low voltage about a few hundred volts [39-41] for the dc loads, which can effectively reduce voltage change rate *dv/dt*, reduce voltage stress on the transformer, thus reduce EMI and increase reliability. Comparing with the FBTL dc/dc converter, the proposed converter makes the power switches with low voltage stress ($V_{in}/4$) applicable to generate the five-level voltages. A switch in series with the flying capacitor is employed in the proposed dc/dc converter structure, which can effectively eliminate the dead time effect along with the proposed modulation strategy. In addition, a capacitor voltage control strategy is proposed to balance the voltage of the flying capacitor, which can ensure the generation of desired multi-level voltage waveforms. The proposed converter is inspired by the conventional 5L-ANPC inverter [42], [43]. However, the proposed voltage control strategy of the flying capacitor and elimination method for the dead time effect mentioned above are original improvements for the 5L-ANPC dc/dc converter. Finally, the proposed converter and capacitor voltage control strategy is validated by simulation as well as experimentation with a down-scale laboratory prototype.

This paper is organized as follows. Section II introduces the structure and modulation strategy of the proposed converter. The dead time effect on the proposed converter and its elimination method are discussed in section III. In section IV, a capacitor voltage control strategy is proposed for balancing the flying capacitor's voltage. Section V presents the simulation and experimentation results to verify the theoretical analysis. Finally, the main contributions of this paper are summarized in Section VI.

II. PROPOSED 5L-ANPC DC/DC CONVERTER

A. Structure of Proposed Converter

Fig. 1 shows the structure of the proposed 5L-ANPC dc/dc converter. In the primary side, two input capacitors C_1, C_2 are used to split the input voltage V_{in} into two voltages V_{c1} and V_{c2}. S_1-S_9 and D_1-D_9 are power switches and power diodes. C_3 is the flying capacitor of the proposed converter. T_r is the medium frequency transformer (MFT) to gain voltage level conversion and galvanic isolation. In the secondary side, there are four rectifier diodes D_{r1}-D_{r4}, an output filter inductor L_o, and an output filter capacitor C_o. i_{c3} is the current flowing through the flying capacitor C_3. i_{Lo} and i_o are the currents flowing through output inductor L_o and load respectively. V_{c3} and V_{out} are the voltage of C_3 and output. V_{ab} and i_p are the primary side voltage and current of MFT. The positive directions of currents i_{c3}, i_p, i_{Lo}, i_o and voltages V_{c1}, V_{c2}, V_{c3}, V_{ab}, V_{out} are defined as shown in Fig. 1. One thing to be mentioned is that S_9 is employed in series with the flying capacitor in order to eliminate the dead time effect, which will be analyzed in detail in Section III.

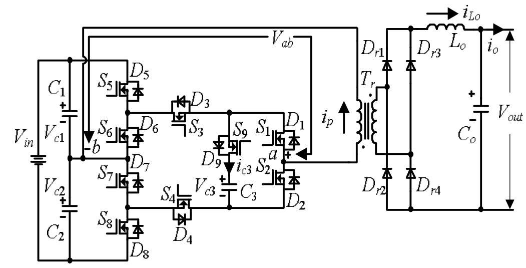


Fig. 1. Structure of the proposed 5L-ANPC dc/dc converter.

B. Proposed Modulation Strategy

A modulation strategy including two operation modes with different switching sequences is proposed to generate five-level voltages on the primary of the transformer (V_{ab}) as shown in Fig. 2, in which (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) are complementary switch pairs; d_{rv1}-d_{rv9} are driving signals for power switches S_1-S_9; D_1-D_4 are duty ratios in one cycle period, which are the same in the operation mode I and II; T_s is the time period of one cycle. In the normal operation conditions, $V_{c1} = V_{c2} = V_{in}/2$ and $V_{c3} = V_{in}/4$.

1) Operation mode I: Fig. 2(a) illustrates the operation mode I in one cycle. In the first half cycle, the driving signal d_{rv1} lags behind d_{rv3} by $(D_2\text{-}D_1)\times T_s/2$. In the second half cycle, d_{rv2} lags behind d_{r4} by $(D_2\text{-}D_1)\times T_s/2$. The duty ratios of d_{rv5} and d_{rv8} are both D_3 and less than 0.5, but d_{rv8} delays $T_s/2$ from d_{rv5}. Similarly, the duty ratios of d_{rv6} and d_{rv7} are the same but more than 0.5 since (d_{rv5}, d_{rv6}) and (d_{rv7}, d_{rv8}) are complementary pairs respectively. Therefore, there is an overlap time ΔT_L between d_{rv6} and d_{rv7} in every half cycle as shown in Fig. 2. In the operation mode I, there are eight switching states namely $V0$, $V2$, $V3$, $V4$, $V5$, $V6$, $V7$, and $V9$ as listed in Table I. The flying capacitor is charged in switching states $V2$ and $V7$, which in turn means the current flowing through the flying capacitor i_{c3} is positive in such two switching states as shown in Fig. 2(a).

2) Operation mode II: The operation mode II is similar to the operation mode I, which is shown in Fig. 2(b). The driving signal d_{rv3} lags behind d_{rv1} by $(D_2\text{-}D_1)\times T_s/2$ in the first half cycle. In the second half cycle, d_{rv4} lags behind d_{rv2} by $(D_2\text{-}D_1)\times T_s/2$. In the operation mode II, there are also eight switching states including $V1$, $V3$, $V4$, $V5$, $V6$, $V8$, and $V9$ as listed in Table I. In addition, the flying capacitor is discharged in switching states $V1$ and $V8$, which in turn means the current flowing through the flying capacitor i_{c3} is negative in such two switching states as shown in Fig. 2(b).

Comparing the operation mode I with the operation mode II as shown in Fig. 2, it can be observed that: 1) the driving signals d_{rv5}, d_{rv6}, d_{rv7}, and d_{rv8} are the same in the operation mode I and

II; 2) the driving signals d_{rv1} and d_{rv3} are shifted with each other between the operation mode I and II, which is the same for d_{rv2} and d_{rv4}.

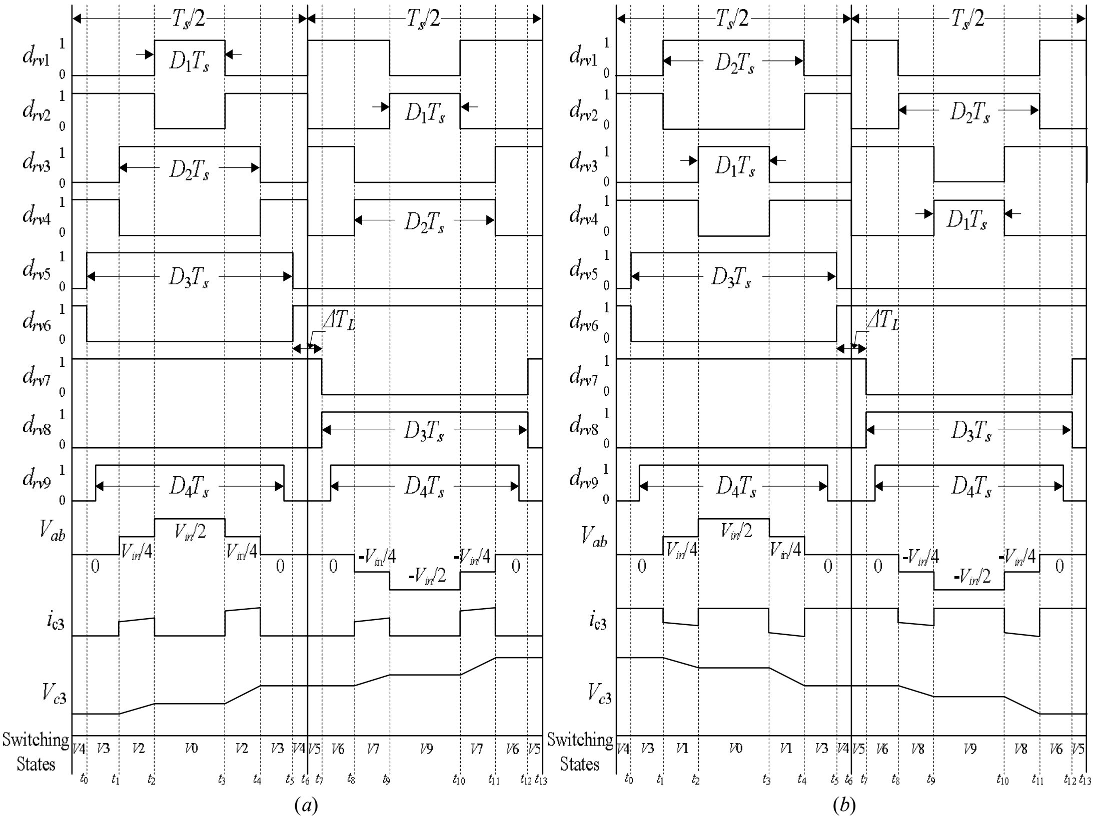


Fig. 2. Proposed modulation strategy. (a) Operation mode I. (b) Operation mode II.

TABLE I
SWITCHING STATES AND CIRCUIT OPERATION STATUSES OF THE 5L–ANPC CONVERTER

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_{ab}	i_{c3}
$V0$	1	0	1	0	1	0	1	0	1	V_{c1} ($V_{in}/2$)	0
$V1$	1	0	0	1	1	0	1	0	1	V_{c3} ($V_{in}/4$)	$-\lvert i_p\rvert$
$V2$	0	1	1	0	1	0	1	0	1	V_{c1}-V_{c3} ($V_{in}/4$)	$+\lvert i_p\rvert$
$V3$	0	1	0	1	1	0	1	0	1	0	0
$V4$	0	1	0	1	0	1	1	0	0	0	0
$V5$	1	0	1	0	0	1	1	0	0	0	0
$V6$	1	0	1	0	0	1	0	1	1	0	0
$V7$	1	0	0	1	0	1	0	1	1	-(V_{c2}-V_{c3}) (-$V_{in}/4$)	$+\lvert i_p\rvert$
$V8$	0	1	1	0	0	1	0	1	1	-V_{c3} (-$V_{in}/4$)	$-\lvert i_p\rvert$
$V9$	0	1	0	1	0	1	0	1	1	-V_{c2} (-$V_{in}/2$)	0

III. Proposed Elimination Method For Dead Time Effect

In this section, an elimination method for the dead time effect by employing a power switch in series with the flying capacitor is proposed along with the proposed modulation strategy to eliminate the high voltage leaps caused by the dead time effect.

A. Analysis of Dead Time Effect

In practical circuits, the dead time has to be set for each complementary switch pairs to avoid that they are switched on at the same time. For instance, if S_5 and S_6 are switched on simultaneously, the input capacitor C_1 will be shorted, which will damage S_5 and S_6 due to the overcurrent. In the operation mode I, if switch S_9 is not employed, the dead time ΔT_d between every two adjacent half cycles would lead a high voltage leap on the primary side voltage of MFT V_{ab} as marked in Fig. 3. The reason of causing such high voltage leaps in the operation mode II is same as that in the operation mode I, so only operation mode I and its equivalent circuits are shown in Fig. 3 and Fig. 4 for explanation. Before analyzing such reason, two simplifications are made here: 1) all the power devices and diodes are ideal, which means rise time and fall time of the power switches and diodes are neglected and the switch junction capacitance effects on the circuit operation are neglected; 2) the dead times are same for all complementary pairs.

Before t_5, V_{ab} is 0 V because S_2, S_4, and S_7 are all in the on-state as shown in Fig. 4(a). At t_5, S_2, S_4, S_5, and S_7 are switched off simultaneously, and thus the transformer's primary current i_p freewheels through C_2, D_8, D_4, and D_2 as shown in Fig. 4(b) (red area), which leads that V_{ab} decreases to $-V_{c2}$ ($-V_{in}/2$) from 0 V. At t_6, S_1, S_3, S_6, and S_8 are switched on, V_{ab} returns to 0 V with the connection of S_1, S_3, and S_6 as shown in Fig. 4(c). At t_{11}, S_1, S_3, S_6, and S_8 are switched off, which causes that V_{ab} increases to V_{c1} ($V_{in}/2$) from 0 V by the path connected through D_1, D_3, D_5, and C_1 as shown in Fig. 4(d). The analysis of following operation behaviors as shown in Fig. 3 (blue area) is similar to that in the last half cycle (red area in Fig. 3), which is not repeated here. Based on above analysis, it can be summarized that a voltage leap of V_{ab} with the amplitude of $V_{in}/2$ or $-V_{in}/2$ would emerge in the dead time between every two adjacent half cycles.

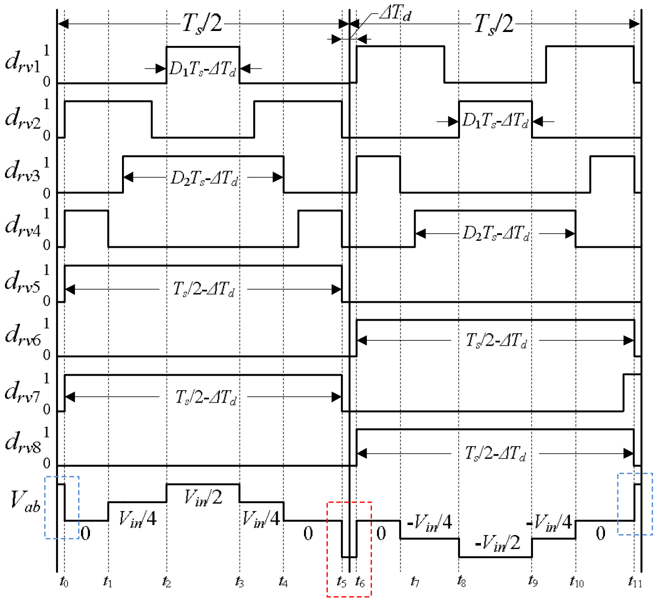


Fig. 3. Operation mode I without S_9.

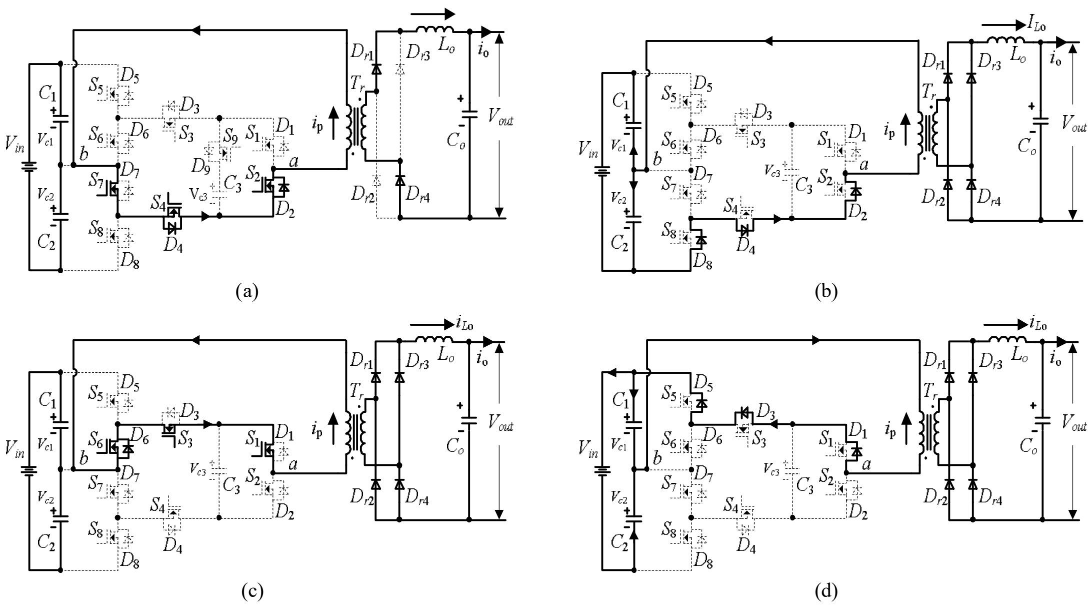


Fig. 4. Equivalent circuits. (a) [t_4 - t_5]. (b) [t_5 - t_6]. (c) [t_6 - t_7]. (d) [t_{11} - t_0].

B. Proposed Elimination Method for Dead Time Effect

These voltage leaps need to be eliminated because they have high voltage change rate dv/dt resulting in large EMI. Keeping S_6 and S_7 both on in the dead time can keep V_{ab} at 0 V and get rid of these voltage leaps, however it will short the flying capacitor C_3 through D_3, D_4, S_6, and S_7 as marked with red color in Fig. 5. In light of this, S_9 in series with the flying capacitor C_3 is proposed to avoid the short of C_3 by switching off S_9 when both S_6 and S_7 are switched on as shown in Fig. 1. Furthermore, after employing S_9, the corresponding switching states $V4$ and $V5$ are also proposed to be applied into the proposed modulation strategy as shown in Fig. 2.

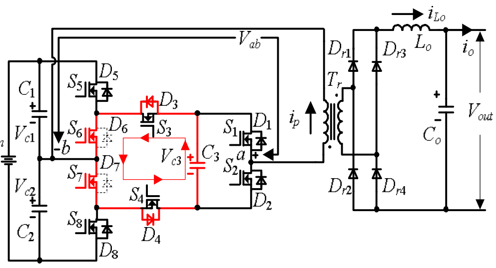


Fig. 5. Short path of C_3 without S_9.

In the operation mode I, the working principles and equivalent circuits after employing S_9 are shown in Fig. 6 and Fig. 7.

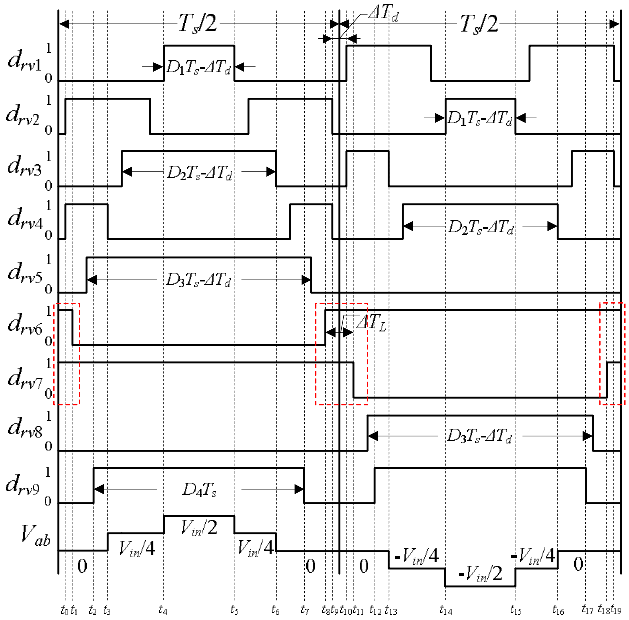


Fig. 6. Operation mode I with S_9.

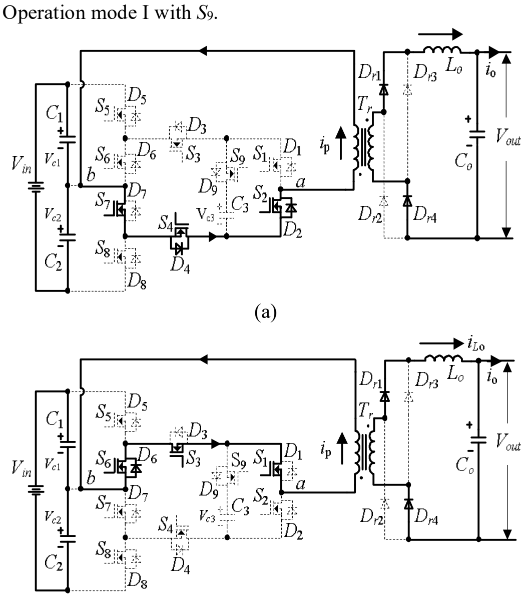


Fig. 7. Equivalent circuits. (a) [t_7 - t_{10}]. (b) [t_{10} - t_{12}].

At t_7, S_9 is switched off, but this switching action has no effect on V_{ab} since C_3 does not involve into the circuit operation at this time. At t_8, S_6 is switched on, V_{ab} remains at 0V because the S_2, S_4, and S_7 are kept on, shorting the primary side of the transformer. Then, though S_2 and S_4 are switched off at t_9, the primary side of the transformer is still short through S_7, D_2, and D_4 respectively. At t_{10}, S_1 and S_3 are switched on, thus the on-state of S_1, S_3, and S_6 keep V_{ab} at 0 V. Finally, S_7 and S_9 are switched off at t_{11} and t_{12} respectively, but making no influence on V_{ab}. From the above analysis, V_{ab} stays at 0V in the period [t_7, t_{12}]. The equivalent circuits in period [t_7, t_{10}] and [t_{10}, t_{12}] are shown in Fig. 7(a) and Fig. 7(b) respectively. At t_{17}, S_9 is switched off for the next half cycle. The following operation works similarly to that in period [t_7, t_{12}] and V_{ab} also maintains at 0 V. One thing to be mentioned is that the duty ratios D_3 and D_4 are set for eliminating the dead time effect, in which D_3 is set shorter than 0.5 to gain overlap time ΔT_L between two switching functions of S_6 and S_7 in every half cycle as marked in Fig. 6. The overlap time ΔT_L needs to be longer than dead time ΔT_d and D_4 is required to be shorter than (D_3-$\Delta T_d/T_s$). Based on the above analysis, the employed S_9 only has switching actions when V_{ab} equals to 0 V. Furthermore, the switching actions of S_9 happen while there is no current flowing through S_9 and have no effect on the V_{ab} and i_p. The voltages on S_1, S_2, S_3, and S_4 could not clamped by the flying capacitor C_3 when S_9 is turned off in the dead time, but increasing the capacitance of the paralleled capacitors of the switches S_3 and S_4 can make the voltages on C_1, C_3 and voltages on C_2, C_4 are balanced. Therefore, the proposed elimination method of the dead time effect by employing S_9 in series with the flying capacitor C_3 would not cause voltage unbalance among the power switches S_1, S_2, S_3, and S_4 in the dead time for the high power applications. In addition, from Fig. 6 it can be observed that: 1) S_5-S_8 and S_9 can achieve zero-current-switching; 2) S_1-S_4 can achieve zero-voltage switch-on in most switching operations except that S_1 cannot achieve zero-voltage switch-on at t_4; S_2 cannot achieve zero-voltage switch-on at t_{14}.

In summary, after using the proposed elimination method for the dead time effect, V_{ab} can be kept at 0 V in the dead time between every two adjacent half cycles in the operation mode I, which avoids causing high voltage leaps. The dead time effect in the operation mode II can also be eliminated with the same method utilized in the operation mode I, which is not repeated here.

IV. Proposed Capacitor Voltage Control Strategy

The voltage balance of the flying capacitor C_3 is one of the important issues in the proposed converter because it directly affects multi-level voltage waveforms. In this section, a capacitor voltage control strategy is proposed.

A. In Operation Mode I

From Fig. 2 (a), in the first half cycle, it can be observed that V_{ab} is positive and the switching states are:

$$V4 \rightarrow V3 \rightarrow V2 \rightarrow V0 \rightarrow V2 \rightarrow V3 \rightarrow V4 \tag{1}$$

According to Fig. 2 and Table I, the charge or discharge of the flying capacitor C_3 occurs when V_{ab} equals $V_{in}/4$ or -$V_{in}/4$, and the related switching states are $V1$, $V2$, $V7$, or $V8$. Furthermore, C_3 is charged in switching states $V2$, $V7$ and is discharged in $V1$, $V8$ respectively. In the first half cycle, the switching state is $V2$ when V_{ab} equals $V_{in}/4$. Therefore, C_3 is charged in the first half cycle according to the above analysis.

In the second half cycle, V_{ab} is negative and the switching states are:

$$V5 \rightarrow V6 \rightarrow V7 \rightarrow V9 \rightarrow V7 \rightarrow V6 \rightarrow V5 \tag{2}$$

Similar to the analysis of the first half cycle, the switching state is $V7$ when V_{ab} equals -$V_{in}/4$ in the second half cycle, so C_3 is also charged and not discharged in the second half cycle. In summary, C_3 is charged but not discharged in the operation mode I.

B. In Operation Mode II

From Fig. 2 (b), in the first half cycle, V_{ab} is positive and the switching states are:

$$V4 \to V3 \to V1 \to V0 \to V1 \to V3 \to V4 \quad (3)$$

In the second half cycle, V_{ab} is negative and the switching states are:

$$V5 \to V6 \to V8 \to V9 \to V8 \to V6 \to V5 \quad (4)$$

With the similar analysis as the operation mode I that the charge or discharge situation of C_3 occurs when V_{ab} equals $V_{in}/4$ or $-V_{in}/4$, it can be observed that the switching states are $V1$ and $V8$ respectively when V_{ab} equals to $V_{in}/4$ and $-V_{in}/4$. Therefore, C_3 is discharged but not charged in the operation mode II.

C. *Proposed Capacitor Voltage Control Strategy*

According to above analysis, the voltage of the flying capacitor C_3 would increase in the operation mode I and decrease in the operation mode II as shown in Fig. 2. Consequently, a capacitor voltage control strategy is proposed for balancing V_{c3} by alternatively utilizing the two operation modes of the proposed modulation strategy as shown in Fig. 8, in which a comparator is used with two input voltages V_{c3} and V_{ref_c3}. V_{ref_c3} is a voltage reference of the flying capacitor C_3 and is normally set at a quarter of input voltage $V_{in}/4$. If V_{c3} is less than V_{ref_c3}, the operation mode I is selected for the next cycle. Otherwise, the operation mode II is chosen for the next cycle when V_{c3} is more than or equals to V_{ref_c3}.

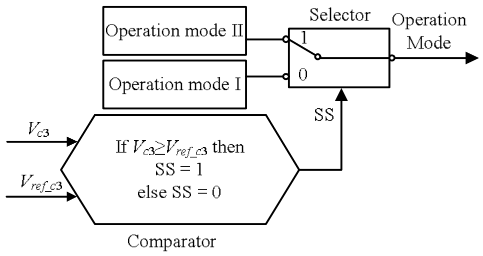


Fig. 8. Diagram of the proposed capacitor voltage control strategy.

V. Simulation And Experimental Verification

A. *Simulation Verification*

In the simulation model, a case which applies the proposed converter to transfer power from the dc bus voltage with 4 kV to the dc loads with the input voltages (800 V) is studied. The parameters of the simulation model are listed in Table II. When the proposed converter operates at a steady state, simulation results are shown in Fig. 9, which includes voltages V_{in}, V_{ab}, V_{c3}, V_{out} and currents i_p, i_o.

In Fig. 9, it can be observed that the five-level voltages are produced on the primary side of the transformer by the proposed modulation strategy, which effectively reduces the voltage change rate *dv/dt*, and the voltage of the flying capacitor V_{c3} can be controlled at 1 kV constantly by utilizing the proposed capacitor voltage control strategy.

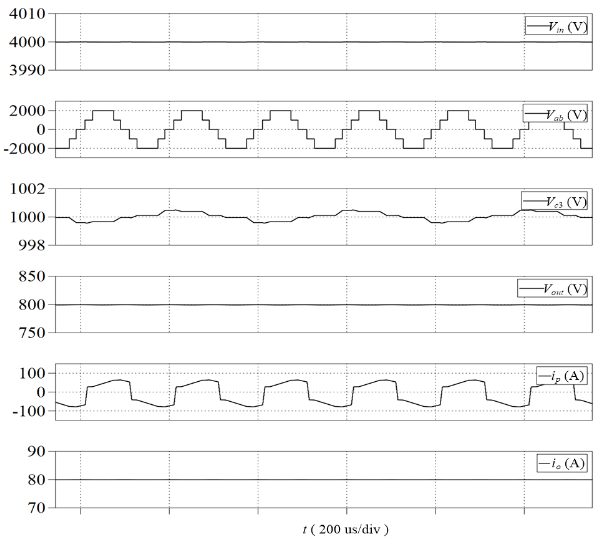
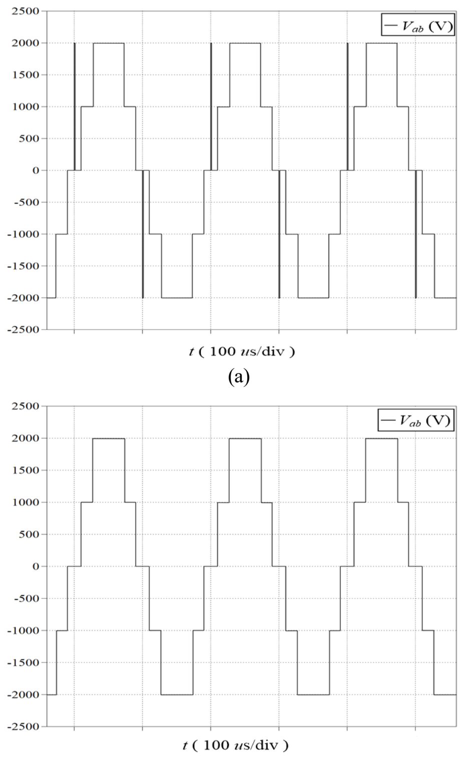


Fig. 9. Simulation results including V_{in}, V_{ab}, V_{c3}, V_{out}, i_p, and i_o.

Through comparing results between without S_9 and with S_9 as exhibited in Fig. 10, it can be observed that the high voltage leaps caused by the dead time effect are effectively eliminated after utilizing the proposed elimination method.



(b)

Fig. 10. Simulation results of V_{ab}. (a) Without S_9. (b) With S_9.

According to the circuit parameters and simulation results of the simulation model, the efficiency by theoretical calculation [44] under the full load (64-kW) is about 94.8%, in which the parameters of FS100R17N3E4 and FF200R33KF2C are used for S_1/D_1-S_4/D_4, S_9/D_9 and S_5/D_5-S_8/D_8 respectively and the parameters of DDB6U144N16 are used for the output rectifier diodes. Fig. 11 presents the theoretically calculated distribution of the power losses under the full load.

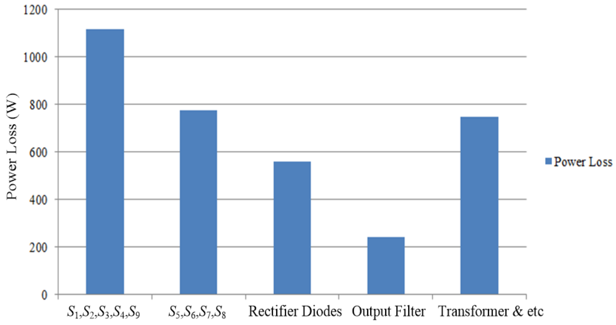
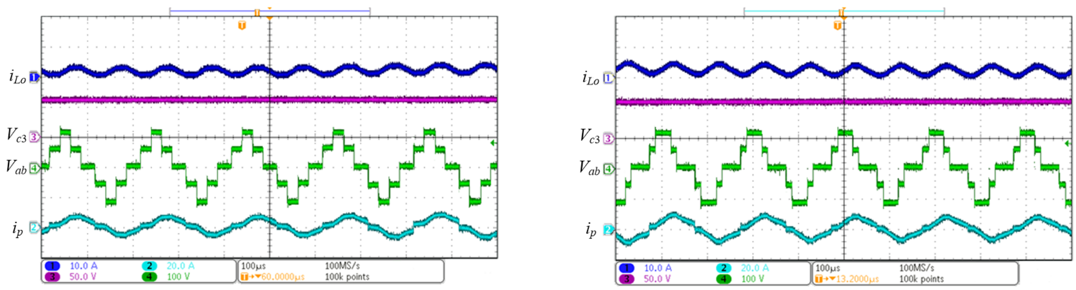


Fig. 11. Caculated power loss distribution under 64-kW (D_2 = 0.35).

B. Experimental Verification

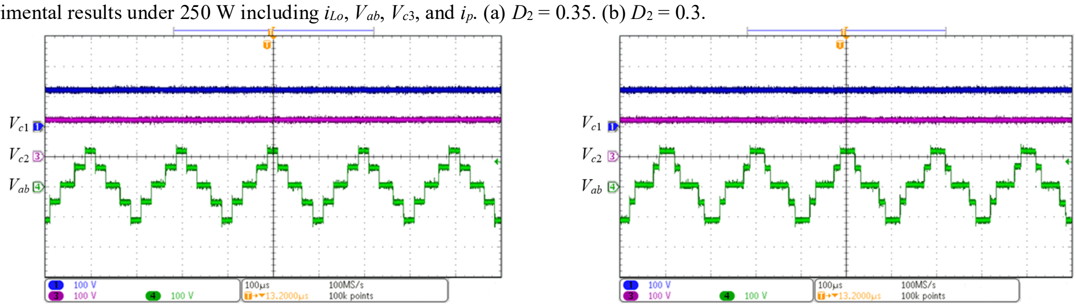
In order to verify the performances of the proposed converter and voltage control strategy, a 1-kW laboratory prototype is built and tested. A simple PI controller is applied in the prototype to control the output voltage. The parameters of the experimental setup are listed in Table III.

The performances of the proposed converter operating at 250 W are shown in Figs. 12-14, in which (a) is with $D_2 = 0.35$, and (b) is with $D_2 = 0.3$. Fig. 12(a) and Fig. 12(b) show V_{ab}, V_{c3}, i_{Lo}, and i_p. It can be seen that the five-level voltages are produced on the primary side voltage of transformer V_{ab}, which can effectively reduce the voltage change rate dv/dt, and the voltage of the flying capacitor V_{c3} is controlled constantly at about 60 V by the proposed capacitor voltage control strategy. The voltages of C_1 and C_2 are about 120 V which is half of input voltage as shown in Fig. 13(a) and Fig. 13(b). In Fig. 14(a) and Fig. 14(b), V_{out}, i_o, and V_{ds_S9} are exhibited. V_{ds_S9} is the drain-source voltage of S_9. It can be seen that the voltage stress of S_9 is only about 60 V, which is a quarter of the input voltage, and V_{out} is controlled at 100 V constantly.



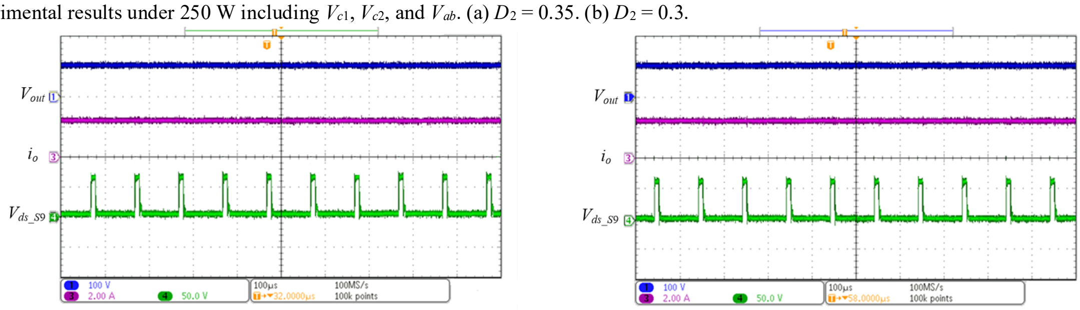
(a) (b)

Fig. 12. Experimental results under 250 W including i_{Lo}, V_{ab}, V_{c3}, and i_p. (a) $D_2 = 0.35$. (b) $D_2 = 0.3$.



(a) (b)

Fig. 13. Experimental results under 250 W including V_{c1}, V_{c2}, and V_{ab}. (a) $D_2 = 0.35$. (b) $D_2 = 0.3$.



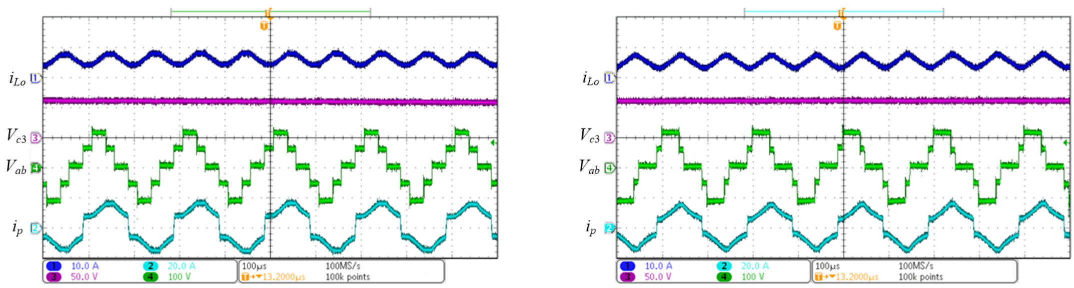
(a) (b)

Fig. 14. Experimental results under 250 W including V_{out}, i_o, and V_{ds_S9}. (a) $D_2 = 0.35$. (b) $D_2 = 0.3$.

Figs. 15-17 show the performances of the proposed converter operating at 500 W, in which (a) is with $D_2 = 0.35$, and (b) is with $D_2 = 0.3$ respectively. V_{ab}, V_{c3}, i_{Lo}, and i_p are shown in Fig. 15(a) and Fig. 15(b). It is can be seen that V_{ab} has five-level voltages and V_{c3} is also kept at about 60 V. Fig. 16(a) and Fig. 16(b) show the votlage of C_1 and C_2, which are about 120 V. In Fig. 17(a) and Fig. 17(b), V_{out}, i_o, and V_{ds_S9} are shown and S_9 only sustains about 60 V which is a quarter of the input voltage.

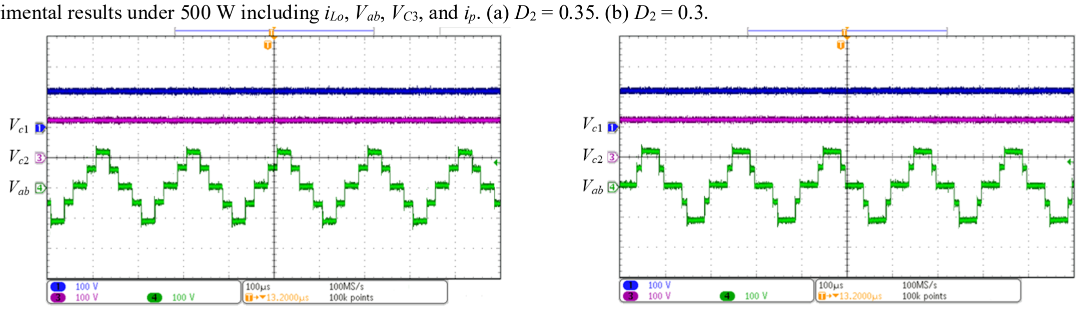
Based on the above experimental results, it can be observed that five-level voltages are generated on the transformer, which can reduce the voltage change rate dv/dt, voltage stress and harmonics on the transformer. Such advantages can not only improve the reliability of the transformer but also improve the reliability of the converter by reducing the EMI.

The comparison results between with S_9 and without S_9 are shown in Fig. 18. The voltage leaps of V_{ab} between every two adjacent half cycles caused by the dead time are effectively eliminated by utilizing the proposed elimination method.



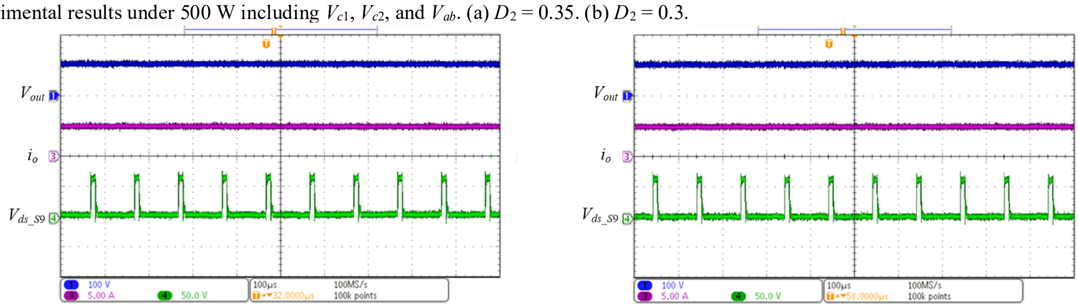
(a) (b)

Fig. 15. Experimental results under 500 W including i_{Lo}, V_{ab}, V_{C3}, and i_p. (a) $D_2 = 0.35$. (b) $D_2 = 0.3$.



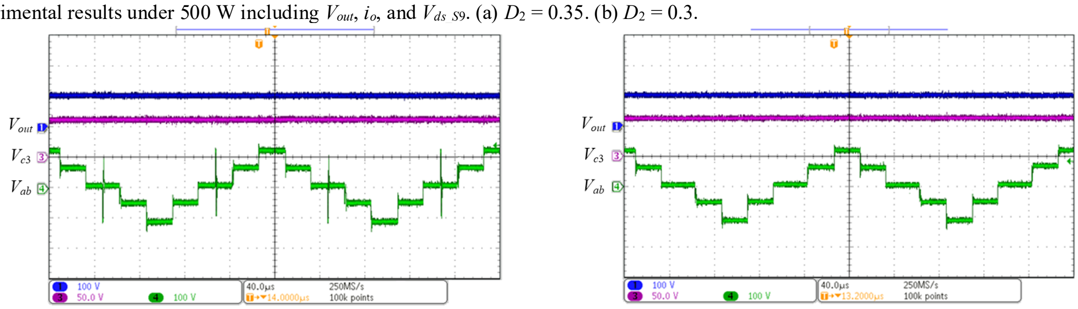
(a) (b)

Fig. 16. Experimental results under 500 W including V_{c1}, V_{c2}, and V_{ab}. (a) $D_2 = 0.35$. (b) $D_2 = 0.3$.



(a) (b)

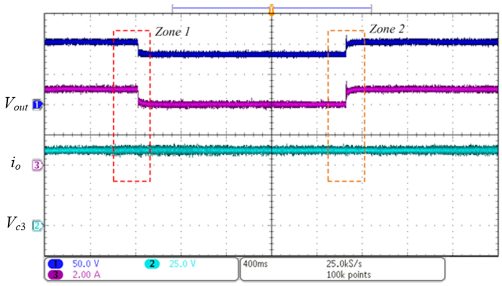
Fig. 17. Experimental results under 500 W including V_{out}, i_o, and V_{ds_S9}. (a) $D_2 = 0.35$. (b) $D_2 = 0.3$.



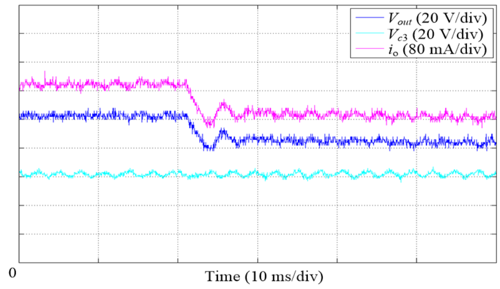
(a) (b)

Fig. 18. Comparison result under 250 W including V_{out}, V_{c3}, and V_{ab} ($D_2 = 0.35$). (a) Without S_9. (b) With S_9.

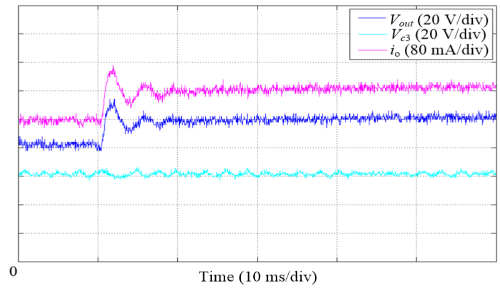
Fig. 19 and Fig. 20 show the dynamic performances of the proposed converter. In Fig. 19(a), the output voltage reference V_{ref_Vo} changes from 100 V to 80 V and finally gets back to 100 V. The details about zone 1 and zone 2 in Fig. 19(a) are shown in Fig. 19(b) and Fig. 19(c) respectively. Fig. 20 exhibits the performance under the load changes, in which the load changs from 40 Ω to 20 Ω and finally sets back to 40 Ω. In summary, the voltage of the flying capacitor V_{c3} is controlled constantly without significant changes under the dynamic tests.



(a)



(b)



(c)

Fig. 19. Dynamic performance (D_2 = 0.35). (a) Output voltage reference changes. (b) Zone 1. (c) Zone 2.

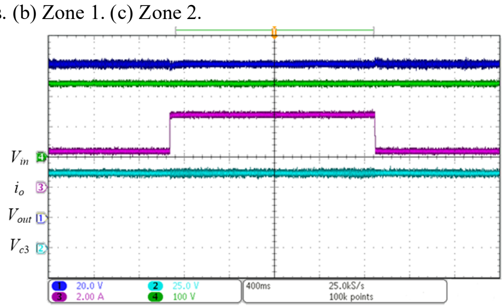


Fig. 20. Dynamic performance under load changes (D_2 = 0.35).

Fig. 21 shows the efficiency curves of the proposed converter under the power variations, in which one is with D_2 = 0.35, and the other one is with D_2 = 0.3. The average deviation between the two efficiency curves is about 0.2%.

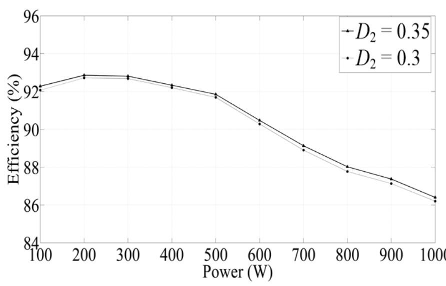


Fig. 21. Efficiency results with D_2 = 0.35 and D_2 = 0.3 under the power variations.

Fig. 22 illustrates the distribution of the power losses in the experimental prototype when D_2 is 0.35 and the output power is 1-kW. It can be obersved that: 1) the switching loss of the power swithes is small because the switching frequency is low (5 kHz) and the power switches can achieve zero-voltage switching or zero-current switching in the most operations; 2) the dominant part of the power losses is the conduction loss of the power switches since the voltage conversion ratio between the input voltage and output voltage in the prototype is small, which means that the primary current is higher. In the full-scale converter like the simulation model, the voltage conversion ratio is high, so the efficiency will increase significantly arising from the decreasing conduction loss of the power switches.

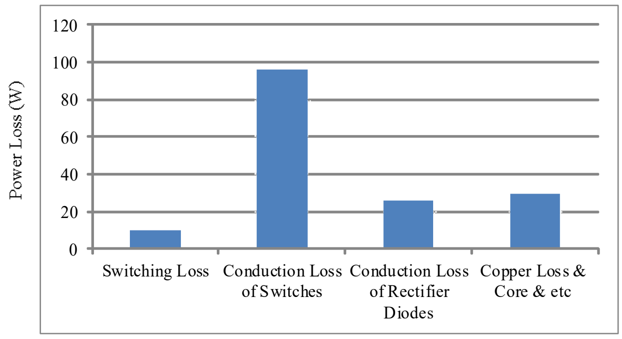


Fig. 22. Power loss distribution under 1-kW (D_2 = 0.35).

VI. Conclusion

This paper has proposed a 5L-ANPC dc/dc converter with a corresponding modulation strategy for the applications in MVDC grids. Due to multi-level voltages generating, the proposed converter can effectively reduce the voltage change rate *dv/dt* and the voltage stress on the transformer, thus reduce EMI and increase system reliability. An elimination method for the dead time effect is proposed by employing a switch in series with the flying capacitor, which can eliminate high voltage leaps caused by the dead time effect. In addition, a capacitor voltage control strategy by alternatively utilizing the two operation modes of the proposed modulation strategy is proposed for balancing the voltage of the flying capacitor, which can ensure the generation of the desired multi-level voltage waveforms. Finally, a simulation model and a down-scale laboratory prototype of the proposed converter have been built. The simulation and experimental results are in line with the theoretical analysis, which validates the feasibility of the proposed converter and voltage control strategy. It is highly recommended that the bidirectional dc/dc converter will be taken into consideration in the future studies, considering that more bidirectional power flows from new smart grid elements (e.g. energy storage system and electric vehicles) emerge in DC grids.

Appendix

See Table II and III.

TABLE II
PARAMETERS OF THE SIMULATION MODEL

Components	Description

Turns Ratio of Transformer	2:1
Output Filter Capacitor C_o (uF)	1500
Output Filter Inductor L_o (mH)	1
Input Capacitors C_1 and C_2 (uF)	6800
Flying Capacitor C_3 (uF)	3500
Input Voltage V_{in} (kV)	4
Output Voltage Reference V_{ref_Vo} (V)	800
Voltage Reference of Flying Capacitor V_{ref_c3} (kV)	1
Switching Frequency (kHz)	5
Load R_o (Ω)	10
Dead Time (us)	1

TABLE III
PARAMETERS OF THE EXPERIMENTAL SETUP

Components	Description
Mosfets S_1/D_1-S_4/D_4, S_9/D_9	IRFP4137PBF
Mosfets S_5/D_5-S_8/D_8	SPW47N60C3
Rectifier Diodes D_{r1}-D_{r4}	FFA60UP30DNTU
Turns Ratio of Transformer	1:2
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (mH)	1
Input Capacitors C_1 and C_2 (uF)	1500
Flying Capacitor C_3 (uF)	1500
Input Voltage V_{in} (V)	240
Output Reference Voltage V_{ref_Vo} (V)	100
Voltage Reference of Flying Capacitor V_{ref_c3} (V)	60
Switching Frequency (kHz)	5
Dead Time (us)	1.5

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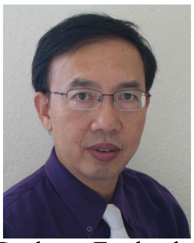

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