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Comparison of a Synchronous Reference Frame Virtual Impedance-Based Autonomous Current Sharing Control with Conventional Droop Control for Parallel-Connected Inverters

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Abstract— In order to provide faster response and better accuracy in contrast to the conventional droop control which has been widely used in the last decade as the decentralized control of parallel converters, a simple and effective autonomous current-sharing controller for parallel three-phase inverters is used. Active or reactive power calculations are unnecessary for this approach. Instead, a synchronous-reference-frame (SRF) virtual impedance loop and an SRF-based phase-locked loop are used. By means of the system transfer functions, stationary analysis is provided in order to identify the inherent mechanism of the direct and quadrature output currents in relation to the voltage amplitude and frequency. Comparison experiments from two parallel inverters are presented to compare the control performance of the conventional droop control to the proposed control, meanwhile to verify the effectiveness of the proposed control strategy in different scenarios.

Keywords— *Parallel inverters, autonomous current sharing, phase-locked loop, virtual impedance, droop control.*

I. INTRODUCTION

Recently, considering the environmental risks and energy access challenge, distributed generation (DG) system as an alternative to traditional central power plant updates grid structures and improves power supply reliability. Microgrid (MG) is a promising decentralized power architecture, which support a flexible and efficient electric grid, by enabling the integration of renewable energy sources (RESs), energy storage systems (ESSs), and demand response [1]-[4]. In order to avoid circulating currents among the parallel DGs in a MG without communication, droop control method is often applied [5]-[7]. Although it only requires local information, it presents a number of stability issues that have been solved.

The first one is that the droop coefficients which regulate frequency and amplitudes are basically proportional terms, so that in order to increase their range of values for improving system dynamics, derivative terms were added [8]-[10]. The second one is that the frequency and voltage are respectively related to active and reactive power when the output impedance of the generator is mainly inductive, e.g. induction generators, however, in an inverter the output impedance can be fixed by means of a fast control loop named virtual impedance. This control loop enforces the inverter to behave in accordance to the inductance-to-resistance ratio (X/R) line

impedance, e.g. mainly resistive in case of low voltage networks [11]-[13]. The third one is that in case of resistive lines and/or virtual impedances, the active power is controlled by the inverter voltage amplitude, while the reactive power flow is dominated by the angle, so that it can be controlled by the frequency of the system [14], [15]. In this sense, the active power-voltage ($P-V$) droop control needs to be used instead of the conventional active power-frequency ($P-f$) droop control, which is contrary to the conventional electrical transmission systems or induction generation dominated systems.

A control architecture based on a virtual resistance (VR), $P-V$ and $Q-f$ droops is used for dealing with the autonomous operation of parallel connected inverters. However, this approach has the inherent drawback that it needs to calculate instantaneous active and reactive powers and then average them through low-pass filters (LPF) whose bandwidth deteriorate the system transient response [9]. Even in three-phase systems, the active and reactive power can be calculated by using the instantaneous power theory, a post-filter processing is necessary in order to completely remove the distorted power components. Furthermore, in a practical situation, the load sharing performance of the conventional droop control is degraded when short lines with small impedance are used, especially in low voltage networks. In this case, a small deviation in voltage frequency and amplitude will result in large power oscillation and even instabilities.

In order to solve these issues, a simpler and faster controller is used in this paper, which consists of a synchronous-reference-frame (SRF) virtual impedance loop, an SRF phase-locked loop (PLL) and a proportional-resonant (PR) controller in voltage control loop. The proposed control strategy provides both instantaneous current sharing and fast dynamic response for paralleled voltage controlled inverters (VCIs). The virtual resistance loop which contains a d -axis virtual resistance loop and a q -axis virtual resistance loop is used to achieve direct and quadrature load currents sharing separately among three-phase inverters. In contrast with the conventional droop control, there is no need to calculate active/reactive powers.

II. CURRENT FLOW ANALYSIS

Each VCI can be modeled by a two-terminal Thévenin equivalent circuit in Laplace based on the equivalent circuit as

shown in Fig. 1:

$$V_{bus}(s) = G_n(s)V_{refn}(s) - [Z_{on}(s) + Z_{line}(s) + Z_{virn}(s)]I_{on}(s) \quad (1)$$

where $V_{refn}(s)$ is the output voltage reference; $G_n(s)$ is the voltage gain. The inner current and voltage loops are responsible for minimizing $Z_{on}(s)$, i. e. by using a proportional + resonant (PR) controller tuned at the line frequency. In this sense, $Z_{on}(s)$ is approximately equal to zero, whereas $G_n(s)$ is equal to 1 at the resonant frequency of PR controller.

Considering that $Z_{line}(s)$ is practically very small in low voltage MGs, $Z_{virn}(s)$ becomes the predominant component. When only virtual resistance is adopted, an equivalent Thévenin circuit can present the closed loop inverter, as illustrated in Fig. 2. The voltage difference between the generated voltage and common bus voltage at the line frequency can be expressed as follows:

$$V_{refn} - V_{bus} = I_{odn}R_{virdn} + jI_{oqn}R_{virqn} \quad (2)$$

where I_{odn} and I_{oqn} are the d and q -axis components of output current, respectively.

In this case, because the voltage reference phasor (V_{ref}) and common bus voltage phasor (V_{bus}) are identical for each DG unit, the different values of $R_{vir d}$ and $R_{vir q}$ will result in different voltage drop that will cause different current output vectors (I_o). The relationship of I_{od} , I_{oq} , $R_{vir d}$ and $R_{vir q}$ can be generalized and expressed for number N of converters as follows:

$$I_{od1}R_{vir d1} = I_{od2}R_{vir d2} = \dots = I_{odN}R_{vir dN} \quad (3a)$$

$$I_{oq1}R_{vir q1} = I_{oq2}R_{vir q2} = \dots = I_{oqN}R_{vir qN} \quad (3b)$$

The d - and q -axis output currents I_{od} and I_{oq} of the paralleled inverters are inversely proportional to the corresponding virtual resistances. Therefore, the direct and quadrature current outputs of each inverter can be regulated independently by adjusting the virtual impedances based on different power rates, commands from energy management system (EMS) or other superior control loops.

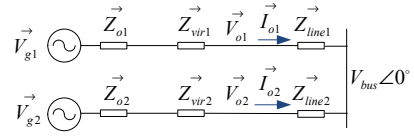


Fig. 1. Equivalent circuit of a parallel inverter system.

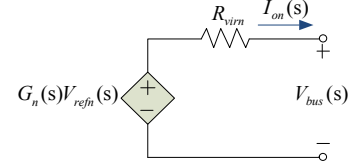


Fig. 2. Equivalent Thévenin circuit of closed-loop inverter.

III. PROPOSED AUTONOMOUS CURRENT-SHARING CONTROLLER

According to the analysis above, a simpler and faster controller is proposed in this paper [16]. The novel control strategy is shown in Fig. 3(b), compared with the improved droop controller in Fig. 3(a).

A. Configuration of the proposed controller

The power stage consist of a three-leg three-phase inverter connected to a DC link, loaded by an L_r - C_f filter, and connected to the AC bus by means of a power line (Z_{line}).

The controller includes a SRF-PLL, a virtual resistance loop ($R_{vir d}$ and $R_{vir q}$), a DC link voltage feed-forward loop, and the conventional PR inner voltage and current controllers (G_v and G_i). Inductive currents and capacitor voltages are transformed to the stationary reference frame ($i_{L\alpha\beta}$ and $v_{c\alpha\beta}$). Output currents are transformed to the SRF (i_{odq}).

A. Control Principle

The proposed controller supplies a reference voltage to the inner loop. The voltage reference is generated by combining the amplitude reference ($|V_{ref}|$) and the phase generated (θ) by the PLL.

Even though the PLL is trying to synchronize the inverter with common AC bus, in case of supplying reactive loads, the

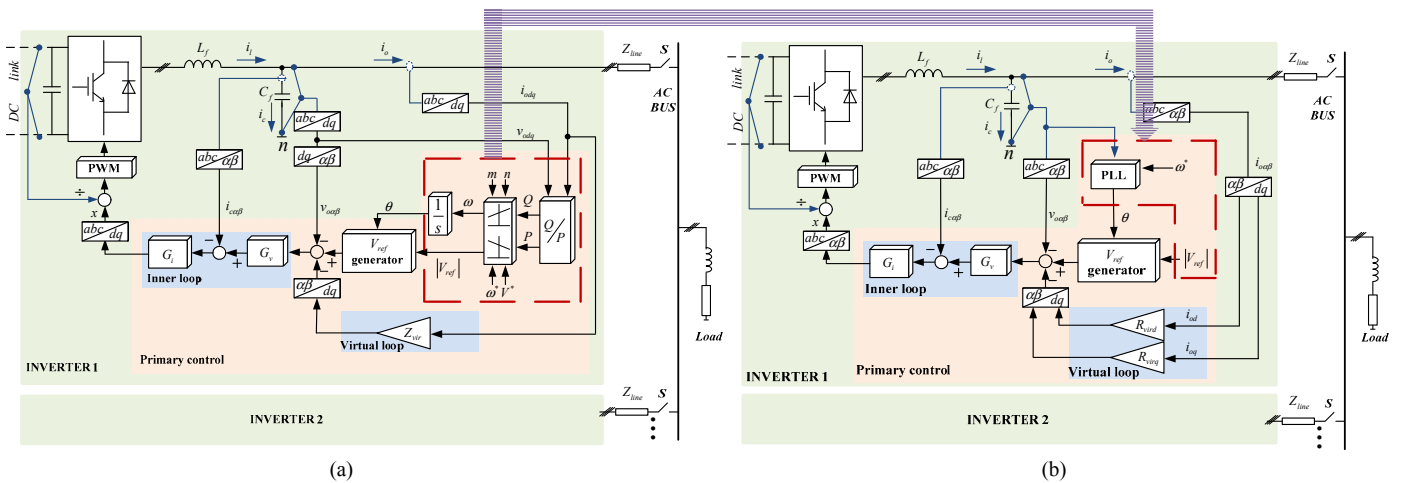


Fig. 3. Control structure comparison between (a) the conventional droop control and (b) the proposed control method

quadrature current flowing through the virtual resistance will produce an unavoidable quadrature voltage drop, which will cause an increase of frequency in PLL. This way, the mechanism inherently endows an I_{oq} - ω droop characteristic to each inverter.

Similarly, in case of supplying active loads, the direct current flowing through the virtual resistance will drop the direct voltage, resulting in a decrease of the output voltage amplitude. Hence, a droop characteristic is also imposed by the virtual resistance adapting the amplitude of output voltage.

The closed loop transfer function $T_{plant}(s)$ can be described as follows:

$$T_{plant}(s) = \frac{V_o(s)}{V_{ref}(s)} = \frac{G(s)[1 + G_{Lequ}(s)Z_{line}(s)]}{1 + G_{Lequ}(s)Z_{line}(s) + G_{vir}(s)G(s) + G_{Lequ}(s)Z_o(s)} \quad (4)$$

Being

$$G(s) = \frac{G_v(s)G_i(s)K_{PWM}}{L_f C_f s^2 + (rC_f + G_i(s)K_{PWM}C_f)s + 1 + G_v(s)G_i(s)K_{PWM}},$$

$$G_v(s) = K_{pv} + \frac{K_{iv}s}{s^2 + \omega_c^2}, \quad G_i(s) = K_{pi}, \quad G_{Lequ}(s) = \frac{1}{R_{Lequ}} + \frac{1}{sL_{Lequ}},$$

$$Z_o(s) = \frac{sL_f + r}{L_f C_f s^2 + (rC_f + G_i(s)K_{PWM}C_f)s + 1 + G_v(s)G_i(s)K_{PWM}},$$

$$Z_{line}(s) = R_{line} + sL_{line}, \quad G_{vir}(s) = \frac{R_{vird}}{R_{Lequ}} + \frac{R_{virq}}{sL_{Lequ}}$$

where $G(s)$ presents the tracking performance of the output voltage following the voltage reference; $Z_o(s)$ is the equivalent output impedance of the inverter; $Z_{line}(s)$ is the line impedance, R_{line} is the line resistor, L_{line} is the line inductance; $G_{Lequ}(s)$ is the equivalent load admittance, R_{Lequ} is the equivalent resistor, L_{Lequ} is the equivalent inductance; $V_o(s)$ is the output voltage; $V_{ref}(s)$ is the reference voltage; $i_o(s)$ is the output current; $G_v(s)$ is the PR voltage control loop; $G_i(s)$ is the proportional current control loop; K_{PWM} is the gain of three phase inverter; L_f , C_f and r are the inductor, capacitor, and inductor ESR of LC filter respectively; K_{pv} and K_{iv} are the proportional and integral coefficients of voltage control loop; ω_c is the resonant frequency of the PR voltage control loop; K_{pi} is the proportional coefficients of current control loop; R_{vird} and R_{virq} are the d -axis and q -axis virtual resistors.

IV. INHERENT DROOP CHARACTERISTIC AND COUPLING ANALYSIS

Considering the mechanism of I_{od} with voltage amplitude and I_{oq} with frequency, two virtual resistances R_{vird} and R_{virq} are employed to share the d - and q - axis load currents among the inverters.

A. I_{oq} sharing

When the inverters and loads all connect to the common AC bus, the proposed controller will make the system stable at

a frequency-stable operation point which may has a small deviation from 50 Hz. The small deviation is determined by the function of PLL, R_{virq} and I_{oq} . Therefore, the parallel inverters will operate at the same system frequency, but with different phase angles that depend on the output quadrature current and q -axis virtual resistance value. Based on (4), as $s=j\omega$, the relationship of R_{vird} , R_{virq} , I_{od} , I_{oq} and angular frequency (ω) can be calculated based on

$$\arctan[T_{plant}(j\omega)] = 0^\circ \quad (5)$$

In order to analyze the relationship of R_{virq} , I_{oq} and ω , R_{vird} and I_{od} are preset to fixed values. The relationship of R_{virq} , I_{oq} and ω without line impedance is shown in Fig. 4 (a). The inherent mechanism of the proposed I_{oq} - ω droop controller is depicted in Fig. 4 (b). As observed in Fig. 4 (b), the quadrature current sharing among the parallel inverters can be adjusted by regulating the q -axis virtual resistance ratio.

By contrast, the relationship of variables R_{vird} , I_{od} and ω without line impedance are derived by assigning R_{virq} and I_{oq} to certain values. The relationship of R_{vird} , I_{od} and ω without line impedance are shown in Fig. 5 (a). Additionally, Fig. 5 (b) is obtained by assuming R_{vird} to different values based on the relationship of R_{vird} , I_{od} and ω under zero line impedance condition. As observed, the influence of I_{od} on ω changes by an exponential dependence when it getting closer to the resonance frequency of PR controller, which means the impact of R_{vird} and I_{od} on ω can be neglected.

B. I_{od} sharing

In order to share active loads, the parallel inverters will have different output voltage amplitude deviations from the voltage amplitude reference $|V_{ref}|$, which depend on the output direct current and d -axis virtual resistance value of each inverter. The voltage drop (ΔV) can be divided into two parts as follows:

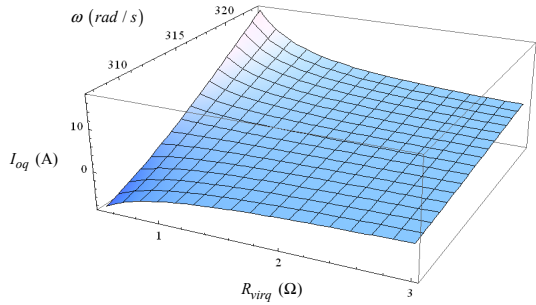
$$\Delta V = I_{od} R_{vird} + |V_{ref}| [1 - |T_{plant}(j\omega_0')|] \quad (6)$$

where the ω_0' is the angular frequency of frequency-stable operation point.

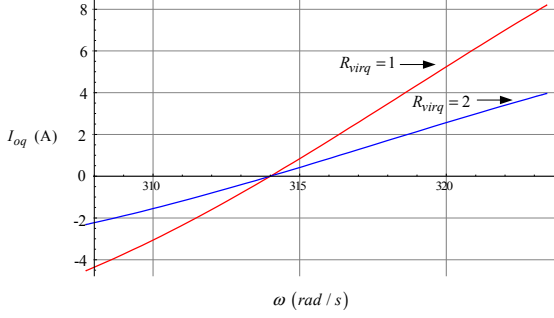
The first part of (6) is the product of d -axis virtual resistance R_{vird} and direct current output I_{od} , which dominantly affects the output voltage amplitude drop. The second part of (6) is caused by the magnitude attenuation of closed-loop transfer function which results from the small but nonlinear frequency deviation due to the characteristic of PR controller. However, as discussed above, the system frequency will be stable and the deviations among the parallel inverters will be equal to each other, that is, the voltage deviations resulting from the second part of (6) are also the same among inverters. Therefore, the influence on the deviations can be neglected. Thus, the per-unit value of output voltage amplitude can be derived as follows:

$$\frac{|V_o|}{|V_{ref}|} = |T_{plant}(s)| = f(I_{od}, I_{oq}, R_{vird}, R_{virq}, \omega) \quad (7)$$

The parameters of R_{virq} and I_{oq} are fixed to analyze the relationship of R_{vird} , I_{od} and V_o . The relationship of R_{vird} , I_{od}

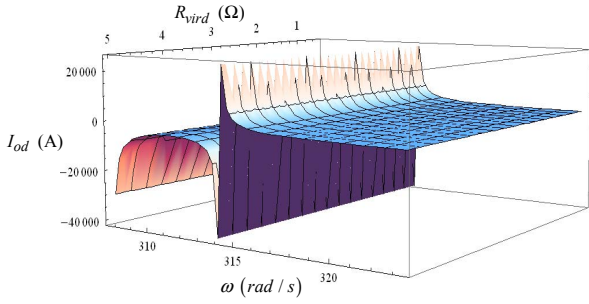


(a)

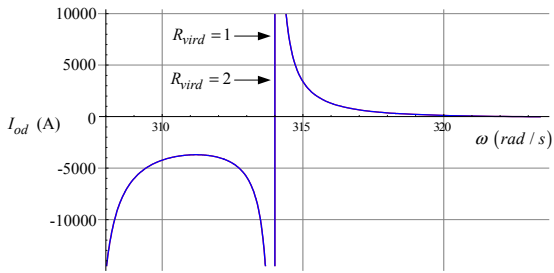


(b)

Fig. 4. The relationship of R_{virq} , I_{oq} and ω without line impedance. (a) The relationship of R_{virq} , I_{oq} and ω , (b) The relationship of I_{oq} and ω when $R_{virq}=1 \Omega/2 \Omega$.



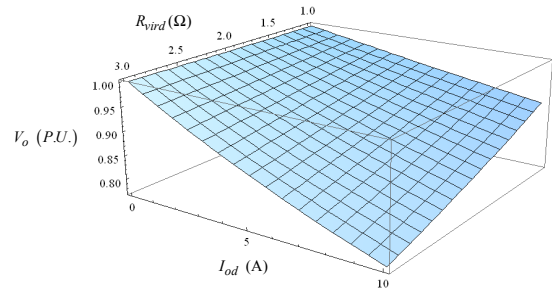
(a)



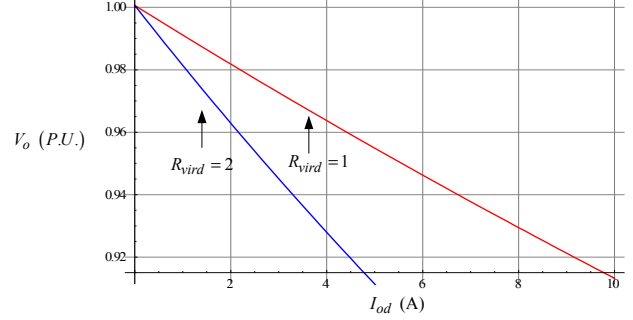
(b)

Fig. 5. The relationship of R_{vird} , I_{od} , and ω without line impedance. (a) The relationship of R_{vird} , I_{od} , and ω , (b) The relationship of I_{od} , and ω when $R_{vird}=1 \Omega/2 \Omega$.

and V_o without line impedance are shown in Fig. 6. Fig. 6 (b) shows the inherent I_{od} - V_o droop mechanism of the proposed controller under zero line impedance condition. As observed, as the output direct current I_{od} increases, the voltage amplitude V_o decreases with different ratio corresponding to different R_{vird} values. Thus, the direct current sharing among the parallel inverters can be adjusted by regulating the d -axis virtual

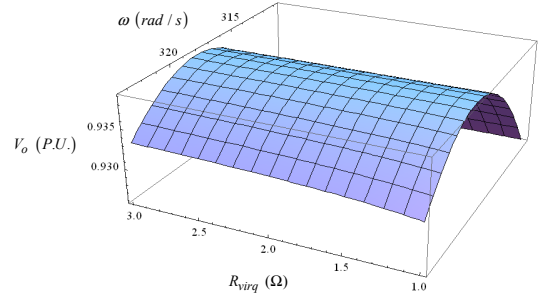


(a)

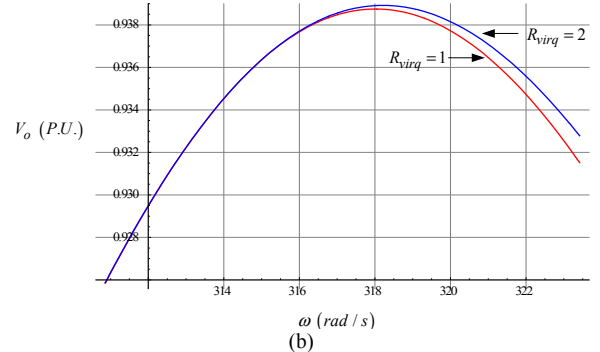


(b)

Fig. 6. The relationship of R_{vird} , I_{od} and V_o without line impedance. (a) The relationship of R_{vird} , I_{od} and V_o , (b) The relationship of I_{od} and V_o when $R_{vird}=1 \Omega/2 \Omega$.



(a)



(b)

Fig. 7. The relationship of R_{virq} , ω and V_o without line impedance. (a) The relationship of R_{virq} , ω and V_o , (b) The relationship of ω and V_o when $R_{virq}=1 \Omega/2 \Omega$.

resistance ratio.

Similarly, R_{vird} , I_{od} are fixed to analyze the effect of frequency deviation on the voltage amplitude V_o without line impedance. The relationships of R_{virq} , ω and V_o without line impedance are shown in Fig. 7 (a). Fig. 7 (b) indicate that the relationship V_o - ω almost immune to R_{virq} . The effects of R_{virq} and ω on V_o are nonlinear but quite small in comparison with

the voltage drop caused by adjusting R_{virid} and I_{od} . Considering that the voltage drop caused by $\Delta\omega$, is approximately the same in each inverter, it can be neglected.

V. EXPERIMENTAL RESULTS

An islanded experimental MG setup, which consists of three Danfoss 2.2 kW inverters, a real-time dSPACE1006 platform, LC filters, line impedances, a resistive load and a resistance – inductance load has been built, as shown in Fig. 8. The switching frequency is set to 10 kHz. The electrical setup and control system parameters are listed in Table I. Load variation scenarios have been considered to test the performances of the proposed controller. In addition, a two parallel-inverters system has been used to compare and evaluate the performance of the proposed control approach with the conventional droop control in different scenarios. In this comparison, the parameters of electrical and inner voltage and current loops are all the same for both control methods.

A. Load step up and step down test

In this test, three parallel inverters have been considered to test the performances of the proposed controller with zero line impedance and two common loads ($Z_{load1}=57+j2.83\Omega$, $Z_{load2}=57\Omega$). Experiments during severe load step up and step down disturbances have been done in RL load and R load. Fig. 9 shows the transient responses of VCIs during load changes. At first, VCI #1, VCI #2 and VCI #3 operate paralleled with Z_{load1} and Z_{load2} from t_1 to t_2 . Then, Z_{load1} is disconnected from MG, which means a nearly 50% step load decrease is applied to the MG output terminal at t_2 . After about 0.1s, the output quadrature current of MG descends to zero, while the output direct current of MG is decreased from 3.4A to 1.7A. At t_3 , Z_{load1} is reconnected to the MG. Thus, the output direct and quadrature currents of MG restore to the initial values. Then, at t_4 , Z_{load2} is disconnected from the MG. As observed in Fig. 9 (b), this action only affect the d -axis current without influencing on q -axis output current. The same performance can be obtained when Z_{load2} is reconnected to MG at t_5 . The load disturbance has little impact on system frequency as the inductive load is small in this test. Note the fast and smooth transient response.

B. Comparison experiments with inductive line impedance

Figs. 10 to 12 shows the experimental results to compare the control performance of the conventional droop control and the proposed control with purely inductive line impedance $L_{line,2}$ which is equal to 1.8 mH.

Fig. 10 shows the transient response when VCI #2 is connected to VCI #1 with the conventional droop controller and the proposed controller separately. As seen in Figs. 10 (a) to 10 (d), VCI #1 is connected to a resistive-inductive load feeding around $(1.16+j 0.4)$ A, while VCI #2 is disconnected. At 2.3 s, VCI #2 is connected to VCI #1, operating in parallel supplying a common load. The direct and quadrature current outputs of VCI #2 are increased by 0.58 A and 0.2 A respectively, whereas the output direct and quadrature currents of the VCI #1 are decreased also by 0.58 A and 0.2 A respectively. The settling time is approximately 5.2 s with the

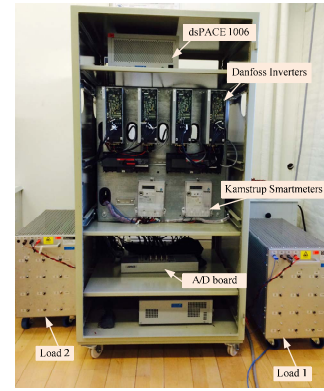


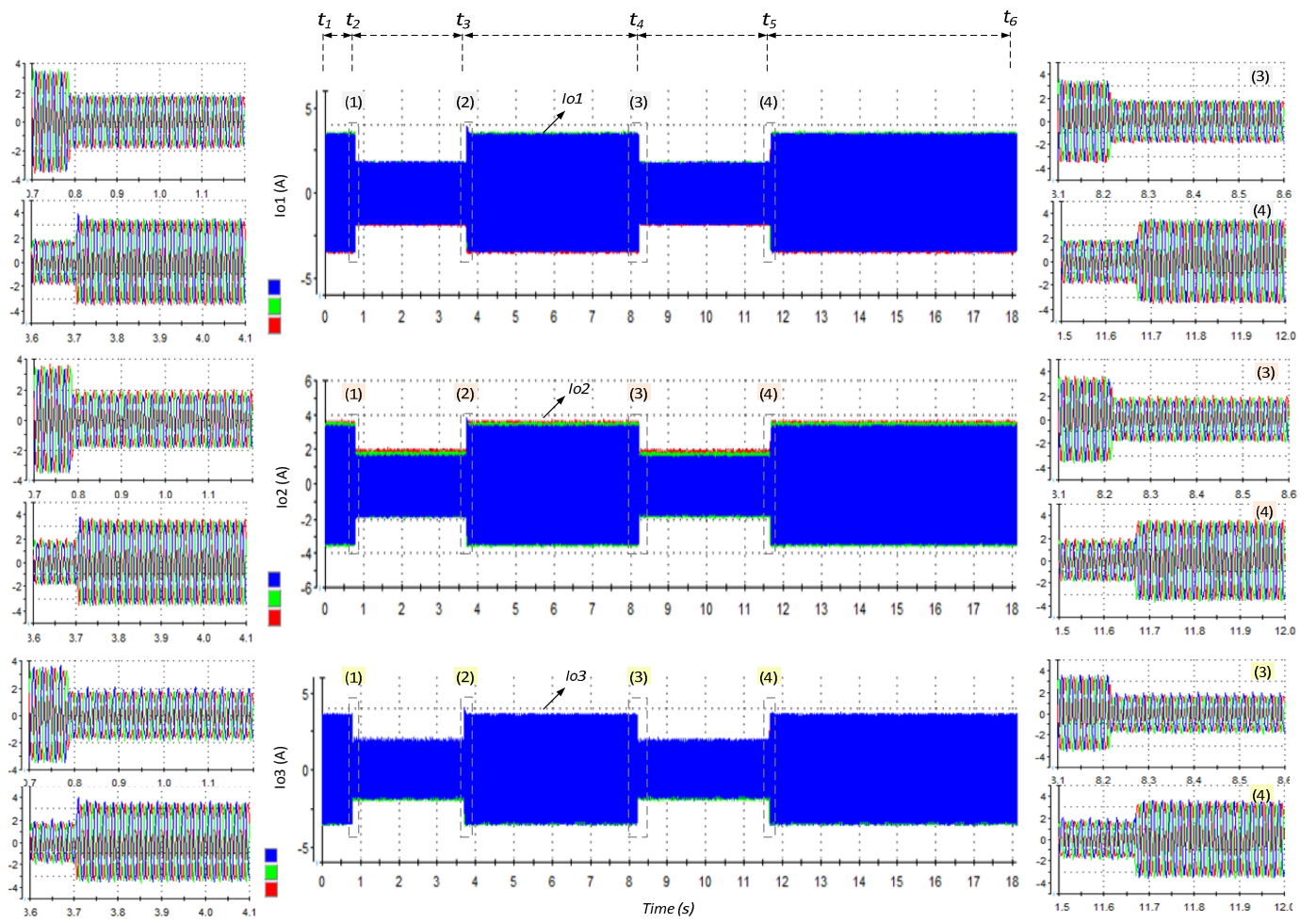
Fig. 8. Experimental setup.

TABLE I
POWER STAGE AND CONTROL SYSTEM PARAMETERS

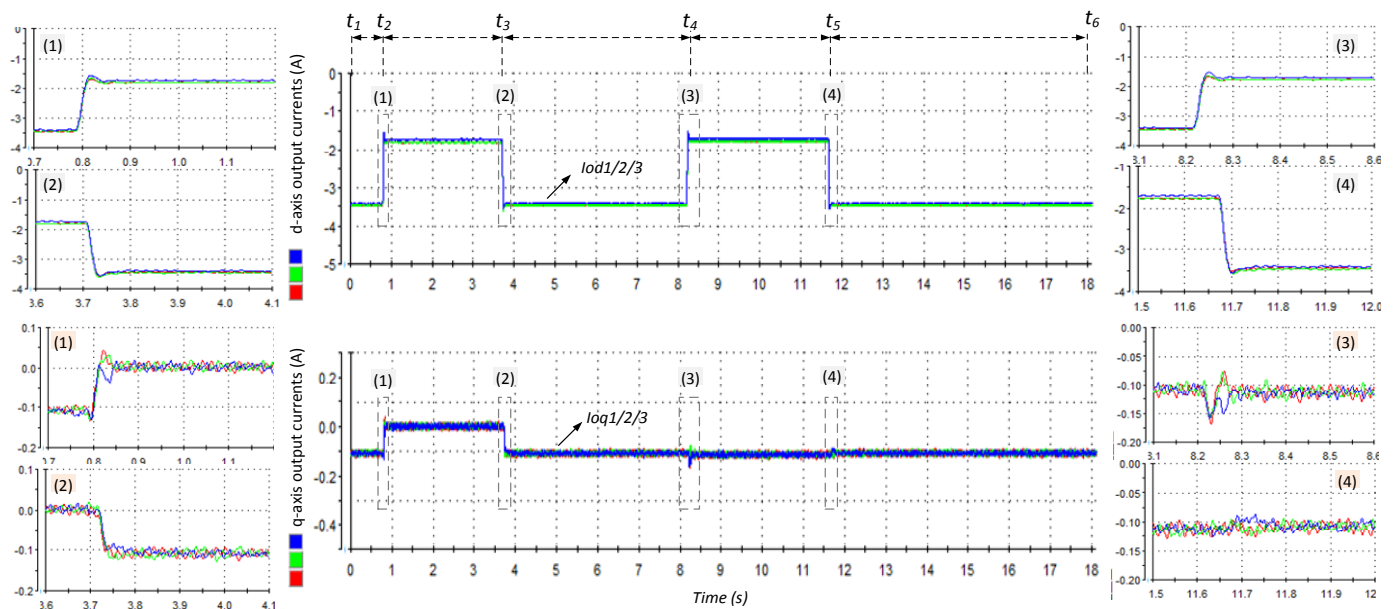
Parameters	Description	Value
Inverter and filter		
V_{dc}/V_{MG}	DC voltage/ MG voltage	650 V/ 311 V
f/f_s	MG / Switching frequency	50 Hz/ 10 kHz
L_f/C_f	Filter inductance/ Filter capacitance	1.8 mH/ 25 μ F
$L_{line,1}$	Resistive – inductive line	1 Ω + 1.7 mH/
$L_{line,2}$	Inductive line	1.8 mH
Z_{load1}/Z_{load2} (A)	Local load #1/ Local load #2	57+j2.83 Ω / 57 Ω
Z_{load}/Z_{test} (B/C)	Local load 1/ Step up load	230+j2.83/ 460 Ω
Inner Loop		
k_{pi}/k_{ii}	Current proportional/ integral term	0.07/ 0
K_{pv}/K_{iv}	Voltage proportional/ integral term	0.04/ 94
Droop Control		
k_{pP}/k_{iP}	P droop proportional/ integral term	5e-7/ 6e-6
k_{pQ}/k_{iQ}	Q droop proportional/ integral term	1e-5/ 0
R_v/L_v	Virtual resistance/ Virtual inductance	2 Ω / 8 mH
Proposed Control		
$K_{p,PLL}/K_{i,PLL}$	PLL proportional/ integral term	1.4/ 1000
R_{virid1}/R_{virq1}	d/q-axis virtual resistance (inverter 1)	2 Ω / 2 Ω
R_{virid2}/R_{virq2}	d/q-axis virtual resistance (inverter 2)	2 Ω / 2 Ω

conventional droop control, whereas the settling time is approximately 1s with the proposed control strategy. Notice that a small overshoot occurs due to small voltage error between inverters at the moment of connection, as shown in Fig. 10 (c). An offset approximately 0.03 A of reactive current when using the droop control can be found in Fig. 10 (c) due to the unbalance between line impedances, which is well suppressed when using the proposed controller as shown in Fig. 10 (d).

Fig. 11 shows the transient response during load step changes in the AC common bus with purely inductive line impedance. In the beginning, the parallel VCIs operate feeding power to the common load Z_{load} . At 1.3 s, an extra 460 Ω resistive load Z_{test} is connected to the common bus. The direct current outputs of VCI #1 and VCI #2 both increase by 0.31 A immediately to supply the needed current with conventional droop control and the proposed controller as shown in Figs. 11 (a) and 11 (b). The quadrature currents output of VCI #1 and VCI #2 with the conventional droop control deviate by approximately 0.03 A because of the coupling between direct and quadrature currents as shown in Fig. 11 (c). However, by using the proposed method the quadrature current outputs of VCI #1 and VCI #2 can maintain their original values, being



(a)



(b)

Fig. 9. Direct and quadrature output currents of DG #1-#3 during load step up and step down.

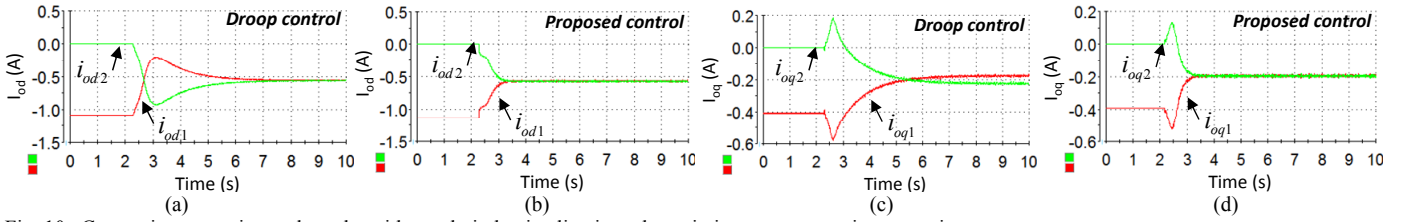


Fig. 10. Comparison experimental results with purely inductive line impedance in inverter connection scenario.

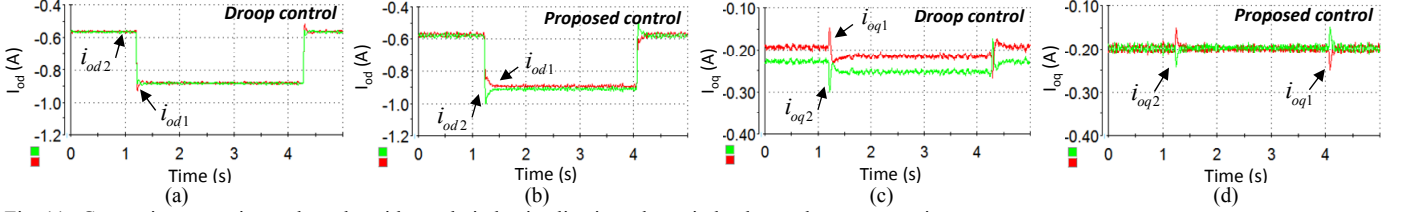


Fig. 11. Comparison experimental results with purely inductive line impedance in load step changes scenario.

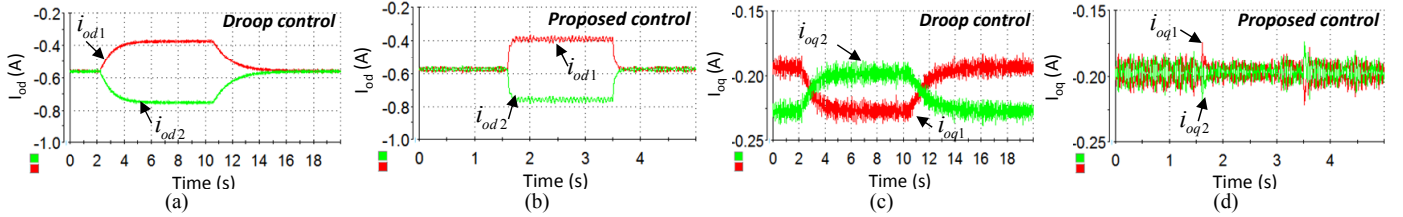


Fig. 12. Comparison experimental results with purely inductive line impedance in ratio changes scenario.

barely affected by the direct output current disturbances as shown in Fig. 11 (d).

The transient response for sudden direct currents sharing ratio changes between the parallel VCIs is illustrated in Fig. 12. In the beginning, the VCI units parallel operate with a common RL load Z_{load} . Both the VCI #1 and VCI #2 feeds are approximately 0.58 A of direct current and 0.2 A of quadrature current. At 2.3 s, the direct current sharing ratio between the parallel VCIs with the conventional droop control has been suddenly changed from 1:1 to 1:2 and then changed back to 1:1 at 10.6 s. As it can be seen in Fig. 12 (a), after about maximum 6 s, the output currents of the parallel VCIs are changed according to the new sharing ratio. Meanwhile, the quadrature current sharing has been affected by the changes on direct current sharing ratio as shown in Fig. 12 (c). By contrast, the direct current sharing ratio between the parallel VCIs with the proposed control approach has also been suddenly changed from 1:1 to 1:2 at 1.6 s and then changed back to 1:1 at 3.5 s. Fig. 12 (b) shows that the direct current outputs of VCIs increase immediately according to the sharing ratio changes and the transient response only lasts 0.2 s. Meanwhile, the quadrature current sharing ratio is kept constant via the decoupling control of the proposed controller.

C. Comparison experiment with resistive-inductive impedance

Figs. 13 to 15 show the experimental results in order to compare the conventional droop control and the proposed control, with resistive-inductive line impedance $L_{line,1}$ which is equal to 1 Ω plus 1.7 mH in three different scenarios. Fig. 13 shows the transient response of direct currents and quadrature currents when the VCI #2 is connected to VCI #1 with the conventional droop controller and the proposed controller

separately. Fig. 14 illustrates the transient response for load step-up changes on AC common bus. Fig. 15 presents the transient response during sudden direct currents sharing ratio changes between the parallel VCIs. Both the conventional droop control and the proposed controller can achieve stable operation. By contrast, the proposed approach can endow the system with faster response speed, smaller overshoot and decoupling control. Oscillation appears in the output current with the conventional droop control due to the resistive-inductive line impedance and the coupling between I_{od} and I_{oq} .

When without line impedance, or highly resistive, the parallel VCIs cannot operate by using the conventional droop control. In contrast, excellent performance can be obtained by using the proposed control as shown in scenario A and Fig. 9.

Based on the above analysis and experimental results, the prominent features of the proposed strategy compared with the conventional power sharing controls are summarized as follows: 1) Fast and robust transient response; 2) Enhanced active/reactive power decoupling; 3) Fast active/reactive power rating step changes; 4) Low impact of the line impedance. 5) Plug'n'play capability when connecting the inverter to the MG or disconnecting a unit (hot-swap); 6) Effective interaction with an energy management system that may change suddenly the active/reactive power ratio. 6) Flexible controllability and higher bandwidth.

VI. CONCLUSION

A simpler and faster controller that comprises a PLL, a virtual resistance loop and a PR controller in inner voltage loop for controlling direct and quadrature load currents separately among parallel three-phase inverters is developed.

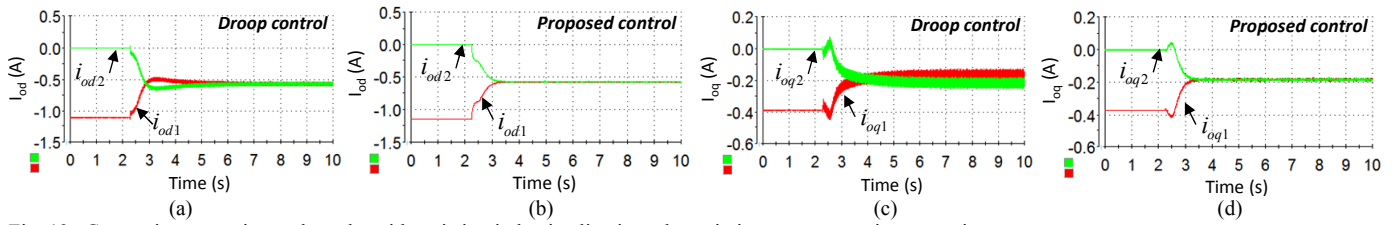


Fig. 13. Comparison experimental results with resistive-inductive line impedance in inverter connection scenario.

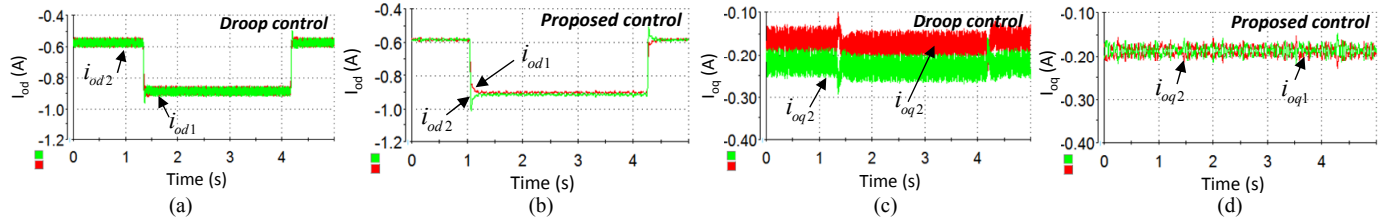


Fig. 14. Comparison experimental results with resistive-inductive line impedance in load step changes scenario.

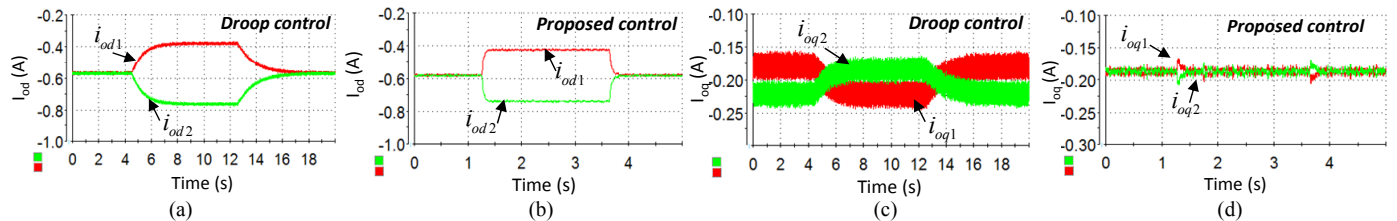


Fig. 15. Comparison experimental results with resistive-inductive line impedance in ratio changes scenario.

Based on the steady state characteristic analysis, by adjusting the d -axis virtual resistance ratio between the parallel inverters, the direct load current sharing can be achieved. Whereas by modifying the q -axis virtual resistance ratio between parallel inverters, the quadrature load current provided will be changed proportionally. The proposed control strategy does apply to low-voltage microgrids and islanded minigrids. In addition, it can also works well with inductive-resistive line impedance and even small purely inductive or resistive line impedance thanks to the use of virtual resistance. Compared with conventional droop control, the described method does not need to calculate active and reactive powers. Thus, the method exhibits faster transient response and better precision. Experimental results are included to show the excellent behavior of the proposed controller.

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