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A GPS-Based Control Method for Load Sharing and Power Quality Improvement in Microgrids

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***Abstract*— This paper proposes a novel control method for accurate sharing of load current among the Distributed Energy Resources (DER) and high power quality operating in islanded ac microgrids. This control scheme is based on hierarchical structure comprising of decentralized primary controllers and a centralized secondary controller. The controllers in the primary level use GPS timing technology to synchronize their local time with a common time reference. In this context, proportional current sharing is achieved by adjusting the reference voltage of each DER unit according to a voltage-current (V-I) droop characteristic. The droop coefficient, which acts as a virtual resistance, is adaptively changed as a function of peak current. This strategy not only simplifies the control design but also enables faster dynamics and higher accuracy of current sharing especially at high loading conditions. The secondary controller produces compensation signals at fundamental and dominant harmonics to improve the voltage quality at a sensitive load bus. Experimental results are presented to validate the efficacy of the proposed method.**

***Keywords*— droop control, disperced generation, power quality, microgrid, hierarchical control, harmonics.**

I. Introduction

Recently, the concept of Microgrid (MG) as a cluster of Distributed Generators, energy storage systems and loads has been gaining more interest in the energy research community especially after approval of the IEEE 1547.4 standard [1]. Distributed Energy Resources (DERs) are mostly integrated in MGs through a power-electronic interface converter which has an inverter as the output stage in the case of ac microgrids [2]. Controlling the DERs inverter as a power quality conditioning device has been studied in detail, in recent years [3-7]. In [3], each DG unit of microgrid is controlled as a negative sequence conductance with the aim of compensating voltage unbalance. This approach is improved in [4] by injecting a voltage reference to the inner control loops of the DG to compensate unbalance in islanded microgrids. In [5] and [6], the inverters emulate a resistance at harmonic frequencies to mitigate harmonic distortion of the voltage. However, the approaches of [3]-[6] are designed to compensate voltage unbalance or harmonics at each DG terminal which may not be desirable when the microgrid sensitive loads are located at other buses which can be electrically far from inverters terminals. To cope with this, the idea of harmonic mitigation based on a hierarchical structure has been introduced in [7]. This hierarchical control structure is made up of primary and secondary levels. The primary controller comprises local DER controllers, which use a combination of droop control method and selective virtual impedance scheme to coordinate the power generation of DERs and share the harmonic loads between them. The secondary controller, produces a compensating signal so as to improve the voltage quality in a so-called Sensitive Load Bus (SLB). The compensation signal is broadcasted to the local controllers to adjust the DER reference voltage accordingly. This idea has been further developed in [8] to improve the steady-state current sharing accuracy. However, the methods of [7] and [8] have some important limitations:

1) The selective virtual impedance scheme is not only complex to implement but also suffers from slow dynamic response.

2) The voltage drop across the lines degrades the performance of virtual impedance scheme in terms of current sharing accuracy. The effect of line impedances can be compensated by means of distributed control techniques as discussed in [9] and [10]. However, since the secondary controller is characterized by slow dynamic response, it does not prevent transient overcurrent stresses.

3) Those method are based on the assumption of and inductive network impedance. However, the low voltage MGs are mainly resistive in practice.

In this paper, a novel hierarchical control scheme is proposed to alleviate the aforementioned problems. The proposed method is comprised of decentralized primary and centralized secondary control level. The primary controller uses the concept of voltage-current droop [11] to enable current sharing with a fast dynamic response. With the intention of preventing overcurrent stresses, an adaptive droop function is adopted, the slope of which is adjusted based on peak output current. The secondary controller improves the quality of voltage by using a simple integral control scheme.

The rest of the paper is organized as follows. The problem of current sharing in presence of nonlinear and unbalanced loads and the existing solutions are addressed in Section II.

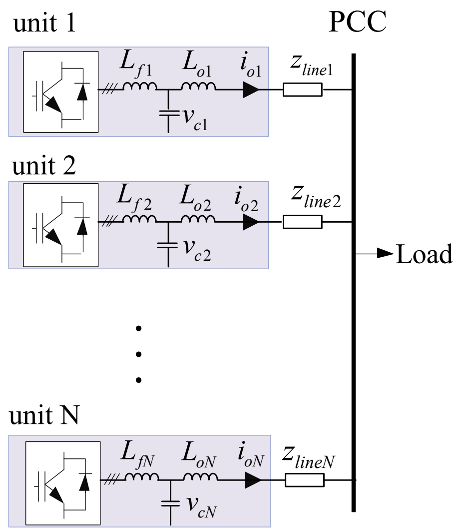


Fig. 1. Schematic diagram of an islanded ac MG

The proposed primary and secondary control schemes are introduced in Sections III and IV, respectively. Experimental results are presented in Section V to verify the efficacy of the proposed control scheme. Section VI concludes the paper.

II. Sharing of Nonlinear Loads in Islanded MGs

Consider the islanded MG of Fig. 1. The MG includes N DER units, which are connected to the point of common coupling (PCC) through low voltage lines. Each DER is comprised of a DC energy source, a power electronic converter and a passive LCL filter. The MG supplies a combination of linear/ nonlinear and balanced/unbalanced loads.

The sharing of load current between the DERs is dependent on the corresponding output voltages. Therefore, it is possible to achieve proper load sharing by coordinating the output voltages of the individual units. In general, such coordination can be achieved by means of a decentralized control structure, as depicted in Fig. 2. The reference voltage is calculated by means of a current sharing scheme based on the local feedback signals. The inner control loops (which are conventionally composed of proportional plus resonant voltage and current controllers [12]) track the reference voltage with a fast dynamic response.

A well-known current sharing approach is virtual impedance strategy. In this approach, the frequency and amplitude of the fundamental positive sequence voltage are calculated based on conventional droop characteristics. Furthermore, the reference voltage is calculated by subtracting a virtual impedance voltage drop from the fundamental positive sequence voltage. The existing virtual impedance methods can be categorized to virtual resistance and selective virtual impedance schemes. In this section, each of the schemes is discussed and its shortcomings are addressed.

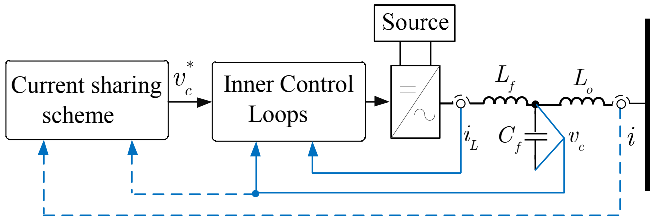


Fig. 2. Generic decentralized control structure for voltage-controlled DERs

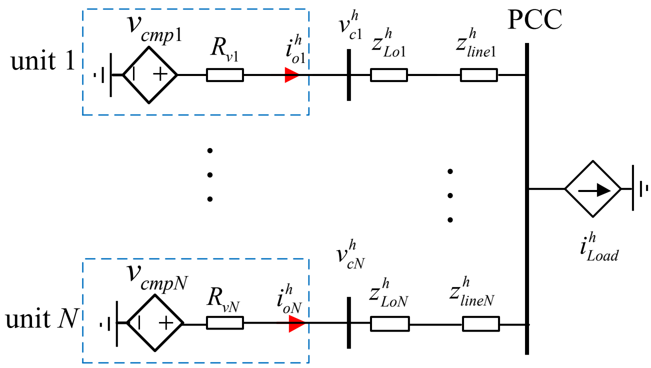


Fig. 3. Equivalent model of the MG for negative sequence and harmonics

A. Virtual resistance scheme

In this scheme, a virtual resistance is introduced in the DER output by adjusting the reference voltage according to [13]:

$$v_c^* = E^{1+} - R_v i_o \qquad (1)$$

where E^{1+} is the fundamental positive sequence voltage, which is obtained from P-V/Q-f droop control method, R_v is the virtual resistance and i_o is the output current. The virtual resistance not only improves the system damping but also enables proper sharing of harmonic and unbalanced currents among the DERs.

To perform proportional current sharing among the DERs, the virtual impedance of each unit is selected inversely proportional to its power rating:

$$R_{v1}.S_{rated1} = R_{v2}.S_{rated2} = \cdots = R_{vN}.S_{ratedN} \qquad (2)$$

in which S_{ratedk} is the rated apparent power of unit k.

The effect of virtual resistance on the sharing of harmonic currents is analyzed based on the equivalent model of Fig. 3. This model is based on the assumption of $v_c = v_c^*$, which is justified by the fact that the dynamics of the inner control loops are are much faster compared with the current sharing scheme. Using the current division rule, the output current of unit k is obtained, as follows:

$$i_{ok}^{h}=\frac{\left(R_{vk}+z_{ck}^{h}\right)^{-1}}{\sum_{i=1}^{N}\left(R_{vi}+z_{ci}^{h}\right)^{-1}}i_{Load}^{h} \quad (3)$$

in which $z_{ck}^{h}=z_{Lok}^{h}+z_{linek}^{h}$ and z_{Lok}^{h} and z_{linek}^{h} are the impedance of output inductor and line of unit k, respectively. Moreover, the effect of compensation voltage, v_s, is neglected.

Comparing (3) and (2), it is observed that the accuracy of current sharing is adversely affected by the output inductor and line impedances. Accurate current sharing necessitates selecting a virtual resistance much larger than z_{ck}^{h}. On the other hand, the value of virtual resistance is limited by the permissible voltage deviations. Therefore, the virtual resistance scheme might suffer from poor sharing accuracy in practice.

B. Selective virtual impedance scheme

Since the fundamental power factor is higher than 0.7 in practice, the voltage deviations caused by a virtual reactance is smaller compared with a virtual resistance of the same value. Therefore, for a specific voltage deviation, a larger virtual reactance can be utilized, which infers better sharing accuracy. In order to gain a desirable sharing accuracy while preserving the improved damping of the virtual resistance method, the selective virtual impedance scheme is utilized [7].

Unlike the virtual resistance, virtual impedance is dependent on the frequency and sequence (positive or negative sequence). For each harmonic component h (h=1+,1-,2+,2-,…), the virtual impedance is introduced as

$$v_{c}^{h*}=E^{h}-Z_{v}^{h}i_{o}^{h} \quad (4)$$

in which E_{k}^{1+} is obtained from conventional P-f/Q-V droop control method and E_{k}^{h} is equal to zero for other components. Moreover, Z_{v}^{h} is the virtual impedance matrix, which is defined as

$$Z_{v}^{h}=\begin{bmatrix} R_{v}^{h} & -h\omega_{0}L_{v}^{h} \\ h\omega_{0}L_{v}^{h} & R_{v}^{h} \end{bmatrix} \quad (5)$$

in which R_{v}^{h} and L_{v}^{h} are the virtual resistance and inductance corresponding with the component h, respectively.

The virtual selective impedance method can be implemented in either dq or $\alpha\beta$ reference frame. In the first approach, the dq components of harmonic order h are extracted by using a combination of $\alpha\beta/dq$ transformation and low pass filters [14]. The reference voltage is then calculated in dq reference frame according to (5) and then converted back to αβ frame. An alternative scheme proposed in [15] extracts the αβ components corresponding to each harmonic of interest by means of the multi-resonant frequency-locked loop method [16] and realizes the virtual impedance according to (5).

The main issue with the selective virtual impedance scheme is its complexity. On top of that, the use of low pass filters for extraction of harmonic components incurs a delay, which slows down the current sharing dynamics.

III. PROPOSED CURRENT SHARING STRATEGY

In this section, a novel decentralized control method based on V-I droop concept [17] is proposed to enable fast and accurate load sharing between the DERs. In this method, GPS timing technology is used to synchronize the DERs with the Coordinated Universal Time (UTC) [18]. The GPS synchronization provides the DERs with a common time stamp (t). Based on the GPS time, the no-load voltage of each DER unit is calculated according to:

$$E_{0,abc}=\begin{bmatrix} E_{0}\sin\omega_{0}t \\ E_{0}\sin\left(\omega_{0}t-2\pi/3\right) \\ E_{0}\sin\left(\omega_{0}t-4\pi/3\right) \end{bmatrix} \quad (6)$$

where ω_0 is the fundamental frequency, and E_0 is the rated voltage. Furthermore, the inverter reference voltage is controlled according to the following adaptive voltage-current droop law:

$$v_{droop,k}=E_{0,abc}-R_{vk}F\left(\hat{i}_{ok}\right)i_{ok} \quad (7)$$

in which R_{vk} is the droop coefficient and $\hat{i}_{ok}$ is the maximum peak of the abc currents of DERk, The adaptive droop function, F, is a piece-wise linear function, which starts at $F_{\min}$ for peak current of zero and increases to 1 when the peak current reaches its maximum value.

Equations (6) and (7) imply that the proposed method fixes the frequency at the nominal value. Therefore, the proposed method features improved power quality compared with the virtual resistance approach. Moreover, the introduction of an adaptive droop function improves the sharing accuracy as detailed in the following text.

The operation of the proposed droop scheme is demonstrated based on the equivalent circuit of Fig. 3. For simplicity, the DERs are considered to have the same rating. Moreover, the dynamics of the inner voltage and current control loops are neglected due to their smaller time constant with respect to the droop controller. The current of DER1 can be expressed as:

$$\frac{i_{1}}{i_{L}}=\frac{R_{v}F\left(\hat{i}_{2}\right)+z_{c2}}{R_{v}F\left(\hat{i}_{1}\right)+R_{v}F\left(\hat{i}_{2}\right)+z_{c1}+z_{c2}} \quad (8)$$

Equation (8) implies that the load sharing between the DERs is dependent on the virtual resistances as well as the output inductor and line impedances. The sharing error can be expressed as

$$\frac{i_1-i_2}{i_L}=\frac{F\left(\hat{i}_2\right)-F\left(\hat{i}_1\right)+\left(z_{c2}-z_{c1}\right)/R_v}{F\left(\hat{i}_1\right)+F\left(\hat{i}_2\right)+\left(z_{c2}+z_{c1}\right)/R_v} \tag{9}$$

In case the impedances z_{c1} and z_{c2} are equal, the load is equally shared between the DERs. However, as the mismatch between the impedances increase, the sharing error is degraded. Without loss of generality, consider the case that $z_{c1} < z_{c2}$. In this case, $i_1 > i_2$ and hence $F(\hat{i}_1) \geq F(\hat{i}_2)$, which implies that the adaptive droop action tends to decrease i_1 and improve the sharing accuracy. Furthermore, as the peak of current reaches the rated current, the function F grows larger. Therefore, the sharing accuracy is better at higher loading conditions, when the DERs are susceptible to overcurrent stresses.

The schematic diagram of the proposed droop control method is illustrated in Fig. 4. Each DER unit is equipped with a GPS receiver, which produces a 1 pulse per second timing signal. The GPS signal is used as a reference to align the local time, *t*, with UTC. The waveform generator block uses the GPS time to obtain the no-load voltage according to (6). The phase current with the largest magnitude is selected by using a combination of absolute and maximum functions. A standard peak detector [19] is implemented digitally to extract the peak current. The peak current is used to compute the adaptive virtual resistance. The DER reference voltage is then calculated by subtracting the voltage drop on the virtual resistance from the no-load voltage.

IV. Harmonic Compensation Scheme

The voltage drops across the virtual resistance, DERs output inductors and the distribution network lines gives rise to voltage distortions at the load buses. In order to improve the quality of voltage, a harmonic compensation scheme is adopted. As shown in Fig. 5, a measurement block measures the voltage at the Sensitive Load Bus (SLB). The positive and negative components of each of the harmonic components are then computed in the corresponding dq reference frame. The components are then transmitted to the secondary controller through a low bandwidth communication (LBC) link.

The secondary controller uses the same control concept as the conventional secondary control scheme [13]. In this method, the compensation signal for each component is calculated by means an integral controller. The reference of the controller, v^h_{ref}, is set to E_0 for $h = 1+$ to ensure the rms voltage is regulated at the rated value and zero for other components to eliminate the unbalance and harmonic distortions. The compensation signals are broadcasted to the primary controllers, in which they are transformed back to the *abc* frame and added to the DER reference voltage.

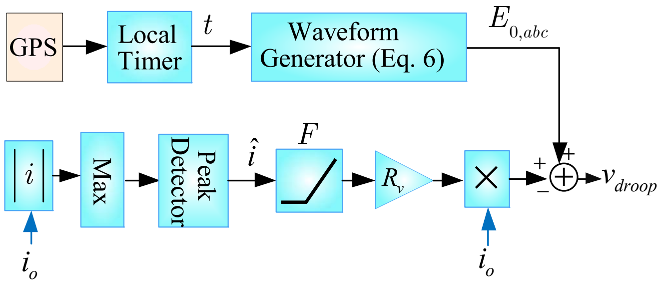


Fig. 4. Proposed droop control method

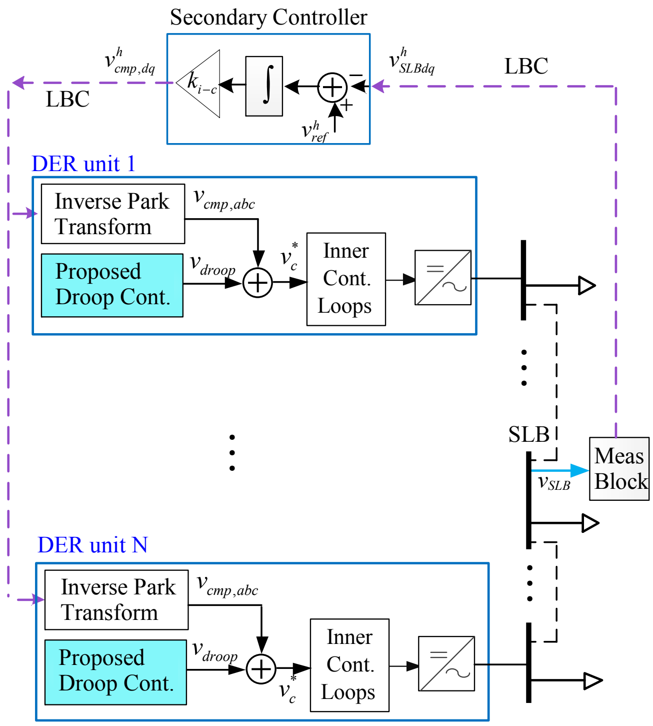
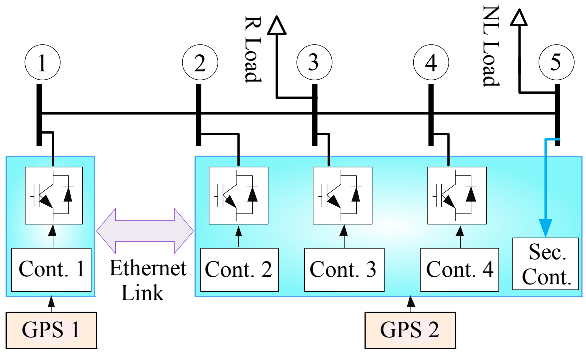


Fig. 5. Proposed harmonic compensation method

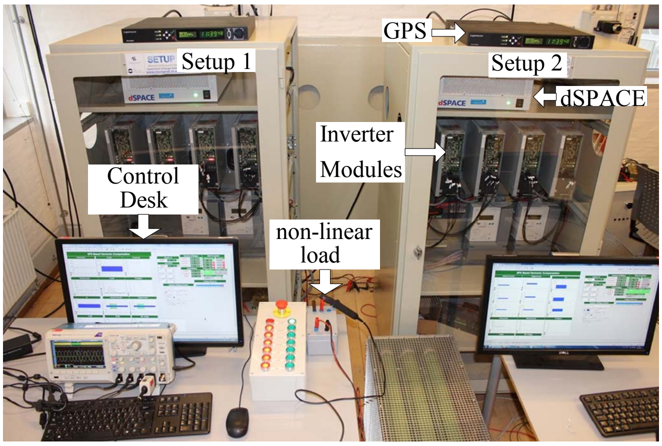
V. Experimental Results

The proposed method has been implemented on a laboratory scale test bed illustrated in Fig. 6. The test bed was prototyped in the Intelligent Microgrid Laboratory at Aalborg University [20]. The test bed includes four DER units and two loads interconnected through resistive line models. Each DER unit is composed of a 2200W Danfoss inverter followed by and LCL filter. A programmable DC power source the inverters. The MG supplies a linear balanced load as well as a nonlinear unbalanced load, which is comprised of a single phase rectifier connected between phase *a* and *b*. The underlying MG was assembled based on two experimental setups, each of which is equipped with a Securecync ® GPS receivers from Spectracom and a dSPACE 1006 digital control platform. An Ethernet communication link is used for broadcasting the secondary controller signal to the local controllers.

The specifications of the test bed as well as the control parameters are listed in Table I. The load impedances are



(a)



(b)

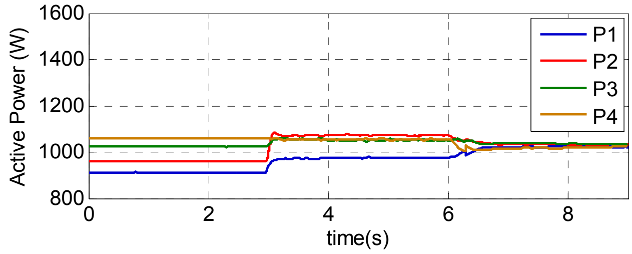
Fig. 6. Laboratory-scale test microgrid: a) schematic diagram, and b) Photo of the hardware

TABLE I. PARAMETERS OF THE TEST MG

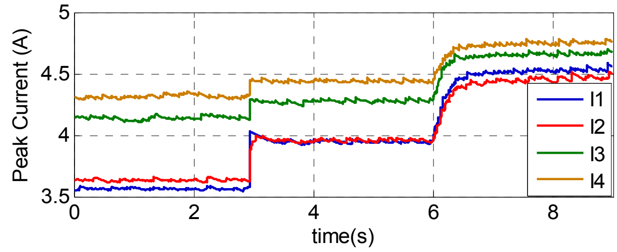
Description	Parameter	Value	Unit
Fundamental Frequency	f_0	50	Hz
Rated phase Voltage	V_{rated}	220	Vrms
Inverter Specifications	$I_{peak,max}$	5	A
	f_{PWM}	10	kHz
LCL Filter	L_f	8.6	mH
	C_f	4.5	µF
	L_c	1.8	mH
Resistive Load	R_1	57	Ω
Nonlinear Load (DC side)	R_{NL}	130	Ω
	C_{NL}	115	µF
Line Impedances	$Z_{line1-2}$	0.22+j0.03	Ω
	$Z_{line2-3}$	0.22+j0.03	Ω
	$Z_{line3-4}$	0.5+ j0.06	Ω
	$Z_{line4-5}$	0.5+j0.06	Ω
V-I droop coefficient	R_v	6.5	Ω

selected so that the full load current is close to the inverters capacity.

In order to verify the efficacy of the proposed method, two cases studies have been tested. In the first case, the effect of adaptive droop function and secondary controller on the current sharing accuracy and power quality is studied. The experimental results for the first case study are shown in Fig.



(a)



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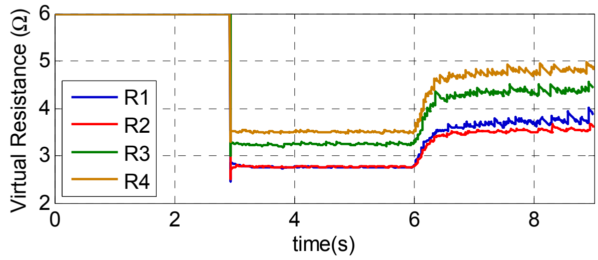
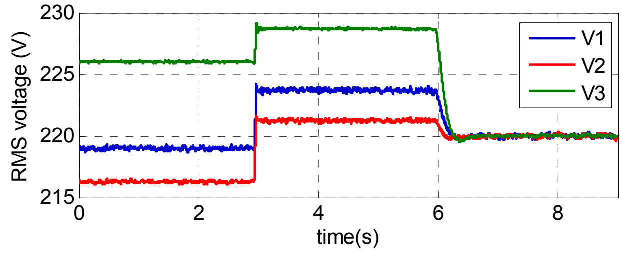
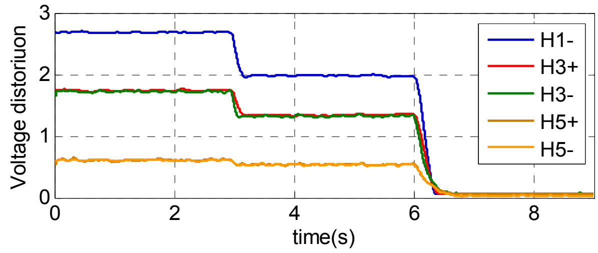


(c)



(d)



(e)

Fig. 7: Performance of the proposed method: a) active power, b) peak current, c) virtual resistance, d) RMS voltage, and e) voltage distortion

7. Prior to t=3s, a fixed virtual resistance is adopted by setting the droop function, F, equal to 1. From Fig. 7(a), it is observed that P1, P2, P3, and P4 are 910 W, 960 W, 1020W, 1050W, respectively. Therefore, the DERs which are electrically closer to the load pick up a larger share from the load. The sharing error is also reflected in peak current, as shown in Fig. 7(b). The rms voltages at the SLB are within the standard range of 0.95pu to 1.05pu thanks to the smart selection of the virtual

resistance. However, the voltage unbalance and harmonic distortions are larger than the acceptable range advised by IEEE Std 519-1992 [21]. Specifically, the unbalance factor (UF) and the third, (H3+ , H3-) and fifth (H5+,H5-) harmonic distortions are at 2.7%, 1.7%, 0.6%, respectively (See Fig. 7 (e)).

At t=3s, the adaptive virtual resistance is activated. As shown in Fig. 7 (c), the DERs which are electrically closer to the load adopt a larger virtual resistance. This way, the adverse effect of line impedances on current sharing accuracy is reduced. As a result, the load sharing accuracy is improved, as depicted in Fig 7(b).

At t=6s, the secondary controller is activated. Consequently, the SLB voltage is regulated at 1pu and the voltage distortions are eliminated. The harmonic compensation results in an increase of the load current, which in turn causes the DER currents to increase. Consequently, the adaptive virtual resistances are increased to improve the sharing accuracy (See Fig. 7(b)).

In the second case, the transient response of the proposed method following a step load change is studied. To that end, the non-linear load is switched on and off at t=3s and t=6s, respectively. The experimental results for the second test are illustrated in Fig. 8. It is observed that the proposed method exhibits a smooth and overdamped dynamic response. Specifically, the DERs power generations change smoothly during the load changes, as shown in Fig. 8(a). Moreover, proportional sharing of the current during the transients prevents overcurrent stresses, as depicted in Fig. 8(b). From Fig. 8(c) and (d), it is observed that voltage of the SLB bus experiences a deviation following the load charges. However, the voltage deviations are within the acceptable range (0.95pu to 1.05pu) and diminish to zero within 0.5s.

VI. Conclusions

A new hierarchical control method consisting of a secondary and local primary control levels is proposed for improving power quality and current sharing accuracy of MGs. Each of the primary controllers utilizes a GPS receiver to synchronize its local time with a common time reference. Furthermore, the frequency of operation is fixed at the rated value and load sharing is achieved through a voltage-current droop characteristic. With the intention of improving the current sharing accuracy at high loading conditions, the droop gain is adjusted as a function of the output current. The secondary control level, which is based on secondary frequency compensation in conventional power systems, eliminates voltage distortions at a sensitive load bus by injecting a compensating signal into the DERs reference voltages.

The proposed method is tested on a laboratory scale experimental setup. Experimental results demonstrate the efficacy of the proposed method in terms of current sharing accuracy and power quality.

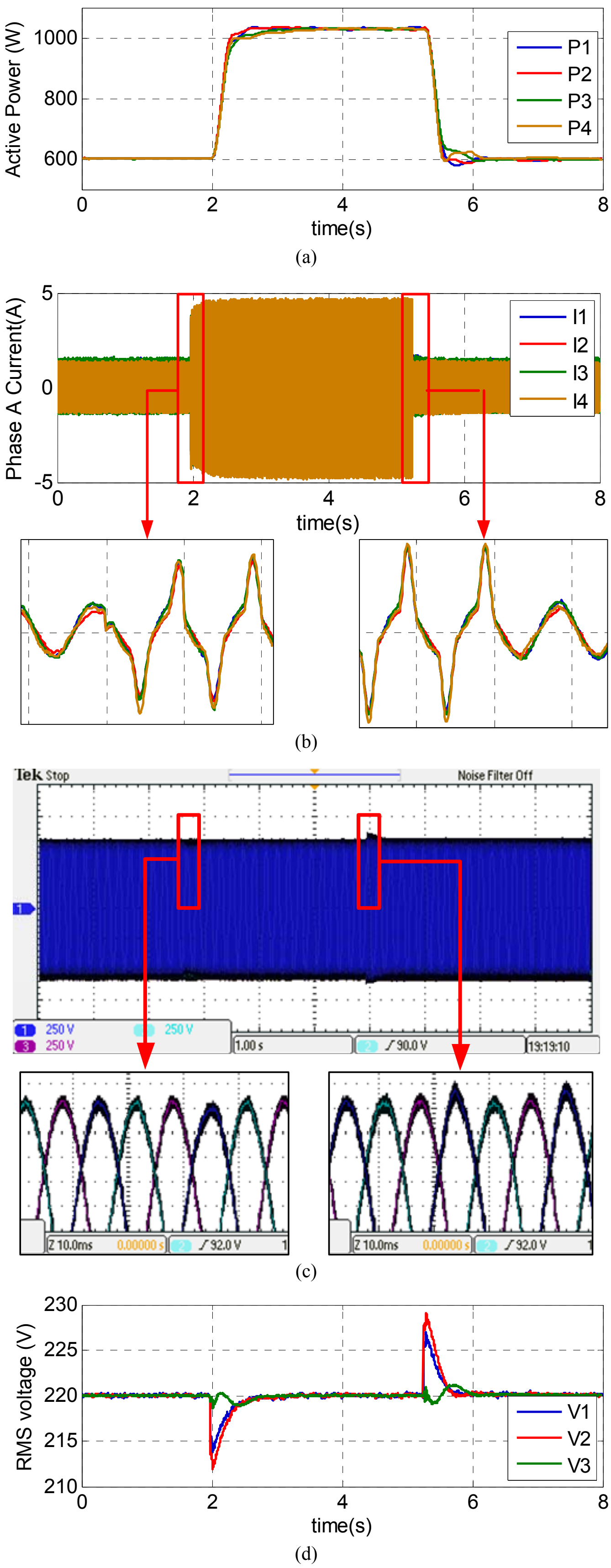


Fig. 8: Performance of the proposed method: a) active power, b) current waveform, c) voltage waveform, and d) RMS voltage

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