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Effect of State Feedback Coupling and System Delays on the Transient Performance of Stand-Alone VSI with LC Output Filter

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***Abstract*— The influence of state feedback coupling in the dynamics performance of power converters for stand-alone microgrids is investigated. Computation and PWM delays are the main factors that limit the achievable bandwidth of current regulators in digital implementations. In particular, the performance of state feedback decoupling is degraded because of these delays. Two decoupling techniques to improve the transient response of the system are investigated, named non-ideal and ideal capacitor voltage decoupling respectively. In particular, the latter solution consists in leading the capacitor voltage on the state feedback decoupling path in order to compensate for system delays. Practical implementation issues are discussed with reference to both the decoupling techniques. A design methodology for the voltage loop, that considers the closed loop transfer functions developed for the inner loop, is also provided. A proportional resonant voltage controller is designed according to Nyquist criterion taking into account application requirements. For this purpose, a mathematical expression based on root locus analysis is proposed to find the minimum value of the fundamental resonant gain. Experimental tests performed in accordance to UPS standards verify the theoretical analysis.**

***Index Terms*— Control system analysis, current control, microgrids, power quality, voltage control**

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I. Introduction

THE dynamics performance of voltage and current regulators play an important role in modern applications of power electronics. The general power converter employed is the Voltage Source Inverter (VSI) operating in voltage or current control mode. Inaccurate design of the inner loops degrades significantly the performance of the overall control system, potentially interfering with outer loops characterized by slower dynamics. This is the case in ac and dc droop-controlled microgrids [1-3], possibly with hierarchical control based on secondary and tertiary control [4-6] and variable speed drives [7], [8]. Thus, effective control of voltage and current is mandatory to succeed in implementing the desired feature of each application. According to [9], it is desirable from any current or voltage regulator the following: i) to achieve zero steady-state error; ii) accurately track the command reference, rejecting any disturbance; iii) have bandwidth as higher as possible; iv) compensate for low order harmonics.

A possible implementation of the inner regulators is based on Proportional Resonant (PR) controllers in the stationary reference frame. Their features are equivalent to two PIs controllers implemented in two synchronous reference frames [10], one for the positive sequence and the other for the negative sequence component of the signal. However, PR controllers are easier to implement being the controlled states on α- and β-axis naturally decoupled. In the synchronous reference frame a decoupling technique is needed since the states on d- and q-axis are not independent [11]. Another advantage is the lesser number of transformations required to reach the $\alpha\beta$ stationary reference frame, which makes PR controllers an attractive solution in low-cost digital signal processor units because of its low computational burden. Furthermore, PR controllers can be directly used in single-phase power converters applications without the need of further modifications [12], [13].

Substantial research activities have been made in the design of regulators for systems with a strong electromotive force,

e.g. grid connected [13-15], and motor drives applications [16, 17]. However, design issues for stand-alone applications have not been so far discussed in depth. In this scenario, the coupling between the inductor current and capacitor voltage significantly degrades the system performance. Moreover, the effect of computation and PWM delays on the achievable bandwidth when voltage decoupling is performed has not been addressed in depth so far.

The main state of the art is analyzed in the following, with special focus on the relevant findings for stand-alone applications. In [18] an analytical method to determine the best possible gains of linear ac current controllers is derived, considering computation and PWM delays. In [19] different multi-loop control approaches using alternative feedback control variables are investigated. A similar analysis is addressed in [20], [21], comparing the use of the inductor and capacitor current as controlled state variables in terms of disturbance rejection properties. In [22], a delay prediction and feedback strategy of the computation delay is proposed to increase the bandwidth of a grid-connected power converter. In [23] a frequency-domain analysis of different resonant current regulators for active power filters (APF) is performed, taking into account computation and PWM delays. In [24] a methodology to assess the transient response of PR current regulators is proposed, aimed to achieve fast and non-oscillating transient responses in grid-connected applications. Recently, a fast acting current control scheme to regulate the load current during all energizing conditions of multiple load transformers powered by a UPS system has been proposed [25]. In [26] a direct discrete-time design approach for current regulators is proposed, leading to the derivation of a small-signal z-domain model. In [27] observers for the capacitor current and disturbance are proposed to achieve a fast and robust current loop, respectively. In [28] a comprehensive review of linear and non-linear current regulators is assessed. Proportional integral and state feedback controllers, along with predictive techniques are discussed. With regard to non-linear regulators, bang-bang and predictive controllers with on-line optimization are reviewed. In [29] the effect of computation and PWM delays, rounding and truncation errors and flux imbalance in the output transformer are analyzed to design an online UPS system. In [30] the design of a multiloop predictive voltage controller is addressed. Feedforward of the capacitor current and a load current estimator are implemented. However, in the papers addressed, the effect and modelling of the delays for islanded systems have not been fully analyzed. When voltage decoupling is performed, the influence of not compensating for computation and PWM delays on the state feedback decoupling path is not taken into account. In fact, in previous works, the decoupling of the controlled states neglects the effect of computation and PWM delays when performed. This is equivalent to consider the decoupling ideal. Nevertheless, system delays degrade the performance of state feedback decoupling. As will be shown in the paper, this effect cannot be ignored, since implies a reduction in the achievable bandwidth.

This paper addresses the abovementioned issues associated to islanded systems and provides feasible solutions to overcome them. A systematic design methodology to mitigate the effect of non-ideal voltage decoupling is provided. Specifically, a low-pass filter cascaded with a lead compensator on the decoupling path has been proposed for further improvements. It must be noticed that even without the one-sample delay introduced by PWM, the latch effect is still present and limit the achievable bandwidth, thus reducing the benefits introduced by the decoupling. Finally, a design methodology for the voltage loop, that considers the closed loop transfer functions developed for the inner loop, is also provided. Its effect is reflected in the Nyquist trajectories calculated for the voltage loop, and hence affects the selection of controller gains. Furthermore, a criterion to select the minimum value of the fundamental resonant gain is proposed, which leads to an easy mathematical formulation for practical design. This work is organized as follows. Firstly, the influence of the delay model on the design of the current regulator is investigated. The inner loop current control with and without state feedback voltage decoupling is analyzed. A feasible solution to compensate for the computation and PWM delays on the state feedback decoupling path is derived. Subsequently, a PR voltage controller design is proposed. Detailed design and tuning is provided according to Nyquist criterion. The theoretical solution is supported by experimental results, according to the IEC 62040 normative for UPS systems.

II. System Description

In isolated microgrids the VSI is equipped with an LC filter at its output. This topology is also considered in UPS systems [20]. In general, it operates in voltage control mode with the capacitor voltage and inductor currents being the controlled states. In some cases the capacitor current is used as controlled state to improve the disturbance rejection properties [19], [20]. In Fig. 1 the block diagram including a three-phase inverter with its inner loops is presented. The purpose of the inner current loop is to track the commands from the outer voltage loop and to ensure fast dynamic disturbance rejection within its bandwidth. Whenever the current regulator is unable to perform properly these tasks, the system performance degrades.

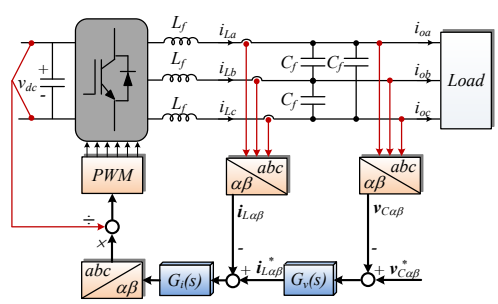


Fig. 1. Block diagram of a three phase VSI with voltage and current loops.

The simplified block diagram of the closed-loop system is shown in Fig. 2 where $\boldsymbol{V}^*_{c\alpha\beta}$ and $\boldsymbol{I}^*_{L\alpha\beta}$ are the reference

capacitor voltage and current vectors and $\boldsymbol{I}_{o\alpha\beta}$ is the output current vector, which acts as a disturbance to the system. $G_i(s)$ and $G_v(s)$ represent the current and voltage regulators transfer functions (TF), $G_{pwm}(s)$ is the TF related to computation and PWM delays, whereas $G_{dec}(s)$ is the TF related to the decoupling of the controlled states.

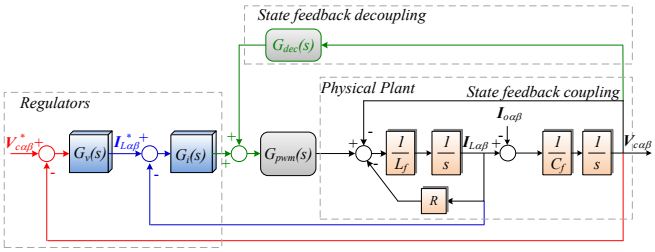


Fig. 2. Simplified block diagram of the closed-loop system.

The design of voltage and current regulators is based on serial tuning, with the innermost loop the first to be designed according to the desirable bandwidth and system damping [31]. In the next section the design of current regulators is discussed, with respect to voltage decoupling and the reduction in the achievable bandwidth whenever the computation and PWM delays are not compensated for on the decoupling path.

III. Current Regulator Design

A usual design approach for current regulators is based on neglecting the cross-coupling between the inductor current and the capacitor voltage. The proportional gain of the current loop is determined by neglecting computation and PWM delays, and the current loop gain k_{pI} is expressed by

$$k_{pI} = 2\pi f_{bw} L_f. \tag{1}$$

Being L_f the filter inductor and f_{bw} the desired bandwidth (in Hz) of the current regulator. However, if the design requires a high bandwidth, the lag introduced by computation and PWM delays in digital implementations have to be considered. The physical delay has the form of an exponential decay ($e^{-T_d s}$). At least two first-order expressions based on rational TF are usually used to approximate this delay [11]: 1) $1/(1+T_d\, s)$; 2) $[1-(T_d/2)s]/[1+(T_d/2)s]$. The frequency responses (FR) of the delay and these two approximations are shown in Fig. 3 with a switching frequency $f_s = 10\ kHz$ and $T_d = 1.5/f_s$. The approximation to be used depends on the frequency range to analyze, and this is coupled to the bandwidth chosen for the regulators. For the approximation using a first order lag $1/(1+T_d\, s)$ the match is satisfactory up to approximately 300 Hz ($f_s/30$). On the other hand, for the approximation using a zero in the right half plane $[1-(T_d/2)s]/[1+(T_d/2)s]$ the match is accurate up to more than 1 kHz ($f_s/10$), which covers the range of the desired current regulator bandwidth ($f_{bw} = 1\ kHz$).

If the inner loop design requires a high bandwidth, as in islanded microgrids where the controller is supposed to control harmonics, the approximation with a zero in the right half plane is preferred. Otherwise, the expected bandwidth does not correspond to the value of the calculated gain.

Fig. 4 shows the block diagram for the inner current loop, designed taking into account the previous considerations. The load impedance is represented by $\boldsymbol{Z}$.

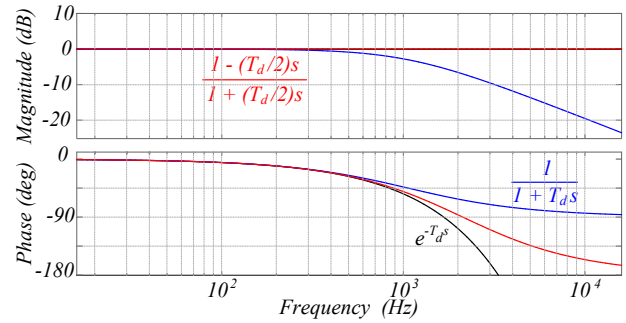


Fig. 3. Frequency response of the delay and its Padè approximations : $\boldsymbol{T_d = 1.5/f_s}$.

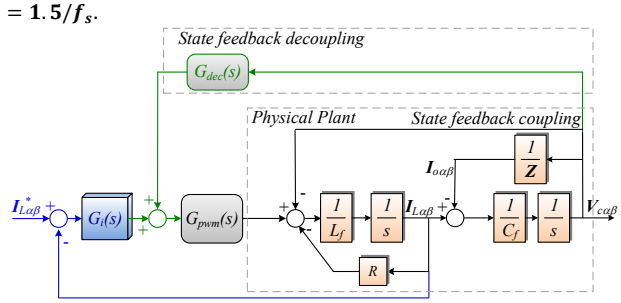


Fig. 4. Block diagram for the inner current loop.

The closed-loop TF of this system is shown in

$$\boldsymbol{I}_{L\alpha\beta}(s) = \frac{G_i(s)G_{PWM}(s)C_f s}{L_f C_f s^2 + RC_f s + G_i(s)G_{PWM}(s)C_f s - [G_{dec}(s)G_{PWM}(s)-1]}\boldsymbol{I}^*_{L\alpha\beta}(s) - \frac{G_{dec}(s)G_{PWM}(s)-1}{L_f C_f s^2 + RC_f s + G_i(s)G_{PWM}(s)C_f s - [G_{dec}(s)G_{PWM}(s)-1]}\boldsymbol{I}_{o\alpha\beta}(s). \tag{2}$$

In the next subsections the effect of $G_{dec}(s)$ on the closed-loop TF of the system is investigated considering four cases: A) Without voltage decoupling; B) Ideal voltage decoupling; C) Non-ideal voltage decoupling with unit transfer function; D) Non-ideal voltage decoupling with lead-lag compensator. For this purpose, a proportional controller is selected as current regulator ($G_i(s) = k_{pI}$). The system parameters used both in the analysis and in the laboratory tests are shown in Table I.

TABLE I
System Parameters

Parameter	Value
Switching frequency	$f_s = 10\ kHz$
Filter inductance	$L_f = 1.8\ mH$
Filter capacitor	$C_f = 27\ \mu F$
Inductor ESR	$R = 0.1\ \Omega$
Linear load	$R_l = 68\ \Omega$
Non linear load	$C_{NL} = 235\ \mu F$ $R_{NL} = 184\ \Omega$ $L_{NL} = 0.084\ mH$

A. Without voltage decoupling

If $G_{dec}(s) = 0$ the controlled states are coupled. From the root locus in Fig. 5, it can be seen that the inner loop, responsible for controlling the inductor current, has always low damping and high overshoot whatever gain is selected. The characteristics of the dominant closed-loop poles are shown, as well as the controller gain for the selected bandwidth of 1 kHz.

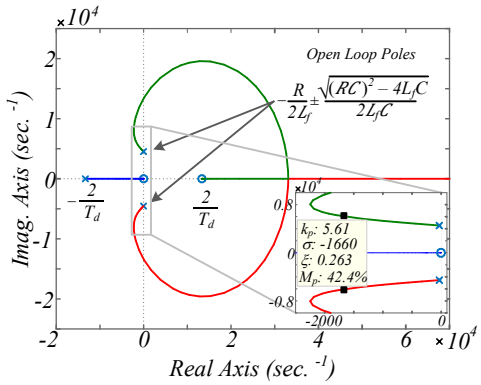


Fig. 5. Root locus for the inner current loop with P regulator and without voltage decoupling: x – open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI}} = \mathbf{5.61}$; o – zeros.

If the controlled states are not decoupled the system is highly load dependent, as can be seen from the FR in Fig. 6.

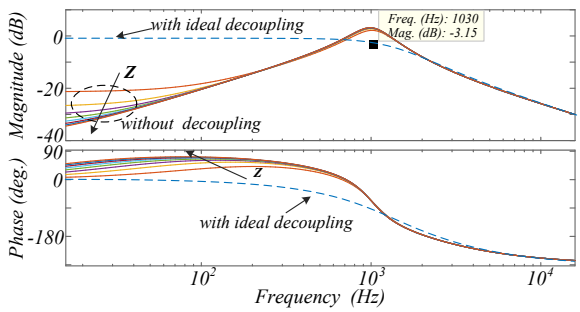


Fig. 6. Closed-loop FR for the inner current loop with P regulator and with ideal and without voltage decoupling – arrows indicate decreasing in load (from rated resistive load until no-load).

The arrow indicates increase in the load impedance, from rated load to open-circuit conditions. For any value of the impedance the system shows a low gain for a broad frequency range including fundamental frequency (50 Hz), which means the command reference is not properly tracked resulting in very high steady-state error. That is why in some research work the use of resonant regulators is suggested for this loop [1]. However, using some resonant structures without voltage decoupling can lead to instability, independently of the regulator gains [32].

B. Ideal voltage decoupling

If it is possible to exactly decouple (cancel) the capacitor coupling, the simplified model in Fig. 7 can be used to analyze the dynamic behavior of the inner current loop.

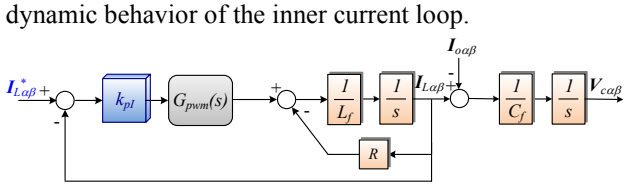


Fig. 7. Simplified block diagram of the inner current loop with *ideal voltage decoupling.*

In this case, *ideal voltage decoupling* is achieved and the correspondent closed-loop TF is

$$\boldsymbol{I}_{L\alpha\beta}(s) = \frac{k_{pI}G_{PWM}(s)}{L_f s + R + k_{pI}G_{PWM}(s)}\boldsymbol{I}^*_{L\alpha\beta}(s). \tag{3}$$

By observing this TF, it is possible to conclude that the output current does not affect anymore the inner current loop. This results in an easier design of the controller, with better dynamics, and with a dynamic behavior not dependent of the load impedance. Considering the approximation with a zero on the right half plane for $G_{PWM}(s)$, the closed-loop TF takes the form of a second order system

$$\boldsymbol{I}_{L\alpha\beta}(s) = \frac{-\frac{k_{pI}}{L_f}s + \frac{2k_{pI}}{L_fT_d}}{s^2 + \left(\frac{2L_f + RT_d - T_dk_{pI}}{L_fT_d}\right)s + \left(\frac{2R + 2k_{pI}}{L_fT_d}\right)}\boldsymbol{I}^*_{L\alpha\beta}(s). \tag{4}$$

Thus, the order of the system is lowered by one degree and higher damping is achieved with less overshoot for the same bandwidth (see Fig. 8). The system is not dependent on the load impedance and almost zero steady-state error can be achieved even with a simple P controller (see Fig. 6). It must be noted that this low steady-state error is dependent on the value of the inductor ESR, that in this case is $R = 0.1\ \Omega$.

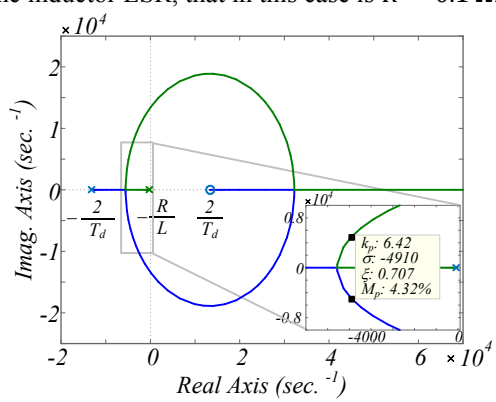


Fig. 8. Root locus for the inner current loop with P regulator and ideal voltage decoupling: x – open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI}} = \mathbf{6.42}$; o – zeros.

However, *ideal voltage decoupling* corresponds to design $G_{dec}(s) = G_{PWM}(s)^{-1}$, which results in an unstable TF if the approximation for $G_{PWM}(s)$ with the non-minimum phase zero is used or it is not practically feasible if the other approximation is employed since a derivative term should be used on the decoupling path. Unfortunately, a pure time delay does not have a realizable inverse [33].

C. Non-ideal voltage decoupling with unit transfer function

If $G_{dec}(s) = 1$, the computation and PWM delays on the state feedback decoupling path are not compensated. The closed-loop TF in (2) is modified accordingly. By substituting $\boldsymbol{I}_{o\alpha\beta}(s) = \boldsymbol{V}_{c\alpha\beta}(s)/\boldsymbol{Z}(s)$, and being $\boldsymbol{V}_{c\alpha\beta}(s) = \left[\boldsymbol{I}_{L\alpha\beta}(s) - \boldsymbol{I}_{o\alpha\beta}(s)\right]/C_f s$, the closed-loop TF in (5), at the bottom of this page, is derived.

$$\boldsymbol{I}_{L\alpha\beta}(s) = \frac{\boldsymbol{Z}(s)C_f^2 sG_i(s)G_{PWM}(s) + G_i(s)G_{PWM}(s)C_f}{\boldsymbol{Z}(s)L_fC_f^2s^2 + \left[\boldsymbol{Z}(s)RC_f^2 + \boldsymbol{Z}(s)C_f^2G_i(s)G_{PWM}(s) + L_fC_f\right]s + \left[\boldsymbol{Z}(s)C_f + RC_f + G_i(s)G_{PWM}(s)C_f - \boldsymbol{Z}(s)C_fG_{PWM}(s)\right]}\boldsymbol{I}^*_{L\alpha\beta}(s). \tag{5}$$

This design approach is named *non-ideal voltage decoupling with unit transfer function*. Compared to *ideal voltage decoupling* (see Fig. 8) the damping of the system degrades with higher overshoot for the same proportional gain (see Fig. 9). However, the damping is still much higher than without voltage decoupling (see Fig. 5).

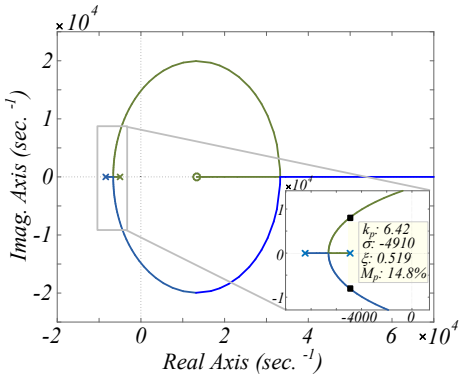


Fig. 9. Root locus for the inner current loop with P regulator and non-ideal voltage decoupling [$\boldsymbol{G_{dec}(s)=1}$]: x – open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI}=6.42}$; o – zeros.

As shown in the FR in Fig. 10, the system is still load dependent, but to a lesser extent than without decoupling.

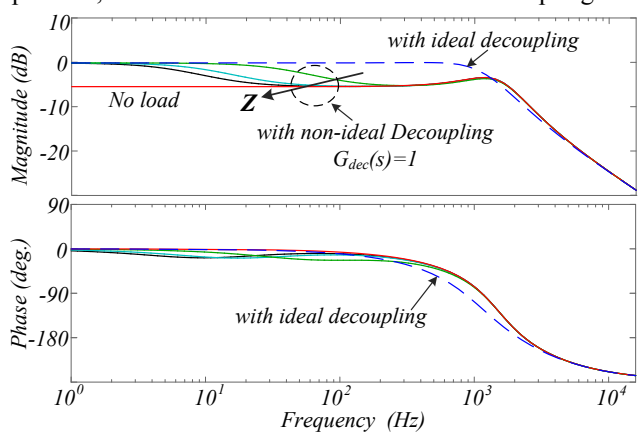


Fig. 10. Closed-loop FR for the inner current loop with P regulator and with non-ideal [$\boldsymbol{G_{dec}(s)=1}$] and ideal voltage decoupling – arrows indicate decreasing in load (from rated resistive load until no-load).

The achievable bandwidth is considerably reduced and limited by the computation and PWM delays, which are not compensated for on the state feedback decoupling path. However, it should be noted that the decoupling provides approximately 0 dB closed-loop gain at low frequency components, as expected from a closed-loop system.

D. Non-ideal voltage decoupling with lead-lag compensator

To overcome the limitation introduced by modelling $G_{dec}(s)=G_{PWM}(s)^{-1}$, a possible solution could be to design $G_{dec}(s)$ as a first order phase-lead compensator with the form

$$G_{lead}(s)=\frac{1+\tau_z s}{1+\tau_p s}. \tag{6}$$

With $\tau_p<\tau_z$ determining the frequency range where positive phase is added to the system. The signal should be advanced to compensate for the lag of $G_{PWM}(s)$ at each frequency. As can be seen in the phase diagram of Fig. 3, the lag increases significantly with the increase in frequency. If $G_{dec}(s)=G_{lead}(s)$ is designed to compensate for the delay at fundamental frequency, the closed-loop TF is almost load independent (see Fig. 11), as if ideal decoupling were performed.

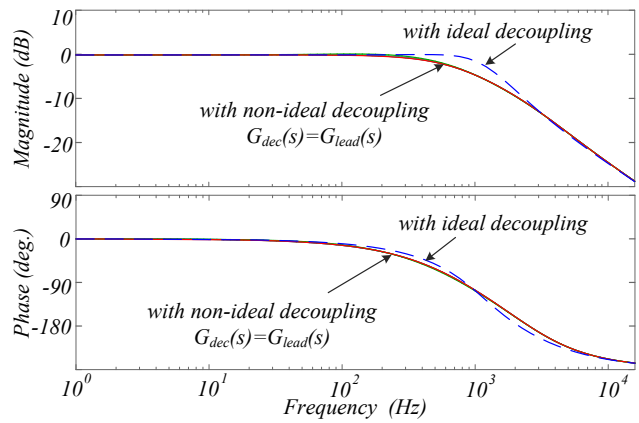


Fig. 11. Closed-loop FR for the inner current loop with P regulator and with non-ideal [$\boldsymbol{G_{dec}(s)=G_{lead}(s)}$] and ideal voltage decoupling.

However, for practical implementations, a low-pass filter $G_{LPF}(s)$ cascaded with $G_{lead}(s)$ is used in order not to amplify high frequency components and noise affecting the measured voltage signal. Thus, the signal is advanced only in a specific frequency range. In the following analysis this implementation is referred to as *non-ideal voltage decoupling with lead-lag compensator*. $G_{LPF}(s)$ introduces an additional lag which $G_{lead}(s)$ should compensate for. Accordingly, the FR of the system (see Fig. 12) degrades compared to the FR in Fig. 11. Nevertheless, this implementation provides better characteristics than the one that does not compensate for the delay ($G_{dec}(s)=1$). In fact, higher values at low frequency and lower load dependency than with *non-ideal voltage decoupling with unit transfer function* can be observed.

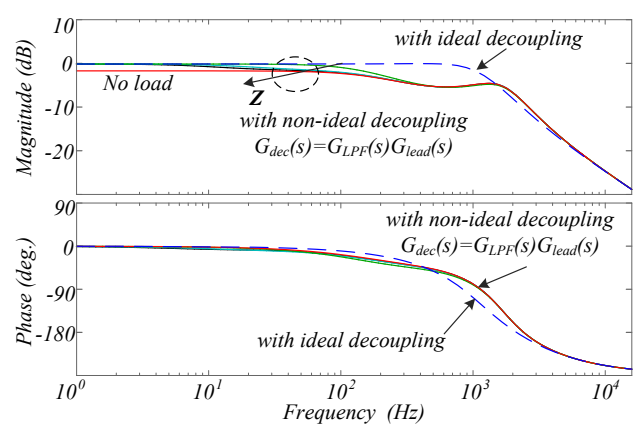


Fig. 12. Closed-loop FR for the inner current loop with P regulator and with non-ideal [$\boldsymbol{G_{dec}(s)=G_{LPF}(s)G_{lead}(s)}$] and ideal voltage decoupling – arrows indicate decreasing in load (from rated resistive load until no-load).

IV. Voltage Regulator Design

A PR structure is implemented in the voltage loop. The addition of resonant filters provides a good steady-state

tracking of the fundamental component and mitigate the main harmonics associated to non-linear loads. The gains of the system are selected to provide also a good dynamics response when the system is tested according to the requirements imposed by the normative for islanded systems. The voltage regulator is based on PR controllers with a lead compensator structure as

$$G_v(s) = k_{pV} + \sum_{h=1,5,7} k_{iV,h} \frac{s\cos(\varphi_h) - h\omega_1 \sin(\varphi_h)}{s^2 + (h\omega_1)^2}. \quad (7)$$

Where h refers to the harmonic order to be compensated. The proportional gain k_{pV} determines the bandwidth of the voltage regulator, and is designed for around 150 Hz. The lead angles at each harmonic frequency are set such that the trajectories of the open loop system on the Nyquist diagram, with the PR regulators at fundamental, 5th and 7th harmonics, guarantee a sensitivity peak η higher than a threshold value [34]. In this work this threshold has been set to $\eta = 0.5$ at no-load condition. After calculating the phase-lead angles, the fundamental resonant gain $k_{iV,1}$ is selected in order to have a fast response to changes in the fundamental component. Equation (6) can be rewritten just for the resonant controller at fundamental, leading to the second-order system

$$G_v(s) = k_{pV} \frac{s^2 + \frac{k_{iV,1}}{k_{pV}}\cos(\varphi_1)s + \left[\omega_1^2 - \frac{k_{iV,1}}{k_{pV}}\omega_1 \sin(\varphi_1)\right]}{s^2 + \omega_1^2}. \quad (8)$$

According to Evans root locus theory, the open loop poles move towards the open loop zeros when the loop is closed. For this reason, the pair of zeros of the PR controller in (7) are moved as furthest as possible from the right half plane. This corresponds to place them on the same location, such that the pair of poles of $G_v(s)$ are coincident. This corresponds to design $k_{iV,1}$ according to

$$k_{iV,1} \geq K \frac{2k_{pV}\xi_{crit}\omega_1}{\cos(\varphi_1)}. \quad (9)$$

Where the lower bound of the inequality refers to $K = 1$, with the damping factor $\xi_{crit} = 1$. For the lead angle at fundamental frequency $\varphi_1 = 3.3°$, the gain is $k_{iV,1} = 31.47$. The upper bound is set by $k_{iV,1}$ values which do not significantly degrade the relative stability of the closed-loop system [7].

The harmonic resonant gains are selected to have reduced transient oscillations [24], as well as to fulfill the requirements set by the UPS standards (see Table II).

TABLE II
VOLTAGE REGULATOR CONTROL PARAMETERS

Parameter		Value	
Proportional gain		$k_{pV} = 0.05$	
Integral gains and lead angles	@50Hz	$k_{iV,1} = 31.47$	$\varphi_1 = 3.3°$
	@250Hz	$k_{iV,5} = 15$	$\varphi_5 = 37°$
	@350Hz	$k_{iV,7} = 15$	$\varphi_7 = 44°$

In Fig. 13 the Nyquist diagram of the system in Fig. 2 with the parameters of Table II is shown. The sensitivity peak is higher than 0.5 at no-load condition and 0.4 at rated load ($Z = 68\ \Omega$), respectively.

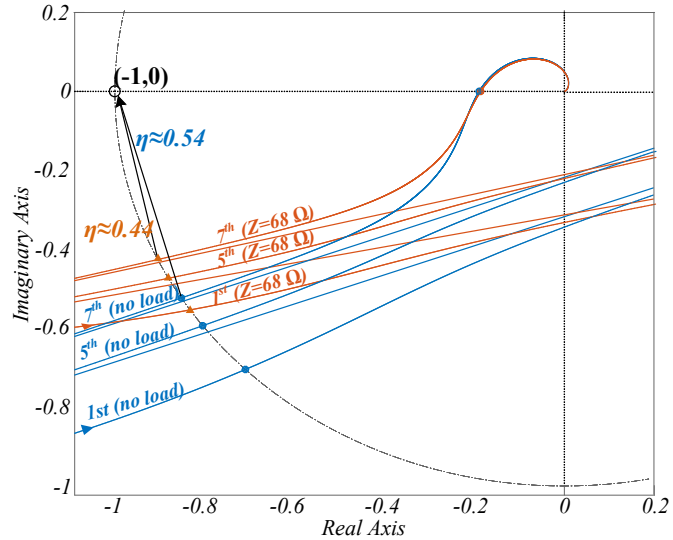


Fig. 13. Nyquist diagram of the system at no-load and rated load ($\boldsymbol{Z} = \mathbf{68}\ \Omega$) conditions.

In the next section, the robustness of the controllers designed is verified via extensive experimental results performing step responses and step load changes with both resistive and non-linear loads.

V. EXPERIMENTAL RESULTS

The system in Fig. 1 was tested to check the theoretical analysis. For this purpose, a low scale test-bed has been built using a Danfoss 2.2 kW converter, driven by a dSpace DS1006 platform. An Analog-to-Digital DS2004 board is used to digitalize the analog signals sensed via LEM current and voltage transducers. A 16-bit high resolution Digital-to-Analog conversion board DS2102 is used to monitor the signals with an oscilloscope. A photo of the experimental setup is shown in Fig. 14.

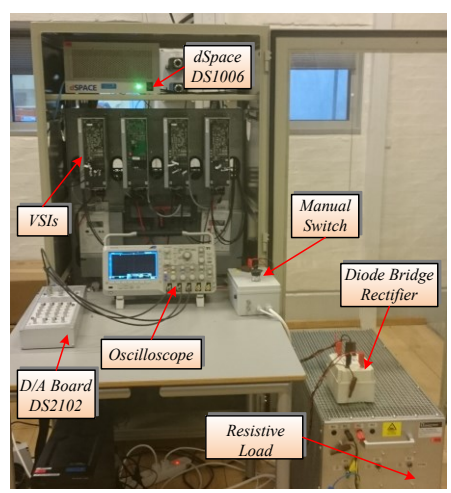


Fig. 14. Photo of the experimental setup.

The filter parameters and operational information are shown in Table I. The implementation of the regulators is made in the discrete time domain using Impulse Invariant as discretization

method for the resonant terms of the voltage regulator [24]. The corresponding transfer function of the resonant filters in the discrete-time domain $R_{1h}^{d}(z)$ is

$$R_{1h}^{d}(z) = T_s \frac{\cos(\varphi_h) - z^{-1}\cos(\varphi_h - h\omega_1 T_s)}{1 - 2z^{-1}\cos(h\omega_1 T_s) + z^{-2}}. \quad (10)$$

A. Current loop experimental tests

Regarding the current loop only, a step response of the inductor current is performed. If voltage decoupling is not performed, due to the low gain at low frequencies (see Fig. 6), a high reference current must be provided to achieve the rated one. However, it was not possible to achieve the rated current since the converter protection activates, due to the high initial current. Thus, in order to obtain step response captures without voltage decoupling a lower reference current is provided. In Fig. 15 it can be seen the current during the transient is higher than the steady-state value because of low damping, as expected from the theoretical analysis. It should be noted the different scales for the reference (50 A/div) and real inductor current in α-axis (5 A/div). This test proves that the current loop is not working properly, since the reference is not tracked.

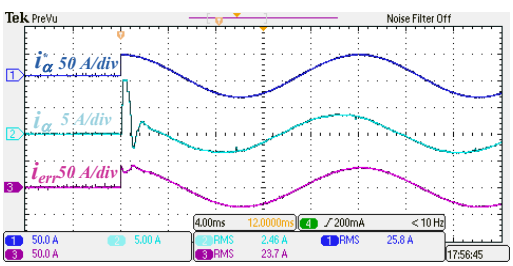


Fig. 15. Step response of the reference current without voltage decoupling: (1) reference; (2) real; (3) inductor current error - (α-axis).

With reference to voltage decoupling with $G_{dec}(s) = G_{LPF}(s)G_{lead}(s)$ the response is much more damped and the steady-state error is almost zero, even if just a P controller is used (see Fig. 16).

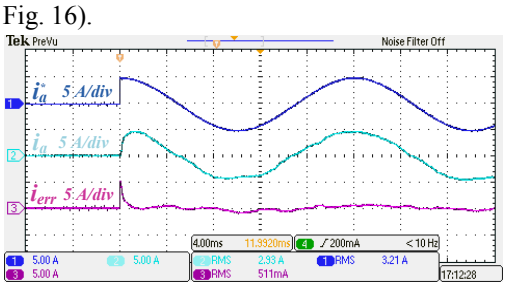


Fig. 16. Step response of the reference current with voltage decoupling and $G_{dec}(s) = G_{LPF}(s)G_{lead}(s)$: (1) reference; (2) real; (3) inductor current error - (α-axis).

In this case, $G_{LPF}(s)$ is designed as a first order IIR Butterworth low-pass filter with a bandwidth of 400 Hz and a sampling frequency of 10 kHz. The lag introduced at fundamental frequency is 7.09°. $G_{lead}(s)$ is designed to compensate for the lag at fundamental frequency introduced by $G_{LPF}(j\omega_1)$ and $G_{PWM}(j\omega_1)$. The discrete-time implementation of the low-pass filter is

$$G_{LPF}(z) = K\frac{a_1 + a_2 z^{-1}}{b_1 + b_2 z^{-1}}. \quad (11)$$

Where $K = 0.1122$, $a_1 = a_2 = 1$, $b_1 = 1$, $b_2 = -0.7757$.

The lead compensator is designed with the form in (6), being $\tau_z = 1.8433 \times 10^{-4}$ and $\tau_p = 3.4354 \times 10^{-5}$. Subsequently the filter is discretized with the Tustin method in order to get the discrete-time implementation.

It can be stated that a simple P controller can be used in the current loop only if voltage decoupling is performed, even if this decoupling is not ideal. Thanks to the capacitor voltage decoupling, the controller tracks the fundamental component with fast transient response.

To verify the behavior of the inner current loop under overload, a step load change more than four times the rated load is performed. The load impedance changes from 68 Ω to 16 Ω while the current reference is kept constant. To keep the inductor current at the same level as before the load change, the output voltage (output of the inner current loop) decreases (see Fig. 17). This proves the controller is able to track any command provided by the outer voltage loop.

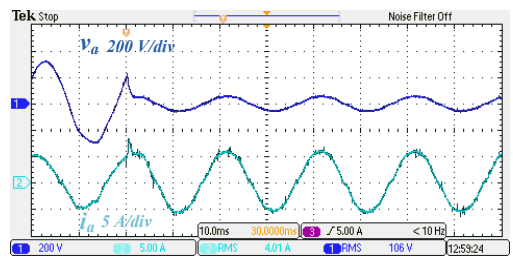
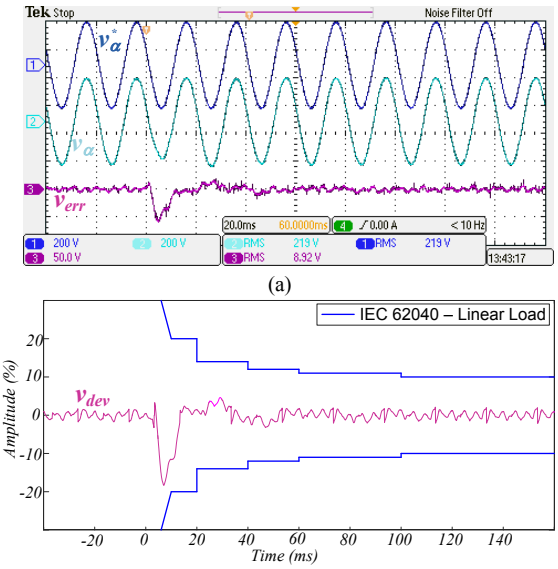


Fig. 17. Step load change (overload) from 68 Ω (rated load) to 16 ohm (4.25 times the rated load): capacitor voltage (output voltage) and inductor current in α-axis.

All the following results (Fig. 18, Fig. 19, and Fig. 20) regarding the voltage loop are obtained with voltage decoupling and a P controller as current regulator.

B. Voltage loop experimental tests

The performance of the proposed current control in combination with the PR voltage loop is analyzed in this section. It is verified that the proposed system solution fulfills the requirements associated to islanded systems. In Fig. 18(a) a 100% linear (resistive) step load change is shown. The results obtained are compared to the envelope of the voltage deviation for linear loads, as reported in the IEC 62040 standard for UPS systems [Fig. 18(b)]. This normative sets the dynamic characteristics of the output voltage for standardized linear and non-linear loads (diode bridge rectifiers with output capacitor). According to the sign of the reference and real capacitor voltage, their difference (voltage deviation v_{dev}) belongs to the under-voltage ($v_{dev} < 0$) or over-voltage ($v_{dev} > 0$) region. It should be noted that the capacitor voltage error can differ from v_{dev} depending on the sign of the reference and real voltage. The values are normalized to the peak voltage. It can be seen that the system reaches steady-state in less than half a cycle after the load step change. The dynamics response is well damped, as predicted by the design, and within the normative limits.

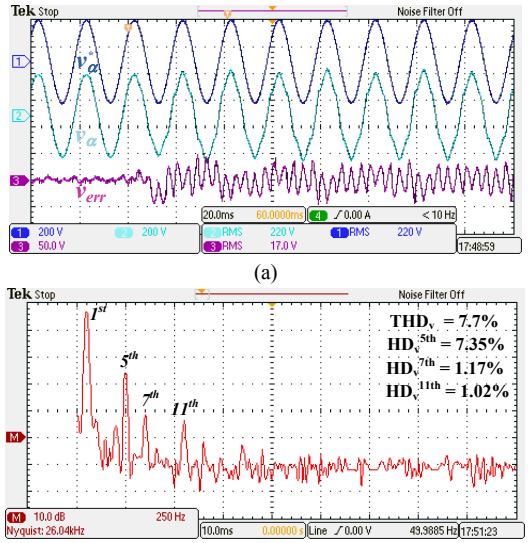


(a)

(b)

Fig. 18. Linear step load changing (0 – 100%): (a) reference (200 V/div), real (200 V/div), and capacitor voltage error (50 V/div) (α-axis); (b) Dynamic characteristics according to IEC 62040 standard for linear loads.

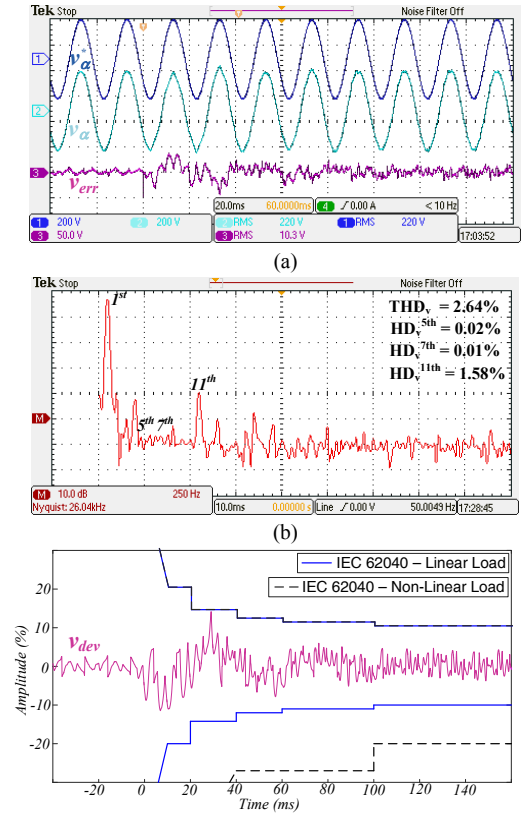
A diode bridge rectifier with capacitor output filter (parameters in Table I) is used as non-linear load. A 100% non-linear step load change is performed without and with harmonic compensators tuned at 5th and 7th harmonics [see Fig. 19(a) and Fig. 20(a)]. From the FFT analysis in Fig. 19(b) and Fig. 20(b) it can be seen the compensation of the harmonics to which the resonant controllers have been tuned. In Fig. 20(c) the results in terms of voltage deviations are compared with the standards set by IEC 62040. It should be noted the dynamic response is even within the limits imposed for linear loads.



(a)

(b)

Fig. 19. Voltage loop without HC and nonlinear load: (a) 100% Step load change, reference (200 V/div), real (200 V/div), and capacitor voltage error (50 V/div) (α-axis); (b) FFT of the capacitor voltage (250 Hz/div).



(a)

(b)

(c)

Fig. 20. Voltage loop with 5th 7th HC and non-linear load: (a) 100% Step load change, reference (200 V/div), real (200 V/div), and capacitor voltage error (50 V/div) (α-axis); (b) FFT of the capacitor voltage (250 Hz/div); (c) Dynamic characteristics according to IEC 62040 standard for linear and non-linear loads.

VI. Conclusions

The effect of state feedback coupling on the dynamics performance of current and voltage regulators for islanded microgrids has been investigated. The benefits of applying capacitor voltage decoupling are motivated by the higher damping of the system, and almost zero steady-state error when a P controller is used for the current loop. The computation and PWM delays are the main responsible to limit the bandwidth that can be achieved by the current regulator. Even if the system delays are not compensated on the decoupling path (non-ideal voltage decoupling), the system shows a higher damping than without decoupling. Further improvement can be obtained by introducing a lead-lag filter in the decoupling path.

A design methodology for PR voltage regulators based on a lead compensator structure is provided, according to the proposed inner current controller. Its effect is reflected in the Nyquist trajectories calculated for the voltage loop, and hence affects the selection of controller gains. A practical design methodology to select the minimum value of the fundamental resonant gain is proposed. The overall solution provides good performance both in steady-state and transients. More specifically, the requirements during transient imposed by the UPS standard IEC 62040 are verified according to the design proposed for the current and voltage regulators. The dynamic

response is even within the standards for linear load in case the 5th and 7th harmonic compensators are activated together with the fundamental gains, when a diode bridge rectifier is supplied.

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