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Small-Signal Modeling of the PVR-Based AD Scheme and Controller Design for Three-Phase Standalone DG System

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Abstract – This paper presents the small-signal state-space modeling and a new multifunctional multi-loop control strategy for three-phase inverter-based islanded DG systems under unbalanced and/or nonlinear load conditions. The proposed control methodology utilizes the parallel virtual resistance (PVR)-based active damping (AD) method for the islanded DG system using an extra feedback capacitor current shaping loop in the stationary reference frame to provide an AD to suppress the resonance-peak of the LC filter and improve both steady-state and transient performances, the inner voltage and current controllers are based on an enhanced proportional resonant (PR) structure to achieve zero steady-state error, and multi-resonant harmonic compensator (MRHC) plus PR controller to prevent low-order load current harmonics to distort the output voltage. The proposed small-signal model of the islanded DG system with multi-loop control strategy in the stationary reference frame is presented. Moreover, an enhanced delay compensation (EDC) scheme based on two integrators of the discrete PR controller is presented to improve stability margins with a higher accuracy compared with the existing methods. Then, a detailed systematic controller parameters design procedure is presented. Finally, simulation and experimental results are provided to validate the effectiveness of the proposed strategy.

Keywords: Active damping, Distributed generation, Small-signal model, Stand-alone mode, Voltage source inverter

1. Introduction

In recent years, decentralized distributed generation (DG) systems based on renewable energy, such as solar power plants or wind turbines, are attracting more and more attention for their environmental friendly characteristics [1], [2]. As an interface between the DG systems and the main grid or the local loads, voltage source inverters (VSIs) are the most commonly used topologies, which can operate in either grid-connected or standalone operation. According to the IEEE standard 1547.4 [3], the local loads should be supplied by the DG in islanded mode, which now acts as a controlled voltage source and the closed-loop control of pulse-width modulation (PWM) inverter with the output voltage compensation is used to achieve better performance [4].

In industrial applications, *LC* filters are usually used as an interface between the VSI and the local loads to effectively mitigate the harmonic contents of inverter output voltages. However, the resonances that arise among the reactive elements of the high-order filters may require a proper damping circuit to stabilize the DG system. Under the unknown output impedance condition, damping may be necessary to mitigate the oscillatory behavior and attenuate the filter resonance of the converter-based system connected to the local loads [5]. A direct way to damp the *LC* filter resonance is to insert an additional resistor in series or parallel with filter inductor or capacitor, which is simple to implement but results in power losses and decrease of the overall system efficiency [6]. The multi-loop control is more advantageous to improve the system stability and dynamic performance and actively damp the resonance oscillations. Several multi-loop control schemes with limited gain of the proportional-integral (PI) controllers at fundamental frequency are implemented in the stationary reference frame, resulting in a poor disturbance rejection capability and steady-state error [7-11]. It was shown in [5, 12] and [13] that the active damping (AD) using capacitor current feedback achieves better disturbance rejection capability than the inductor current feedback regardless of controller type in multi-loop control strategies. Moreover, the method of the capacitor current shaping loop to provide AD is simpler and more cost effective.

In addition, there might be a large number of unbalanced and nonlinear loads in three-phase islanded DG system due to the increasing use of power electronic loads. Therefore, the power quality of the islanded DG system can be

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deteriorated under unbalanced and nonlinear load conditions since it lacks the voltage and frequency support from the utility. Nevertheless, islanded DG system should be able to operate under unbalanced and/or nonlinear load conditions without any performance degradations [14]. Based on the IEEE standards 1159-2009 and 1547.4 [3, 15], the voltage unbalance factor (VUF) and the voltage total harmonic distortion (THD) for sensitive loads should be maintained below 2% and 5%, respectively. The parallel and/or series active power filters (APFs) are usually utilized to compensate voltage unbalance and harmonics in the distribution networks [16]. However, it is not practical to install pure APFs in small islanded DG system.

The possible solution is to adapt the control schemes of the interfacing VSIs in order to achieve the voltage unbalance and harmonics compensation. The repetitive control strategy has been proposed to reduce harmonic distortion of the output voltage with its excellent ability to eliminate disturbances. However, it shows poor performance under non-periodic disturbances, slow dynamics, and poor tracking accuracy, which limit the practical application of this technique [17, 18]. Moreover, the dead-beat, the sliding-mode, the adaptive and neural networks control strategies have also been proposed to regulate the standalone DG system. But many of these control strategies present some sort of shortcomings, for instance, complex design and hardware implementation, complexity in modeling, increased steady-state errors and sensitivity to system parameters and load conditions [19-23]. The proportional resonant (PR) controller can provide infinite gain at the selected resonant frequencies to suppress the effect of unwanted harmonics, ensuring zero steady-state error when tracking ac reference at selected frequencies, the controllers with a single PR structure are able to control both positive and negative sequence components at the same time [24-26].

In majority of the relevant literature, the various control strategies for standalone DG system have been investigated. A synchronous reference frame PI (SRFPI) controller with an inner capacitor current regulating loop is proposed to regulate the instantaneous output voltage of the single phase inverter in standalone mode in [5], which guarantees zero steady-state error at the fundamental frequency and improves system stability. The stability analysis and design of multiple control loops for a single phase inverter have been presented in [13], and the LC filter has been designed to reduce the PWM harmonics of the inverter and the active damping using closed-loop current control is designed and compared with passive damping. In [27], the multiple-feedback control loops of the output voltages and inductor currents are presented. However, this controller yields zero output impedance of the uninterrupted power supply (UPS), provided that estimated filter parameters match their actual values. Controlling the charging and discharging of the capacitor connected across the load for single phase inverter is used in [28], but the output voltages and currents contain distortion and have steady-state error. Moreover, inverters are sometimes modelled in the state-space model with the power devices in the inverter, which is represented as ideal switches. Under this assumption, some accuracy is lost but the simulation time is normally reduced [29, 30]. A common simplification is to consider the average behavior of the switched circuit over a period and to linearize the switching circuit by creating a small-signal model. The small-signal model of standalone DG system in the stationary reference frame is still needed for modeling.

In this paper, a new multifunctional multi-loop control strategy with parallel virtual resistance (PVR)-based AD method for three-phase islanded DG system is proposed to regulate the instantaneous output voltage and improve steady-state and transient performance. The main contributions of this paper are summarized as follows:

1) Development of a multi-loop structure with PVR-based AD scheme for three-phase islanded DG system to damp the resonance and mitigate the oscillatory behavior.
2) The detailed small-signal state-space model of the main circuit and control scheme with the PR regulator of the three-phase standalone DG system in the stationary reference frame is proposed to assess the features of the whole DG system.
3) A multi-resonant harmonic compensator (MRHC) based on the enhanced delay compensation (EDC) scheme for the main voltage-harmonic orders is adopted to gain higher accuracy, which prevents the low-order load current harmonics to distort the VSI output voltages, especially under nonlinear and/or unbalanced load conditions.

The rest of this paper is outlined as follows. The principle and small-signal analysis of the proposed control strategy are presented in Section II. The selective harmonic compensation control strategy is presented in Section III. Simulation and experimental results of a 2.2 kVA three-phase inverter system are presented to verify the validity of the proposed approach in Section IV. Finally, Section V concludes this paper.

2. Principle and Small-Signal Analysis of the Proposed Control Strategy

The power stage of a three-phase DG system consisting of a three-phase PWM inverter and an *LCL* filter is presented in Fig. 1. In some previous works, the *LCL* output filter was model as a whole third order system, but this is not the case in the standalone DG system, in which the capacitor voltage, inverter current and capacitor current are controlled, thus it can be seen as an *LC* filter plus an additional L_o [5, 7]. Transition between the grid-connected

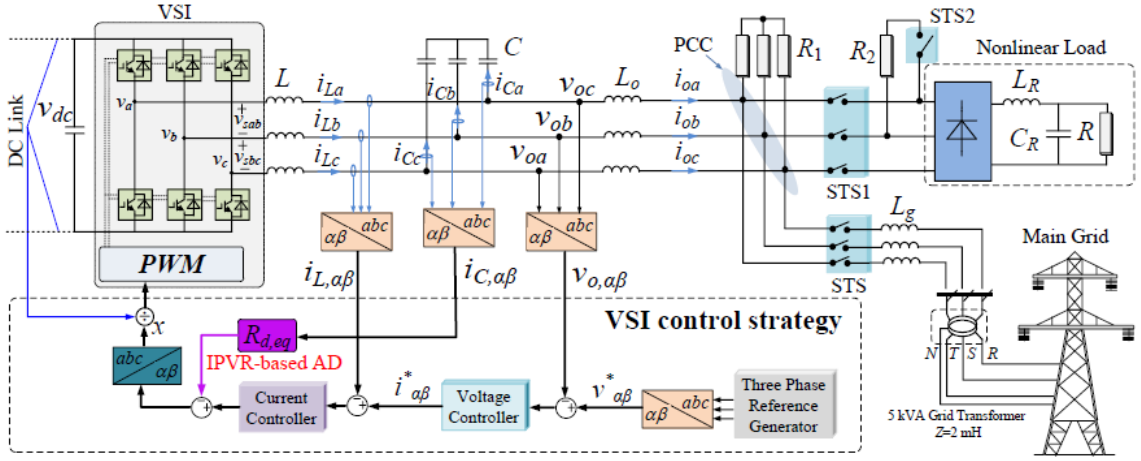


Fig. 1. Power stage of a three-phase DG system.

mode and stand-alone mode is realized through the static transfer switch (STS) while only the islanded mode operation is considered in this paper. In addition, different load conditions, e.g., unbalance loads and nonlinear loads are switched on or off by STS1 and STS2.

2.1 Proposed PVR-base AD and controller parameters design for the islanded DG system

In general, the passive damping method usually inserts an additional resistor in series or parallel with the filter capacitor or inductor, and it has been widely adopted for its simplicity. Considering the transition between grid-connected mode and stand-alone mode of this DG system, the less attenuation is caused in the low frequency (LF) region and high frequency (HF) region in the grid-connected DG system when a series and/or parallel resistor is connected with L, respectively. Moreover, the less attenuation is also caused in the grid-connected DG system when a series resistor is connected with filter capacitor C and there is no impact on the LF and HF regions when a parallel resistor is connected with C.

Therefore, the passive damping of the capacitor (C) connected in parallel with resistor (R_d) can be chosen to damp the resonance and mitigate the oscillatory behavior between the grid-connected and standalone mode, and the diagram of the standalone mode of the DG control system is depicted in Fig. 2. To avoid the inconvenient decoupling, the three-phase system can be modeled in two independent single-phase systems by the $abc/\alpha\beta$ coordinates transformation principle. As shown in Fig. 2, the transfer function from $v_{o,\alpha\beta}$ to $v_{r,\alpha\beta}$ can be expressed as

$$G_r(s)=\frac{v_{o,\alpha\beta}(s)}{v_{r,\alpha\beta}(s)}=\frac{R_d}{LCR_d s^2+Ls+R_d} \tag{1}$$

However, an excessive power loss is inevitable by using this approach and other passive damping methods.

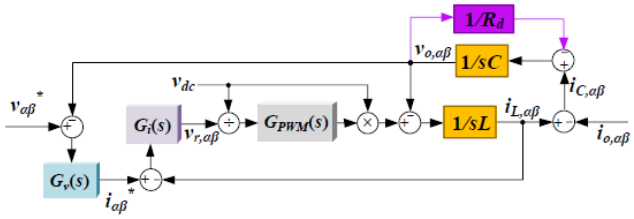


Fig. 2. Passive damping of output filter using parallel resistor across capacitor.

In order to overcome the drawbacks resulted from the passive damping methods, the active damping method of a virtual resistor in parallel with the LC-filter capacitor that uses control algorithms instead of a real resistor is proposed, which is applied to the islanding mode to reject the resonance and realize a good robustness. After an approximate equivalent transformation to the damping resistance branch in Fig. 2 is achieved, it can be equivalently transformed to Fig. 3 and $R_{d,eq}=L/(CR_d)$, which represents the value of the PVR-based AD scheme. Therefore, the transfer function from $v_{o,\alpha\beta}$ to $v_{r,\alpha\beta}$ can be expressed as

$$G_{eq-r}(s)=\frac{v_{o,\alpha\beta}(s)}{v_{r,\alpha\beta}(s)}=\frac{1}{LCs^2+CR_{d,eq}s+1} \tag{2}$$

As shown in Fig. 3, the block diagram of the proposed multifunction control system with the PVR-based AD scheme in the islanded DG system is implemented in the stationary reference frame. The error signals obtained by comparing the measured output voltage and the generated voltage references value in the stationary reference frame are regulated by the PR controller and/or MRHC to generate references for the current loop. The reference current signals are then compared with the corresponding inverter currents, and are regulated by the PR controller to produce voltage commands. Moreover, an inner active damping loop is adopted to ensure the effective damping of

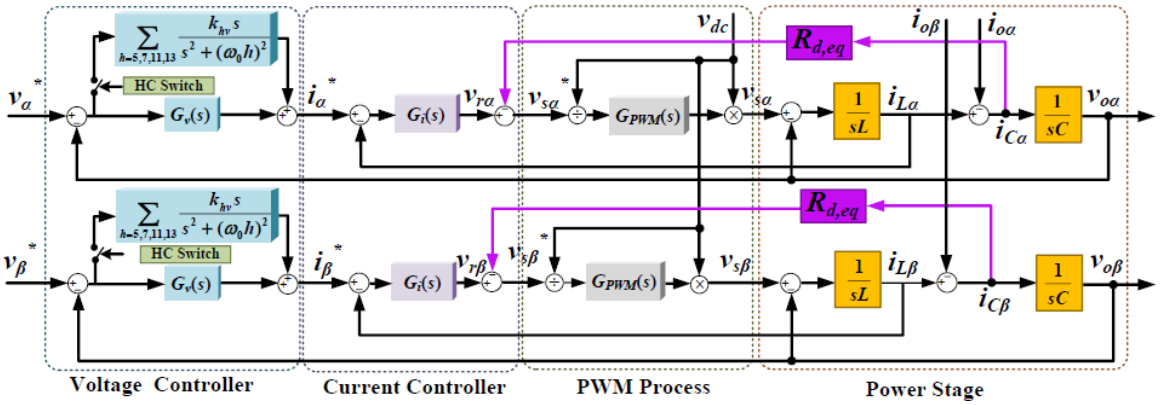


Fig. 3. Structure of proposed control system including voltage and current controllers, harmonic compensation, and PVR-based AD scheme.

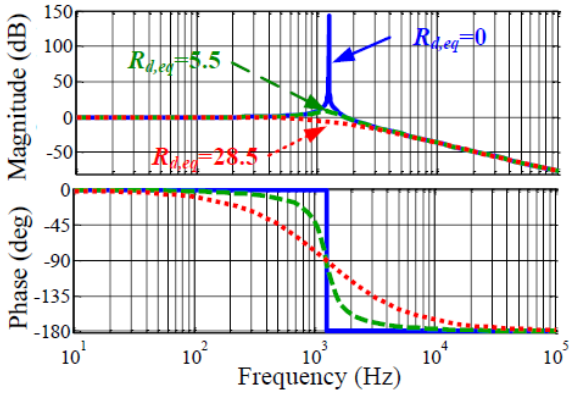


Fig. 4. Bode diagram of virtual resistance compared with *LCL* filter.

the resonance associated with the output LC filter.

The aim of the virtual resistance is to attenuate the resonance peak of the *LC* filter. And now, how to determine the value of $R_{d,\mathrm{eq}}$ is considered. According to (2), it is a second order plant model, which results in a resonance peak [31]. In addition, according to the control theory, the resonance of the second order plant is determined by the damping factor ξ. To eliminate the resonance, let ξ=0.707, thus the value of $R_{d,\mathrm{eq}}$ is set to 28.5. The bode diagram of the system with and without using the virtual resistance are clearly shown in Fig. 4.

Assuming that the nominal load impedance is Z_o, then in the block diagram of Fig. 3, i_o=v_o/Z_o can be replaced. In Fig. 3, $G_{PWM}(s)$ represents the PWM transfer function, which is usually modeled as a delay element [5]. Consequently, the transfer functions of the output voltage and PWM process can be derived as

$$v_{o,\alpha\beta}(s)=\frac{G_v(s)G_i(s)G_{PWM}(s)Z_o v^*_{\alpha\beta}}{LCZ_o s^2+ps+G_i(s)G_{PWM}(s)(1+G_v(s)Z_o)+Z_o}-\frac{Ls+G_i(s)G_{PWM}(s)}{LCs^2+qG_i(s)G_{PWM}(s)+1}i_{o,\alpha\beta}(s) \quad (3)$$

$$G_{PWM}(s)=\frac{1}{1+1.5T_s s} \quad (4)$$

where $v^*_{\alpha\beta}$, $i_{o,\alpha\beta}$, and T_s are respectively the reference voltage, output current and sampling time in the $\alpha\beta$ reference frame, and p=L+$CZ_oR_{d,\mathrm{eq}}$+$CG_i(s)G_{PWM}(s)Z_o$, q=$(R_{d,\mathrm{eq}}+1)Cs$+$G_v(s)$.

As shown in Fig. 3, the proposed control strategy is based on the stationary reference frame, including voltage and current control loops. Since there is a significant advantage in the implementation of PR controllers in a stationary reference frame compared to the use of PI controllers working in a *dq* synchronous reference frame, a PR structure is used in voltage and current controllers [24], [26]. Therefore, under linear and balanced load conditions, the transfer function of the voltage and current controllers are described as follows

$$G_v(s)=k_{pv}+\frac{k_{rv}s}{s^2+h^2\omega_0^2},\quad G_i(s)=k_{pi}+\frac{k_{ri}s}{s^2+h^2\omega_0^2} \quad (5)$$

where k_{pv} and k_{pi} are the proportional term coefficients, k_{rv} and k_{ri} are the resonant term coefficients at ω_0 =2πf_0, and h=1.

The proportional gain and resonant gain of the PR compensator are set such that the damping factor of the dominant poles of the inner current loop system becomes 0.707. In this case and using the control system parameters in Table 1, the proportional and resonant gains are set to be 3 and 50, respectively.

According to (3), the closed-loop transfer function of the islanded DG system can be written as

$$H(s)=\frac{v_{o,\alpha\beta}}{v^*_{\alpha\beta}}=\frac{b_4s^4+b_3s^3+b_2s^2+b_1s+b_0}{a_6s^6+a_5s^5+a_4s^4+a_3s^3+a_2s^2+a_1s+a_0} \quad (6)$$

where the parameters a_0~a_6 and b_0~b_4 are defined as

$$\begin{cases} a_0 = (Z_o + k_{pi} + Z_o k_{pi} k_{pv})\omega_0^4 \\ a_1 = (L\omega_0^2 + k_{ri} + CZ_o R_{d,eq}\omega_0^2 + CZ_o k_{pi}\omega_0^2 + Z_o k_{pv} k_{ri} + Z_o k_{pi} k_{rv})\omega_0^2 \\ a_2 = (2Z_o + 2k_{pi} + CZ_o k_{ri} + 2Z_o k_{pi} k_{pv} + CLZ_o\omega_0^2)\omega_0^2 + Z_o k_{ri} k_{rv} \\ a_3 = k_{ri} + 2L\omega_0^2 + Z_o k_{pi} k_{rv} + Z_o k_{pv} k_{ri} + 2CZ_o\omega_0^2 (k_{pi} + R_{d,eq}) \\ a_4 = 2CLZ_o\omega_0^2 + Z_o + k_{pi} + CZ_o k_{ri} + Z_o k_{pi} k_{pv} \\ a_5 = L + CZ_o R_{d,eq} + CZ_o k_{pi} \\ a_6 = CLZ_o \end{cases}$$

$$\begin{cases} b_0 = Z_o k_{pi} k_{pv}\omega_0^4 \\ b_1 = Z_o\omega_0^2 (k_{pi} k_{rv} + k_{pv} k_{ri}) \\ b_2 = Z_o (2k_{pi} k_{pv}\omega_0^2 + k_{ri} k_{rv}) \\ b_3 = Z_o (k_{pi} k_{rv} + k_{pv} k_{ri}) \\ b_4 = Z_o k_{pi} k_{pv} \end{cases} \tag{7}$$

From (6), the characteristic equation of the closed-loop transfer function can be obtained as

$$a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0 = 0 \tag{8}$$

By applying the Routh-Hurwitz stability criterion to (8), considering the aforementioned design procedure and employing the parameters in Table 1, the values of k_{pv}, k_{rv} are designed to be 0.175 and 200, respectively.

Table 1. Control system parameters

Symbol	Quantity	Value
v_g	grid voltage	311 V
f	grid frequency	50 Hz
L_o	output inductance	1.8 mH
L	filter inductance	1.8 mH
C	filter capacitance	9μF
v_{dc}	dc-link voltage	650 V
f_s	switching frequency	10 kHz
R_1	balanced resistive load	230 Ω
R_2	unbalanced load	460 Ω
L_R, C_R, R	nonlinear load	84μH, 235μF, 230Ω

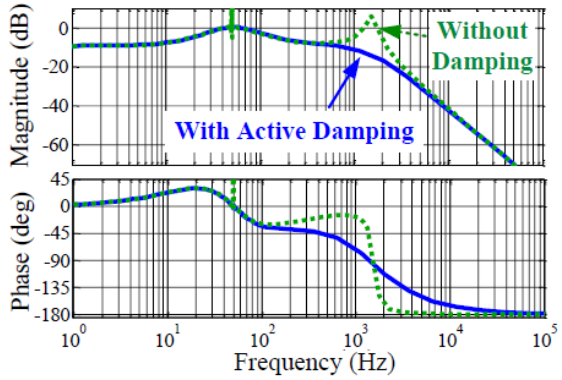


Fig. 5. Bode plots of closed-loop system under linear load conditions with and without PVR-based AD strategy.

The Bode plots of $H(s)$ under nominal load for the proposed PVR-based AD control method and conventional control method are shown in Fig. 5. It can be observed that the PVR-based AD strategy ensures effective damping for the resonance peaks, ensuring a sufficient stability margin.

2.2 Small-signal model of the islanded DG system

In this section, a small-signal model is presented for the proposed control strategy of the subsystems: the inner voltage and current controllers with the PVR-based AD scheme, output filter and load model [30].

2.2.1 Voltage Controller:

As shown in Fig. 6(a), output voltage control of the voltage controller block diagram is achieved with a PR controller. The state variable (Φ) and the corresponding state equations can be expressed as

$$\frac{d\Phi_\alpha}{dt} = v_\alpha^* - v_{o\alpha}, \quad \frac{d\Phi_\beta}{dt} = v_\beta^* - v_{o\beta} \tag{9}$$

Then, the algebraic equations can be derived as

$$i_\alpha^* = k_{pv}(v_\alpha^* - v_{o\alpha}) + \frac{k_{rv} s^2}{s^2 + \omega_0^2}\Phi_\alpha \tag{10}$$

$$i_\beta^* = k_{pv}(v_\beta^* - v_{o\beta}) + \frac{k_{rv} s^2}{s^2 + \omega_0^2}\Phi_\beta \tag{11}$$

By linearizing the state-space form of the voltage controller, the reference input and the feedback input can be obtained as

$$\begin{bmatrix} \Delta\dot{\Phi}_{\alpha\beta} \end{bmatrix} = [0]\begin{bmatrix} \Delta\Phi_{\alpha\beta} \end{bmatrix} + \mathbf{A_{v1}}\begin{bmatrix} \Delta v_{\alpha\beta}^* \end{bmatrix} + \mathbf{A_{v2}}\begin{bmatrix} \Delta i_{L\alpha\beta} \\ \Delta v_{o\alpha\beta} \\ \Delta i_{C\alpha\beta} \end{bmatrix} \tag{12}$$

were

$$\begin{bmatrix} \Delta\Phi_{\alpha\beta} \end{bmatrix} = \begin{bmatrix} \Delta\Phi_\alpha & \Delta\Phi_\beta \end{bmatrix}^T \tag{13}$$

$$\mathbf{A_{v1}} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \quad \mathbf{A_{v2}} = \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \tag{14}$$

And $\Delta i_{\alpha\beta}^*$ is defined as

$$\begin{bmatrix} \Delta i_{\alpha\beta}^* \end{bmatrix} = \mathbf{B_v}\begin{bmatrix} \Delta\Phi_{\alpha\beta} \end{bmatrix} + \mathbf{C_{v1}}\begin{bmatrix} \Delta v_{\alpha\beta}^* \end{bmatrix} + \mathbf{C_{v2}}\begin{bmatrix} \Delta i_{L\alpha\beta} \\ \Delta v_{o\alpha\beta} \\ \Delta i_{C\alpha\beta} \end{bmatrix} \tag{15}$$

where

$$\mathbf{B_v}=\begin{bmatrix} k_{rv}s^2/(s^2+\omega_0^2) & 0 \\ 0 & k_{rv}s^2/(s^2+\omega_0^2) \end{bmatrix},$$
$$\mathbf{C_{v1}}=\begin{bmatrix} k_{pv} & 0 \\ 0 & k_{pv} \end{bmatrix}, \mathbf{C_{v2}}=\begin{bmatrix} 0 & 0 & -k_{pv} & 0 & 0 & 0 \\ 0 & 0 & 0 & -k_{pv} & 0 & 0 \end{bmatrix}. \quad (16)$$

2.2.2 Current Controller:

As shown in Fig. 6(b), the current control structure is also achieved with a PR controller. Θ represents the state variable and the state equations are

$$\frac{d\Theta_\alpha}{dt}=i_\alpha^*-i_{L\alpha}, \quad \frac{d\Theta_\beta}{dt}=i_\beta^*-i_{L\beta} \quad (17)$$

Then, the algebraic equations can be derived as

$$v_{s\alpha}^*=k_{pi}(i_\alpha^*-i_{L\alpha})+\frac{k_{ri}s^2}{s^2+\omega_0^2}\Theta_\alpha-R_{d,eq}i_{C\alpha} \quad (18)$$

$$v_{s\beta}^*=k_{pi}(i_\beta^*-i_{L\beta})+\frac{k_{ri}s^2}{s^2+\omega_0^2}\Theta_\beta-R_{d,eq}i_{C\beta} \quad (19)$$

The linearized state-space form of the current controller can be derived as

$$\begin{bmatrix}\dot{\Delta\Theta}_{\alpha\beta}\end{bmatrix}=[0]\begin{bmatrix}\Delta\Theta_{\alpha\beta}\end{bmatrix}+\mathbf{A_{i1}}\begin{bmatrix}\Delta i_{\alpha\beta}^*\end{bmatrix}+\mathbf{A_{i2}}\begin{bmatrix}\Delta i_{L\alpha\beta}\\ \Delta v_{o\alpha\beta}\\ \Delta i_{C\alpha\beta}\end{bmatrix} \quad (20)$$

where

$$\begin{bmatrix}\Delta\Theta_{\alpha\beta}\end{bmatrix}=\begin{bmatrix}\Delta\Theta_\alpha & \Delta\Theta_\beta\end{bmatrix}^T \quad (21)$$

$$\mathbf{A_{i1}}=\begin{bmatrix}1&0\\0&1\end{bmatrix}, \quad \mathbf{A_{i2}}=\begin{bmatrix}-1&0&0&0&0&0\\0&-1&0&0&0&0\end{bmatrix} \quad (22)$$

And $\Delta v_{s\alpha\beta}^*$ is defined as

$$\begin{bmatrix}\Delta v_{s\alpha\beta}^*\end{bmatrix}=B_i\begin{bmatrix}\Delta\Theta_{\alpha\beta}\end{bmatrix}+\mathbf{C_{i1}}\begin{bmatrix}\Delta i_{\alpha\beta}^*\end{bmatrix}+\mathbf{C_{i2}}\begin{bmatrix}\Delta i_{L\alpha\beta}\\ \Delta v_{o\alpha\beta}\\ \Delta i_{C\alpha\beta}\end{bmatrix} \quad (23)$$

where

$$\mathbf{B_i}=\begin{bmatrix} k_{ri}s^2/(s^2+\omega_0^2) & 0 \\ 0 & k_{ri}s^2/(s^2+\omega_0^2) \end{bmatrix},$$
$$\mathbf{C_{i1}}=\begin{bmatrix} k_{pi} & 0 \\ 0 & k_{pi} \end{bmatrix}, \mathbf{C_{i2}}=\begin{bmatrix} -k_{pi} & 0 & 0 & 0 & -R_{d,eq} & 0 \\ 0 & -k_{pi} & 0 & 0 & 0 & -R_{d,eq} \end{bmatrix}. \quad (24)$$

2.2.3 Output LC filter

By using *Kirchhoff's Voltage Law* and *Kirchhoff's Current Law* [2], the *LC* output filter shown in Fig.1 yields the following differential equations

$$\begin{cases}\mathbf{T}_L\dfrac{d\mathbf{I}_L}{dt}=\dfrac{1}{L}\mathbf{U}_s-\dfrac{1}{L}\mathbf{T}_L\mathbf{V}_o\\ C\dfrac{d\mathbf{V}_o}{dt}=\mathbf{I}_C=\mathbf{I}_L-\mathbf{I}_o\end{cases}, \quad \mathbf{T}_L=\begin{bmatrix}1&-1&0\\0&1&-1\\-1&0&1\end{bmatrix} \quad (25)$$

where $\boldsymbol{U}_s=[u_{sab}, u_{sbc}, u_{sca}]^T$ is the inverter output line to line voltage vector, $\boldsymbol{I}_L=[i_{La}, i_{Lb}, i_{Lc}]^T$ is the inverter phase current vector, $\boldsymbol{I}_o=[i_{oa}, i_{ob}, i_{oc}]^T$ is the load phase current vector, $\boldsymbol{I}_C=[i_{Ca}, i_{Cb}, i_{Cc}]^T$ is the capacitor phase current vector, $\boldsymbol{V}_o=[v_{oa}, u_{ob}, u_{oc}]^T$ is the load line to neutral voltage vector.

Thus, the state space equation of the system in $\alpha\beta$ frame is obtained as follows

$$\begin{bmatrix}\dot{\Delta i}_{L\alpha\beta}\\ \Delta v_{o\alpha\beta}\\ \Delta i_{C\alpha\beta}\end{bmatrix}=\mathbf{A_{LC}}\begin{bmatrix}\Delta i_{L\alpha\beta}\\ \Delta v_{o\alpha\beta}\\ \Delta i_{C\alpha\beta}\end{bmatrix}+\mathbf{B_{LC}}\begin{bmatrix}\Delta v_{s\alpha\beta}\end{bmatrix}+\mathbf{C_{LC}}\begin{bmatrix}\Delta i_{o\alpha\beta}\end{bmatrix} \quad (26)$$

where

$$\mathbf{A_{LC}}=\begin{bmatrix}1/C&0&0&0&0&0\\0&1/C&0&0&0&0\\0&0&-1/L&0&0&0\\0&0&0&-1/L&0&0\\C&0&0&0&0&0\\0&C&0&0&0&0\end{bmatrix},$$
$$\mathbf{B_{LC}}=\begin{bmatrix}1/L&0\\0&1/L\\0&0\\0&0\\0&0\\0&0\end{bmatrix}, \quad \mathbf{C_{LC}}=\begin{bmatrix}0&0\\0&0\\-1/C&0\\0&-1/C\\0&0\\0&0\end{bmatrix}. \quad (27)$$

2.2.4 Complete Model of the VSI System:

A complete small-signal model of the DG system can be obtained by combining small-signal models of the voltage and current controllers, output *LC* filter, given by (12), (15), (20), (23), and (26). The state variable Ψ and complete model of the VSI can be obtained as

$$\begin{bmatrix}\dot{\Delta\Psi}_{inv}\end{bmatrix}=\mathbf{A_{INV}}\begin{bmatrix}\Delta\Psi_{inv}\end{bmatrix}+\mathbf{B_{INV}}\begin{bmatrix}\Delta i_{o\alpha\beta}\end{bmatrix} \quad (28)$$

$$\begin{bmatrix}\Delta i_{o\alpha\beta}\end{bmatrix}=\mathbf{C_{INV}}\begin{bmatrix}\Delta\Psi_{inv}\end{bmatrix} \quad (29)$$

where

$$\left[\Delta\Psi_{inv}\right]=\left[\Delta\Phi_{\alpha\beta}\ \ \Delta\Theta_{\alpha\beta}\ \ \Delta i_{L\alpha\beta}\ \ \Delta v_{o\alpha\beta}\ \ \Delta i_{C\alpha\beta}\ \ \Delta i_{o\alpha\beta}\right]^T \quad (30)$$

$$\mathbf{A_{INV}}=\begin{bmatrix}\mathbf{0} & \mathbf{0} & \mathbf{A_{v2}} & \mathbf{0}\\ \mathbf{A_{i1}B_v} & \mathbf{0} & \mathbf{A_{i1}C_{V2}+A_{i2}} & \mathbf{0}\\ \mathbf{B_{LC}C_{i1}B_v} & \mathbf{B_{LC}B_i} & \mathbf{A_{LC}+B_{LC}(C_{i1}C_{v2}+C_{i2})} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0}\end{bmatrix}_{12\times12} \quad (31)$$

$$\mathbf{B_{INV}}=\begin{bmatrix}\mathbf{0}\\ \mathbf{0}\\ \mathbf{0}\\ \mathbf{C_{LC}}\end{bmatrix}_{12\times2} \quad (32)$$

$$\mathbf{C_{INV}}=\begin{bmatrix}\mathbf{0}\ \mathbf{0}\ \mathbf{0}\ \mathbf{0}\ \mathbf{0}\ \mathbf{I}\end{bmatrix}_{2\times12} \quad (33)$$

2.2.5 Load Model:

A general RL load is considered in this paper. The state equations of the RL load connected at the node are

$$\frac{di_{load\alpha}}{dt}=-\frac{R_{load}}{L_{load}}i_{load\alpha}+\frac{1}{L_{load}}v_{o\alpha} \quad (34)$$

$$\frac{di_{load\beta}}{dt}=-\frac{R_{load}}{L_{load}}i_{load\beta}+\frac{1}{L_{load}}v_{o\beta} \quad (35)$$

Hence, the small-signal state-space model of load is given by

$$\left[\Delta\dot{i}_{load\alpha\beta}\right]=\mathbf{A_{load}}\left[\Delta i_{load\alpha\beta}\right]+\mathbf{B_{load}}\left[\Delta v_{o\alpha\beta}\right] \quad (36)$$

Where

$$\mathbf{A_{load}}=\begin{bmatrix}-\frac{R_{load}}{L_{load}} & 0\\ 0 & -\frac{R_{load}}{L_{load}}\end{bmatrix},\quad \mathbf{B_{load}}=\begin{bmatrix}\frac{1}{L_{load}} & 0\\ 0 & \frac{1}{L_{load}}\end{bmatrix}. \quad (37)$$

2.2.6 Complete model of the whole DG system:

Now, the complete VSI system small-signal state-space model and hence the system state matrix [as given in (38)] can be obtained by using the models given by (28), (29), and (36).

$$\begin{bmatrix}\Delta\dot{\Psi}_{inv}\\ \Delta i_{load\alpha\beta}\end{bmatrix}=\mathbf{A_{sys}}\begin{bmatrix}\Delta\Psi_{inv}\\ \Delta i_{load\alpha\beta}\end{bmatrix} \quad (38)$$

where

$$\mathbf{A_{sys}}=\begin{bmatrix}\mathbf{A_{INV}+B_{INV}C_{INV}} & \mathbf{0}\\ \begin{bmatrix}\mathbf{0}\ \mathbf{0}\ \mathbf{0}\ \mathbf{B_{load}}\ \mathbf{0}\ \mathbf{0}\end{bmatrix} & \mathbf{A_{load}}\end{bmatrix}_{14\times14} \quad (39)$$

Substituting parameters of Table 1, the voltage and current controllers and the active damping value to the matrix $\mathbf{A_{sys}}$, and the eigenvalues of the matrix $\mathbf{A_{sys}}$ defined by (39) are calculated as

$\lambda_1=\lambda_2=-3.537\times10^4$, $\lambda_3=\lambda_4=-1$, $\lambda_5=\lambda_6=-56$, $\lambda_6=\lambda_8=-556$, $\lambda_9=\lambda_{10}=\lambda_{11}=\lambda_{12}=\lambda_{13}=\lambda_{14}=0$.

Note that all the non-zero poles of the matrix $\mathbf{A_{sys}}$ are real and the DG system is over-damped and stable [32].

3. Selective Harmonic Compensation

The selective harmonic compensation is performed by placing resonant peaks at the dominant frequencies for compensation. It can be implemented in the stationary or synchronous frame. For the former, the MRHC is commonly used. As shown in the standalone DG system of Fig. 1, the voltage controller should take the dominant harmonic components of the load currents (i.e. 5th, 7th, 11th, and 13th) into consideration under nonlinear and/or unbalanced load conditions. And the voltage controller with the MRHC plus PR is described as follows

$$G_v(s)=k_{pv}+\frac{k_{rv}s}{s^2+\omega_0^2}+\sum_{h=5,7,11,13}\frac{k_{hv}s}{s^2+(\omega_0 h)^2} \quad (40)$$

where k_{hv} represents the resonant coefficient terms for h-order harmonic.

Fig. 7 shows the Bode diagram of the closed-loop system transfer function under nonlinear and/or unbalanced load conditions with the PVR-based AD strategy. As it can be seen, the gain and the phase angle of the closed-loop transfer function are respectively unity (0 dB) and zero degrees at the fundamental frequency and at 5th, 7th, 11th, and 13th harmonic frequencies, which means the system obtains the zero-error tracking capability at the fundamental frequency and the typical voltage harmonic frequencies as well.

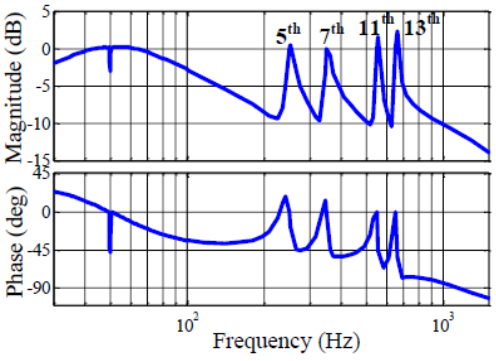


Fig. 7. Bode diagram of closed-loop system under nonlinear and unbalanced load conditions with PVR-based AD strategy.

However, the system delay (mainly due to PWM generation process, computation, and the hardware filtering) affects the system performance and may cause instability [33-35]. In order to compensate the system delay, a phase lead angle φ_h^* may be introduced in the vicinity of the resonant frequency $h\omega_0$ of a PR controller. And the delay compensation in PR controllers which is expressed in the s-domain can be obtained as [33]

$$G_{PRh}(s) = k_{ph} + \sum_{h=1,5,7,11,13} k_{rh} \frac{s\cos(\varphi_h^*) - h\omega_0 \sin(\varphi_h^*)}{s^2 + h^2\omega_0^2} \quad (41)$$

where k_{ph} and k_{rh} are the proportional and resonant gains at the selective harmonics, respectively, φ_h^* is the compensation phase lead angle, i.e., the desired φ_h value, h is the harmonic order. In the continuous domain, φ_h=φ_h^* is assumed in $G_{PRh}(s)$.

3.1 Discretization of PR controllers based on the two integrators

In order to implement the delay compensation scheme in (41), the forward integrator of the resonant part is discretized by a pure forward differentiator, i.e., $s = (z\text{-}1)/T_s$, and the feedback integrator is discretized by pure backward differentiator, i.e., $s = (1\text{-}z^{-1})/T_s$. Thus, the transfer function can be expressed as

$$G_{PRh}(z) = k_{ph} + \sum_{h=1,5,7,11,13} k_{rh}T_s \frac{z^{-1}\left[\cos(\varphi_h^*) - h\omega_0 T_s \sin(\varphi_h^*)\right] - z^{-2}\cos(\varphi_h^*)}{1 - 2z^{-1}(1 - h^2\omega_0^2 T_s^2/2) + z^{-2}} \quad (42)$$

However, the discretization process of the transfer function (42) generally causes the inaccuracies since it does not provide infinite gain at the desired frequency $h\omega_0$, so a significant error may appear in the steady-state. Moreover, (42) provides a phase lead angle different from the reference, i.e., $\varphi_h \neq \varphi_h^*$, so stability margins and dynamic performance are deteriorated. In fact, this discrepancy is dependent on combination of T_s and $h\omega_0$, leading to a big and random uncertainty [34, 35].

In order to avoid uncertainties that could lead to an unstable system or a poor performance, it is preferable to seek for an alternative method to perform the delay compensation [36]. Fig. 8 shows an enhanced delay compensation (EDC) based on PR controller, which is expressed as

$$G_{PRh}^{enh}(z) = k_{ph} + \sum_{h=1,5,7,11,13} k_{rh}T_s \frac{\cos(\varphi_h^*) - z^{-1}\cos(\varphi_h^* - h\omega_0 T_s)}{1 - 2z^{-1}\cos(h\omega_0 T_s) + z^{-2}} \quad (43)$$

The enhanced PR controller with added features for gaining better accuracy is shown in Fig. 8. The first feature is to modify the phase lead input φ_h^* so that accurate zeros can be obtained. The second added of (43) is multiplied by an additional z^{-1} term, and φ_h^* is added to the phase that corresponds to one sample delay at the resonant frequency ($h\omega_0 T_s$). In this manner, the delay introduced by the z^{-1} term is compensated by the increase in the leading angle, and the resulting φ_h is equal to that of (43). The phase lead angle φ_h^* needed for the PR controllers can be approximated as [36]

$$\varphi_h^* = \frac{\pi}{2} + \frac{3}{2}h\omega_0 T_s \quad (44)$$

For evaluating robustness subject to wide $R_{d,eq}$ variation ($R_{d,eq}$=1, 2, 4, 8, 16, 28.5, 50 and 100), the z-domain root loci analysis is illustrated in Fig. 9 by using the ZOH method, where $G_v(s)$ and $G_i(s)$ are discretized with the EDC scheme based on two integrators which is shown in (43). As shown in Fig. 9, either too small or too large $R_{d,eq}$ will affect the stability of the system and the poles mostly stay within the unit circle when $R_{d,eq}$ is appropriate. A compromise between stability and dynamic performance is achieved by choosing $R_{d,eq}$=28.5.

3.2 Harmonic impedance

Harmonic impedance is an effective criterion to assess the effect of harmonic load currents on the output voltage

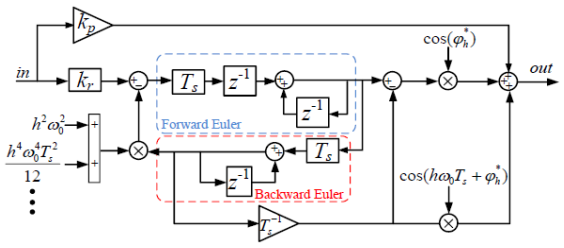


Fig. 8. Block diagram of an EDC based on PR controller.

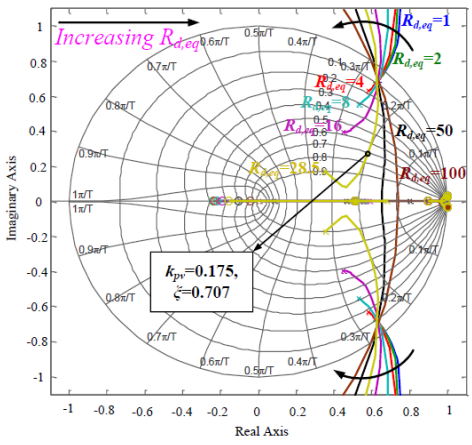


Fig. 9. Root loci of the IPVR-based AD control scheme with different $R_{d,eq}$.

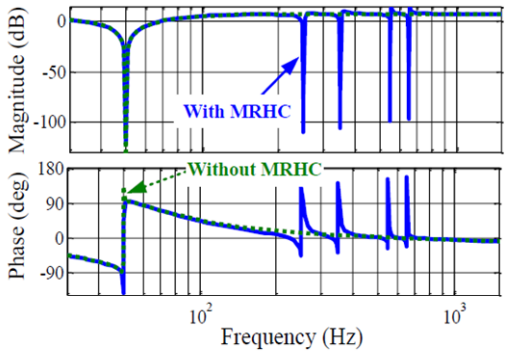


Fig. 10. Bode plots of the output impedance with and without the MRHC of the closed-loop islanded DG system.

distortion. To limit the voltage distortion caused by harmonic currents, the harmonic impedance should be ideally zero. The output impedance transfer function of the islanded mode in stationary frame is defined as

$$Z_{out}(s) = -\frac{v_o(s)}{i_o(s)}\bigg|_{v^*(s)=0} \tag{45}$$

where i_o and v_o are the output current and voltage of the islanded system in stationary frame, respectively.

The attenuation at high-amplitude low-order harmonics may not be adequate, especially under highly distorted load conditions. In order to overcome this problem, a MRHC can be added to the suggested control scheme as depicted in Fig. 3 and the harmonic compensation (HC) switch is switched on.

To better visualize the effect of the added MRHC, the Bode plots of Z_{out} for the inverter at a specific harmonic frequency with and without using the harmonic compensator are compared in Fig. 10. Note that the output impedance is calculated for the closed-loop system according to Fig. 3 and (45). As shown in Fig. 10, the solid line indicates the output impedance with the harmonic compensator, including four modules tuned at the 5th, 7th, 11th, and 13th harmonic frequencies, since they are the most dominant components in the load current. The dashed line indicates the output impedance without using the harmonic compensator. It can be observed that the harmonic compensator results in notches at the concerned frequencies. Therefore, the output voltage harmonic distortion is significantly reduced. Additionally, it is worth mentioning that the added resonant compensators have a negligible effect on the dynamic performance of the islanded system, since they only respond to the frequencies around the resonant frequencies.

4. Simulation and Experimental Results

In this section, simulation and experimental results which all are based on the digital control algorithms have been obtained in order to verify the proposed control strategy. The system parameters are given in Table 1.

The steady-state performance of the standalone DG system with PVR-based AD method under the resistive load is investigated as shown in Fig. 11, where the excellent reference tracking with the elimination of the steady-state error is well achieved.

The steady-state simulation waveforms of the standalone DG system without PVR-based AD method under the resistive load is shown in Fig. 12, and the lack of the active damping causes the oscillations and even instability.

Moreover, the transient simulation waveforms for a load step from half load to full load with the proposed method is considered. Fig. 13 depicts that a good dynamic performance can be achieved.

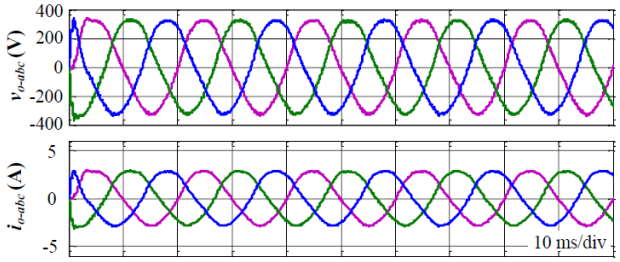


Fig. 11. Steady-state simulation results of the standalone DG system with PVR-based AD method under balanced resistive load (R_1=115 Ω).

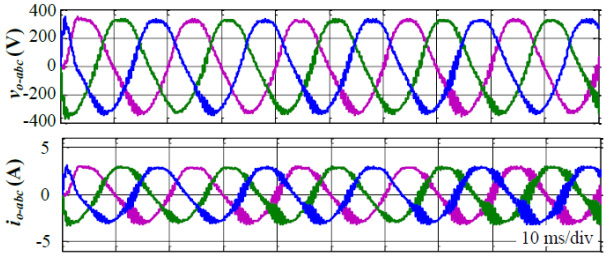


Fig. 12. Steady-state simulation results of the standalone DG system without PVR-based AD method under balanced resistive load (R_1=115 Ω).

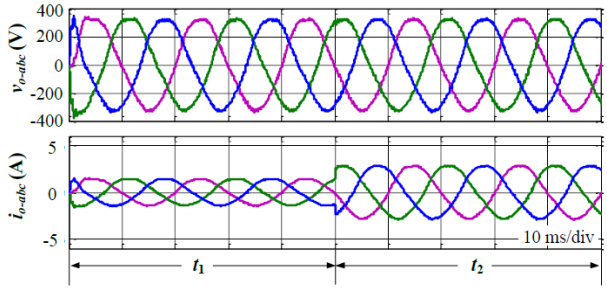


Fig. 13. Transient simulation results of the standalone DG system with PVR-based AD method under balanced resistive load (R_1 from 230 Ω (t_1) to 115 Ω (t_2)).

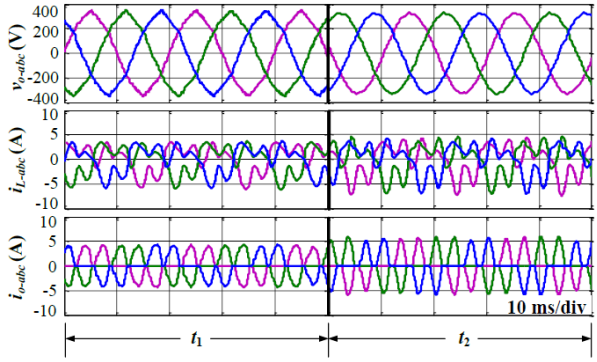


Fig. 14. Simulation results of the standalone DG system for nonlinear load conditions with PVR-based AD method (t_1: without the MRHC, t_2: with the MRHC).

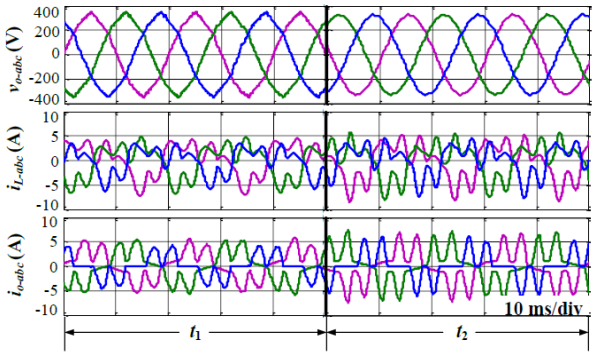


Fig. 15. Simulation results of the standalone DG system for unbalanced plus nonlinear load conditions with PVR-based AD method (t_1: without the MRHC, t_2: with the MRHC).

Fig. 14 shows the simulation results of the VSI in the standalone DG system for nonlinear load conditions with PVR-based AD method. As shown in Fig. 14, the voltage controller without the MRHC during the period of t_1 and the MRHC is added to the voltage controller during the period of t_2. The total harmonic distortions (THDs) of the load output voltages are 5.94% for t_1 and 1.88% for t_2, respectively.

Fig. 15 shows the simulation results of the VSI in the islanded DG system for unbalanced plus nonlinear load conditions with PVR-based AD method. During the period t_1, the voltage controller without the MRHC, then harmonic compensation is added to the voltage controller during the period of t_2. The THDs of the load output voltages are 5.95% and 1.90%, respectively.

In order to test the feasibility of the theoretical analysis, an experimental standalone DG system setup was built and test with the parameters described in Table 1. Fig. 16 depicts the experimental schematic consisting of a Danfoss 2.2 kW inverter, resistive/diode rectifier loads, and a dSPACE1006 controller to implement the proposed control algorithms.

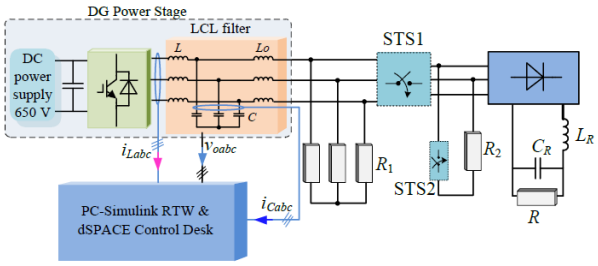


Fig. 16 Experimental setup of the standalone DG system.

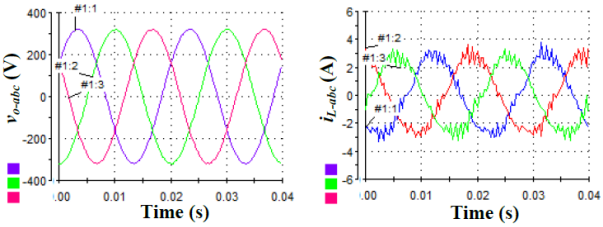


Fig. 17. Experimental results of the standalone DG system for balanced resistive load with $R_{d,eq}$=5.5 (230Ω). (a) Load voltages; (b) Inverter currents.

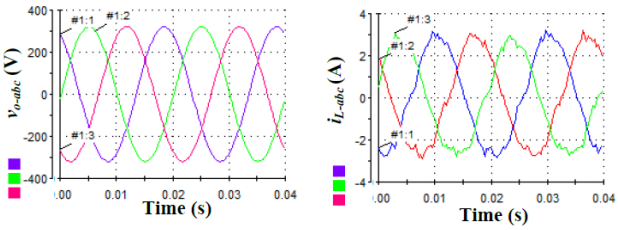
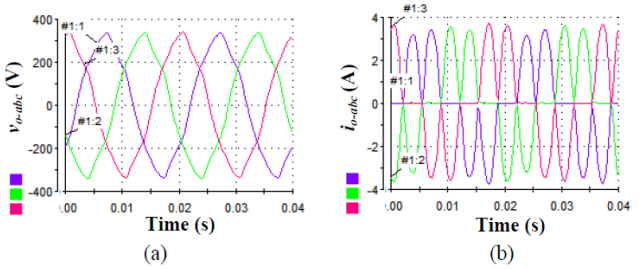


Fig. 18. Experimental results of the standalone DG system for balanced resistive load with $R_{d,eq}$=28.5(230Ω). (a) Load voltages; (b) Inverter currents.

To demonstrate the need for active damping and its benefits, Figs. 17 and 18 show the experimental results of the standalone DG system under balanced resistive load without and with using the PVR-based AD method, respectively. As shown in Fig. 17, it can be clearly observed that the inverter currents are distorted with the large harmonics, being consistent with the aforementioned theoretical analysis.

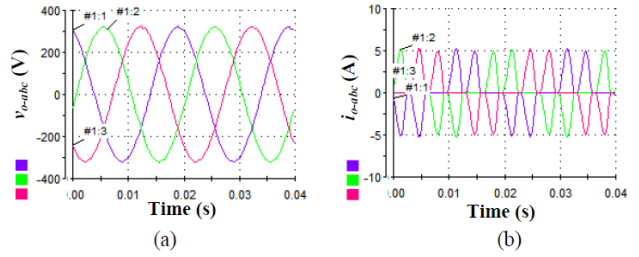
Fig. 18 shows the experimental results for $R_{d,eq}$=28.5. It can be observed that the inverter current harmonics are significantly reduced, which is also in good agreement with the theoretical analysis. It is found that a good performance is achieved when $R_{d,eq}$ is proper chosen in the islanded mode for balanced linear loads.

Figs. 19 and 20 show the experimental results of the standalone DG system under a nonlinear load with $R_{d,eq}$=28.5. As shown in Fig. 19, the load voltages are heavily distorted by the nonlinear load and the THD of the load voltages is 5.45% without using the harmonic compensator in the voltage controller. Fig. 20 shows the



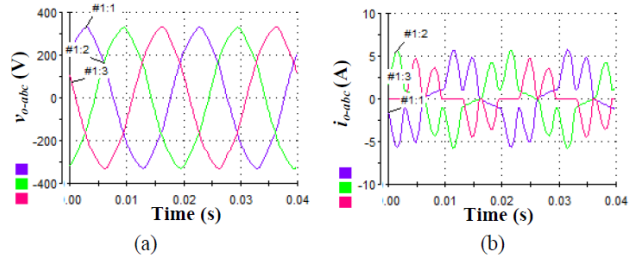
(a) (b)

Fig. 19. Experimental results of the standalone DG system under a nonlinear load with $R_{d,eq}$=28.5 without the MRHC in the voltage loop. (a) Load voltages; (b) Load currents.



(a) (b)

Fig. 20. Experimental results of the standalone DG system under a nonlinear load with $R_{d,eq}$=28.5 with the MRHC in the voltage loop: (a) Load voltages; (b) Load currents.



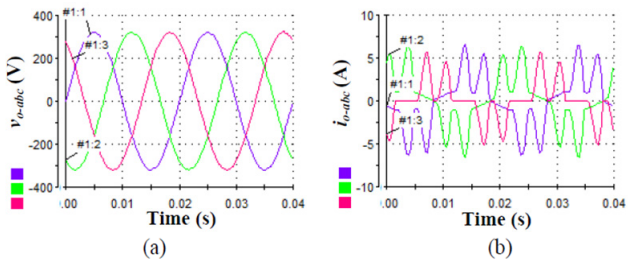
(a) (b)

Fig. 21. Experimental results of the standalone DG system under unbalanced plus nonlinear load with $R_{d,eq}$=28.5 without the MRHC in the voltage loop: (a) Load voltages; (b) Load currents.

experimental results of the voltage PR controller with the MRHC (from 5th to 13th with k_{5v} =40, k_{7v} =40, k_{11v} =20 and k_{13v} =20) and the THD of the load voltages is reduced to 0.50%.

In order to verify the effectiveness of the proposed method under unbalanced plus nonlinear load condition, a single-phase load between phases *A* and *B* which is connected through the STS2 and a three-phase rectifier load are shown in Fig. 16(a). The circuit parameters used in the experimental are the same as given in Table 1 with k_{5v} =50, k_{7v} =40, k_{11v} =20 and k_{13v} =20, respectively.

Figs. 21 and 22 show the experimental results of the standalone DG system under unbalanced plus nonlinear load condition with $R_{d,eq}$=28.5. As shown in Fig. 21, when the voltage controller without using the harmonic compensator, the load output voltages are heavily distorted



(a) (b)

Fig. 22. Experimental results of the standalone DG system under unbalanced plus nonlinear load with $R_{d,eq}$= 28.5 with the MRHC in the voltage loop: (a) Load voltages; (b) Load phase currents.

by the unbalanced and nonlinear loads and the THD of load voltages is 5.94%.

The experimental results of the voltage controller with using the harmonic compensator from 5th to 13th and the THD of the load voltages is 0.53%, which is shown in Fig. 22. It can be concluded that the voltage controller with the EDC based on the PR and the MRHC obtains lower output-voltage unbalance and THD than the conventional PR controller. Additionally, the proposed PVR-based AD method and the multi-loop control strategy help to improve the output voltage and current quality further.

5. Conclusion

This paper has proposed a multi-loop control strategy with PVR-based AD strategy under balanced resistive load and/or unbalanced resistive load and/or nonlinear load of three-phase VSI operating in islanded DG system. Besides, the new modeling and analysis of the whole system in small-signal state-space form is proposed and an overdamped feature of the system is achieved through the eigenvalues. The voltage and current controllers are based on an enhanced PR structure with delay compensation to achieve better accuracy under different load conditions. Moreover, the MRHC effectively prevents the low-order harmonic currents to distort the load output voltages under unbalanced and/or nonlinear load conditions. The proposed strategy uses the current of the filter capacitor and inductor as the feedback signals to compensate the load disturbances and actively damp the resonances. At the same time, an outer voltage loop regulates the output voltage, and ensures zero steady-state error and system stability over a wide range of operating conditions. Based on this model, a detailed design procedure with consideration of the practical implementation aspects has been analyzed.

To support the validity of the proposed control algorithm, the simulation and experimental results of the standalone DG system have been carried out by using the Matlab/ Simulink software and the experimental results obtained from the prototype DG system test-bed with dSPACE1006 controller under various loads are presented to validate the

effectiveness of the proposed strategy.

Acknowledgement

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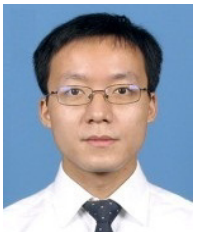

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