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A Current Limiting Strategy to Improve Fault Ride-Through of Inverter Interfaced Autonomous Microgrids

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***Abstract*—With high penetration of distributed energy resources (DER), fault management strategy is of great importance for the distribution network operation. The objective of this paper is to propose a current and voltage limiting strategy to enhance fault ride-through (FRT) capability of inverter-based islanded microgrids (MGs) in which the effects of inverter control system and inverter topology (four/three-wire) are considered. A three-phase voltage-sourced inverter (VSI) with multi-loop control system implemented in synchronous, stationary, and natural reference frames is employed in this study for both four- and three-wire configurations. The proposed strategy provides high voltage and current quality during overcurrent conditions, which is necessary for sensitive loads. Several time-domain simulation studies are conducted to investigate the FRT capability of the proposed strategy against both asymmetrical and symmetrical faults. Moreover, the proposed method is tested on the CIGRE benchmark microgrid to demonstrate the effectiveness of the proposed limiting strategy.**

***Index Terms*—Current control, fault current limiters, fault ride-through (FRT), reference frame, transient response, voltage limit, voltage-sourced inverter (VSI).**

I. Introduction

DURING the last decades, the penetration of distributed energy resources (DER) has increased due to economical, technical, and environmental concerns [1], [2]. Microgrids (MGs) have emerged as a potential solution for integrating DERs into the distribution networks operating in either grid-connected or islanded (autonomous) modes [3], [4]. Many DERs are often connected to the MG using a power-electronic interface converter acting as voltage-sourced inverter (VSI) [5]. This is due to the flexibility of control system of this converter for generating regulated output voltage with high power quality to supply sensitive loads. Droop method as a decentralized control is often implemented in the case of parallel inverters connected to the MG to avoid circulating currents [6]–[8].

A voltage-controlled VSI is usually used in an autonomous mode, where the frequency and voltage are not dictated by the grid. It usually regulates voltage and frequency at the DER terminal using a multi-loop control structure [9]. This control system can be implemented in the synchronous reference frame (SYRF or $dq0$ coordinates), stationary reference frame (STRF or $\alpha\beta\gamma$ coordinates), or natural reference frame (NARF or abc coordinates) [10].

During short-circuit faults and overload conditions, inverter current should be limited to prevent damage to semiconductor switches because an inverter has a low thermal inertia [11]–[13]. This task is usually performed using a current limiting strategy embedded in the inverter control system. There are two main limiting strategies [10]: instantaneous saturation limit and latched limit. The former limiter prevents its input signal from increasing beyond a predefined value. Although this strategy is simple to implement, in the case of a sinusoidal input signal, the output is distorted due to crest clipping. In the latched limit strategy, the current reference of the inverter is replaced with a predefined current reference during overcurrent conditions. In the cases of SYRF and STRF, this limiter completely opens the voltage control loop and consequently the inverter may experience overvoltage in healthy phase(s) during unbalanced faults [10]. If this happens, the sinusoidal voltage waveform may be clipped which results in harmonic distortion. To solve this problem, [14] employs a virtual resistance in parallel with the filter capacitance in SYRF in which the latched current reference is reduced proportionally to the output voltage. Thus, the latched current reference is decreased due to virtual resistance action. Moreover, this approach reduces the inverter output voltage. In [15], a current limiting control technique for multi-module parallel UPS inverter is proposed in which the current command of the slave is generated by its previous module and limited in amplitude using instantaneous saturation. Therefore, the output current of inverters is distorted. Moreover, this method requires communication links and high bandwidth control loops. The work presented in [16] proposes a dynamic current limiting approach implemented in SYRF in which both direct and quadrature current components are limited. In [17], using average and second harmonic components of real and reactive powers, grid-connected inverter current references are generated in SYRF to limit the fault current. Distortion-free saturation strategies for a three-phase three-wire inverter are proposed in [18] in which the control system is implemented in SYRF while a similar procedure can be used for STRF case. In [19], a hardware-circuit-based hysteresis

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current control strategy is proposed to limit output currents of three-phase three-wire inverters in which the control system is implemented in SYRF. Moreover, a current limiting strategy of hardware blockage with the instantaneous currents, combined by software current limit with the average current, is proposed in [20] for three-phase inverters with the control implemented in SYRF. On the other hand, some methods employ fault current limiter (FCL) to limit converter current [21]. However, using external devices increases the cost and decreases the reliability of the system. Also, FCL sizing is another challenge [22].

The effect of inverter control system and inverter topology (four/three-wire) on the limiting strategy is not fully addressed yet. This paper presents a current and voltage limiting strategy which is implemented in the inverter control system. This strategy can be implemented in various reference frames and for different inverter topologies. The fault ride-through (FRT) capability of the proposed strategy employed in a VSI including both voltage and current control loops during both asymmetrical and symmetrical faults is analyzed. Specifically, the objectives of this paper are as follows:

- To investigate the performance of main current limiting strategies during various fault conditions.
- To limit both inverter current and voltage using only a current limiter considering the effects of adopted reference frame, inverter topology, and fault type.
- To provide high quality of voltage and current waveforms during various fault conditions which is necessary for the sensitive loads.
- To make smooth transitions during both fault inception and fault clearing instants.
- To retain voltage magnitude controllability in healthy phase(s) during various fault conditions which allows continuous feeding of single-phase sensitive loads.
- To verify the proposed limiting strategy using a benchmark MG.

This paper is organized as follows. The DER control system structure is described in Section II. The performance of main current limiting strategies is analyzed in Section III. Section IV is dedicated to the proposed limiting strategy. Simulation results are presented in Section V to verify the performance of the proposed strategy. Finally, Section VI concludes this paper.

II. Basic Structure of DER Control

Fig. 1 shows a three-phase 380 V, 50 Hz islanded study test system including a 10 kVA DER and two parallel 3 kW resistive loads. The system is simulated in MATLAB/Simulink environment for both four- and three-wire configurations to explain and investigate the new theory presented in this paper through studying a number of fault scenarios. Three-wire topology is usually used for MGs implemented in the medium-voltage distribution network. On the other hand, the low-voltage MGs are designed with four wires to connect the single-phase loads. There are three ways for connecting a VSI to a four-wire network [23]: (1) through a delta/wye-grounded transformer, (2) using split dc-link capacitors and connecting

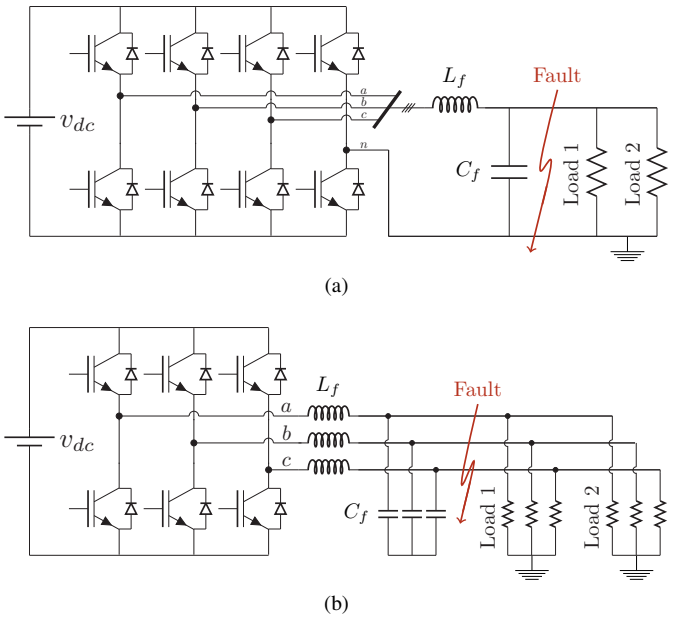

Fig. 1. Schematic diagram of the example test system. (a) Four-wire topology; (b) Three-wire topology.

the mid-point of the dc-link to the neutral point, and (3) using a four-leg topology and connecting the midpoint of the fourth (neutral) leg to the neutral point. As shown in Fig. 1(a), the four-leg structure is adopted in this work. The DER interface is a voltage-controlled VSI for controlling amplitude and frequency of the DER output voltage which is suitable for islanded operation of MG. Droop control, a common technique based on local measurements, is used to calculate the voltage reference v_o^{ref} for VSI. Fig. 2 shows the VSI control structure including an inner current control loop and an outer voltage control loop. The outer control loop is designed to regulate the voltage across the filter capacitance C_f by calculating the inductor current reference i_L^{ref} for the current control loop. The task of the inner control loop is to increase power quality by controlling the current through the filter inductor L_f. The inner loop provides the inverter switching voltage reference [10]. In this work, a proportional-integral (PI) controller is used as the voltage control for SYRF case while a proportional + resonant (PR) controller is employed for this purpose in STRF and NARF cases. However, a proportional controller is used as the current control for all reference frames. The power generated by the primary source is first stored in the DC link and then converted to the AC power by the inverter. The DC link capacitor is sized to decouple the primary source dynamics from those of the network. For fault analysis, the prime mover is considered ideal and the DC bus dynamics are neglected [24].

III. Inverter Current Limiting

Current limiting is performed using the current limit block in the output of voltage control, as shown in Fig. 2. This section investigates the effects of fault type and adopted reference frame on the performance of two main current limiting strategies: instantaneous saturation limit and latched limit [10], [25].

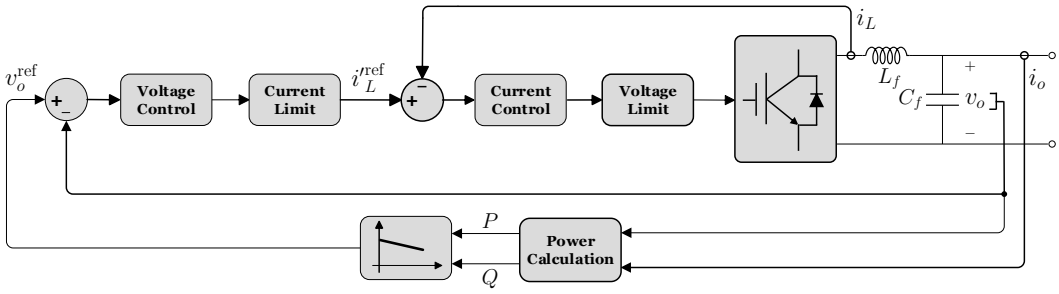

Fig. 2. DER power stage and multi-loop control system.

A. Instantaneous Saturation Limit Strategy

The instantaneous saturation limit strategy saturates every component of the inductor current reference as

$$i_L'^{\text{ref}} = \begin{cases} i_{\text{th}}, & i_L^{\text{ref}} > i_{\text{th}} \\ -i_{\text{th}}, & i_L^{\text{ref}} < -i_{\text{th}} \\ i_L^{\text{ref}}, & \text{otherwise}, \end{cases} \tag{1}$$

where i_{th} is the maximum allowable peak current or current threshold in the limiting strategy. In this paper, i_{th} is adopted equal to two times the inverter rated peak current, i.e., 2 pu. Also, $i_L'^{\text{ref}}$ refers to the limited inductor current reference which is applied to the inner current controller. Although the implementation of this technique is simple, the inverter voltage and current waveforms are distorted due to crest clipping of the current reference when it is a sinusoidal waveform. Table I shows the maximum total harmonic distortion (THD) in output voltage and current of DER as well as inductor current peak $i_{L,\max}$ and output voltage peak $v_{o,\max}$ achieved in different reference frames for four- and three-wire configurations of Fig. 1 under both asymmetrical and symmetrical faults. This table shows that the inverter voltage and current are extremely distorted in the cases of STRF and NARF for all fault types. In contrast, since SYRF works with DC signals and clipping a DC signal results in another DC signal, the saturation limit implemented in SYRF provides sinusoidal waveforms in the case of a symmetrical fault. During unbalanced conditions, however, sinusoidal ripples at two times the nominal frequency (2ω) appear in the current reference in SYRF case. Thus, during an asymmetrical fault, this sinusoidal current reference is clipped and consequently the inverter voltage and current waveforms are deteriorated.

On the other hand, in three-wire systems, the zero-sequence voltage can appear during unbalanced conditions whereas the currents flowing in the three phases do not contain zero-sequence components [5]. Therefore, the inverter control structure is implemented in two axes for SYRF and STRF cases. In such systems, during a single-phase to ground fault, the fault current is produced only due to grounding the loads (since neutral wire is not available). Therefore, the inverter current may not be increased largely. In the case of NARF, voltage control contains a zero-sequence component due to the zero-sequence component of output voltage. This zero-sequence component increases the inductor current reference which can be detected by the instantaneous saturation limit. In the cases of SYRF and STRF, however, since the two-axis voltage control does not contain a zero-sequence component, the inductor current reference does not exceed its threshold for the single-phase to ground fault and consequently the instantaneous limiting strategy is not activated. It should be noted that in the case of multi-phase faults, as the fault current can flow between faulty phases, the inductor current reference exceeds its threshold in all reference frames and consequently the instantaneous saturation limit is activated.

Among all reference frames, only NARF can limit the magnitude of the inductor current during both symmetrical and asymmetrical faults, as shown in Table I. This is due to the fact that in the NARF case, current reference limiting is independently implemented in each phase whereas in the SYRF/STRF case, this limiting is performed on the $dq(0)/\alpha\beta(\gamma)$ coordinates. Indeed, although the current reference are limited in SYRF/STRF, its inverse Park/Clarke transformation yields to inaccurate current reference limiting in the abc coordinates and consequently the inverter current exceeds the current threshold. Besides, the inverter experiences overvoltage in all reference frames, as shown in Table I.

B. Latched Limit Strategy

In the latched limit strategy, i_L^{ref} is replaced by a predefined current reference vector. Specifically, the latched limit strategy is expressed in (2a) for NARF case and in (2b) for SYRF and STRF cases.

$$i_{L,j}'^{\text{ref}} = \begin{cases} i_{L,j}^{\text{lat}}, & I_{L,j}^{\text{ref}} > i_{\text{th}}/\sqrt{2} \\ i_{L,j}^{\text{ref}}, & \text{otherwise} \end{cases} \; ; \; j = a, b, c \tag{2a}$$

$$\overrightarrow{i'}_{L,dq(0)/\alpha\beta(\gamma)}^{\text{ref}} = \begin{cases} \overrightarrow{i}_{L,dq(0)/\alpha\beta(\gamma)}^{\text{lat}}, & |\overrightarrow{i}_{L,dq(0)/\alpha\beta(\gamma)}^{\text{ref}}| > i_{\text{th}} \\ \overrightarrow{i}_{L,dq(0)/\alpha\beta(\gamma)}^{\text{ref}}, & \text{otherwise}, \end{cases} \tag{2b}$$

where I_L^{ref} refers to the RMS value of the inductor current reference and i_L^{lat} is the predefined current reference. Due to independent control of each phase in NARF case, i_L^{ref} is replaced by i_L^{lat} only in the faulty phase(s), as described in (2a), and consequently the voltage is fully controlled by the droop method in the healthy phase(s). Based on (2b), an identical current reference is applied during asymmetrical and symmetrical faults in both SYRF and STRF cases. Thus, the outer voltage control loop is completely opened in the

TABLE I
PERFORMANCE OF INSTANTANEOUS SATURATION LIMIT STRATEGY

Frame	Fault Type	$\mathbf{THD_V}$ (%)	$\mathbf{THD_I}$ (%)	$i_{L,\max}$ (p.u.)	$v_{o,\max}$ (p.u.)
Four-Wire Configuration					
NARF	*a-g*	20.7	20.7	2	1
	a-b-g	21	20.9	2	1
	a-b	34.2	19.2	2	1
	a-b-c-g	20.9	20.8	2	0.16
SYRF	*a-g*	17.7	17.7	3.77	0.98
	a-b-g	26.2	26.2	3.77	0.82
	a-b	25.4	33	2.76	0.86
	a-b-c-g	0.23	0.23	2	0.16
STRF	*a-g*	12	12	3.07	0.93
	a-b-g	25.9	25.9	3.69	0.97
	a-b	14.8	22	2.57	1.13
	a-b-c-g	20.7	20.7	2.79	0.22
Three-Wire Configuration					
NARF	*a-g*	57.2	57.2	1.68	1.36
	a-b-g	23.4	23.3	2	1
	a-b	26.4	25.2	2	0.98
	a-b-c-g	14.1	14.1	2	0.16
SYRF	*a-g*	0.54	0.54	1.65	1.59
	a-b-g	24.7	24.8	2.58	0.91
	a-b	17.2	25.1	2.6	0.64
	a-b-c-g	0.42	0.42	2	0.16
STRF	*a-g*	0.42	0.42	1.69	1.6
	a-b-g	25	24.3	2.77	1.67
	a-b	20.9	23.9	2.54	1.15
	a-b-c-g	22.7	22.7	2.79	0.22

TABLE II
PERFORMANCE OF LATCHED LIMIT STRATEGY

Frame	Fault Type	$\mathbf{THD_V}$ (%)	$\mathbf{THD_I}$ (%)	$i_{L,\max}$ (p.u.)	$v_{o,\max}$ (p.u.)
Four-Wire Configuration					
NARF	*a-g*	0.27	0.27	2	1
	a-b-g	0.27	0.27	2	1
	a-b	0.37	0.37	2	1
	a-b-c-g	0.13	0.13	2	0.16
SYRF	*a-g*	0.53	0.53	2	1.84
	a-b-g	0.41	0.41	2	1.85
	a-b	0.42	0.42	2	1.84
	a-b-c-g	0.26	0.26	2	0.16
STRF	*a-g*	1.08	1.08	2	2.23
	a-b-g	1.05	1.05	2	2.22
	a-b	1.02	1.02	2	2.23
	a-b-c-g	0.21	0.21	2	0.16
Three-Wire Configuration					
NARF	*a-g*	26.5	26.5	1.35	1.18
	a-b-g	1.45	1.45	2	0.97
	a-b	0.95	1.3	2	0.97
	a-b-c-g	0.06	0.06	2	0.16
SYRF	*a-g*	0.36	0.36	1.41	1.54
	a-b-g	0.56	0.56	2	2.32
	a-b	0.58	0.63	2	1.84
	a-b-c-g	0.18	0.18	2	0.16
STRF	*a-g*	0.45	0.45	1.81	1.6
	a-b-g	0.2	0.19	2	2.3
	a-b	0.06	0.19	2	1.83
	a-b-c-g	0.14	0.14	2	0.16

overcurrent conditions. Since no crest clipping occurs in this limiting strategy, the inverter currents are sinusoidal and properly limited. Table II shows the simulation results for Fig. 1 in which the latched limit strategy is used. These results prove the ability of latched limit strategy for limiting the inverter current and for producing the high quality of output voltage and current waveforms. However, during asymmetrical faults, inverter may experience an overvoltage in the healthy phase(s) in the cases of SYRF and STRF. The reason of this phenomenon is that the latched limit strategy injects a current with an amplitude equal to i_{th} into both faulty and healthy phases [14]. In such situations, if the instantaneous saturation limit is used as the voltage limit in the inner current control loop, the switching voltage reference is clipped and therefore both inverter voltage and current waveforms are distorted.

On the other hand, in the case of NARF for three-wire VSI, since only the voltage control loop in the faulty phase(s) is opened and its current reference is replaced by the latched limit, voltage control contains a zero-sequence component during asymmetrical ground faults. This component increases the inductor current reference which can not be tracked by the current controller in the case of a single-phase to ground fault because the inverter current is not increased during this fault, as mentioned in Subsection III-A. Consequently poor power quality results. Also, in this condition, the inverter experiences an overvoltage in the faulty phase. However, during the two-phase to ground fault, since the fault current can flow between faulty phases, the current control loop can effectively track inductor current reference and no distortion appears in the inverter voltage and current waveforms. During the single-phase to ground fault in the cases of SYRF and STRF, since the magnitude of current reference vector is not large enough to exceed its threshold, the latch limit is not activated. As observed in Table II, in such conditions, inverter experiences overvoltages.

IV. PROPOSED LIMITING STRATEGY

As mentioned above, the inverter control system, inverter topology, and fault type affect the current limiting performance. Consequently, these factors should be considered in the every current limiting strategy. The poor power quality is mainly due to crest clipping of the sinusoidal reference signal. Therefore, it should be ensured that no clipping occurs during overcurrent condition to avoid distortion. To do this, this paper proposes a limiting strategy which limits the magnitude of the inductor current reference to i_{th} during overcurrent conditions in which unlike latched limit, voltage control loop remains closed. The proposed limiting strategy is shown in Fig. 3 in which a current limiting factor (CLF) is applied to the inductor current reference. This reduction prevents the current reference

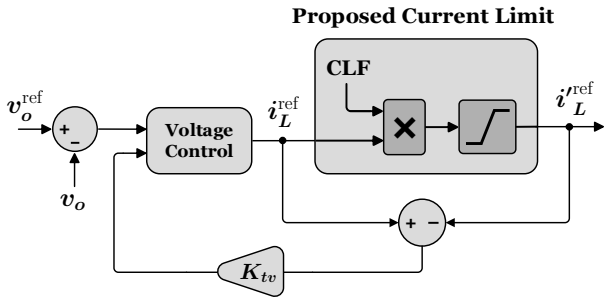

Fig. 3. Schematic diagram of the proposed limiting strategy.

from exceeding its threshold during a fault. Moreover, the voltage controller is equipped with an anti-windup strategy in which conditional integration method is employed to prevent windup of the controller integrator [26]. In this method, the difference between the inductor current reference and limited inductor current reference is fed back through the gain K_{tv} to reduce the error input going to the integrator. The proposed strategy should be equipped with an instantaneous saturation limit which is set to i_{th}, as shown in Fig. 3. The reason for this is that a temporary limiting strategy is required to protect the inverter against large currents from overcurrent inception to the proposed method activation instant. After activation of the proposed limiting strategy, as the current reference is limited, the instantaneous saturation limit does not affect this reference. This auxiliary limiter is required for smooth transition during both fault inception and fault clearing instants.

A. Basic Structure of the Proposed Strategy

The schematic diagram of the proposed strategy for NARF case is shown in Fig. 4(a). During normal conditions, no limiting is required and therefore CLF $= 1$. If the RMS value of the inductor current reference I_L^{ref} in one phase exceeds its threshold, the proposed strategy is activated and adjusts CLF so that i'^{ref}_L is limited to i_{th}. As observed, CLF is only calculated and applied to the faulty phase(s) which is due to ability of NARF for independent control of each phase. Thus, the voltage magnitude is fully controlled by the droop method in the healthy phase(s). In this work, RMS calculation is performed on a half-cycle to improve the speed of proposed method response during both fault occurrence and fault clearing instants. The proposed strategy in NARF case can be expressed as

$$i'^{\text{ref}}_{L,j} = \text{CLF}_j \times i^{\text{ref}}_{L,j};\ \ j = a, b, c, \tag{3}$$

where

$$\text{CLF}_j = \begin{cases} \dfrac{i_{\text{th}}}{\sqrt{2} \times I^{\text{ref}}_{L,j}}, & I^{\text{ref}}_{L,j} > \dfrac{i_{\text{th}}}{\sqrt{2}} \\ 1, & \text{otherwise} \end{cases};\ \ j = a, b, c. \tag{4}$$

The schematic diagram of the proposed limiting strategy for SYRF and STRF cases is shown in Fig. 4(b). Since in SYRF and STRF cases, the three-phase system is considered as a single unit (not a superposition or sum of three

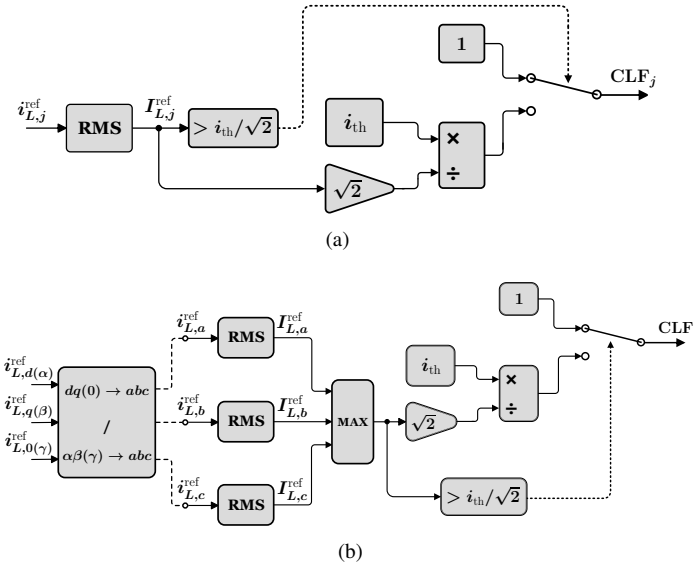

Fig. 4. Implementation of the proposed strategy. (a) NARF case for phase j, $j = a, b, c$; (b) SYRF and STRF cases.

single-phase circuits [27]), independent calculation of CLF in each axis is not effective. Therefore, in the cases of SYRF and STRF, CLF calculation is also performed using phase components. Since the amplitudes of phase components are equal/proportionl to that of $dq0$ or $\alpha\beta\gamma$ components (depending on amplitude/power invariantly of the transformation [28]), CLF calculation using phase components results in amplitude limiting in SYRF/STRF case. First, inductor current reference produced by the voltage control loop is transformed to the abc coordinates. As the three-phase system is considered as a unit, one CLF is applied to all axes. This CLF is calculated based on the maximum inductor current reference to ensure current limiting in all axes. Since the current references in all axes are reduced by this CLF, voltage magnitude may be also decreased in the healthy phase(s). Consequently, voltage magnitude is not determined completely by the droop method in SYRF and STRF cases. The proposed strategy in SYRF and STRF cases can be expressed as

$$i'^{\text{ref}}_{L,j} = \text{CLF} \times i^{\text{ref}}_{L,j};\ \ j = d(\alpha), q(\beta), 0(\gamma), \tag{5}$$

where

$$\text{CLF} = \begin{cases} \dfrac{i_{\text{th}}}{\sqrt{2} \times \max(I^{\text{ref}}_{L,j})}, & \max(I^{\text{ref}}_{L,j}) > \dfrac{i_{\text{th}}}{\sqrt{2}} \\ 1, & \text{otherwise} \end{cases};\ j = a, b, c. \tag{6}$$

On the other hand, as mentioned in Subsection III-A, since the current reference does not exceed its threshold during the single-phase to ground fault in the cases of SYRF and STRF, the proposed strategy is not activated during this type of fault and consequently the inverter experiences an overvoltage.

The proposed strategy can also applied to the three-wire configuration using (3)-(6) and current and voltage limiting is achieved. However, in the case of NARF, since voltage

control contains a zero-sequence component during asymmetrical ground faults while this component is not available in the current control loop, power quality is poor. This problem does not appear in the cases of SYRF and STRF, because the control system is implemented in dq and $\alpha\beta$ coordinates, respectively, and consequently there is no zero-sequence component in the voltage control.

B. Hybrid Reference Frame Limiting Strategy

The basic form of the proposed limiting strategy suffers from (1) voltage magnitude controllability in healthy phase(s) in SYRF and STRF cases for four-wire configuration and in all reference frames for three-wire configuration, (2) poor power quality in NARF case for three-wire configuration, and (3) overvoltage during the single-phase to ground fault in the cases of SYRF and STRF due to deactivation of the proposed method (see Table III). To address these issues, this paper proposes the hybrid reference frame limiting (HRFL) strategy, as shown in Fig. 5(a). In the cases of SYRF and STRF, an auxiliary parallel control system is implemented in NARF to utilize its voltage magnitude controllability in the healthy phase(s). In the three-wire configuration, HRFL includes only the parallel voltage control and its current control remains in SYRF/STRF to circumvent the low power quality in NARF case because there is no zero-sequence component in the current control. When a fault occurs, the inverter is controlled by the parallel control system. Fig. 5(b) shows the schematic diagram of the control logic circuit used to detect an overcurrent condition. As investigated in [10], among various current-set/reset and voltage-set/reset combinations, the best performance for the latched limit is achieved by the current-set and voltage-reset strategy. This scheme is adopted in this work. When the RMS value of the inductor current reference produced by the parallel control exceeds its threshold at least in one phase, a signal is sent to the inverter control system to change the operating mode to NARF. After the fault clears, the inverter voltage is restored and a reset signal is sent to the inverter control system to reactivate the main control loops. The reset signal is produced when the inverter output voltage in all phases is greater than $V_{\text{reset}} = 0.8$ pu$/\sqrt{2}$. In the case of NARF for the three-wire topology, the auxiliary control system is also required to overcome the poor power quality caused by the current control during asymmetrical ground faults. In this case, HRFL strategy includes only the parallel current control implemented in STRF to exclude the zero-sequence component from the current reference. By doing this, the current control can effectively control the inductor current. The temporary instantaneous saturation limit of Fig. 3 must be used in both main and parallel control systems to provide smooth transition during fault inception and fault clearing instants.

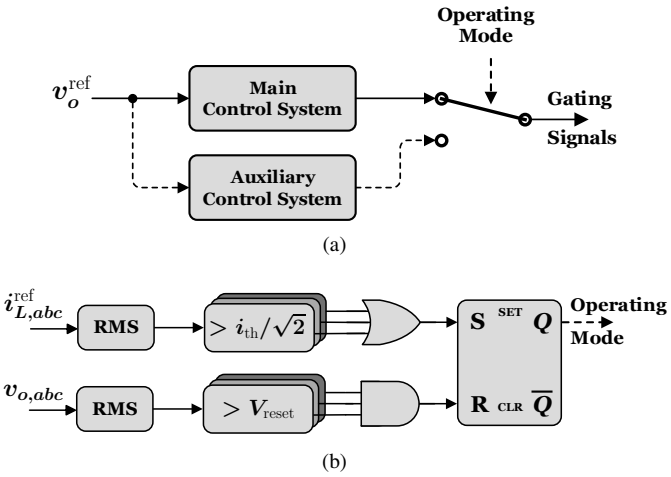

Fig. 5. (a) Implementation of HRFL strategy; (b) Schematic diagram of the control logic for overcurrent detection.

V. Simulation Results

A. Example Test System

The performance of the proposed limiting strategy is investigated for the test system of Fig. 1; various faults are simulated across load 1 with the fault resistance is set to 1.2 Ω. These faults occur at $t = 0.2$ s and they are automatically cleared at $t = 0.3$ s. First, the inverter voltage and current waveforms for four-wire configuration during a single-phase to ground fault are shown in Fig. 6 in which the control system is implemented in NARF and the basic structure of the proposed limiting strategy is used. The inductor current closely tracks its limited reference and no distortion appears in the inverter output voltage and current waveforms. Moreover, voltage magnitude in the healthy phases is fully controlled by the droop method due to independent control of each phase. Moreover, the computed CLF during this fault is shown in the last row of Fig. 6. Instantaneous saturation limit action can be observed in the first cycle after fault inception. Since the inductor current reference is sinusoidal during fault and the instantaneous limiting is provided by the auxiliary instantaneous saturation limiter, the current reference is properly restored from the fault condition. Consequently, smooth transition during fault clearing is achieved which proves the FRT capability of the proposed strategy. Fig. 7 shows the simulation results for the three-wire configuration during a two-phase fault when the control system is implemented in SYRF and the basic structure of the proposed limiting strategy is used. The inductor current is properly limited and no distortion appears in the output voltage and current waveforms. Although the voltage magnitude is properly limited, it also drops in the healthy phase. The proposed method indirectly limits the inverter voltage by properly limiting the inductor current and consequently there is no need to use voltage limit in the inner current control loop. Table III shows the THD of the output voltage and current as well as inductor current and output voltage peaks obtained when the basic form of proposed limiting strategy is active for four- and three-wire configurations during various fault types.

Fig. 8 shows the inverter voltage and current waveforms in the four-wire configuration during a two-phase to ground fault when HRFL strategy is used and the main control system is implemented in STRF. As observed, the inductor current properly tracks its limited reference and no distortion appears in the output voltage and current waveforms. The control logic operation is shown in the first row of Fig. 8 which properly changes the operating mode of the control system in both

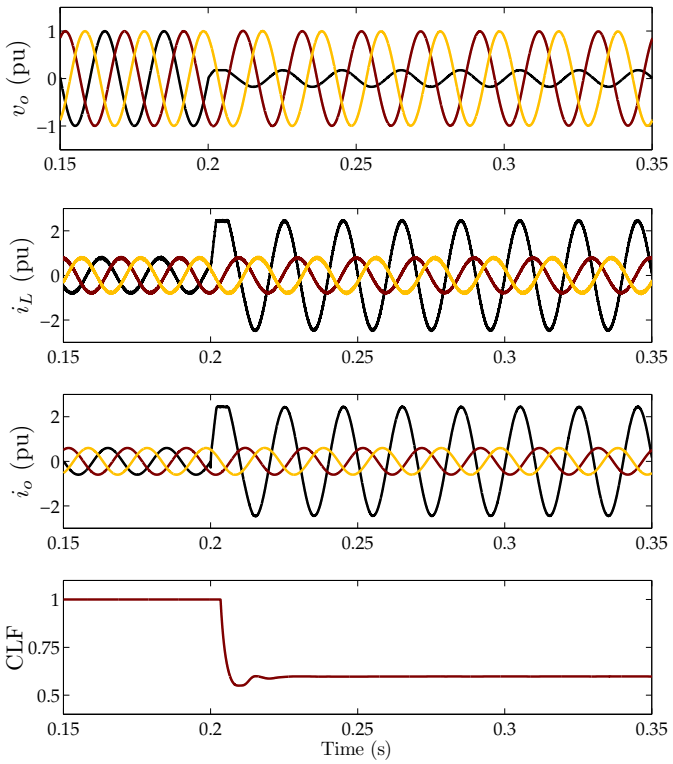

Fig. 6. Output voltage, inductor current, and output current waveforms of four-wire inverter as well as computed CLF by the proposed limiting strategy during an *a-g* fault. The control system is implemented in NARF.

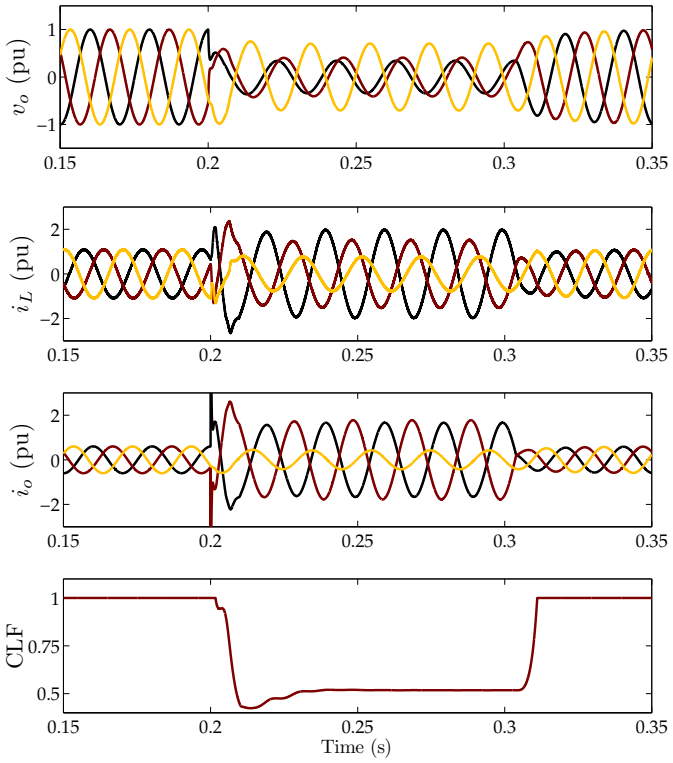

Fig. 7. Output voltage, inductor current, and output current waveforms of three-wire inverter as well as computed CLF by the proposed limiting strategy during an *a-b* fault. The control system is implemented in SYRF.

TABLE III
PERFORMANCE OF BASIC FORM OF PROPOSED LIMITING STRATEGY

Frame	Fault Type	$\mathbf{THD_V}$ (%)	$\mathbf{THD_I}$ (%)	$i_{L,\max}$ (p.u.)	$v_{o,\max}$ (p.u.)
Four-Wire Configuration					
NARF	*a-g*	0.98	0.98	2	1
	a-b-g	1.07	1.06	2	1
	a-b	0.77	0.61	2	1
	a-b-c-g	1.1	1.1	2	0.14
SYRF	*a-g*	0.45	0.45	2	0.82
	a-b-g	0.47	0.47	2	0.82
	a-b	0.7	1.61	2	0.83
	a-b-c-g	0.38	0.38	2	0.14
STRF	*a-g*	1.08	1.08	2	0.79
	a-b-g	1.14	1.14	2	0.78
	a-b	0.89	0.79	2	0.79
	a-b-c-g	1.13	1.13	2	0.14
Three-Wire Configuration					
NARF	*a-g*	25.3	25.3	0.61	1
	a-b-g	11.3	11.3	1.69	1
	a-b	1.7	1.63	2	0.82
	a-b-c-g	0.38	0.38	2	0.16
SYRF	*a-g*	0.5	0.5	1.52	1.57
	a-b-g	1.46	1.46	1.93	1
	a-b	0.51	1.16	1.93	0.74
	a-b-c-g	0.2	0.2	2	0.16
STRF	*a-g*	0.38	0.38	1.63	1.61
	a-b-g	0.2	0.2	2	1
	a-b	0.19	0.21	2	0.76
	a-b-c-g	0.16	0.16	2	0.16

fault inception and fault clearing instants. Due to implementing voltage control loop in NARF during fault, voltage magnitude is fully controlled by the droop method in the healthy phase. It should be noted that in the SYRF/STRF case, since the temporary instantaneous limiting is performed in $dq(0)/\alpha\beta(\gamma)$ coordinates, the inverter current is not properly limited in abc coordinates during first cycle after fault inception, as mentioned in Subsection III-A and as shown in Figs. 7 and 8. However, this delay is short and the produced overcurrent does not damage the inverter switches. Moreover, since the simulated faults in the sample study system are across the filter capacitor, the inverter may experience a transient overshoot in the inverter output current in the fault inception. However, it vanishes almost instantaneously and therefore, it can be ignored. If the simulated fault is electrically far from the inverter, this overshoot is degraded (as shown in Fig. 10). Table IV shows the performance of HRFL strategy for four- and three-wire configurations and for various reference frames during different fault types. It demonstrates the high quality of output voltage and current waveforms as well as proper limiting of inductor current and output voltage.

B. CIGRE Benchmark Microgrid

In order to validate the applicability of the proposed limiting strategy, the modified CIGRE benchmark microgrid [29] is

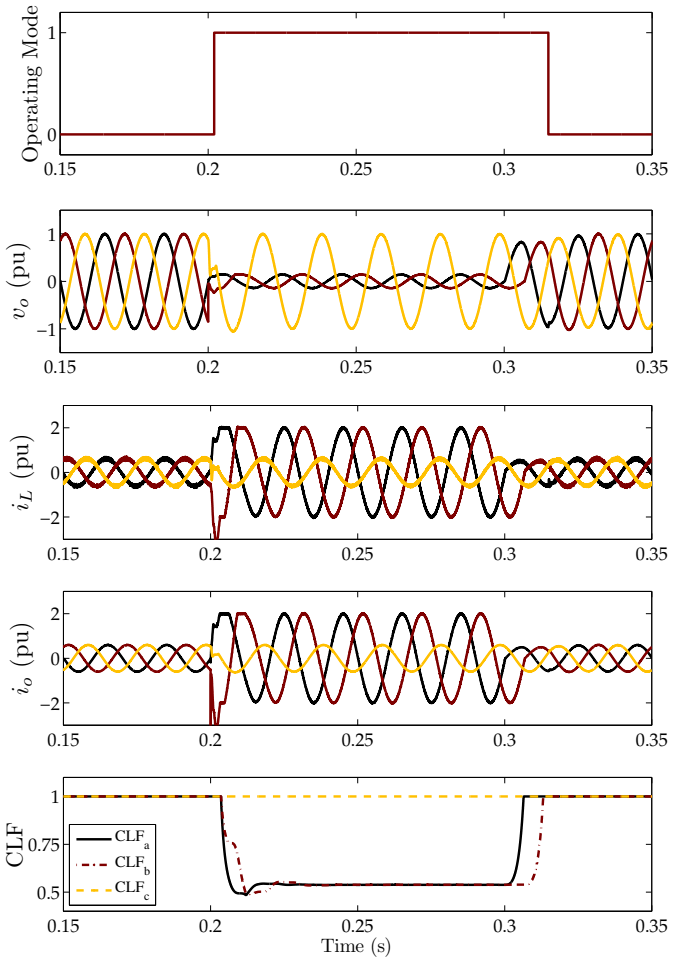

Fig. 8. Output voltage, inductor current, and output current waveforms of four-wire inverter as well as the operating mode signal and computed CLF by the HRFL strategy during an *a-b-g* fault. The main control system is implemented in STRF.

studied. The single-line diagram of this test system is shown in Fig. 9. The CIGRE benchmark represents common low voltage (four-wire) distribution feeders with a variety of load types and includes five DER units. In this study, the control system of DER 1 and DER 4 is implemented in NARF while the controllers of DER 2 and DER 5 are implemented in SYRF. Moreover, the control system of DER 3 is implemented in STRF. The loads are residential type and different power factors are assigned to them to replicate various loading conditions. The parameters of the benchmark are presented in Table V. Two fault scenarios are simulated.

1) Three-phase Line to Ground Fault: The objective of the first scenario is to evaluate the performance of the basic form of proposed limiting strategy during a symmetrical fault. For this purpose, this strategy is implemented in all DERs and a solid three-phase to ground fault occurs across the load 4 (F1 in the Fig. 9). The fault is initiated at $t = 10$ s and is automatically cleared at $t = 11$ s. Table VI shows maximum THD in output voltage and current of all DERs as well as their inductor current and output voltage peaks. As shown, the inverter output voltage and current waveforms of all DERs are

TABLE IV
PERFORMANCE OF HYBRID REFERENCE FRAME LIMITING STRATEGY

Frame	Fault Type	$\mathbf{THD_V}$ (%)	$\mathbf{THD_I}$ (%)	$i_{L,\max}$ (p.u.)	$v_{o,\max}$ (p.u.)
Four-Wire Configuration					
NARF	*a-g*	1.22	1.22	2	1
	a-b-g	1.28	1.28	2	1
	a-b	1.32	1.2	2	1
	a-b-c-g	1.1	1.1	2	0.15
SYRF	*a-g*	0.95	0.95	2	1
	a-b-g	1.05	1.05	2	1
	a-b	0.77	0.59	2	1
	a-b-c-g	1.08	1.08	2	0.15
STRF	*a-g*	0.93	0.93	2	1
	a-b-g	1.08	1.08	2	1
	a-b	0.78	0.62	2	1
	a-b-c-g	1.08	1.07	2	0.15
Three-Wire Configuration					
NARF	*a-g*	0.43	0.43	0.64	1
	a-b-g	0.47	0.47	1.75	1
	a-b	0.42	0.51	2	1
	a-b-c-g	0.38	0.38	2	0.16
SYRF	*a-g*	0.54	0.54	0.61	1
	a-b-g	0.52	0.52	1.73	1
	a-b	0.47	0.58	2	1
	a-b-c-g	0.46	0.46	2	0.16
STRF	*a-g*	0.44	0.44	0.64	1
	a-b-g	0.47	0.47	1.74	1
	a-b	0.41	0.5	2	1
	a-b-c-g	0.39	0.39	2	0.16

sinusoidal during the fault conditions. Moreover, the inductor currents of all DERs are satisfactorily limited.

2) Line-to-Line Fault: To verify the performance of HRFL strategy during and subsequent to unbalanced faults, the second scenario is studied in which this strategy is employed in all DERs and an asymmetrical fault occurs in the beginning of the connecting feeder of DER 3 (F2 in the Fig. 9). This fault is a solid two-phase fault that initiates at $t = 10$ s and lasts for 50 cycles. The simulation results including all DER voltage and current waveforms are in Fig. 10. Sinusoidal waveforms are achieved for all DERs during fault. Also, The inverter current is properly limited and no overvoltage appears during the fault. Moreover, proper transition to and recovery from the fault condition are obtained. The detailed results are shown in Table VI, which shows the effectiveness of the proposed limiting strategy.

VI. CONCLUSION

Fault management of a microgrid is of great importance to prevent voltage and current violations, and it is highly affected by the DER control system. The performance analysis of main current limiting strategies against various fault conditions shows that the instantaneous saturation limit leads to (1) poor power quality, (2) inaccuracy in the current limiting for SYRF and STRF cases, and (3) overvoltage in all reference

TABLE V
CIGRE TEST SYSTEM PARAMETERS

DER Parameters							
Type	**Parameter**	**Symbol**	**DER 1**	**DER 2**	**DER 3**	**DER 4**	**DER 5**
Electrical	Rated power	S_n (kVA)	40	40	25	15	15
	Rated voltage	V_n (V)	400	400	400	400	400
	DC bus voltage	V_{dc} (V)	1000	1000	1000	1000	1000
	Fundamental frequency	f_0 (Hz)	50	50	50	50	50
	Switching frequency	f_{sw} (kHz)	5	5	5	5	5
	Filter inductance	L_f (mH)	1	1	3	5	5
	Filter capacitance	C_f (μF)	100	100	60	30	30
	Isolated transformer series impedance	$\overline{Z}_{eq}$ (Ω)	0.5+j1.22	0.42+j1.01	0.63+j1.52	0.75+j1.82	0.75+j1.82
Droop Control	Active power droop coefficient	m_p	0.31	0.31	0.49	0.82	0.82
	Reactive power droop coefficient	n_q	0.075	0.075	0.12	0.2	0.2
	Power calculation cut-off frequency	ω_c (rad/s)	$2\pi \times 5$	$2\pi \times 5$	$2\pi \times 5$	$2\pi \times 5$	$2\pi \times 5$
Control Loops	Voltage control proportional term	k_{pv}	5	6	9	5	6
	Voltage control resonant (integral) term	k_{iv}	500	300	500	500	300
	Voltage control limiting gain	k_{tv}	0.5	0.5	0.5	0.5	0.5
	Voltage control cut-off frequency	ω_{cv} (rad/s)	2	–	2	2	–
	Current control proportional term	k_{pi}	1000	100	1000	1000	100
Load Parameters							
Type	**Parameter**	**Symbol**	**Load 1**	**Load 2**	**Load 3**	**Load 4**	**Load 5**
Electrical	Rated active power	P_n (kW)	5	45	20	10	20
	Power factor	$\cos\phi$	0.85	0.8	0.9	0.85	0.8

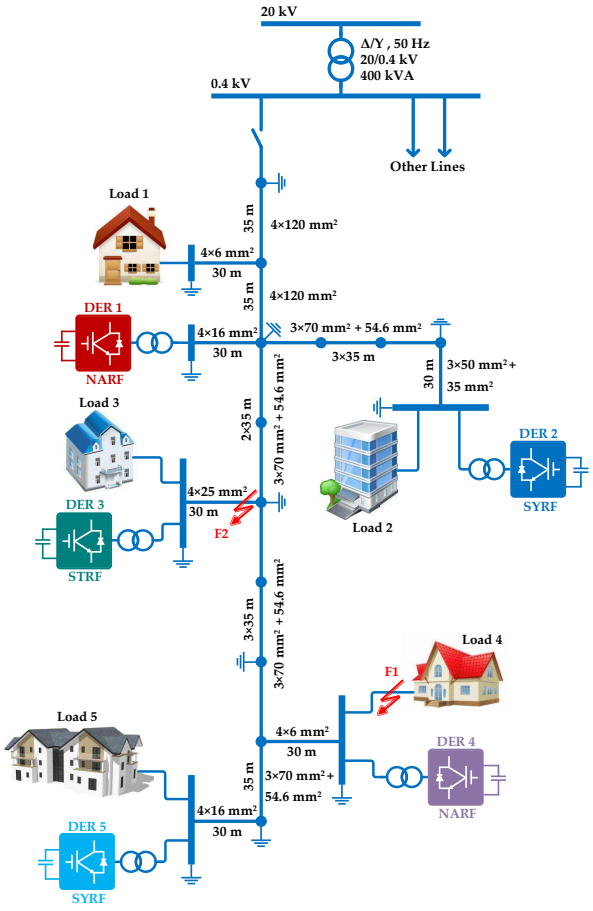

Fig. 9. Modified CIGRE benchmark microgrid.

TABLE VI
PERFORMANCE OF PROPOSED LIMITING STRATEGY FOR CIGRE TEST SYSTEM

Fault Type	**DER**	$\mathbf{THD_V}$ (%)	$\mathbf{THD_I}$ (%)	$i_{L,\max}$ (p.u.)	$v_{o,\max}$ (p.u.)
a-b-c-g	DER 1	1.11	0.3	2	0.86
	DER 2	1.15	0.33	2	0.73
	DER 3	0.83	0.29	2	0.64
	DER 4	1.47	0.27	2	0.38
	DER 5	1.17	0.21	2	0.44
a-b	DER 1	1.24	0.43	2	0.9
	DER 2	1.32	0.48	2	0.93
	DER 3	1.03	0.38	2	0.86
	DER 4	1.8	1.22	2	0.82
	DER 5	1.67	0.79	2	0.85

frames. Also, the latched limit results in (1) poor power quality and some overvoltages in the healthy phase during a single-phase to ground fault in the case of NARF in three-wire configuration, and (2) overvoltage in the healthy phase(s) in the case of an asymmetrical fault when the inverter control system is implemented in SYRF/STRF.

This paper provides a solution for fault management of inverter-based islanded MGs considering the effects of inverter control system, inverter topology, and fault type. The proposed strategy is developed based on the ability of NARF for independent control of each phase. The basic form of proposed limiting strategy has simple design while suffers from voltage magnitude controllability in healthy phase(s) and poor power quality in some conditions. To solve these problems, the

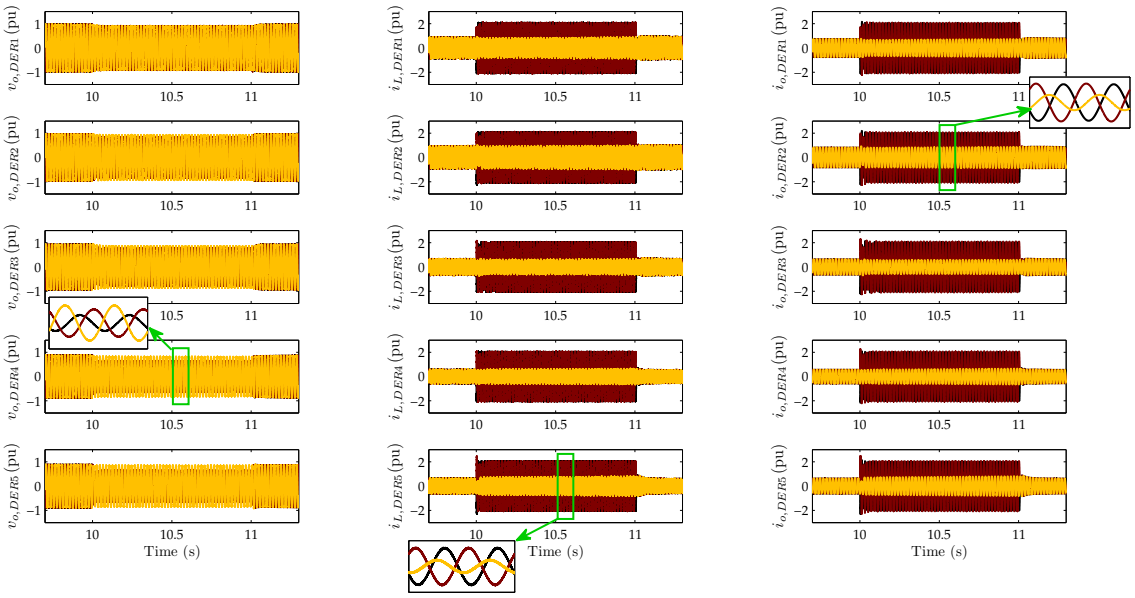

Fig. 10. Output voltage, inductor current, and output current waveforms of the CIGRE test system during an *a-b* fault when the HRFL strategy is used.

hybrid reference frame limiting strategy is proposed in which an auxiliary control system is employed beside the main control system and consequently the voltage magnitude is fully controlled by the droop method in healthy phase(s). The proposed strategy indirectly limits the inverter output voltage by properly limiting inductor current and consequently no voltage limit is required in the inner current control loop.

Several fault scenarios performed on a sample system and CIGRE benchmark microgrid verify the effectiveness of the proposed strategy for limiting output voltage and inductor current and improving the FRT capability of the VSI during both asymmetrical and symmetrical faults. Smooth transition from normal mode to limiting mode and back again is satisfactorily achieved by the proposed strategy. Moreover, as this strategy is based on the calculations in phase coordinates, it can be employed in single-phase VSI application.

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