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Control Strategies for Trap Filter Interfaced Three-Phase Grid Connected Converters

by

Min Huang

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Thesis Title: Control Strategies for Trap Filter Interfaced Three-Phase Grid Connected Converters

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Name of supervisors: Prof. Frede Blaabjerg

Name of co-supervisors: Prof. Poh Chiang Loh

List of publication: Listed in § 1.4

This present report combined with scientific papers which are listed in § 1.4 has been submitted for assessment in partial fulfilment for the Degree of Doctor of Philosophy (Ph.D.) in Electrical Engineering. The scientific papers are not included in this version due to copyright issues. Detailed publication information is provided in § 1.4 and the interested reader is referred to the original published papers. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty of Engineering and Science, Aalborg University.

Preface

First, I would like to show my sincere gratitude to my supervisor, Prof. Frede Blaabjerg, for his continuous guidance and impressive knowledge during the Ph. D. project period. His encouragement and patient guidance I received from during my Ph.D. study will be precious supportiveness for my career and through my future life. Furthermore, I am sincerely grateful to Prof. Poh Chiang Loh for his inspired suggestions and patient corrections of my papers. I also want to show my regards to Xiongfei Wang for his invaluable help to my project and research.

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Min Huang
September, 2015
Aalborg east, Denmark

Abstract

In order to utilize renewable energy systems power electronics are needed to convert the generated energy into the grid. The AC-DC and DC-AC power conversion are dominant in wind power system and photovoltaic system. However, the use of PWM scheme introduces undesirable harmonics and it is necessary to use filter. In order to enhance the grid integration of the renewable energy systems, the filter plays an important role. Even though this topic has already been widely studied, there are many optimizations and problems to be solved, like how to design a filter for grid-connected converters in distributed generation system in order to get a lower loss and higher efficiency? How to solve the stability and robustness problems of high order filter based converters? Are there any ways to obtain a stable and robust system from the control or design?

The main work of the project has studied the above mentioned topics, which is divided into two parts including six chapters. The first part analyzes the design and control of filter-based voltage source converter and the second part investigates the design and stability issues of current source converter with trap filter. The structure of the thesis is constituted by the following chapters:

Chapter 1 presents the motivation and background of the project. Then, the project objectives and the related publication list are addressed. Chapter 2 proposes the modeling of a grid-connected three phase voltage source converter and the converter output spectrum analysis. A basic parameter design is proposed for high order filters and also the stability issues of *LLCL*-filter-based grid-connected inverter with grid current control is analyzed. Chapter 3 investigates the impedance-based active damping methods for voltage source converter with *LLCL* filter. Different active dampers based on *LC* trap are compared. An enhanced filter design method is also described in Chapter 4. The proposed strategy results in a better system performance and also in less sensitivity to the source inductance from the grid even with no damping added to the grid converter. Chapter 5 presents the design and control of the current source converter with *LC* + trap filter. Chapter 6 comes to the conclusion of the thesis.

The main contribution of this project is developing the design and control of the trap concept based filter for voltage source converter and current source converter, which includes: optimized filter design for voltage source converter to improve the robustness and stability considering the delay effect. Investigate different damping methods, including active damping and passive damping in order to stabilize the whole system dealing with resonance issues. Also the *LC* trap filter application for current source converters to reduce the size of the filter and get a higher power factor is studied.

Dansk Resumé

For at udnytte vedvarende energi er der behov for effektelektronik til at omdanne den genererede energi til elnettet. AC-DC og DC-AC konvertering er dominerende i vindkraftsystemer og solcelleanlæg. Men brugen af PWM introducerer uønskede harmoniske, og gør det nødvendigt at anvende et filter. For at øge integration af vedvarende energisystemer i elnettet, spiller filteret en vigtig rolle. Selvom dette emne allerede er blevet bredt studeret, er der mange optimeringer og problemer, der skal løses. F.eks. hvordan designer man et filter til nettilsluttede konvertere i decentrale produktionssystemer for at få et lavere tab og højere effektivitet? Hvordan løses stabilitets- og robusthedsproblemer med højere ordens filtre baserede konvertere? Er der nogen måder at opnå et stabilt og robust system fra kontrollen eller designet?

Hovedarbejdet af projektet har studeret de ovennævnte emner, som er opdelt i to dele, herunder seks kapitler. Den første del analyserer design og kontrol af filterbaserede spændingskilde konvertere og den anden del undersøger design og stabilitet af strømkilde konverter med fælde filter. Strukturen i afhandlingen udgøres af følgende kapitler:

Kapitel 1 præsenterer motivationen og baggrunden for projektet. Derefter er projektets målsætninger og den tilhørende publikationsliste behandlet. Kapitel 2 foreslår modelleringen af en netforbundet trefaset spændingskilde konverter og analysering af konverter udgangsspektrum. Et grundlæggende parameter design for højere ordens filtre er foreslået, og stabilitetsproblemer for *LLCL* filterbaserede nettilsluttede konvertere med netside strømkontrol er også analyseret. Kapitel 3 undersøger impedans-baserede aktive dæmpning metoder til spændingskilde konverter med *LLCL*-filter. Forskellige aktive dæmpere baseret på *LC* fælde sammenlignes. En forbedret filter design metode er også beskrevet i kapitel 4. Den foreslåede strategi resulterer i en forbedret systemydelse og også i mindre følsomhed over for kildeinduktansen fra elnettet, også uden tilføjet dæmpning til netkonverteren. Kapitel 5 præsenterer design og kontrol af strømkilde konverteren med *LC* + fælde filter. Kapitel 6 præsenterer konklusionen af afhandlingen.

Det vigtigste bidrag af dette projekt, er at udvikle designet og kontrollen af det fælde koncept baserede filter for spændingskilde konverter og strømkilde konverter, som inkluderer: optimeret filter design til spændingskilde konverter for at forbedre robustheden og stabiliteten i forhold til forsinkelseffekten. Undersøge forskellige dæmpningwmetoder, herunder aktiv og passiv dæmpning med henblik på at stabilisere hele systemet i forhold til resonans problemer. Også anvendelsen af *LC* fældefilteret for strømkilde konvertere for at reducere størrelsen af filteret og få en højere effektfaktor er undersøgt.

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Journal Papers

J.1 M. Huang, X. Wang, P. C. Loh, F. Blaabjerg and W. Wu, "Stability analysis and active damping for *LLCL*-filter-based grid connected inverter," *IEEJ Trans. Industry App.*, vol. 4, no. 3, pp. 187-195, 2015.

J.2 M. Huang, X. Wang, P. C. Loh, and F. Blaabjerg, "Active damping of *LLCL* filter resonance Based on *LC*-trap voltage or current feedback," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2337-2346, 2016.

J.3 M. Huang, X. Wang, P. C. Loh, and F. Blaabjerg, "*LLCL*-filtered grid converter with improved stability and robustness," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3958-3967, 2016.

J.4 W. Wu, Y. Sun, **M. Huang**, X. Wang, H. Wang, F. Blaabjerg, M. Liserre, H. Chung, "A robust passive damping method for *LLCL* filter based grid-tied inverters to minimize the effect of grid harmonic voltages," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3279-3289, 2014.

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C.1 M. Huang, F. Blaabjerg, W. Wu, Y. Yang, "Step by step design of a high order power filter for three phase three-wire grid-connected inverter in renewable energy system," in *Proc.IEEE PEDG* 2013, pp. 1-8, July, 2013.

C.2 M. Huang, P. C. Loh, W. Wu, F. Blaabjerg, "Stability analysis and active damping for *LLCL*-filter based grid connected inverter," in *Proc. IEEE IPEC* 2014, pp. 2610-2617, May. 2014.

C.3 M. Huang, P. C. Loh, F. Blaabjerg, "The overview of damping methods for three-phase grid tired inverter with *LLCL*-filter," in *Proc. IEEE EPE* 2014, pp. 1-9, Aug. 2014.

C.4 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Resonant-inductor-voltage feedback active damping based control for grid-connected inverters with *LLCL*-filters," in *Proc. IEEE ECCE* 2014, pp. 1194-1201, July, 2014.

C.5 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Active damping of *LLCL*-filter resonance based on *LC*-trap voltage and capacitor current feedback," in *Proc. IEEE APEC* 2015, pp. 2903-2910, March, 2015.

C.6 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Design of *LLCL*-filter for grid-connected converter to improve stability and robustness," in *Proc. IEEE APEC* 2015, pp. 2959 - 2966, March, 2015.

C.7 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Design of the LC + trap filter for a current source rectifier," in *Proc. IEEE EPE* 2015, Sep., 2015.

C.8 Xiongfei Wang, **M. Huang**, H. Bai, P. C. Loh, F. Blaabjerg, "Influence of modulation method on using *LC*-traps with single-phase voltage source converters," in *Proc. IEEE EPE* 2015, Sep., 2015.

C.9 P. Geng, W. Wu, **M. Huang**, F. Blaabjerg, "Efficiency analysis on a two-level three-phase quasi-soft-switching inverter," in *Proc. IEEE APEC* 2013, pp. 1206-1212, Jan. 2013.

C.10 W. Wu, Z. Lin, Y. Sun, X. Wang, **M. Huang**, H. Wang, F. Blaabjerg, H. Chung, "A hybrid damping method for *LLCL*-filter based grid-tied inverter with a digital filter and an RC parallel passive damper," in *Proc. IEEE ECCE* 2013, pp. 456-463, 2013.

C.11 W. Wu, Y. Sun, Z. Lin, **M. Huang**, F. Blaabjerg, H. Chung, "A modified *LLCL*-filter with the reduced conducted EMI noise," in *Proc. IEEE EPE* 2013, pp. 1-10, 2013.

Part I Report

Chapter 1 Introduction

This chapter firstly presents the background and motivation of the Ph.D. project. It also includes a short introduction to grid-connected converters for renewable energy system, followed by the objectives and limitations of the project. Then, the thesis structure is presented to give a better understanding about the flow of this research work. All the publications related to this work are listed at the end of this chapter.

1.1 Background and motivation

1.1.1 Renewable energy sources

In recent years, the research on the renewable energy sources with power electronics converters as interface for distributed generation (DG) systems and energy storage devices has become one of the very popular activities, where the DG systems are usually powered by photovoltaic (PV) cells, wind turbines, wave generators, fuel cells, small hydro and gas powered Combined Heat and Power (CHP) stations [1-3]. Such systems are being developed and installed all over the world. Numerous scenarios projected the levels of renewable energy for 2020, but they are already surpassed by 2010 [4-6]. Today, renewable energy technologies are seen not only as a tool for improving the energy security, but also as a way to mitigate greenhouse gas emissions and to provide direct and indirect social benefits [5]. In order to enable renewable energies like photovoltaic technology and wind turbine systems to be connected to the grid system, power electronics is the key technology [7-9].

Figure 1.1 shows the global new investment in renewable power and fuels for the developed, developing countries and the world in total. It was estimated as to be USD 214.4 billion in 2013, USD 250 billion in 2012 and reach highest record level in 2011[5]. However this is now again increasing. The total new investment in renewable power and fuels was at least USD 270 billion in 2014 including the unreported investments in hydropower projects larger than 50 MW.

For the first time, the world added more solar PV than wind power capacity. Solar PV and hydropower were essentially tied, each accounting for about one-third of new capacity. Solar PV has continued to expand at a rapid rate, with growth in global capacity averaging almost 55% annually over the past five years. The most significant growth occurred in the power sector with the global capacity exceeding 1,560 gigawatts (GW) up more than 8% over 2012. Hydropower rose by 4% to approximately 1,000 GW, and other renewables collectively grew nearly 17% to more than 560 GW.
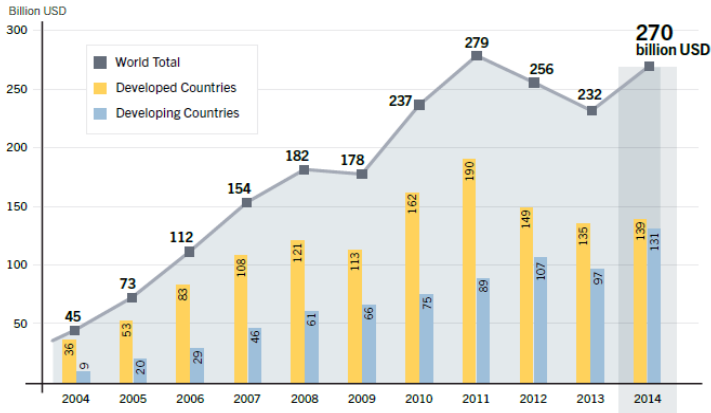
Figure 1.1: Global new investment in renewable power and fuels, developed and developing countries, 2004-2014 [5].
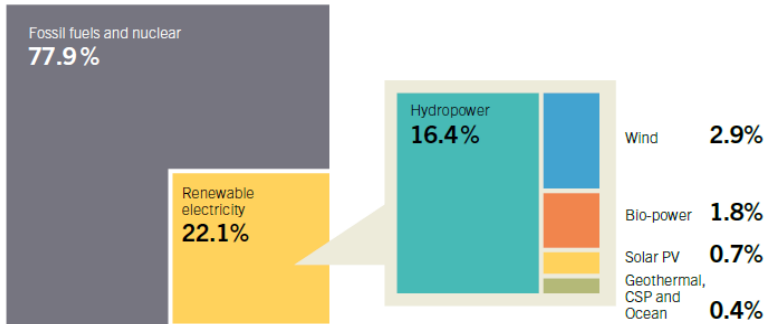
Figure 1.2: Estimated renewable energy share of global electricity production in 2020 [7].

It can be seen from Figure 1.2 that renewable energy accounted for approximately 22%, with 16% provided by hydropower, 2.8% from wind, 0.7% from solar, and 1.8% from biomass [5]. Fossil fuels and nuclear accounted for the most important part, which is around 78.9%. Denmark banned the use of fossil fuel-fired boilers in new buildings as of 2013 and the aim is to provide almost 40% of total heat supply from rewable energy by 2020.

1.1.2 Power converters for distributed generation system

However, in order to utilize these renewable energy systems power electronics are needed to convert the energy to grid. The AC-DC and DC-AC power conversion are the dominant system in wind power system to convert the energy to variable AC voltage and current by generators [10]. In the photovoltaic application, the DC-DC and DC-AC conversions are needed to convert the solar energy to DC voltage or
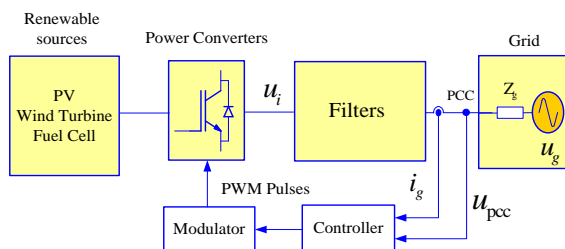
Figure 1.3: Block diagram of a distributed power generation system.

| (a) | (b) |
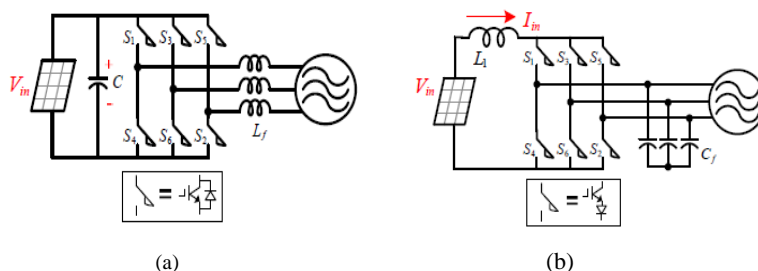
Figure 1.4: Traditional topology of (a) Voltage Source Converter, and (b) Current Source Converter interfaced to the grid with a photovotaicl system as source.

current. Figure 1.3 shows a general block diagram of a distributed power generation system.

This distributed power generation system consists typically of six parts:

(1) Input Power Sources. As shown in Figure 1.3, there are many renewable energy sources, which can be used as the input power for a distributed power generation system. PV cells, wind turbines and fuel cells are the three most used renewable energy sources using grid interfaced converters.

(2) Power Converters. Power converters have made our modern power systems more efficient, more flexible and more sustainable. A wide variety of power converter topologies have been proposed for interfacing distributed energy units to the grid [1, 11-12]. The Current Source Converter (CSC) and Voltage Source Converter (VSC) are two types of the most common converters in the DC-AC or AC-DC power conversion and Figure 1.4 shows the three phase topologies of the VSC and CSC. For VSC, the dc-link voltage is constant with a capacitor in the dc-link. A diode is usually connected in parallel with a switch to conduct the reverse current and short circuit should be avoided for each leg. For CSC, the dc-link current is constant with an inductor. A diode is normally connected in series with a switch to block the reverse voltage and open circuit should be avoided in the circuit.
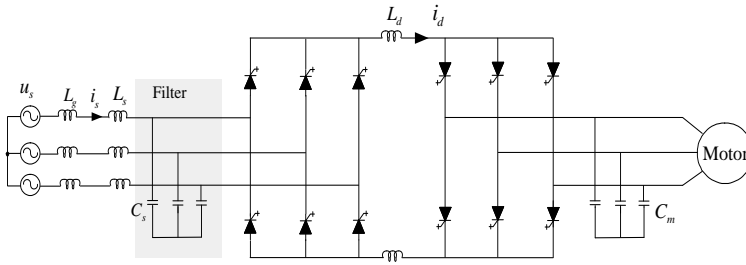
Figure 1.5: Current source drive system.

The recent advances in semiconductor devices and magnetic components technology help current source converters (CSCs) to be considered in many applications such as renewable energy systems, STATCOMs, high-voltage direct current transmission systems, motor drives as shown in Figure 1.5. The Current Source Converter can also serve as an active power filter to compensate the harmonics and reactive components. Refs. [13] and [14] compare the difference between the current source and voltage source shunt active power filters based on theoretical analysis and laboratory prototypes. Compared with CSC-based active power filter, the VSC-based active power filter has better controllability and reliability, but has higher losses [15]. What's more, current source rectifier (CSR) can step down the input voltage and get a lower DC voltage without transformer which can be used as buck rectifier or in parallel operation [16, 17].

The increasing use of VSCs can be found in the transportation electrification, e.g. electric railways [18], electric automobiles [19], and shipboard power systems [20]. CSCs. although not as popular as VSCs, have been widely applied in medium voltage motor drives, wind energy power generation, Superconductor Magnetic Energy Storage (SMES), melting system, and also high-voltage direct current (HVDC) transmission systems [21, 22]. In the medium voltage drive systems, pulse-width modulated (PWM) CSCs have also shown some unique advantages, such as four-quadrant operation, and also an inherent short circuit protection [23-25]. But overvoltage occurs when the current of the dc-link inductor is interrupted due to fault gate drive signals or power shutting off for current source converters. This may cause breakdown and failure for semiconductor.

(3) Filters. The use of PWM schemes introduce undesirable harmonics that may disturb other sensitive loads/equipment on the grid and may also result in extra power losses. Hence, a low-pass power filter is required between the grid converter and the grid to attenuate the high-frequency PWM harmonics to limit the harmonic content of the grid-injected current at the Point of Common Coupling (PCC) [26, 27].
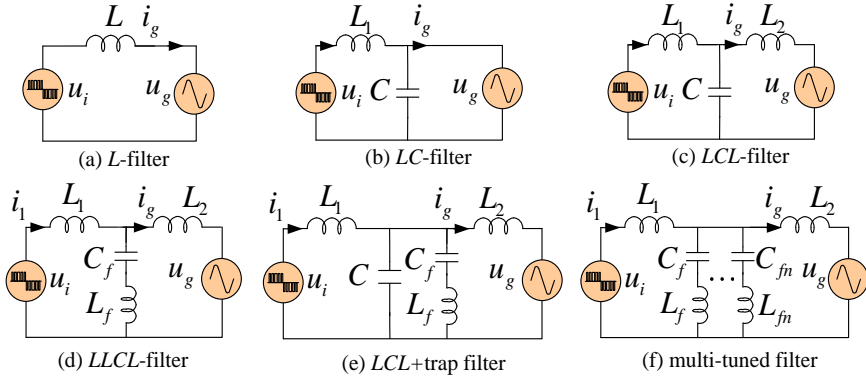
Figure 1.6: Topologies of different filters for voltage source converter.

Typically, a simple series inductor L is used as the filter interface between the power converters in the renewable energy system as shown in Figure 1.6(a). But it only has 20 *dB/dec* attenuation around the switching frequency, so a high value of inductance needs to be adopted in order to reduce the current harmonics, which would lead to a poor dynamic response of the system and a higher power loss. In contrast to the typical *L* filter, *LC* components have 40 *dB/dec* attenuation around the switching frequency which gives a better damping effect. A high order *LCL* filter can even achieve a 60 *dB/dec* harmonic attenuation performance with less total inductance, significantly smaller size and cost, especially for applications above several kilowatts [28, 29]. Recently other topologies have been discussed and are shown in Figure 1.6. It has been demonstrated that the required inductance and capacitance can be further reduced by replacing the middle *C* branch of an *LCL* filter with a series *LC* trap, which is also called an *LLCL* filter [30, 31]. In order to improve the attenuation at the high frequency, the *LC* trap can be paralleled with the *C* branch as shown in Figure 1.6(e) [32, 33]. In order to further reduce the size of the filter, a multi-tuned filter has been proposed [34], but it brings complexity to the circuit and has possible parallel resonances between the multi-tuned traps. High order filters may have resonance problems, which should be solved in order to get a more stable and reliable system.

For the current source converters, an *LC* filter is normally required on the current source rectifier ac input side in order to assist the commutation of the switching device, also to improve the source current waveforms, and also to enhance the power factor. In order to get a higher power factor, the trap concept can also be used for current source converters and the filter topologies are very similar to the voltage source converters.

(4) Grid. Long distance distribution lines will introduce inductive or capacitive impedance to the grid. In the weak grid, the grid impedance is large and in the strong grid, the grid impedance is small. The resonance frequencies of the used high order filters are sensitive to the grid impedance and it can influence the operation of the power converter system [35-37].

(5) Modulator. The deadtime is required to avoid the short circuit of each leg for voltage source converter. There are many modulation methods can be implemented to generate the drive signals. For high power converter system, Selective Harmonic Elimination (SHE) modulation can effectively reduce the low order harmonic distortion for current source converter when the switching frequency is several hundred Hertz. But the traditional SHE is an offline modulation with calculated switching angles which can not compensate the grid background harmonics. Online modulation methods like Carrier based Modulation (CM) and Space Vector Modulation (SVM) can achieve fast dynamic response and especially be implemented in a relatively higher switching frequency [38]. Due to the commutations, an overlap-time of the switches is required to ensure a continuous current flow, which can be realized by delaying a sufficient turn off time [39].

(6) Controller. Many control strategies have been proposed and implemented including deadbeat control [40], repetitive control [41], adaptive control [42], H-infinity control [43] and classical proportional integral (PI) and proportional resonant (PR) control [44-46]. PI and PR control methods are mainly discussed in this thesis. PR can provide a larger gain at the fundamental frequency to eliminate the steady state error compared with PI regulator and Harmonic Compensation (HC) performs well to reject the grid harmonic distortion [46].

1.2 Project objectives and limitations

1.2.1 Problem statement and objectives

In order to reduce the current harmonics around the switching frequency, a large input inductance may be connected in the system. But a large inductance will reduce the system dynamics and the operation range of the converter and also increase the dc-voltage. In order to enhance the grid integration of the renewable energy systems, the filter plays an important role in close relation with the current controller. Even though this topic has already been widely studied, there are many optimization methods and still problems need to be solved.

The overall objective is to study the interaction between the passive filter and controller in order to ensure good control performance, stability, high efficiency, and good power quality. Following sub-topics are:

- *Many filter types can be used and they have their advantages and disadvantages in different applications. How to design a filter for grid-connected converters in distributed generation system in order to get small size and low losses?*
- *How to solve the stability and robustness problems of the high order filter based converters? Can it be solved from the filter design or from the system control?*
- *Many active damping methods and passive damping methods for the filter resonance problem exist. Are there any ways to compare them as well as find the best solution?*
- *The resonance of the filter is influenced by the grid and hence the stability and reliability are influenced. Are there any ways to obtain a stable and robust system from the control or design at varying grid impedance?*
- *How to design the trap filter for current source converter and also solve potential resonance problems?*

The objectives of this project are listed in details.

(1) Design high-order filter for grid-connected converters in distributed generation system.

Many researches have focused on the filter design in order to get a high harmonic attenuation of the harmonics and also a smaller size to reduce the cost. It is still necessary to propose a simple design procedure to make this clear. The research aims to include the filtering characteristics and the parameter design criteria of the filter, as well as the controllers like the proportional-resonant indirect current control strategy and the Proportional-Resonant direct current control strategy with or without damping. A high-order filter with trap circuit is mainly studied in order to get a smaller filter size. At the same time, the stability and robustness of the system can be improved. But the components are influencing each other as the passive components will have parameter variation due to the usage and their wear-out. The deviation can be studied by assuming a +20% change of the capacitor, and a ±20% variation of the inductor.

(2) Investigate different damping methods, including active damping and passive damping in order to stabilize the whole system in terms of stability.

Focus is on the current control technique for a three-phase grid-tied converter. The higher order resonance introduces a potential instability to the overall system, which should be properly damped either passively or actively. Different damping methods have their advantages and disadvantages. However, in digital-controlled systems, sampling and transport delays caused by controller and the PWM modulation will affect the system stability and should be taken into account.

(3) Robustness of the system in respect to the grid parameter variations.
Depending on the grid configuration, a large variation of grid impedance values can challenge the control of the inverter and the grid filter design in terms of stability. The research goal of this thesis is to find the optimum method to design a filter or controller, which is not sensitive to the grid parameters.
Both simulations and experiments are done in order to verify it.

1.2.2 Project Limitations

The performance and comparisons of the control methods under different grid disturbances are investigated by MATLAB/ Simulink, where PLECS Blockset is used to build the electrical circuit of the converter system and Simulink toolboxes are used to develop the control systems. The PLECS software is known as high speed simulation tools for power electronics circuits. The experimental system is limited to a single system based on a Danfoss FC302 converter connected to the grid through an isolating transformer. DC-link of the converter is tied to a Delta Elektronika power source, and its control is realized with a dSPACE DS1103 controller and DS1007 controller. The board is connected to a FPGA device, which is linked to the driver by optic fibre.

In order to make sure the outcome of this research is applicable for different types of the renewable energy sources, the proposed trap filter design and the simulations are carried out on a traditional topology. In order to simplify the research objects and build a filter interfaced power converter in the toolbox of Simulink. Then simulation can be carried out by using basic control methods to get system stable. The design and control methods developed in this thesis can later be adopted for other topologies and applications. All the filter components used for the experimets may have parasitic resistances, which are not measured.

1.3 Thesis outline

The research of this project is organized in the form of a Ph. D. thesis. The thesis includes a report of the project findings and a collection of the related publications to show the details through the entire research work. The report is a brief summary of the project, which is divided into six chapters. The structure of the report is constituted by the following chapters:

Chapter 1. Introduction
This chapter presents the background and the motivation of the project. Then, the project objectives and the related publication list are addressed.

Chapter 2. Filter Design and Stability Analysis for Voltage Source Converters in Distributed Generation System

In this chapter, a grid-connected three phase voltage source converter with *LLCL* filter is modelled and the converter output voltage spectrum is analyzed. Then, a basic design method for high order filter is proposed. However, the stability of the high order based grid-connected inverter is analyzed and a critical resonant frequency for the *LLCL* filter is identified, when sampling and transport delays are considered. In the high-resonant-frequency region, active damping is not required; in the low-resonant-frequency region active damping is necessary.

Chapter 3. Impedance-Based Active Damping Methods for Voltage Source Converters

This chapter investigates the capacitor current feedback and *LC*-trap voltage feedback for *LLCL* filter with its limitations clarified with and without considering the delays. The characteristic equivalent circuits for all active dampers are also derived, which are based on formulated impedance transfer functions. Simulation and experimental results are given in order to verify the analysis. A simple proportional damper is used with much faster dynamics and less anticipated complications compared to other more advanced techniques.

Chapter 4. Design of LLCL-Filtered Grid Converter with Improved Stability and Robustness

This chapter proposes a new filter design method for *LLCL* filter from the point of stability and robustness of the overall system. The design procedure is also described. It is thus an enhanced method even with no damping added to the grid converter. The parameter design method can also be applied to the lower order *LCL* filter with only a slight modification needed. The proposed strategy results in a better system performance and also less sensitivity to the source inductance from the grid.

Chapter 5. Trap Filter application for Current Source Converters

This chapter proposes a series *LC* and paralleled *LC* trap filter for current source converters to reduce the size of the filter and to get a higher power factor. Different from the voltage source converter, the current source converter using PWM modulation generate discontinous current. Hence, the filter design method should consider the voltage ripple. The trap filter effects at the selected frequency are analyzed using SVM modulation. This chapter also briefly investigates the passive and active damping methods to damp out the *LC* resonances with the proposed trap filters. Virtual impedance control can also be applied to the current source converter. With an increased switching frequency, the control loop and damping method are easier to design.

Chapter 6. Conclusions

This chapter gives the conclusions and summarizes the main contributions of the project. Also, future researches based on the project are presented.

1.4 Selected papers of publications

The research outcomes of this thesis are disseminated via a number of papers published in conference proceedings and journals. A list of the papers derived from this project, which are published till now or have been submitted, is given as follows:

J.1 M. Huang, X. Wang, P. C. Loh, F. Blaabjerg and W. Wu, "Stability analysis and active damping for *LLCL*-filter-based grid connected Inverter," *IEEJ Trans. Industry App.*, vol. 4, no. 3, pp. 187-195, 2015.

J.2 M. Huang, X. Wang, P. C. Loh, and F. Blaabjerg, "Active damping of *LLCL*-filter resonance based on *LC*-trap voltage or current feedback," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2337-2346, 2015.

J.3 M. Huang, X. Wang, P. C. Loh, and F. Blaabjerg, "*LLCL*-filtered grid converter with improved stability and robustness," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3958-3967, 2016.

C.1 M. Huang, F. Blaabjerg, W. Wu, Y. Yang, "Step by step design of a high order power filter for three phase three-wire grid-connected inverter in renewable energy system," in *Proc.IEEE PEDG* 2013, pp. 1-8, July, 2013.

C.2 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Resonant-inductor-voltage feedback active damping based control for grid-connected inverters with *LLCL*-filters," in *Proc. IEEE ECCE* 2014, pp. 1194-1201, July, 2014.

C.3 M. Huang, P. C. Loh, W. Wu, F. Blaabjerg, "Stability analysis and active damping for *LLCL*-filter based grid connected inverter," in *Proc. IEEE IPEC* 2014, pp. 2610-2617, May. 2014.

C.4 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Active damping of *LLCL*-filter resonance based on *LC*-trap voltage and capacitor current feedback," in *Proc. IEEE APEC* 2015, pp. 2903-2910, March, 2015.

C.5 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Design of *LLCL*-filter for grid-connected converter to improve stability and robustness," in *Proc. IEEE APEC* 2015, pp. 2959 - 2966, March, 2015.

C.6 M. Huang, Xiongfei Wang, P. C. Loh, F. Blaabjerg, "Design of the *LC* + trap filter for a current source rectifier," in *Proc. IEEE EPE* 2015, Sep., 2015.

Chapter 2 Filter Design and Stability Analysis for Voltage Source Converters in DG System

This chapter firstly introduces different filter types. Then a basic filter design method is given for high order filter based on grid current harmonics limitation. Also, the stability of the high order based grid-connected inverter is analyzed and a critical resonant frequency for the *LLCL* filter is identified when sampling and transport delays are considered. In the high-resonant-frequency region, active damping is not required; in the low-resonant-frequency region active damping is necessary.

2.1 Introduction

As discussed in Chapter 1, due to the energy crisis, the Distributed Generation (DG) systems using clean renewable energy sources like solar, wind, etc., have become an important issue in the technical research. These renewable sources are connected to the power grid through grid-connected converters, which with the advancement of semiconductor technology, are almost always switching at high frequencies. Such switching with rapid state transitions and the use of pulse width modulation (PWM) introduces undesirable harmonics [28]. Hence, a low-pass power filter is inserted between the Voltage Source Inverter (VSI) and the grid to attenuate the high-frequency PWM harmonics to a desirable limit.

Typically, an *L* filter is adopted to attenuate the switching harmonics. But a high value of inductance needs to be adopted to reduce the current harmonics around the switching frequency, which would lead to a poor dynamic response of the system and also more power losses. In contrast to the typical *L* filter, a high order filter can achieve a high harmonic attenuation performance with less total inductance (L_1+L_2), with smaller size and cost due to the high harmonics [48-50]. Figure 2.1 shows the structure of three-phase three-wire grid-connected inverter with different high order filters: *LCL* filter, *LLCL* filter with one trap [30] and *LLCL* filter with two traps [31].

The applications of *LLCL* filter for a three-phase three-wire Shunt Active Power Filter (SAPF) [51] and a Large-Scale Wave Power Plant [52] have been analyzed. Ref. [34] has analyzed the character of multiple shunt RLC trap filters, but detailed design procedures are not given. Ref. [28] presented a design procedure using a trial and error method. Some other *LCL* filter design guidelines, criteria and optimizing
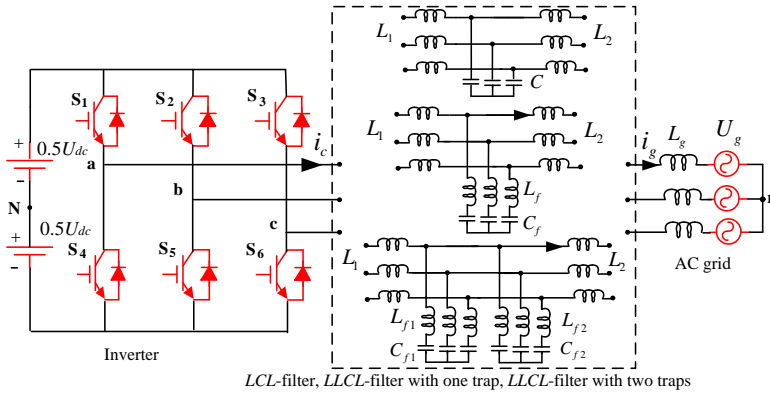
Figure 2.1: Structure of three-phase three-wire inverter with different high order filters.

processes were also proposed in [53-56]. However, the design principle and method of the three-phase three-wire power filter need to be further described in detail even though there are a vast of majorities in literature that introduce the *LCL* filter and *LLCL* filter design for grid interface converter [31, 32].

The middle *LC*-trap of the Filter in the Figure 2.1 is star or wye configured, but it can also be delta-configured, if preferred. The star configuration may however be more attractive, because of its smaller inductance requirement, and hence smaller accompanied parasitic resistance.

But for high order filters, they many have resonant problems. To suppress the possible resonances of an *LCL* filter or *LLCL* filter, active damping [57, 66] or passive damping [67-71] methods can be adopted. Passive damping is realized by adding additional components in the system but it causes a decrease of the overall system efficiency. Due to high efficiency and flexibility, the active damping method might be preferred, although at the risk of higher cost of sensors and more control complexity. Normally, the digital sampling and transport delays caused by the controller and modulation, as well as discretization effects should be taken into account.

2.2 Inverter-side current harmonic analysis for a three-phase voltage source inverter

The lower limit of the filter inductance is determined by the harmonic requirement of the grid-injected current according to IEEE 519-1992 [72], and as specified in Table 2.1 I_g is the nominal grid-side fundamental current. The harmonic currents can be calculated by the corresponding harmonic voltage amplitudes at different harmonic frequencies to the impedance characteristic of the filter.

Table 2.1:   Maximum permitted harmonic current distortion in percentage of current I_g according to *IEEE* 519-1992.

Individual Harmonic Order h	$h<11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 < h$	THD
Percentage (%)	4.0	2.0	1.5	0.6	0.3	5.0

(a)   (b)
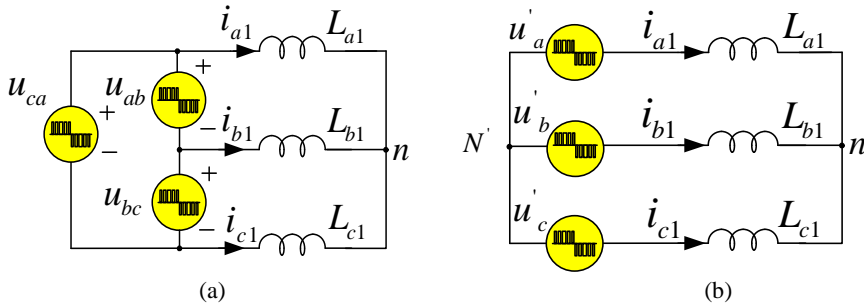
Figure 2.2: Simplified three-phase voltage source inverter with (a) line to line voltage in high frequency, (b) equivalent output voltage sources.

In this chapter, only asymmetrical regular sampled Sinusoidal Pulse Width Modulation (SPWM) will be discussed, but the method presented can also be applied to other modulation techniques with slight modifications according to the output voltage characteristics.

In the SPWM mode, the amplitude of the inverter phase voltage harmonics based on the Bessel functions is given as the following [73]:

$$u_{aN}(n,m) = \left| \frac{2U_{dc}}{\pi} \frac{1}{m} J_n \left(m \frac{\pi}{2} M \right) \sin \left(\frac{(m+n)\pi}{2} \right) \right| \qquad (2.1)$$

where $u_{aN}(n,m)$ is the amplitude of the phase voltage harmonic; M is the modulation index; U_{dc} is the DC link voltage; m is carrier band number $[1, \infty)$; n is side band number $(-\infty, +\infty)$ and $Jn(x)$ is referred as the integrals of the Bessel function, which is expressed as $J_n(x) = (1/\pi) \int_0^\pi \cos(n\pi - x\sin\tau)d\tau$, showing the different sideband harmonic magnitude.

Usually, a three-phase three-line inverter is divided into three equal single phase circuits to analyze the amplitude of the inverter current harmonics. Figure 2.1 can be simplified as shown in Figure 2.2(a), where u_{ab}, u_{bc} and u_{ca} are three phase line voltages; L_{a1}, L_{b1} and L_{c1} are converter-side inductors; i_{a1}, i_{b1} and i_{c1} are inverter-side currents in three-phase respectively.
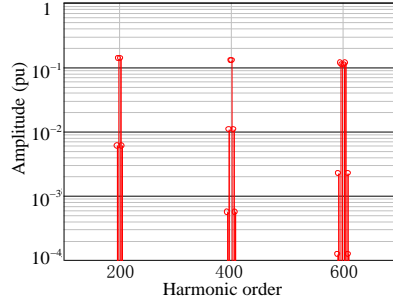
Figure 2.3: Line to line output switched voltage spectrum when M is 0.9, U_{dc} is 700V, f_{sw} is 10 kHz and fundaental frequency is 50 Hz.

According to the inverter three phase voltage functions [73], the output line to line voltage u_{ab}, u_{bc} and u_{ca} can be derived as (2.2):

$$u_{ab} = \frac{\sqrt{3}}{2}U_{dc}M\cos(\omega_0 t + \frac{\pi}{6}) + \frac{4U_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\cdot\sin\left[\frac{(m+n)\pi}{2}\right]\sin n\frac{\pi}{3}\cos\left[m\omega_s t + n(\omega_o t - \frac{\pi}{3}) + \frac{\pi}{2}\right]$$

$$u_{bc} = \frac{\sqrt{3}}{2}U_{dc}M\cos(\omega_0 t - \frac{\pi}{2}) + \frac{4U_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\cdot\sin\left[\frac{(m+n)\pi}{2}\right]\sin n\frac{\pi}{3}\cos\left[m\omega_s t + n\omega_o t - \frac{\pi}{2}\right]$$

$$u_{ca} = \frac{\sqrt{3}}{2}U_{dc}M\cos(\omega_0 t + \frac{5\pi}{6}) + \frac{4U_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\cdot\sin\left[\frac{(m+n)\pi}{2}\right]\sin n\frac{\pi}{3}\cos\left[m\omega_s t + n(\omega_o t + \frac{\pi}{3}) + \pi\right]$$

$$(2.2)$$

where ω_s and ω_o are the switching frequency and fundamental switching frequency in radians per second, respectively. For a symmetrical three-phase circuit, three-phase line to line voltage can be converted into three-phase phase voltage, as shown in Figure 2.2(b). The equivalent phase voltage can be derived as given in (2.3):

$$u'_a = \frac{u_{ab}}{\sqrt{3}}\angle -30°, \; u'_b = \frac{u_{bc}}{\sqrt{3}}\angle -30°, \; u'_c = \frac{u_{ca}}{\sqrt{3}}\angle -30° \tag{2.3}$$

Note that the neutral point of "N'" is the equivalent neutral point, which is obtained from the balanced three inverter-side line to line voltages and it is different from the neutral point of "N" as labeled in Figure 2.1 and Figure 2.2(a).

According to (2.2), the main harmonics spectrum magnitudes (p.u.) of the line to line inverter output voltage by the sinusoidal pulse-width modulated waveform (SPWM) from the voltage source inverter are shown as an example in Figure 2.3 under the condition that the modulation index M is 0.9, U_{dc} is 700V, converter-side inductance L_1 is 2.4 mH, the switching frequency f_{sw} is 10 kHz and the fundamental frequency is 50 Hz.
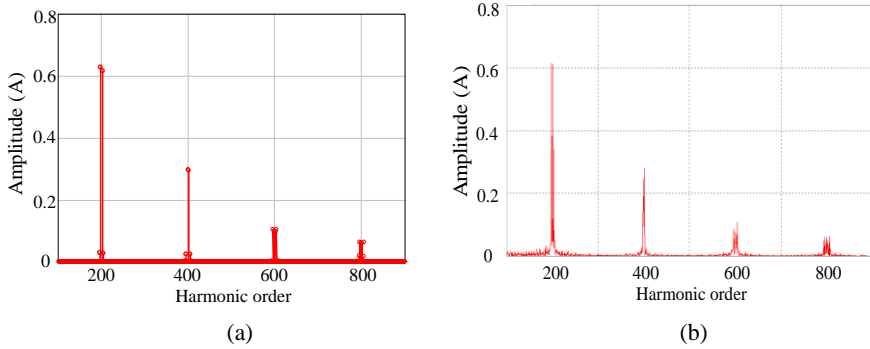
Figure 2.4: Harmonic spectrum of output current of voltage source inverter when M is 0.9, U_{dc} is 700V, f_{sw} is 10 kHz and f_o is 50 Hz (a) the calculated result and (b) the simulated result.

The amplitudes of the equivalent inverter output voltage harmonics $\left|U_A(n,\ m)\right|$ and the ideal amplitudes of the converter-side current harmonic $\left|I_{AM}\right|$ can be derived:

$$\left|U_A(n,m)\right| = \frac{\left|4U_{dc}J_n\left(m\frac{\pi}{2}M\right)\sin\left[(m+n)\frac{\pi}{2}\right]\sin\left(n\frac{\pi}{3}\right)\right|}{\sqrt{3}\left|m\pi\right|} \tag{2.4}$$

$$\left\|I_{AM}\right\|_{\omega \neq \omega_o} = \frac{\left|U_A(n,m)\right|}{\left|Z_1(j\omega)\right|} \tag{2.5}$$

Since the angle does not change the spectrum of the amplitude, the voltage spectrum of the equivalent phase voltage, u'_a, can also be depicted in Figure 2.2 based on (2.3). The harmonic currents can be calculated by the corresponding harmonic voltage amplitudes at different harmonic frequencies, as shown in Figure 2.4 (a). Figure 2.4 (b) shows the simulated result, which is almost the same as the calculated results. Hence, the proposed method of the equivalent output phase voltage based on line to line voltage spectrum is accurate for designing the high order output filter.

2.3 Design procedure of the high order filter

Some design limitations must be addressed as discussed in [28, 30]. The three-phase three-line high order filter design procedure can be derived as:

1) In order to meet a specific current ripple requirement, the inductance can be calculated from the equation [74]:

$$L_1 \geq \frac{U_{dc}}{8 f_{sw} (\alpha I_{ref})} \tag{2.6}$$

where I_{ref} is the rated reference peak current, f_{sw} is the switching frequency, α is the inverter-side current ripple ratio, which generally is lower than 40% for *LCL* filter [4]; *α* can be up to 60% for an *LLCL* filter as it has a better harmonic attenuation at the converter switching frequency [32].

2) Select the total capacitance to achieve the maximum reactive power absorbed at rated conditions from the grid.

$$\left(C_{f1} + C_{f2}\right) \leq 0.05 C_b \tag{2.7}$$

3) Decide the resonant circuit. Since the L_{f1}-C_{f1} and L_{f2}-C_{f2} circuit has a low impedance at the switching frequency and the double of the switching frequency, then, L_{f1} and L_{f2} can be calculated as:

$$\frac{1}{\sqrt{L_{f1} C_{f1}}} = \omega_s, \frac{1}{\sqrt{L_{f2} C_{f2}}} = \omega_{s2} \tag{2.8}$$

where ω_{s2} is twice of the switching frequency in radians per second.

4) Selection of L_2.

For the *LCL* filter L_2 has the objective to attenuate each harmonic around the switching frequency down to 0.3% as given in Table 2.1. Then it can be described as given in (2.9):

$$\frac{\frac{4U_{dc}}{3\sqrt{3}\pi} \times \max\left(\left|J_2\left(\frac{\pi}{2}M\right)\right|, \left|J_4\left(\frac{\pi}{2}M\right)\right|\right) \times \left|G_{u_i \to i_g}(j\omega_s)\right|_{L_{f1,2}=0}}{I_{ref}} \leq 0.3\% \tag{2.9}$$

where J_2 (1/2πM) and J_4 (1/2πM) are the Bessel functions corresponding to the 2nd and 4th and the sideband harmonics at the switching frequency.

For an *LLCL* filter with one trap based three-phase inverter, the uppermost harmonics will appear around the double of the switching frequency.

$$\frac{\frac{4U_{dc}}{3\sqrt{3}\pi} \times \max\left(\left|J_1\left(\pi M\right)\right|, \left|J_5\left(\pi M\right)\right|\right) \times \left|G_{u_i \to i_g}(j2\omega_s)\right|_{L_{f2}=0}}{I_{ref}} \leq 0.3\% \tag{2.10}$$

where J_1 (πM) and J_5 (πM) are the Bessel functions corresponding to the 1st and 5th sideband harmonics at the double of the switching frequency.

For an *LLCL* filter with two traps based three-phase inverter, the uppermost harmonics will appear around the triple of the switching frequency.

$$\frac{\frac{4U_{dc}}{3\sqrt{3}\pi} \times \max\left(\left|J_2\left(\frac{3}{2}\pi M\right)\right|, \left|J_4\left(\frac{3}{2}\pi M\right)\right|, \left|J_8\left(\frac{3}{2}\pi M\right)\right|\right) \times \left|G_{u_i \to i_g}(j3\omega_s)\right|}{I_{ref}} \leq 0.3\% \quad (2.11)$$

where J_2 $(3/2\pi M)$, J_4 $(3/2\pi M)$ and J_8 $(3/2\pi M)$ are the Bessel functions corresponding to the 2nd, 4th and 8th sideband harmonics at the triple of the switching frequency.

5) Verify the resonance frequency obtained. Due to inductors L_{f1} and L_{f2} are small, the resonant frequency ω_r can be derived approximately to be:

$$\omega_r \approx \frac{1}{\sqrt{\left(\frac{L_1 L_2}{L_1 + L_2}\right)(C_{f1} + C_{f2})}} \quad (2.12)$$

It is necessary to check whether the resonant frequency is in a range between ten times the line frequency and one-half of the switching frequency, $10f_o \leq f_r \leq 0.5 f_{sw}$. If not, the parameters should be re-selected from step 2.

2.4 Filter Design Example

Under the rated condition of that $f_{sw} = 10$ kHz, $U_{dc} = 700$V, $P_{rated} = 6$ kW, the grid phase to phase voltage is 400 V/50 Hz, and the sine-triangle, and asymmetrical regular sampled PWM are applied, design examples of the *LCL* filter and *LLCL* filter are given as the following:

1) Based on the constraint of the total inductor and inverter-side current ripple, a 30% current ripple can be obtained to design L_1. Then the inverter-side inductor is selected to be 2.4 mH.

2) The total capacitor value is designed as 4 μF to limit the reactive power which should meet the constraint of 5%. Then, the capacitance of C_{f1} and C_{f2} are set to the same.

3) Based on (2.9), (2.10) and (2.11), the value of L_2 for the three types of high order filters can be calculated. L_2 is selected to be 0.25 mH for the *LLCL* filter with two traps, 1.2 mH for *LLCL* filter with one trap and 2.4 mH for *LCL* filter according to the functions to calculate them.

4) For the *LC* resonant circuits, L_{f1} and L_{f2} can be chosen based on the chosen capacitors and the switching frequency.
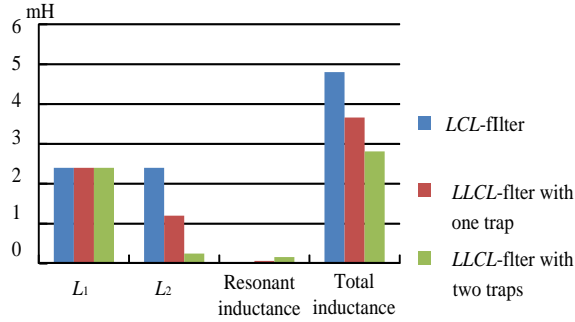
Figure 2.5: Comparisons of different inductors in the three designed cases.

Table 2.2:   Filter parameters for voltage source inverters.

Filters	Parameters		Values
LLCL filter (two *LC* traps)	Converter side inductor	L_1	2.4 mH
	Grid side inductor	L_2	0.25 mH
	Resonant circuit inductor	L_{f1}	128 µH
	Resonant circuit inductor	L_{f2}	32 µH
	Resonant circuit capacitor	C_{f2}	2 µF
	Resonant circuit capacitor	C_{f1}	2 µF
LLCL filter (one *LC* trap)	Converter side inductor	L_1	2.4 mH
	Grid side inductor	L_2	1.2 mH
	Resonant circuit inductor	L_f	64 µH
	Resonant circuit capacitor	C_f	4 µF
LCL filter	Converter side inductor	L_1	2.4 mH
	Grid side inductor	L_2	2.4 mH
	Filter capacitor	C	4 µF

Table 2.2 shows the parameters of the designed filters. Figure 2.5 shows the calculated inductance for three cases. Compared with the *LCL*-filter, under sine-triangle, and asymmetrical regular sampled PWM, the total inductance of *LLCL* filters with one trap and two traps can be reduced by 25% and 40% respectively. The *LLCL* filter with two *LC* traps can reduce the grid-side current ripple at the switching frequency and the double of the switching frequency, but it makes the circuit more complicated.

2.5 Stability analysis of *LLCL*-filter-based grid-connected inverter

The basic design method for high order filters and size comparison has been illustrated. In terms of size and volume, the *LLCL* filter is proper choice compared to other high order filters. In addition to an active damping method, the Proportional -
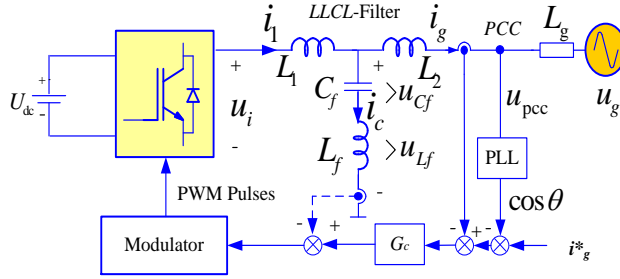
Figure 2.6: General control structure of three-phase *LLCL*-filter-based grid-connected inverter with.capacitor current feedback.
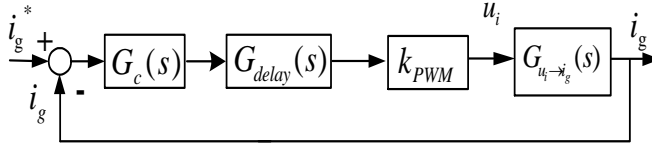
Figure 2.7: Block diagram of grid current feedback control.

Resonant (PR) controller is also used in this chapter to control the current. PR can provide larger gain at the fundamental frequency in order to eliminate the steady state error compared with PI regulator [75, 76].

2.5.1 Modeling of *LLCL*-filtered grid-connected inverter

Figure 2.6 illustrates a grid converter powered by dc voltage U_{dc} and filtered by a *LLCL* filter comprising L_1, L_2, L_f and C_f. L_g is the grid impedance. The converter output voltage and current are notated as u_i and i_1, whose values are determined by only a single feedback loop for regulating the grid current i_g. u_{Cf} is the output voltage of the capacitor, u_{Lf} is the output voltage of the resonant inductor, u_c is the voltage of L_f-C_f circuit and u_g is the grid voltage.

The inverter system in one phase can be represented as following:

$$\begin{cases} L_1 \dfrac{di_1}{dt} = u_i - u_{Cf} - u_{Lf} \\[2mm] \left(L_2 + L_g\right)\dfrac{di_g}{dt} = u_{Cf} + u_{Lf} - u_g \\[2mm] C_f \dfrac{du_{Cf}}{dt} = i_1 - i_g \\[2mm] u_{Lf} = L_f \left(\dfrac{di_1}{dt} - \dfrac{di_g}{dt}\right) \end{cases} \quad (2.13)$$
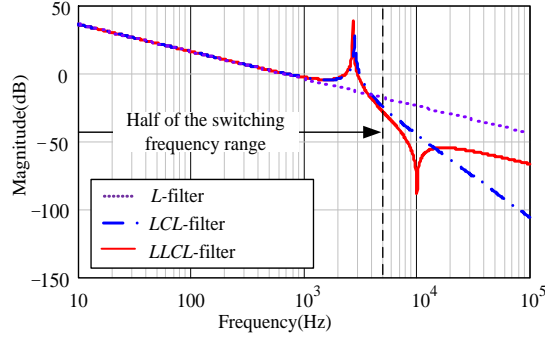
Figure 2.8: Bode plots of transfer functions i_g (s) / u_i (s) for different filters.

Figure 2.7 shows the block diagram for the control loop. $G_c(s)$ is a PR controller for tracking the reference $i_g{}^*$ as shown in (2.14), where k_p and k_i are representing its proportional gain and the integral gain of the fundamental resonant frequency respectively. $G_{delay}(s)$ represents computational and modulation delays. The open loop transfer functions i_g (s) / u_i (s) is expressed in (2.15)

$$G_c(s) = k_p + \frac{k_i s}{s^2 + (\omega_0)^2} \tag{2.14}$$

$$G_{u_i \to i_g}(s) = \frac{i_g}{u_i} = \frac{L_f C_f s^2 + 1}{\left[L_1 L_2 C_f + (L_1 + L_2) L_f C_f \right] s^3 + (L_1 + L_2) s} \tag{2.15}$$

Figure 2.8 shows bode plots of transfer functions i_g (s) / u_i (s) for different filters. For *L* filter, $L = 3.6$ mH. For *LCL* filter, $L_1 = 2.4$ mH, $L_2 = 1.2$ mH and $C_f = 4$ μF. For *LLCL* filter, $L_1 = 2.4$ mH, $L_2 = 1.2$ mH, $L_f = 64$ μH and $C_f = 4$ μF. The characteristics of the three filters at the low frequencies are similar. The dominant harmonics of the grid-side current of the *LLCL* filter will be around the double of the switching frequency since the harmonics around the switching frequency are attenuated by the trap circuit L_f-C_f. That is the reason that the *LLCL* filter has a smaller inductance or capacitance than the *LCL* filter when they meet the same harmonic requirement of the grid-injected current.

The resonant frequency of the *LLCL* filter can be higher than the resonant frequency of the *LCL* filter due to a smaller size. The ratio of the resonant frequency and the sampling frequency is related to the stability of the *LCL* filter due to the delay. It means that if an *LCL* filter with high resonance frequency is chosen the design of the active damping gets more difficult and a poorer robustness is obtained.

Table 2.3: *LLCL*-filter parameters and resonant frequency of the three cases under study.

Case I	Case II	Case III
L_1=2.4 mH	L_1=2.5 mH	L_1=3 mH
L_2=1.2 mH	L_2=2 mH	L_2=2.4 mH
C_f= 2 μF	C_f= 8 μF	C_f= 8 μF
L_f= 128 μH	L_f= 32 μH	L_f= 32 μH
f_r=3.69 kHz	f_r=1.67 kHz	f_r=1.52 kHz
f_r/f_s =0.369	f_r/f_s =0.167	f_r/f_s =0.153

2.5.2 Stability of *LLCL*-filter-based grid-connected inverter with different resonant frequencies

T_s is the sampling period. The inverter can be modeled as a linear gain k_{PWM}, expressed as $k_{PWM} = 0.5U_{dc}$. In the s-domain one sample period delay $e^{-T_s s}$ is included due to computation in a real application. When the PWM reference is held on and compared to the triangular carrier to generate the duty cycle, a Zero-Order-Hold (ZOH) is in series of the open loop and discretization of the system introduces a delay [60], as shown in (2.16). A PWM delay of a half sampling period is introduced. Hence, the total delay in the continuous form is shown in (2.17). $G(s)$ is the open transfer function of the grid current feedback control.

$$G_{ZOH}(s) = \frac{(1-e^{-T_s s})}{s} \simeq T_s e^{-j0.5\omega T_s} \tag{2.16}$$

$$G_{delay}(s) = e^{-1.5T_s s} \tag{2.17}$$

$$G(s) = G_{delay}(s)k_{PWM}G_c(s)G_{u_i \to i_g}(s) \tag{2.18}$$

Table 2.3 shows three different cases with different resonant frequencies. f_r is the resonance frequency. Figure 2.9 shows the bode plot of the forward path transfer function for the grid current feedback control. It can be seen from Figure 2.9 that the *LLCL* filter resonance has no influence on the system stability, when the resonant frequency is high (Case I), because the phase is already well below -180° before the resonant frequency due to the sampling and transport delay. When the resonant frequency is low (Case III), the phase curve passes through -180° at the resonant frequency and the system is not stable without damping. When active damping is added in Case III, the resonance is damped and the system can be stable. This analysis identifies that there is also a critical resonant frequency for the *LLCL*-filter, and above it, active damping can be avoided by adjusting the controller gain. When
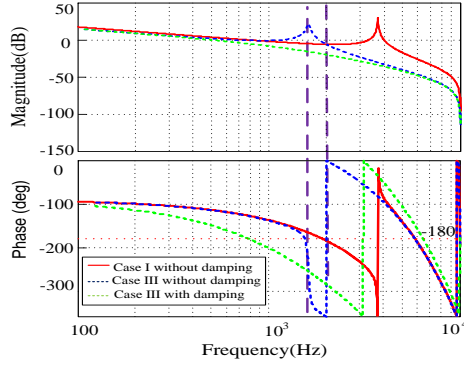
Figure 2.9: Bode plot of the forward path transfer function for the grid current feedback control with the parameters in Table 2.3.

a Zero-Order-Hold (ZOH) is in series of the open loop, discretization of the system introduces delay too.

$G_c(s)$ can be regarded as k_p at the crossover frequency. When $\angle G_o(j\omega_k) = -\pi$, the phase of the single open loop is shown in (2.19). The root of the function can be calculated as $\omega_k = \pi/(3T_s)$. If a phase angle is already below $-180°$ at this resonant frequency, the system can be stable. It can also be deduced that the critical frequency $f_k = f_s/6$.

$$\angle G(j\omega_k) = \angle \left\{ \begin{array}{c} e^{-j\omega_k T_s} \cdot \dfrac{1-e^{-j\omega_k T_s}}{j\omega_k} \\ \cdot \dfrac{1-L_f C_f \omega_k^2}{j\left[(L_1+L_2)\omega_k - \left(L_1 L_2 C_f + (L_1+L_2)L_f C_f\right)\omega_k^3\right]} \end{array} \right\} = -\pi \tag{2.19}$$

Hence, a single loop is sufficient to keep the system stable when the resonant frequency is above the critical frequency and active damping is necessary when the resonant frequency is below the critical frequency.

For the example shown in Table 2.3, the critical frequency f_k is 1.68 kHz. The closed loop root loci of the three cases in Table 2.3 are shown in Figure 2.10.

Figure 2.10(a) depicts the case when the resonant frequency of the *LLCL* filter is above the critical frequency. The poles initially track inside the unit circle. Figure 2.10(b) shows the case when the resonant frequency of the *LLCL* filters is at the critical frequency and the system is unstable. When the resonant frequency is less than the critical frequency the system will always be unstable regardless of what the proportional gain is without damping, as shown in Figure 2.10(c).
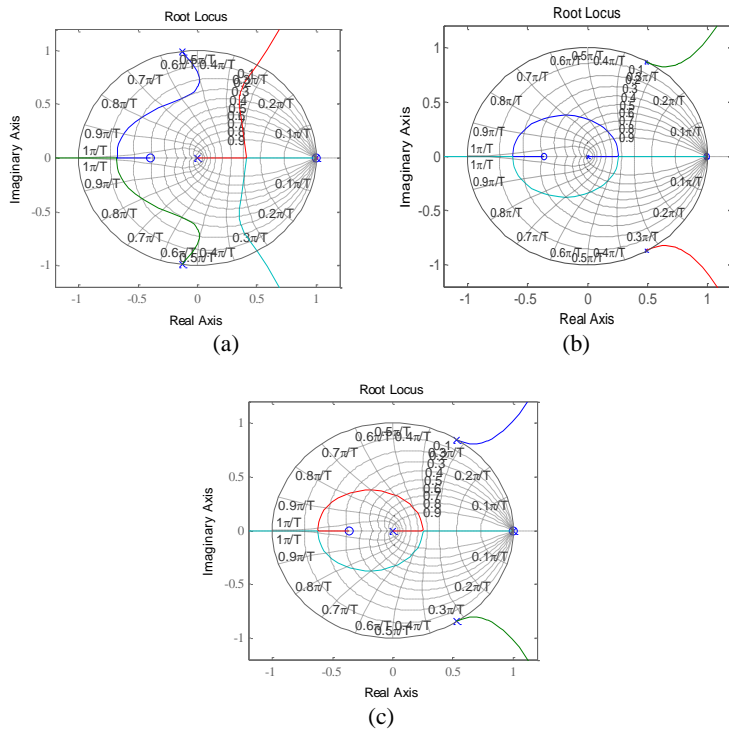
Figure 2.10: Root loci of grid current feedback (without damping) of different cases specified in Table 2.3. (a) Case I, (b) Case II, (c) Case III.

2.5.3 PR Controller Gain Design

The maximum possible controller gains for the system can now be analytically determined using the concepts developed in [60, 64, 77]. The proportional gain is then set to achieve unity gain at the desired crossover frequency f_c / ω_c.

For a single loop control, the phase angle at the crossover frequency can be described in (2.20). As shown in Figure 2.8, the *LLCL* filter is approximated to an *L* filter in the low frequency range. In addition, the cross-over frequency ω_c can be determined as [60]:

$$\omega_c = \frac{\pi / 2 - \Phi_m}{3T_s / 2} \qquad (2.20),$$

where Φ_m is the desired phase margin and T_s is the sampling period.
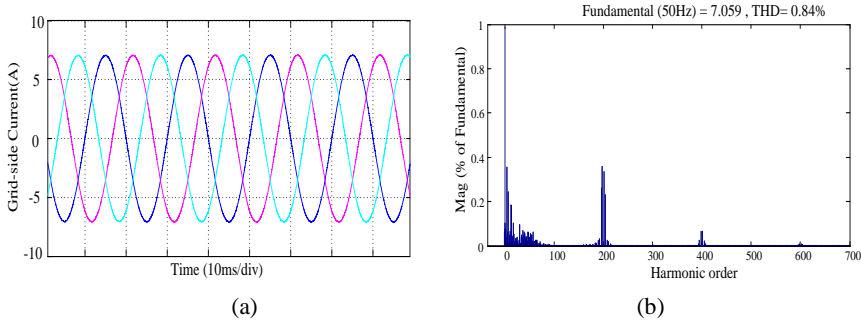
Figure 2.11: Grid-side currents of *LCL* filter based inverter. (a) Current waveforms and (b) The current spectrum.

The system open-loop gain achieves unity at ω_c. Then the maximum gain can be calculated as:

$$\left|G(j\omega_c)\right| \approx \left|\frac{k_p\sqrt{(\omega_c\tau)^2+1}}{\omega_c\tau}\right|\left|\frac{1-e^{-j\omega_c T_d}}{j\omega_c}\right|\left|\frac{k_{PWM}}{j(L_1+L_2)\omega_c}\right| \tag{2.21}$$

$$k_p \approx \frac{\omega_c(L_1+L_2)}{k_{PWM}} \tag{2.22}$$

Obtain the value of k_p and f_c to satisfy all the requirements according to (2.20), and (2.22), f_c= 1 kHz is chosen to obtain fast dynamic response. Then k_p is calculated as 0.065 according to (2.22).

2.6 Simulation and experimental results

2.6.1 Simulation results of *LCL* filter and *LLCL* filter

In order to illustrate the harmonic attenuation of different filters and verify the stability of the *LLCL* filter based grid-connected inverter, a three-phase inverter with 6 kW rated power is simulated using PLECS Blockset and MATLAB. The switching frequency is 10 kHz and the DC link voltage is 700 V. As discussed before, the *LLCL* filter can get the same harmonic attenuation as the *LCL* filter with a smaller inductance or capacitance, which means *LLCL* filter has some superiority.
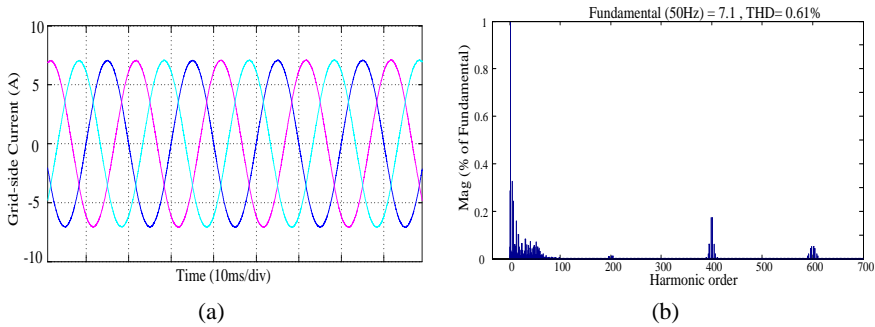
Figure 2.12: Grid-side currents of *LLCL* filter based inverter. (a) Current waveforms and (b) The current spectrum.
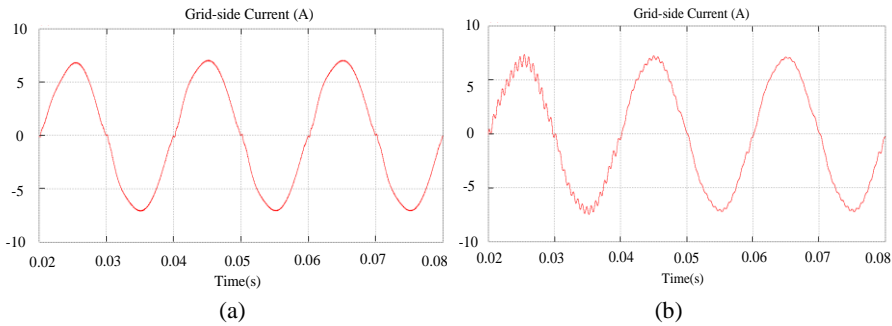
Figure 2.13: Grid-side current waveform of (a) Case I (f_r = 3.69 kHz) and (b) Case II (f_r = 1.67 kHz).

Figure 2.11 and Figure 2.12 show the grid-side currents of an *LCL* filter based inverter and *LLCL* filter based inverter respectively. For the *LCL* filter, L_1 = 2.4 mH, L_2 = 1.2 mH and C_f = 4 μF; For the *LLCL* filter, L_1 = 2.4 mH, L_2 = 1.2 mH, L_f = 64 μH and C_f = 4 μF. The resonance frequencies of the *LCL*-filter and *LLCL* filter are all above $f_s/6$, so the system can be stable without damping. The grid-current THD of the *LCL* filter based inverter is 0.84% and the harmonics around the switching frequency are higher than 0.3% of the fundamental current. The grid-current THD of the *LLCL* filter based inverter is 0.61% and dominant harmonics are around the double of the switching frequency. It shows the *LLCL* filter has better harmonics attenuation compared to the *LCL* filter.

2.6.2 Simulation results of stability analysis

Then, in order to investigate the stability of the system without damping at different resonant frequencies, the *LLCL* filter is analyzed into three cases (one with a high resonant frequency, one with a critical resonant frequency and one with a low
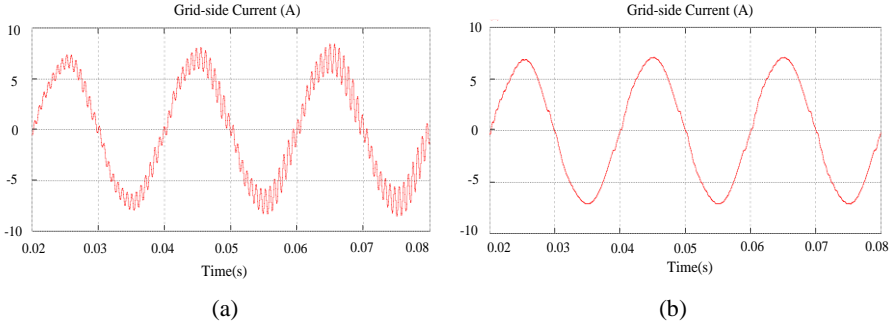
Figure 2.14: Grid-side current waveform of Case II when (a) $L_2 + L_g =$2.4 mH ($f_r = 1.60$ kHz), (b) $L_2 + L_g = 1.2$ mH ($f_r = 1.95$ kHz).

resonant frequency) as shown in Table 2.3. The desired phase margin Φ_m should be larger than 40º in order to get a good dynamic response and stability margin. The crossover frequency is selected to be 1 kHz in order to obtain fast dynamic response. According to (2.20) - (2.22), the controller gain is calculated as $k_p = 0.06$ and $k_i = 20$.

(1) Case I: high frequency $f_r =$3.69 kHz

In Case I, the resonant frequency is high (3.69 kHz) and the crossover frequency is set to 1 kHz in order to get a fast response and to meet a phase margin limitation. It can be seen from Figure 2.13(a) the system is stable.

(2) Case II: critical frequency $f_r =$1.67 kHz

As it is mentioned before, there is a critical frequency for the *LLCL* filter. It is calculated as $f_s /6$ based on the function (2.19). It can be seen from Figure 2.13(b) the system is almost unstable at the critical frequency. When the grid impedance L_g is increased from 0 mH to 0.4 mH, the resonant frequency will be reduced to 1.6 kHz, which is below the critical frequency and the system is unstable, as shown in Figure 2.14(a). When the grid-side inductance L_2 is changed to 1.2 mH, the resonant frequency is increased to 1.95 kHz and the system is changed from an unstable state to a stable state, as shown in Figure 2.14(b).

(3) Case III: Low frequency $f_r =$1.52 kHz

In Case III, the resonant frequency is low (1.52 kHz). It can be seen from Figure 2.15 that the system is unstable without damping.

So, when designing the parameters it is better to make the resonant frequency higher in order to get a better stability and robustness. When the resonant frequency is lower or nearby the critical frequency, the active damping method is necessary to be used. In this chapter, take Case III as an example, the active damping with capacitor current feedback is used.
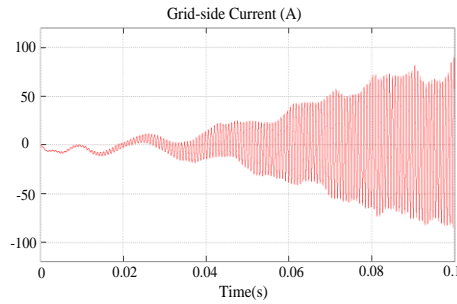
Figure 2.15: Grid-side current waveform of Case III (f_r = 1.52 kHz).

| (a) | (b) |
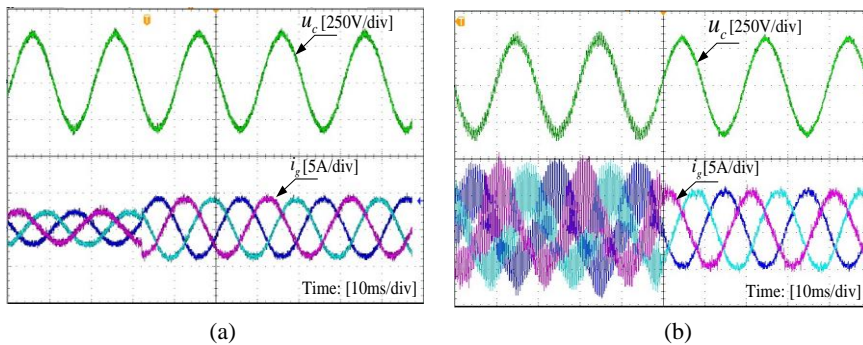
Figure 2.16: Experimental results of (a) high resonant frequency case without active damping Case I and (b) low resonant frequency case when active damping is enabled Case III.

2.6.3 Experimental results

An experimental setup consists of a 2.2 kVA Danfoss three-phase converter connected to the grid through an isolating transformer and the DC-link supplied by Delta Elektronika power source. The control algorithm is implemented on a dSPACE DS1103 board. Figure 2.16(a) shows the dynamic transition of the grid-side currents and L_f-C_f circuit voltage in the high resonant frequency case (Case I) when the power is increased without active damping. The reference current steps from 2.4 A-4.8 A and the system can be stable without damping, when the ratio of the resonant frequency to the control frequency is higher than 1/6. Figure 2.16(b) shows the grid-side currents and L_f-C_f circuit voltage, when the active damping is enabled in the low resonant frequency case (Case III).

So, when designing the parameters it is better to make the resonant frequency higher in order to get a better stability and robustness. When the resonant frequency is lower or nearby the critical frequency, the active damping method is necessary to be used.

2.7 Summary

This chapter has introduced a harmonic current calculation method and a step by step design method of the high order power filter in the three-phase three-wire grid-connected inverter. Compared with the *LCL* filter, the total inductance of *LLCL* filters with one trap and two traps can be reduced.

Stability of *LLCL*-filter-based grid-connected inverter with different resonant frequencies is analyzed. In the low resonant frequency case, or critical case, the resonant frequency is easy to be changed due to the parameter variation and the grid impedance variation. Then, damping methods are necessary to be used and demonstrated to be effecient. The next chapter investigates different impedance based active dampers in order to solve the resonance problems. What's more, robustness of different active dampers is also compared.

Chapter 3 Impedance-Based Active Damping Methods for Voltage Source Converters

As discussed in Chapter 2, the resonant frequency can easily to be changed due to the parameter and grid impedance variation in the high resonant frequency case, or in the critical case with grid current control. Therefore, the damping methods are necessary to be used. Active damping is a competitive alternative since it only involves modifying the converter control, and is hence more efficient. It is also more flexible with many control possibilities which are available for selection. Among them, the multi-loop active damping methods are the most widely discussed. In this chapter active damping methods are analysed by using the concept of the equivalent impedance with and without the delay effect of a filter-based voltage source grid-connected inverter. Generally, the virtual impedance loop can be embedded as an additional degree of freedom for active stabilization and disturbance rejection. Their corresponding equivalent circuits for the purpose of resonance damping are given in order to identify whether the feedback coefficient should be negative or positive for the different state-feedback methods. The grid current control is designed using Proportional Resonant control and Harmonic Compensation for harmonics elimination.

3.1 Control of *LLCL*-filtered grid converter

3.1.1 Modeling of *LLCL*-filter-based grid-connected inverter

Figure 3.1 shows a three-phase grid converter with an *LLCL* filter comprising converter-side inductance L_1, grid-side inductance L_2, trap inductance L_f and capacitance C_f. The inverter output voltage and current are represented as u_i (phase voltage) and i_1, and the grid voltage and current are represented as u_g and i_g; i_c is the capacitor current; u_{LC} is the output voltage across the *LC* trap; u_{Lf} is the output voltage of the resonant inductor, and L_g is the grid impedance.

The grid converter in Figure 3.1 is also commonly damped by feeding back a variable, which for the *LCL* filter, typically is chosen as the capacitor current i_c [60, 64]. The same i_c can be fed back for the *LLCL* filter, but it will be demonstrated later that the trap voltage u_{LC} is a better feedback variable which can preserve both
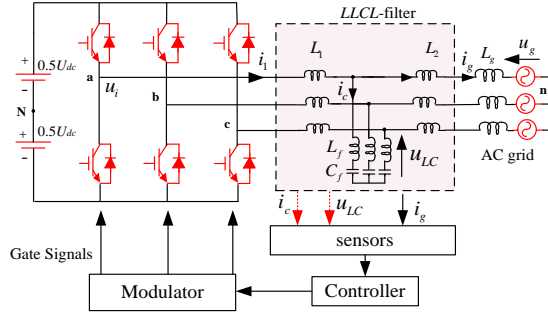
Figure 3.1: Three-phase grid converter with an *LLCL* filter.

simplicity and also robustness. The common purpose is to damp the resonance at ω_r = $2\pi f_r$. Neglecting the influence of the grid impedance and the Equivalent Series Resistances (ESRs) of inductors and capacitors, expressions can be extracted from any of the following open- loop transfer functions i_g to u_i, i_c to u_i and u_{LC} to u_i are given as:

$$G_{u_i \to i_g}(s) = \frac{i_g}{u_i} = \frac{L_f C_f s^2 + 1}{C_f \left[L_1 L_2 + (L_1 + L_2)L_f\right]s\left(s^2 + \omega_r^2\right)} \tag{3.1}$$

$$G_{u_i \to u_{LC}}(s) = \frac{u_{LC}}{u_i} = \frac{L_2 s(L_f C_f s^2 + 1)}{C_f \left[L_1 L_2 + (L_1 + L_2)L_f\right]s\left(s^2 + \omega_r^2\right)} \tag{3.2}$$

$$G_{u_i \to i_c}(s) = \frac{i_c}{u_i} = \frac{L_2 s^2}{\left[L_1 L_2 + (L_1 + L_2)L_f\right]s\left(s^2 + \omega_r^2\right)} \tag{3.3}$$

It is assumed in (3.1)-(3.3) that the grid inductance is zero. But in some situations, the resonance frequency f_r of the system is then affected by the grid variations [35-37] when L_2 is changed to $L_2 + L_g$.

The controller used here is the standard proportional-resonant controller with selective harmonic compensation [79-82]. Transfer function of the controller is provided in (3.4) as:

$$G_c(s) = K_p + \sum_{h=1,5,7} \frac{K_{ih}s}{s^2 + (\omega_0 h)^2} \tag{3.4}$$

where $\omega_o = 2\pi f_o$ is the fundamental angular frequency of the grid, K_p is the proportional gain, and K_{ih} is the resonant gain of harmonic order h.
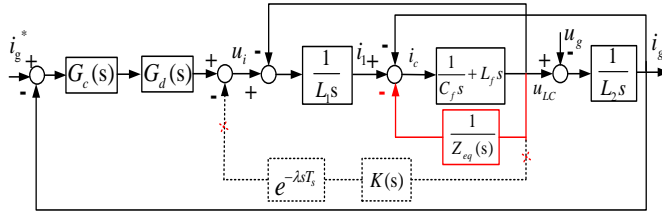
Figure 3.2: Grid current control with damper based on trap voltage feedback.
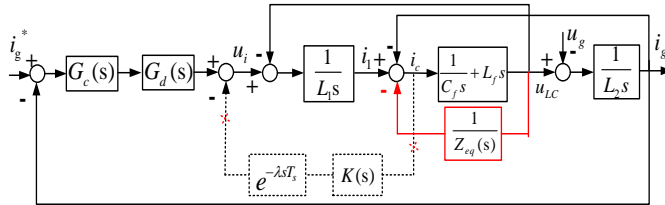
Figure 3.3: Grid current control with damper based on trap current feedback.

3.1.2 Block diagrams of different active dampers

Figure 3.2 shows the control block diagram of the grid converter when its active damping is implemented by feeding back the trap voltage u_{LC}, which can also be fed into a phase-locked-loop for synchronizing the desired grid current with u_{LC}. An extra sensor can be saved in this way. In the meantime, the feedback path with the 1 / $Z_{eq}(s)$ block should be ignored first and it will be explained in the next section.

The feedback variable u_{LC} is then passed through a damper $K(s)$ and a delay block $G_d(s) = e^{-\lambda s T_s}$, which is also added after the grid current controller $G_c(s)$. λ is the delay here and is normalized with respect to the sampling period T_s. The sampling frequency is labeled as f_s (1 / T_s), which can be set equal to the converter switching frequency or higher. Conceptually, a higher sampling frequency gives rise to a smaller delay which is less impactful to the system. Cases with higher sampling frequency are considered as analogue systems ($\lambda = 0$).

Instead of the trap voltage, the trap current i_c can also be sensed and fed back for damping the resonance, as shown in Figure 3.3. Also the feedback path with the 1 / $Z_{eq}(s)$ block in the figure should be ignored first, since it will be explained further in the virtual impedance part.
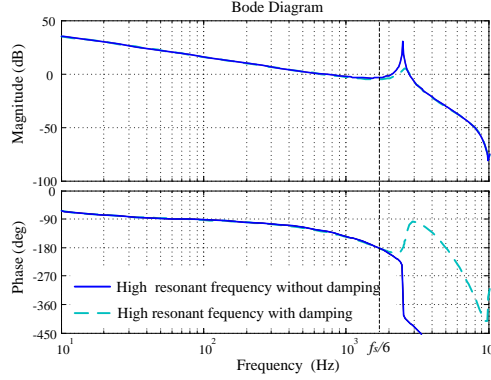
Figure 3.4: Bode plots of open-loop i_g (s) / u_i (s) with and without damping at high resonance frequency.

3.1.3 Effects of delay $G_d(s)$

The first delay of T_s is coming from the usual process of sampling data, performing the computation, and updating the signal for pulse-width modulation one sampling period later [83, 84]. After the signal is updated, it is held constant by the digital dpulse-width modulator over the next full sampling period. This process can be approximated by a zero-order hold with the following transfer functions expressed in both s and $j\omega$.

$$H_o(s) = \frac{1 - e^{-T_d s}}{s} \tag{3.5}$$

$$H_o(j\omega) = \frac{1 - e^{-j\omega T_s}}{j\omega} = \frac{\sin(0.5\omega T_s)}{0.5\omega} e^{-j0.5\omega T_s} \approx T_s e^{-j0.5\omega T_s} \tag{3.6}$$

$$G(s) = G_{delay}(s) k_{PWM} G_c(s) G_{u_i \to i_g}(s) \tag{3.7}$$

Clearly, the H_o ($j\omega$) function in (3.5) indicates a second delay of $0.5T_s$, which gives a total delay of $1.5T_s$ ($\lambda = 1.5$) when added to the computational delay of T_s. Figure 3.4 shows the Bode plots of the open-loop transfer function i_g (s) / u_i (s) at high resonance frequency as expressed in (3.7) with and without damping. Table 3.1 show the parameters used for the plots. It can be seen from Figure 3.4 that this delay will not destabilize the system even without damping added for the grid current control. The only requirement is to make the resonance f_r to be higher than the critical frequency of f_s / 6, above which the system phase would have fallen well below −180° caused by the delay. Hence, the sudden phase transition of f_r after f_s / 6

Table 3.1: Parameters of *LLCL* filter based voltage source inverter.

Symbol	Meaning	Value
U_{dc}	DC-link voltage	650 V
U_g	Grid phase voltage	230 V
L_1	Converter-side inductor	1.8 mH
L_f, C_f	Trap circuit parameter	64 μH, 4 μF
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	10 kHz
f_r	Resonance frequency	2.45 kHz
L_2	Grid-side inductor	2 mH
L_g	Grid inductance (unless stated otherwise)	0 mH
T_s	Sampling period	100 μs

will then have no prominent influence on the system stability. If the proportional trap current damping is now added to the system with its resonance still kept above f_s / 6, the dashed lines in Figure 3.4 show that the system phase crosses −180º twice. The reason is related to the Non-Minimum-Phase (NMP) response and it means an initial decrease before increasing to track the raised command reference. The stability of the system must then be determined by the Nyquist stability criterion, which has proven that for a stable *LCL*-filtered system, its magnitude margins at f_s / 6 and f_r must be larger and smaller than zero, respectively.

Comparatively, it is therefore advisable for the converter to operate undamped if $f_r > f_s$ / 6. However, such condition may not be satisfied if the filter inductances L_x (x = 1, 2 or f), filter capacitance C_f and grid inductance L_g, according to (3.1)-(3.3) but with L_2 replaced by $L_2 + L_g$. The frequency f_r will then move towards the condition of $f_r < f_s$ / 6. When that happens, damping may be unavoidable. It might therefore be more attractive to design maximum $f_r < f_s$ / 6 at the beginning with damping added, $L_g = 0$ assumed, and the smallest filter inductances and capacitance considered ($L_x − \Delta L_x$ and $C_f − \Delta C_f$, where Δ represents percentage variation). As L_x, C_f and L_g subsequently increase, f_r will only move leftwards of the maximum value without breaching the desired condition of $f_r < f_s$ / 6. Both uniformity and robustness are ensured. In the case of adding more *LC*-traps to the *LLCL* filter in order to creating a wider attenuating notch around the converter switching frequency, the principle of ensuring maximum $f_r < f_s$ / 6 should similarly be applied even with more resonance peaks present.

The level of robustness can next be studied by inserting a large shunt capacitance between L_2 and L_g as shown in Figure 3.1. The variations of L_g will then not affect the resonance frequency f_r greatly, but at the cost of a shunt capacitance. Alternatively, the critical frequency of f_s / 6 can be increased, where one way to

achieve it is documented in [72], but only for an *LCL* filter with a proportional active damper based on capacitor current feedback. The new critical frequency achieved is f_s / 4, which theoretically, is obtained by eliminating time difference between the capacitor current sampling and modulation reference updating instants. It therefore requires a unique sampling pattern, which first must be supported by the control platform. In order to avoid modifying the standard sampling pattern, the next part of this chapter analyzes a few alternatives, whose common basic principle is to raise the critical frequency by re-shaping the virtual filter impedance. Such re-shaping can be done by choosing an appropriate damping function for $K(s)$ in Figure 3.2 or Figure 3.3. It is therefore much simpler with an even higher level of robustness demonstrated (a critical frequency higher than f_s / 4).

3.2 General virtual impedance model

To derive the circuit equivalence of the damper shown in Figure 3.2, the usual feedback path through $K(s)$ has been changed by shifting its output node from after $G_d(s)$ to after 1 / sL_1. The modified path through 1 / $Z_{eq}(s)$ is drawn using a solid line in Figure 3.2. Similar shifting can also be applied to Figure 3.3, which is in addition to its output node, and has its input node shifted from i_c to u_{LC}. The modified damping path through 1 / $Z_{eq}(s)$ is again drawn using a solid line in Figure 3.3. Undoubtedly, $Z_{eq}(s)$ for both figures are different, but in terms of circuit equivalence, they can both be represented by Figure 3.5, where $Z_{eq}(s)$ has been separated into $R_{eq}(s)$ and $X_{eq}(s)$ in series. The precise forms assumed by $R_{eq}(s)$ and $X_{eq}(s)$ depend on the damping function $K(s)$ and feedback variable chosen, as explained in the following.

3.2.1 *LC*-trap voltage feedback

Using the *LC*-trap voltage feedback for damping as seen in Figure 3.2, the generalized expression derived for representing $Z_{eq}(s)$ can be given in (3.8).

$$Z_{eq}(s) = s \cdot L_1 / K(s) \cdot e^{\lambda s T_s} \tag{3.8}$$

The exponential delay function in (3.8) can be expanded like in (3.9), allowing $Z_{eq}(s)$ to be written as a real and an imaginary term like in (3.10).

$$e^{j\omega\lambda T_s} = \cos\omega\lambda T + j\sin\omega\lambda T \ , \ s \rightarrow j\omega \tag{3.9}$$

The real term is for the resistive damping, while the imaginary term provides a degree of freedom for shifting the system resonance frequency. Polarities and frequency dependencies of both terms depend on the precise chosen damping function $K(s)$, which for preserving simplicity of the overall system has been limited
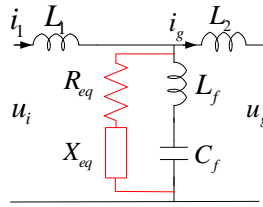
Figure 3.5: Generalized equivalent circuit for the active damper.

to five common functions of k, ks, k/s, $ks/(s+\tau)$ and $k/(s+\tau)$. The parameters k and τ are used with these functions for representing their damping gain and cut-off angular frequency, respectively.

Substituting the functions into (3.8) to (3.10) it leads to the R_{eq} and X_{eq} expressions shown in Table 3.2. No doubt, Table 3.1 can be simplified by setting $\lambda = 0$ for representing an analogue system without delay (or a digital system with extremely fast sampling).

The simplified R_{eq} and X_{eq} can then be drawn like shown in Figure 3.6 with R_d and L_d given in (3.11). These representations show that for all dampers, the polarities of R_{eq} and X_{eq} remain unchanged upon fixing k in (3.11). In addition, using a simple k damper, no resistive damping is introduced. A simple k damper is therefore not recommended for an analogue system.

$$Z_{eq}(j\omega) = R_{eq}(\omega) + jX_{eq}(\omega) \tag{3.10}$$

$$R_d = \frac{L_1}{k} , \ L_d = \frac{j\omega L_1}{k} \tag{3.11}$$

But it is different when the computational delay is considered for a regularly sampled system. To illustrate this, the simple k damper is again considered. Its R_{eq} in Table 3.2 is no longer zero unlike in Figure 3.6(a). It can either be positive or negative depending on k and the angular frequency ω that needs damping, which for the system shown in Figure 3.1, is the resonance frequency f_r. Preferably, R_{eq} should not be negative since it will introduce open-loop Right-Half-Plane (RHP) poles to the grid current control scheme shown in Figure 3.2. The closed-loop response of the scheme will then have NMP characteristics. It is therefore recommended to have a positive R_{eq}, which for the k damper, can be achieved by setting both of the conditions given in (3.12). The condition with $f_r < f_s / 3$ is however preferred because of the uniformity reasons explained.

$$k < 0 \text{ and } \omega = 2\pi f_r < 2\pi f_s / 3, \text{ or}$$

$$k > 0 \text{ and } \omega = 2\pi f_r > 2\pi f_s / 3 \tag{3.12}$$
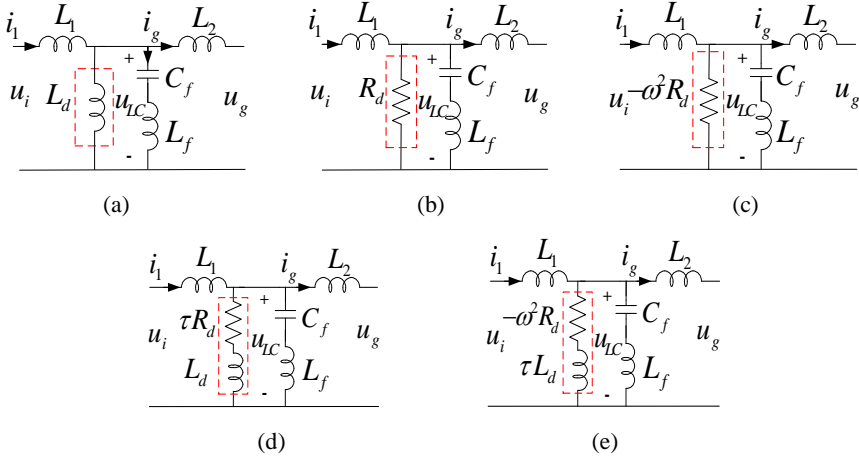
Figure 3.6: Circuit equivalences of active dampers (dashed) in *LLCL* filter (a) *k*, (b) *ks*, (c) *k/s*, (d) *ks/(s+τ)* and (e) *k/(s+τ)* dampers based on trap voltage feedback and no delay.

Table 3.2: Equivalent R_{eq} and X_{eq} of different dampers based on trap voltage feedback.

$K(s)$	k	ks	k/s	$ks/(s+\tau)$	$k/(s+\tau)$
$R_{eq}(\omega)$	$-\frac{L_1\omega}{k}\cdot\sin\lambda\omega T_s$	$\frac{L_1}{k}\cdot\cos\lambda\omega T_s$	$\frac{-L_1\omega^2}{k}\cdot\cos\lambda\omega T_s$	$\frac{L_1\tau}{k}\cdot\cos\lambda\omega T_s-\frac{L_1\omega}{k}\cdot\sin\lambda\omega T_s$	$-\frac{L_1\omega^2}{k}\cdot\cos\lambda\omega T_s-\frac{L_1\tau\omega}{k}\cdot\sin\lambda\omega T_s$
$X_{eq}(\omega)$	$\frac{L_1\omega}{k}\cdot\cos\lambda\omega T_s$	$\frac{L_1}{k}\cdot\sin\lambda\omega T_s$	$-\frac{L_1\omega^2}{k}\cdot\sin\lambda\omega T_s$	$\frac{L_1\tau}{k}\cdot\sin\lambda\omega T_s+\frac{L_1\omega}{k}\cdot\cos\lambda\omega T_s$	$-\frac{L_1\omega^2}{k}\cdot\sin\lambda\omega T_s+\frac{L_1\tau\omega}{k}\cdot\cos\lambda\omega T$
f_n	$f_s/3$	$f_s/6$	$f_s/6$	see Figure 3.7(a)	see Figure 3.7(b)

The critical frequency here is thus $f_n = f_s / 3$ for the simple *k* damper. The same analysis can be performed with the other four dampers. Their respective critical frequencies f_n are summarized in Table 3.2, where it should be noted that the high-pass *ks/(s+τ)* and low-pass *k/(s+τ)* dampers do not have fixed f_n.

Instead, their f_n increase with their angular cut-off frequencies $\tau = 2\pi f_{nc}$, as shown in Figure 3.7. Regardless of that, f_n of the *k/(s+τ)* damper is always higher than that of the *ks/(s+τ)* damper when using the same f_{nc}. The former is thus preferred with its f_n approaching of the simple *k* damper as f_{nc} increases like in Figure 3.7(b). Both *k* and *k/(s+τ)* dampers are therefore more robust if the trap voltage of the regularly sampled system is fed back. This is in despite of the *k* damper has being proven earlier not to be suitable for an analog system (see Figure 3.6(a)).

(a)   (b)

Figure 3.7: Critical frequency f_n versus cutoff frequency $f_{nc} = \tau / (2\pi)$ of the (a) $ks/(s+\tau)$ and (b) $k/(s+\tau)$ dampers based on trap voltage feedback.
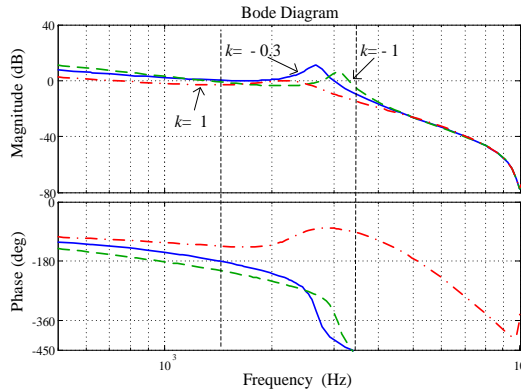
Figure 3.8: Bode plots of Figure 3.4 with the k damper.

To further illustrate the removal of negative resistance and hence NMP response, open-loop Bode plots of Figure 3.2 are plotted in Figure 3.8 with $K(s) = k$ considered as an example. With $k < 0$, the two representative phase plots are clearly decreasing monotonically with their phase values at f_r well below $-180°$. They are therefore like the solid traces drawn in Figure 3.4 with no open-loop RHP poles and hence no NMP influences. However it should be noted that out of the two negative k values, only the case with $k = -0.3$ is stable because of its small positive phase margin.

The other with $k = -1$ is unstable because its phase has fallen below $-180°$ at the gain crossover frequency. Such instability is however not foretold by (3.12) and its accompanied circuit equivalence because they do not consider the grid current controller $G_c(s)$. By itself, (3.12) only helps with deciding the polarity of k and placement of f_r in order to avoid the NMP response.

Table 3.3:   Equivalent R_{eq} and X_{eq} of different dampers based on trap current feedback.

$K(s)$	k	ks	k/s	$ks/(s+\tau)$	$k/(s+\tau)$
$R_{eq}(\omega)$	$A\cos\lambda\omega T$	$B\sin\lambda\omega T$	$-C\sin\lambda\omega T$	$A\cos\lambda\omega T + B\tau\sin\lambda\omega T$	$\tau A\cos\lambda\omega T - C\sin\lambda\omega T$
$X_{eq}(\omega)$	$A\sin\lambda\omega T$	$-B\cos\lambda\omega T$	$C\cos\lambda\omega T$	$A\sin\lambda\omega T - \tau B\cos\lambda\omega T$	$\tau A\sin\lambda\omega T + C\cos\lambda\omega T$
f_n	$f_s/6$	$f_s/3$	$f_s/3$	see Figure 3.10(a)	see Figure 3.10(b)

3.2.2 *LC*-Trap current feedback

It is presently seen that the k damper provides the fastest and most robust performance when used with a regularly sampled system with *LC*-trap voltage feedback. How it is compared with the popular capacitor or *LC*-trap current damper is investigated, beginning with the generalized expression in (3.13) for representing $Z_{eq}(s)$ in Figure 3.3.

$$Z_{eq} = \frac{L_1\left(1+s^2 L_f C_f\right)}{C_f K(s)} \cdot e^{\lambda s T_d} \tag{3.13}$$

$$A = \frac{L_1\left(1-\omega^2 L_f C_f\right)}{C_f k}, \; B = \frac{L_1\left(1-\omega^2 L_f C_f\right)}{\omega C_f k}, \; C = \frac{L_1\omega}{C_f k} - \frac{L_1 L_f \omega^3}{k} \tag{3.14}$$

Table 3.3 shows the R_{eq} and X_{eq} related to the trap current feedback. An observation noted from (3.14) is A, B and C are always larger than zero before the converter switching frequency ($\omega < 2\pi f_s = 2\pi f_s =1/\sqrt{L_f C_f}$). They are therefore treated as positive since the usual controllable range is only up to the Nyquist frequency, which is half of the sampling frequency. The same expressions in (3.14) can similarly be used with an *LCL* filter with capacitor current feedback, but only after setting L_f to zero. With a non-zero L_f, the performances of both filters are rightfully different even though they can be close to each other when L_f is small. However that depends on the converter switching frequency, from which L_f is computed. With delay set to $\lambda = 0$ to represent an analogue system, Figure 3.9 shows the equivalent circuit obtained with the five damping functions of k, ks, k/s, $ks/(s+\tau)$ and $k/(s+\tau)$.

The expressions for R_v, L_v, L_{v1} and C_v in the figure are given in (3.15), which are clearly all positive when k is positive and $0 < \omega < 2\pi f_s$. The resistance in Figure 3.9(a) is therefore also positive, implying that the k damper can be used with an analogue system, where the trap current is fed back in the control system.
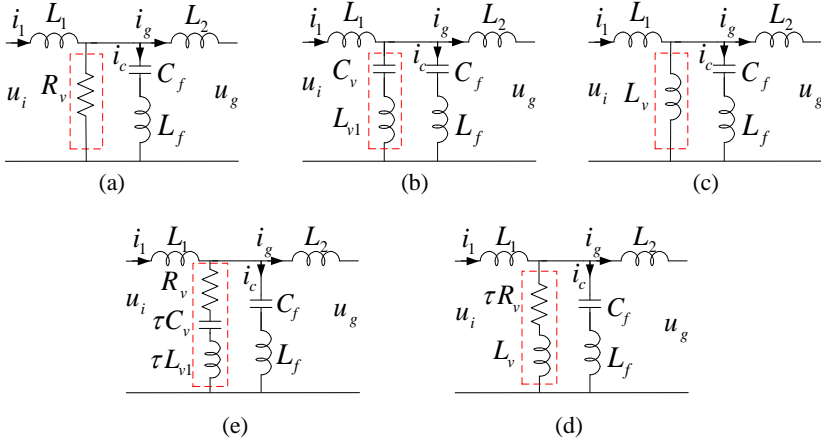
Figure 3.9: Circuit equivalences of (a) k, (b) ks, (c) k/s, (d) $ks/(s+\tau)$ and (e) $k/(s+\tau)$ dampers based on trap current feedback and no delay in the system.

$$R_v = \frac{L_1\left(1-\omega^2 L_f C_f\right)}{C_f k}, L_v = j\left(\frac{L_1\omega}{C_f k} - \frac{L_1 L_f \omega^3}{k}\right)$$

$$L_{v1} = \frac{j\omega L_1 L_f}{k}, C_v = \frac{L_1}{j\omega C_f k} \tag{3.15}$$

With a delay of $\lambda = 1.5$ is now considered, and Figure 3.9 is no longer applicable since R_{eq} can be either positive or negative depending on the chosen parameters. To illustrate, the simple k damper is again considered. Its R_{eq} is positive only when either conditions in (3.16) are satisfied.

$$k > 0 \text{ and } \omega = 2\pi f_r < 2\pi f_s / 6, \text{ or}$$
$$k < 0 \text{ and } \omega = 2\pi f_r > 2\pi f_s / 6 \tag{3.16}$$

The critical frequency is thus $f_n = f_s / 6$, which is visibly smaller than the *LC*-trap voltage feedback through the same k damper. To increase it to $f_s / 3$, the ks ($k > 0$) and k/s ($k < 0$) dampers should be used, which when summed in proportion to the L_f / C_f ratio and multiplied with the trap current. Practically, the ks and k/s dampers are not encouraged since the former can cause noise amplification, while the latter depends on the initial point of integration. They are therefore replaced by the high-pass $ks/(s+\tau)$ and low-pass $k/(s+\tau)$ dampers, whose critical frequencies f_n are no longer fixed.

Instead, they vary with the cutoff frequencies $\tau = 2\pi f_{nc}$, as shown in Figure 3.10. In particular, the $ks/(s+\tau)$ damper has always a higher critical frequency f_n than $f_s / 6$,
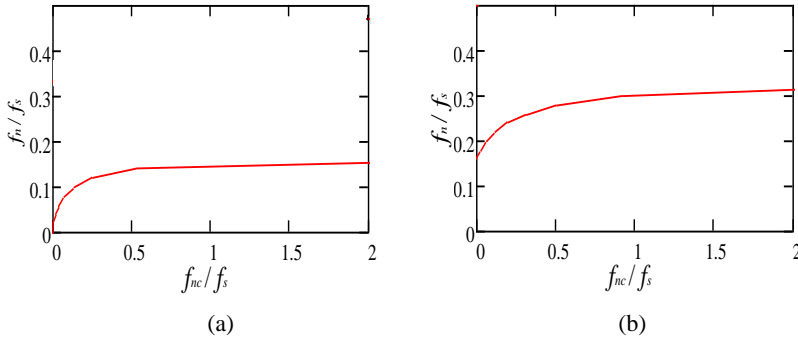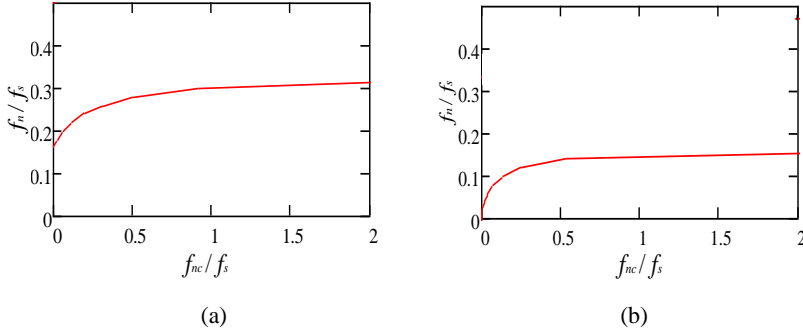
Figure 3.10: Critical frequency f_n versus cutoff frequency $f_{nc} = \tau / (2\pi)$ of the (a) $ks/(s+\tau)$ and (b) $k/(s+\tau)$ dampers based on trap current feedback.

which eventually saturates at $f_s / 3$ as f_{nc} increases. It is therefore a more robust damper in terms of avoiding NMP response compared to the k damper.

3.3 z-domain root-locus analyses

The equivalent impedance models shown before are to derive circuit equivalences for showing how different active dampers modify the original *LLCL* filter. Since the actual filter components are continuous and a discrete power filter does not exist physically, the equivalent circuit derivations are presented in the *s*-domain with the delay block represented by an exponential term. However, the overall discrete control design can be performed in the *s*-domain before discretization or directly in the *z*-domain. The latter is generally recognized as being more precise and hence performed in this section for direct programming to a digital signal processor [85-87].

3.3.1 z-domain transfer functions

To connect the discrete grid current controller G_c (z) and damper K (z) to the continuous *LLCL* and grid parameters, a zero-order-hold block is inserted between them, as shown in Figure 3.11. The resulting discrete open-loop transfer functions derived for representing the trap voltage and trap current dampers are then provided in (3.17) and (3.18), respectively.

K (s) is discretized by the Tustin method when $\tau = 10000$ and $\lambda = 1.5$ as shown in Table 3.4. Controller G_c (z) must next be discretized according to, but for the following evaluation, only a simplified form of G_c $(z) = K_p$ is used since the resonant terms in the controller will not influence the system response at the resonance frequency f_r.

Table 3.4: Discretized active damper $K(z)$ with sampling time 0.1 μs.

$K(s)$	k	ks	k/s	$ks/(s+\tau)$	$k/(s+\tau)$
$K(z)$	k	$\dfrac{2\times10^{4}\times k(z-1)}{z+1}$	$\dfrac{5\times10^{-5}\times k(z+1)}{z-1}$	$\dfrac{6\cdot67\times10^{-1}\times k(z-1)}{z-0.3333}$	$\dfrac{3\cdot33\times10^{-5}\times k(z+1)}{z-0.3333}$
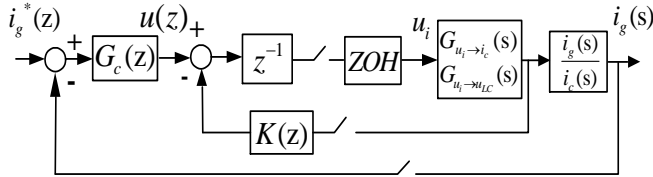
Figure 3.11: Discretized grid current control scheme with active damping.

$$\frac{i_g(z)}{i^*_g(z)} = G_c(z) \cdot \frac{G_{u_i \to u_{LC}}(z)}{z + K(z)G_{u_i \to u_{LC}}(z)} \cdot \frac{i_g(z)}{u_{LC}(z)} \tag{3.17}$$

$$\frac{i_g(z)}{i^*_g(z)} = G_c(z) \cdot \frac{G_{u_i \to i_c}(z)}{z + K(z)G_{u_i \to i_c}(z)} \cdot \frac{i_g(z)}{i_c(z)} \tag{3.18}$$

3.3.2 Root-locus analyses with different active dampers in z-domain

This part demonstrates how different active dampers can stabilize a system with no initially damping. The initial step is thus to select a high enough K_p that will marginally push the system in Figure 3.1 to instability when undamped. That means placing the poles on the z-domain unit circle when $k = 0$ for representing no damping. The value is found to be $K_p = 23.9$. Active damping is then added by increasing $|k|$ with either positive or negative polarity. The former is represented by a solid root loci drawn in Figure 3.12, while the latter is represented by dashed loci. Although increasing $|k|$ can stabilize the system, instability will resurface when $|k|$ becomes too high. This trend can be seen in Figure 3.12, where the root loci of five practically feasible dampers are shown with either trap voltage or current feedback.

To be more specific, Figure 3.12(a) shows the k-damped converter with trap-voltage feedback remaining stable only in the range of $-0.3 < k < 0$. Being a negative k and with $f_r < f_s / 3$ based on the parameters listed in Table 3.1, the converter will also not experience any NMP response. The same k damper can equally stabilize the system when the trap current is fed back. However, the stable range is now $0 < k < 11.6$, which will unfortunately produce an NMP response since k is positive and $f_r > f_s / 6$.

44
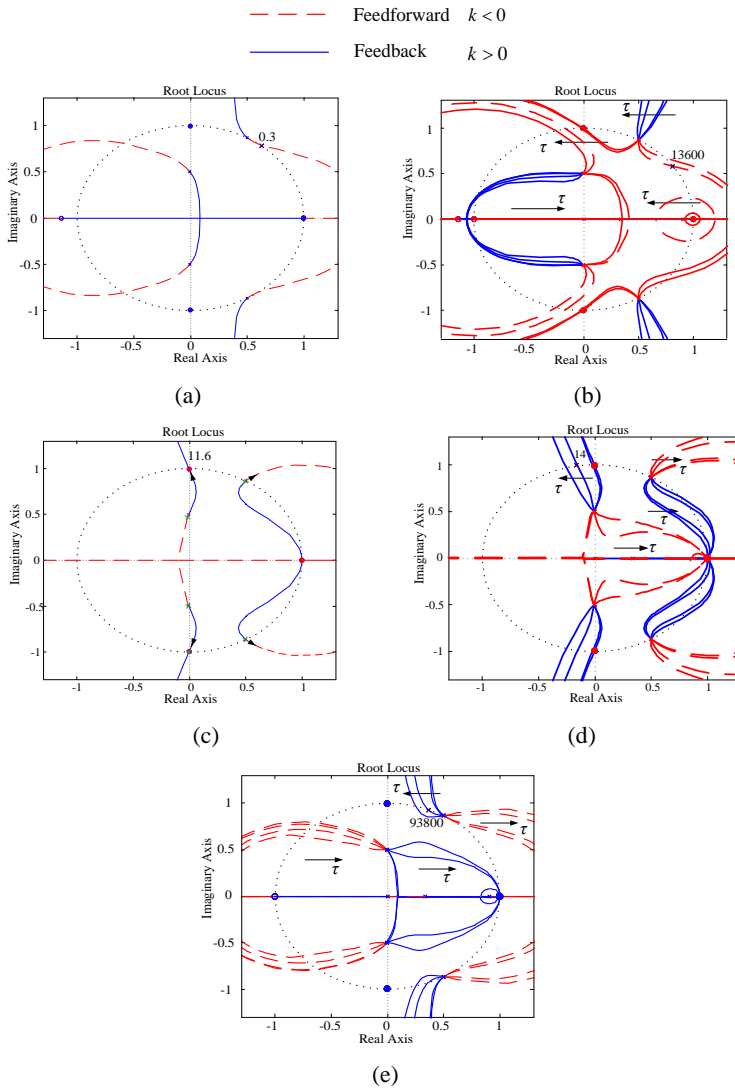
Figure 3.12: Root loci in z-domain of (a) *k* damper based on trap voltage feedback, (b) *k/(s+τ)* damper based on trap voltage feedback, (c) *k* damper based on trap current feedback, (d) *ks/(s+τ)* based on trap current feedback and (e) *k/(s+τ)* damper based on trap current feedback obtained by varying *k* with $K_p = 23.9$.

Table 3.5: Comparison of different active dampers with different feedback.

Sensed Variable	Trap voltage, u_{LC}	
Damper Type	k	Low-pass, $k/(s+\tau)$
Stable Range	$-0.3 < k < 0$	Negative k Lower limit dependent on τ
Critical Frequency, f_n	$f_s / 3$	Between $f_s / 6$ and $f_s / 3$
Features	Simple	Tunable with τ

Sensed Variable	Trap current, i_c		
Damper Type	k	High-pass, $ks/(s+\tau)$	Low-pass, $k/(s+\tau)$
Stable Range	$0 < k < 11.6$	Positive k Upper limit dependent on τ	Positive k Upper limit dependent on τ
Critical Frequency, f_n	$f_s / 6$	Between $f_s / 6$ and $f_s / 3$	Between 0 and $f_s / 6$
Features	Simple	Tunable with τ, but may have noise complication	Tunable with τ

Unlike the k damper, the other three plots in Figure 3.12 for representing low-pass and high-pass dampers with either trap voltage or current feedback have more loci in them, introduced by varying their angular cutoff frequency τ. Each of them has its own stable range for k even though with different polarity. They are therefore suitable dampers, whose stable k ranges can be widened by increasing τ. However, with NMP criterion included, Figure 3.10(b) shows that the low-pass damper with trap current feedback is the least preferred, since it has the smallest critical frequency f_n ($< f_s / 6$).

3.3.3 Comparison

For an easier comparison, results from the analyses performed for different dampers are summarized in Table 3.5. In terms of simplicity and dynamics, the k damper with trap voltage feedback is preferred, while in terms of flexible tuning (with τ), the low-pass damper with trap voltage feedback is recommended. The high-pass damper with trap current feedback can also be an option, but the presence of a high-pass filter will always inherit concern of noise complications depending on the operating conditions.

3.3.4 Experimental results

The experimental setup consists of a 2.2-kW Danfoss FC302 converter connected to the grid through an isolating transformer. The DC-link of the converter is tied to a Delta Elektronika power source, while its control is realized with a dSPACE
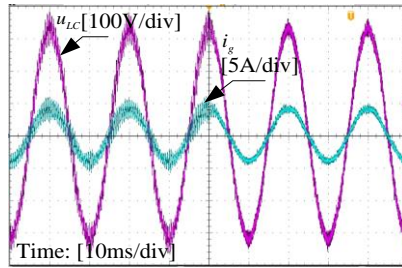
(a) $k = -0.25$
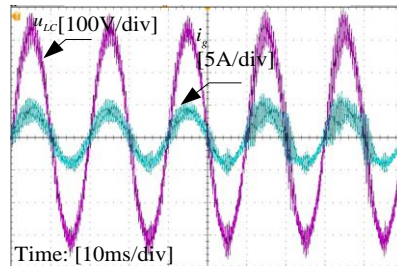
(b) $k = 0.1$
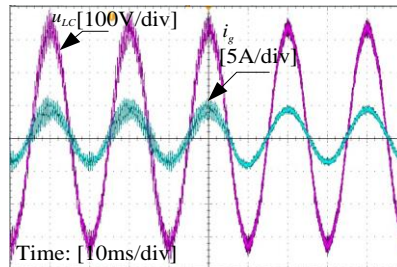
(c) $k = 12200$ and $\tau = 10000$

Figure 3.13: Trap voltage u_{LC} and grid current i_g obtained with (a) negative k, (b) positive k and (c) low-pass $k/(s+\tau)$ dampers (trap voltage feedback and $L_g = 0$) activated in the middle.

DS1103 controller. The parameters used for the setup are similar to those used for the analysis and given in Table 3.1. Like the root-locus analyses, each experiment is started with no damping ($k = 0$), $K_p = 23.9$ and $L_g = 0$. The converter is thus marginally stable with observable oscillations. After introducing damping ($k \neq 0$), the oscillation should be attenuated rapidly if the damper is stable and experiences no NMP response. Otherwise, the oscillation will continue or be amplified if the system is unstable, or will increase before gradually diminish if the system has a NMP characteristic.
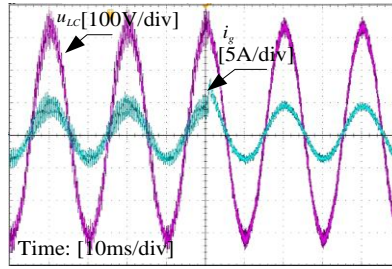
(a) $k = 6$
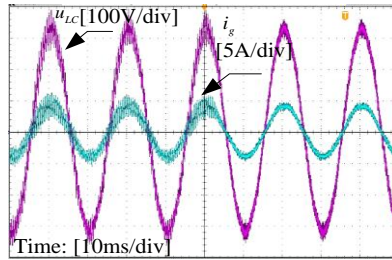
(b) $k = 8$ and $\tau = 10000$
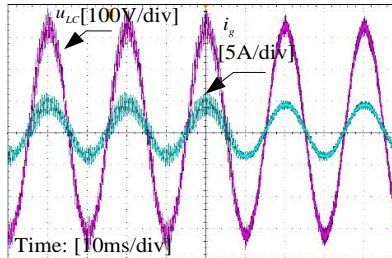
(c) $k = 30000$ and $\tau = 10000$

Figure 3.14: Trap voltage u_{LC} and grid current i_g obtained with (a) k, (b) high-pass $ks/(s+\tau)$ and (c) low-pass $k/(s+\tau)$ dampers (trap current feedback and $L_g = 0$) activated in the middle.

With this understanding, the experimental trap voltage u_{LC} and grid current i_g waveforms obtained with dampers based on trap voltage feedback are shown in Figure 3.13. In particular, Figure 3.13(a) shows that with $k = -0.25$, the system is stable. Moreover, since $f_r < f_s / 3$ (see Table 3.1), the system does not experience any NMP response. The initial oscillations diminish rapidly. The same favorable response is seen in Figure 3.13(c), where the results from the low-pass damper are shown. The parameters chosen for the low-pass damper are $k = 12200$ (positive) and $\tau = 10000$. An unstable response is however observed with the k damper in Figure 3.13(b), because of its positive k value intentionally chosen for illustration (see Figure 3.12 (a) and stable k range in Table 3.3).
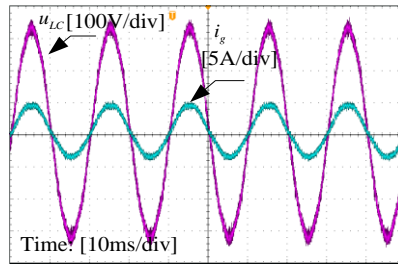
(a) $k = -0.25$
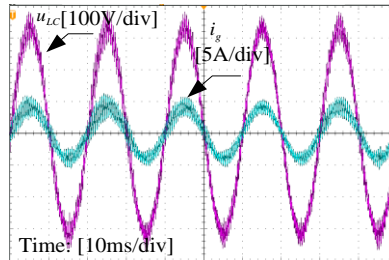
(b) $k = 6$
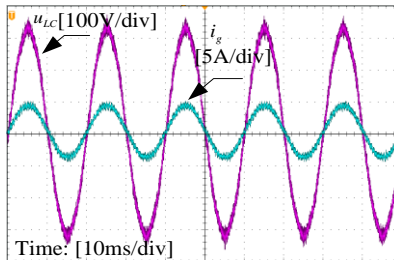
(c) $k = 8$ and $\tau = 10000$

Figure 3.15: Trap voltage u_{LC} and grid current i_g obtained with (a) k damper and trap voltage feedback, (b) k damper and trap current feedback, and (c) high-pass $ks/(s+\tau)$ damper and trap current feedback ($L_g = 4.8$ mH).

The same analysis can be performed as shown in Figure 3.14 based on trap current feedback. All dampers tested are stable, but the k and low-pass dampers are shown to have NMP responses.

The reason is related to their low critical frequency expressed as $f_n = f_s / 6$, which according to values from Table 3.5, is smaller than f_r. Based on the impedance analysis, these dampers are thus NMP, but have slightly different response characteristics caused by their different damping functions. To illustrate, Figure 3.14(a) and (c) are compared, where it can be seen that with the dynamically fast k damper, the grid current oscillation in Figure 3.14(a) surges prominently before

diminishing rapidly. The surge of the grid current is however less obvious with the slower low-pass damper, as seen in Figure 3.14(c). Its oscillation also diminishes slower.

Figure 3.15 show the results from three different dampers after increasing the grid inductance L_g to 4.8 mH. The converter-side inductance L_1 has also been increased to 3.6 mH with the other filter parameters kept unchanged. The purpose is to significantly bring down the resonance frequency f_r to 1.62 kHz according to (3.1), but with L_2 replaced by $L_2 + L_g$. This value is closer to $f_n = f_s / 6$ of the k damper with trap current feedback, which according to Table 3.2 will result in zero resistive damping ($R_{eq} \approx 0$). Its results in Figure 3.15(b) are seen to be oscillatory. In contrast, the results in Figure 3.15(a) for the k damper with trap voltage feedback and Figure 3.15(c) for the high-pass damper with trap current feedback are not degraded. The common reason is related to their higher critical frequency ($f_n = f_s / 3$), which will never be exceeded regardless of how L_g varies. They are therefore robust dampers that can be safely used with a grid converter.

3.4 Summary

This chapter analyses different active dampers based on their non-minimum-phase responses and stability criteria for the *LLCL*-filtered voltage source converter. Different circuit equivalences of the dampers with and without delays considered are developed to get the essential behavior of the different dampers. However an optimal damper, which is designed in the analogue system, may become suboptimal due to the delay when a regularly sampled system is used.

Several suitable dampers based on the trap circuit are identified for the regularly sampled system. Both simple k and low-pass dampers with trap voltage feedback have high critical frequency, and are hence more robust to variations of the grid and filter parameters. Analyses are then performed to identify their respective stable k ranges, which for the low-pass damper with trap voltage feedback can be widened by increasing its cutoff frequency. However this flexibility is at the expense of a slower dynamics. Experimental results have confirmed these expectations and the unmatched fast dynamic of a simple k damper with trap voltage feedback.

Chapter 4 Design of *LLCL*-Filtered Grid Converter with Improved Stability and Robustness

Chapter 2 has illustrated a basic design method for high order filter. Considering the size and volume of the high order filer, the *LLCL* filter is a proper choice to use. Chapter 3 investigates and compares different active dampers for *LLCL* filters when the resonance frequency is placed below one-sixth of the sampling frequency. Even if the resonance frequency of the designed filter is above one-sixth of the sampling frequency, the system is not very robust since a change in the grid impedance may accidentally push the resonance peaks below f_s / 6. This chapter will propose a new design method to improve the system robustness and stability of the *LLCL*-filtered grid converter by using a passivity-based design method without active damper, which can also be applied for an *LCL*-filtered grid converter.

4.1 Norton equivalent model

Figure 4.1 shows the *LLCL*-filtered converter with a single control loop. The single feedback loop with only a current controller is realized in the stationary *αβ*-frame. Between the voltage u_{pcc} at the Point-of-Common-Coupling (PCC) and grid voltage u_g is the grid impedance Z_g, whose value is normally changing. Figure 4.2 shows the Norton equivalent model of a grid-connected converter with grid current control [88–91]. The dotted block is the cable capacitance C_g and line impedance L_g. The derivations of the terminal behavior of the grid current control are shown as given below. Figure 4.3 illustrates the control loop diagram. The impedances Z_{L1}, Z_{LC} and Z_{L2} represent L_1, the middle L_fC_f trap and L_2, respectively. Table 4.1 shows the system parameters. The open loop transfer functions i_g / u_i and i_g / u_{pcc} are expressed in (4.1) and (4.2), respectively.

$$G_1 = \frac{i_g}{u_i}\bigg|_{u_{pcc}=0} = \frac{Z_{CL}}{Z_{L1}Z_{L2} + Z_{L1}Z_{CL} + Z_{L2}Z_{CL}} \qquad (4.1)$$

$$G_2 = \frac{i_g}{u_{pcc}}\bigg|_{u_i=0} = \frac{Z_{L1} + Z_{CL}}{Z_{L1}Z_{L2} + Z_{L1}Z_{CL} + Z_{L2}Z_{CL}} \qquad (4.2)$$
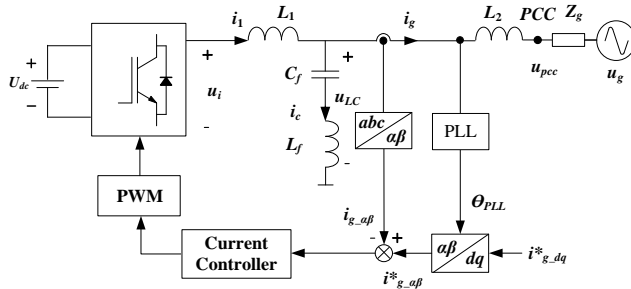
Figure 4.1: *LLCL*-filtered converter with a single control loop.
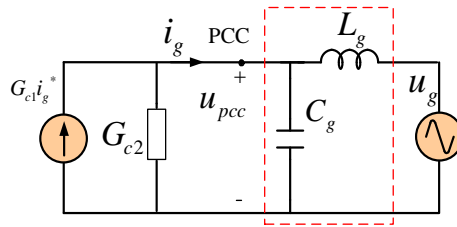
Figure 4.2: Norton equivalent model of the grid-connected converter through a cable using grid current control.
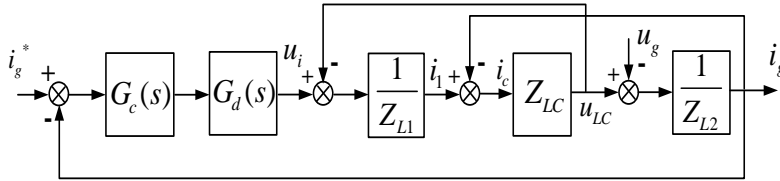
Figure 4.3: Grid current control of an *LLCL*-filtered converter.

Table 4.1: System parameters for studies.

Symbol	Definition	Value
U_{dc}	DC link voltage	730 V
U_g	Grid voltage	400 V
f_o	Grid frequency	50 Hz
$T_s = 1/f_s$	Sampling period	100 μs
$f_{sw} = f_s$	Switching frequency	10 kHz

The controller $G_c(s)$ can be a Proportional-Resonant (PR) controller with multiple resonant peaks at low-order harmonic frequencies, expressed as:

$$G_c(s) = K_p + \sum_{h=1,5,7,11,13} \frac{K_{ih}s}{s^2 + (\omega_0 h)^2} \tag{4.3}$$

where $\omega_o = 2\pi f_o$ is the fundamental angular frequency, K_p is the proportional gain, and K_{ih} is the resonant gain at harmonic order h. Delay $G_d(s)$ is expressed as $e^{-\lambda T_s s}$. $T_s = 1 / f_s$ is the sampling period, f_s is sampling frequency and λ is the delay time coefficient normalized with T_s.

The open-loop gain T, closed-loop gain G_{c1} and closed-loop output admittance G_{c2} of the single-loop grid current control can then be determined as:

$$T = G_c G_d G_1 \tag{4.4}$$

$$G_{c1} = \frac{T}{1+T} \tag{4.5}$$

$$G_{c2} = \frac{G_2}{1+T} = 1/(\frac{1}{G_2} + \frac{T}{G_2}) \tag{4.6}$$

4.2 Concept of passivity

In order to make a linear continuous system $G(s)$ to be passive, it must satisfy two requirements at the frequency ω, given by the following [91, 93]:

1) $G(s)$ has no Right-Half-Plane (RHP) poles, and

2) $\mathrm{Re}\left\{G(\mathrm{j}\omega)\right\} \geq 0 \Leftrightarrow \arg\left\{G(\mathrm{j}\omega)\right\} \in \left[-90°,\ 90°\right], \forall \omega > 0.$

The stability of the system in Figure 4.2 is only decided by the closed-loop output admittance G_{c2} of the converter, which hence also be passive. However passivity of G_{c2} is not always ensured especially, when the computational delay G_d is considered as shown in Figure 4.2. The term of G_{c2} in (4.6) depending on the delay is written as G_{2T}, which is expressed:

$$G_{2T} = \frac{G_2}{T} = \frac{1-(L_1+L_f)C_f\omega^2}{K_{PWM}K_p(1-C_f L_f\omega^2)}e^{j\lambda T_s\omega} = \frac{1-(L_1+L_f)C_f\omega^2}{K_{PWM}K_p(1-C_f L_f\omega^2)}\left[\cos(\lambda T_s\omega)+\mathrm{j}\sin(\lambda T_s\omega)\right] \tag{4.7}$$

To make sure the real part of G_{c2} is positive, several importance frequencies f_{rc}, f_{sw} and f_{rd} are defined in (4.8):

$$\begin{cases} f_{rc} = \dfrac{1}{2\pi\sqrt{(L_1+L_f)C_f}} \\[2mm] f_{sw} = 1/(2\pi\sqrt{L_f C_f}) \\[2mm] f_{rd} = \dfrac{f_s}{4\lambda} \end{cases} \tag{4.8}$$

Table 4.2: *LLCL* filter parameters used in Figure 4.4.

Symbol	$f_{rc} > f_r/6$	$f_{rc} = f_r/6$	$f_{rc} < f_r/6$
L_1	2.2 mH	2.2 mH	2.2 mH
L_2	1.8 mH	1.8 mH	1.8 mH
L_f	128 μH	64 μH	32 μH
C_f	2 μF	4 μF	8 μF
f_{rc}	1.19 kHz	1.67 kHz	2.34 kHz
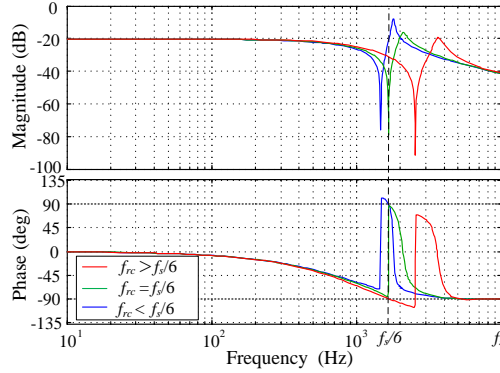
Figure 4.4: Bode plots of closed-loop output admittance G_{c2} with different f_{rc} values.

The real part of (4.7) can be simplified as described in (4.9).

$$Re\{G_{2T}\} = \frac{1-\left(\omega/(2\pi f_{rc})\right)^2}{K_{PWM}K_p(1-\left(\omega/(2\pi f_s)\right)^2)} cos(\frac{\pi}{2} \times \frac{\omega}{(2\pi f_{rd})}) \tag{4.9}$$

The denominator of (4.9) will always be positive under normal operation up to the Nyquist frequency $\omega < \pi f_s$. The polarity of (4.9) is therefore solely determined by two terms in the numerator, from which the following three observations can be drawn.

1) By setting $f_{rc} < f_{rd}$, (4.9) will be negative in the range of $f_{rc} < \omega / (2\pi) < f_{rd}$.
2) By setting $f_{rd} < f_{rc}$, (4.9) will be negative in the range of $f_{rd} < \omega / (2\pi) < f_{rc}$.
3) By setting $f_{rc} = f_{rd}$, (4.9) will always be positive.

The third condition will let (4.7) always to be positive, and hence robust passive output admittance G_{c2} will always appear across the converter model shown in Figure 4.2. The overall system is thus always stable regardless of how the grid impedance changes. Figure 4.4 shows the Bode plots of close output admittance with the case of $\lambda = 1.5$, and $f_{rd} = f_s / 6$ based on the filter parameters in Table 4.2.
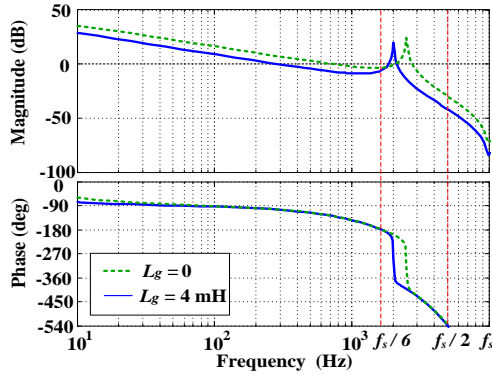
Figure 4.5 Bode plots of open-loop control gain T with different L_g values using $L_1 = 1.8$ mH, $L_2 = 2$ mH, $L_f = 64$ μH and $C_f = 4$ μF.

The aim of the task is to identify regions, where G_{c2} becomes negative, or has a phase exceeding 90° or falling below −90°. The identification then leads to the following three summarized observations.

1) Phase greater than 90° only happens between f_{rc} and $f_s / 6$ if $f_{rc} < f_s / 6$.
2) Phase smaller than −90° only happens between $f_s / 6$ and f_{rc} if $f_s / 6 < f_{rc}$.
3) Phase will always be between −90° and 90° if $f_{rc} = f_s / 6$.

As anticipated, $f_{rc} = f_{rd}$ is the optimal equality if both stability and robustness are to be ensured simultaneously.

4.3 Criterion for stability and robustness without damping

For most digitally controlled systems, a delay of $\lambda = 1.5$ is common [94, 95]. f_{rd} is then $f_s / 6$, which is also the frequency derived for an other aspect related to an *LLCL*-filtered converter, according to (4.7). To be more precise, it has been proven in chapter 2 that if the system resonance frequency f_r is placed above $f_s / 6$, no damping is needed for stabilizing the *LLCL*-filtered converter. This can be seen from Figure 4.5, where the frequency responses of the open-loop gain T in (4.4) without damping have been plotted. The system is stable since its phase crosses −180° before the resonance peak at f_r, especially for the case of $L_g = 0$. As L_g increases to 4 mH, the system is still stable, but its resonance peak has moved closer to $f_s / 6$. This movement will continue as L_g increases further until the resonance peak could eventually falls below $f_s / 6$. If that happens, the system cannot be stabilized without damping methods. The study in therefore lacks robustness, which has now been solved in this chapter by deriving the optimal equality of $f_{rc} = f_{rd} = f_s / 6$.

The equality is however tough to satisfy precisely since f_{rc} depends on the filter parameters L_1, L_f and C_f, which can still vary even though not as much as the grid impedance. A more relaxed condition can therefore be helpful, and it is provided in (4.10) with the system resonance frequency f_r included.

$$f_{rd} = f_s / 6 \le f_{rc} < f_r \qquad (4.10)$$

If f_{rc} is higher than $f_s / 6$ in (4.10) it will create an interval ($f_s / 6 < \omega / (2\pi) < f_{rc}$), within which the real part of the converter output admittance G_{c2} in Figure 4.4 will become negative, and hence no longer passive. However, this interval will never be entered by the system resonance frequency f_r, with $\dfrac{L_1 \left(L_2 + L_g \right)}{L_1 + L_2 + L_g} = L_1 // \left(L_2 + L_g \right) < L_1$.

The resonance frequency f_r will therefore always be higher than f_{rc} regardless of how L_g varies. Condition (4.10) is thus a strong design criterion newly formulated for the *LLCL* filter, which guarantees both stability and robustness even with no damping added to the converter. The same criterion in (4.10) can also be applied to an *LCL* filter by setting $L_f = 0$. It should however be noted that for an *LCL* filter, its harmonic attenuation around the switching frequency can be decreased by keeping its resonance frequency f_r above $f_s / 6$. Its attenuation will, in fact, approach the level of a large first-order *L* filter. This problem is not experienced by an *LLCL* filter because of its tuned $L_f C_f$ trap added for removing harmonics around the switching frequency.

4.4 Parameter design procedure

When designing a power filter, the base impedance of the applied system can be defined using values from Table 4.1. If the rated power P_o is 5kW, the base impedance, base capacitance and base inductance can be calculated as $Z_b = \dfrac{U_g^2}{P_o} = 32$

Ω, $C_b = \dfrac{1}{\omega_o Z_b} = 100\ \mu\text{F}$, $L_b = \dfrac{Z_b}{\omega_o} = 102\ \text{mH}$.

4.4.1 Filter parameter design

Based on the derivations presented in [96-99], filter design can be addressed as given below. L_1 can be sized with $L_1 = U_{dc} / (8 f_s \alpha I_{ref})$, where U_{dc} is the dc-link voltage [74]. This means the peak-to-peak current ripple at the converter switching frequency f_s does not exceed α times of its peak rated current I_{ref}. According to [32], α can be up to 60 % for an *LLCL* filter with better harmonic attenuation at the converter switching frequency. Substituting values from Table 4.1, a more
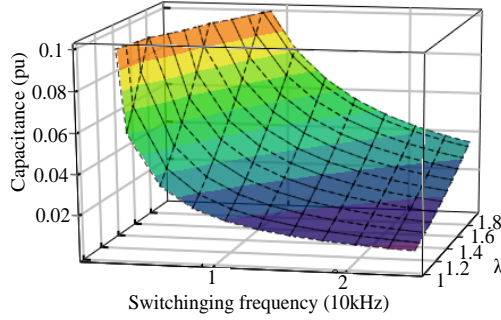
Figure 4.6: Capacitance variation with switching frequency and delay λ.

(a)   (b)
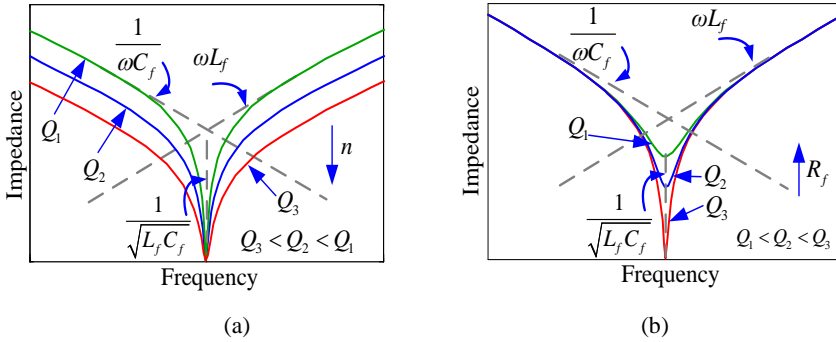
Figure 4.7: *LC* trap impedance variation with (a) different *n*, (b) different R_f.

conservative *α* of 49 % eventually gives L_1 = 1.8 mH used for the experimental filter and implemented for testing.

From (4.8), C_f can be calculated after deciding on L_1, as $f_s = 1/\left(2\pi\sqrt{L_fC_f}\right)$ and a value for $f_{rc} \geq f_s / (4\lambda)$ ($f_{rc} = f_s / 6$ if $\lambda = 1.5$). The value C_f is not unique and varies with other parameters used for computing it. This is demonstrated in Figure 4.6, where C_f (in *p.u.*) is shown to increase with smaller f_s and larger λ. In terms of its base value, C_f is then constrained according to C_f = 5% × C_b. which for the implemented filter, is calculated as 4.9 µF with $\lambda = 1.5$ and f_s = 10 kHz.

After deciding on C_f = 4.9 µF, the inductance L_f = 52 µH can be calculated immediately since they form a series trap at the converter switching frequency of f_s = 10 kHz. The extent of the attenuation introduced by the series trap is however influenced by its quality factor Q, which definition is provided in (4.11) and (4.12):

$$Q = \frac{1}{R_f}\sqrt{\frac{L_f}{C_f}}$$

(4. 11)

$$n = \sqrt{\frac{L_f}{C_f}} \qquad (4.\,12)$$

where R_f represents the combined equivalent series resistance of L_f and C_f. The quality factor Q therefore depends on both R_f and n, and their influence on the series trap impedance are illustrated in Figure 4.7. Figure 4.7 (a) shows that the trap width can be broadened by increasing n, and hence Q, without affecting the minimum achievable attenuation. This can be helpful if the sideband harmonics centered at the switching frequency. In contrast, Figure 4.7 (b) shows that the width of the trap is not significantly changed by increasing R_f, and hence decreasing Q. The depth is changed by R_f. The minimum trap impedance is raised, which will cause that the attenuation will not to be effective.

It is therefore preferred to keep R_f low, especially when the damping is not required. The value of Q should therefore be closer to 50, if the usual practical range of $10 \leq Q \leq 50$ is considered [32]. The Inductance L_2 is designed as the last step, which needs to attenuate the harmonics around the double of the switching frequency to be lesser than 0.3% according to the IEEE 519-1992 standard [72]. Based on this, L_2 is chosen as 1.2 mH. The overall range of the system resonance frequency f_r variation can then be computed by substituting extreme values of the grid inductance L_g. The lowest f_r computed will however still be higher than the f_{rc} computed using (4.8) and (4.10) will always be met, implying that the designed *LLCL*-filtered converter will always be robust stable regardless of how L_g varies.

4.4.2 Other Constraints

The flow chart of the proposed parameter design procedure is shown in Figure 4.8 to make sure that other converter and grid limitations are coordinated. One of them is related to the total inductance $(L_1 + L_2)$ and its voltage drop, which if it is excessive, will raise the minimum required dc-link voltage, and hence increase the system losses. It is therefore advisable to limit $(L_1 + L_2)$ below 0.1 *p.u.*. Such limitation can be realized by increasing the converter switching frequency and / or capacitance C_f, as demonstrated in Figure 4.9. Lowering of $(L_1 + L_2)$ must however not be too excessive since low-order harmonics in the grid current must be kept below the IEEE 519-1992 standard.
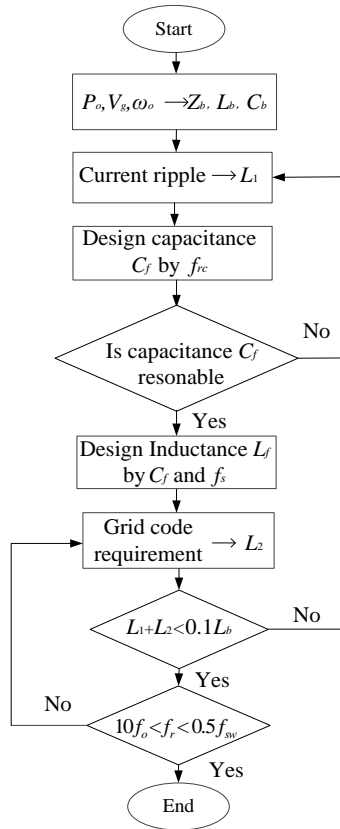
Figure 4.8: Flow chart showing the proposed parameter design procedure.
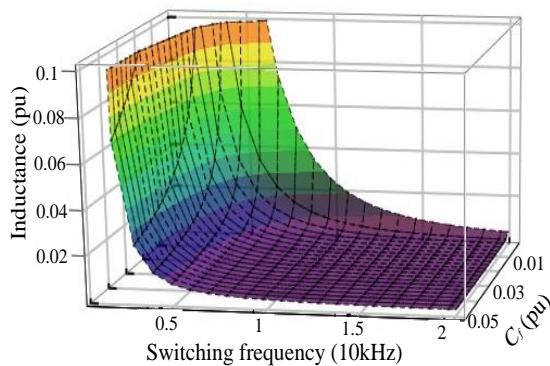
Figure 4.9 Total inductance variation with capacitance and switching frequency with $U_{dc} = 730\text{V}$.

The next issue to check is whether the system resonance frequency f_r is above ten times the line frequency and below the Nyquist frequency, which is half the

Table 4.3: Filter parameters for *LLCL* filter.

Symbol	Definition	Case I	Case II
L_1	Inverter-side inductor	1.8 mH	1.8 mH
L_2	Grid-side inductor	1.2 mH	1.2mH
L_f	Resonant inductor	52 μH	38 μH
C_f	Capacitor	4.9 μF	6.7 μF
f_r	Resonant frequency ($L_g = 0$ mH)	2.56 kHz	2.23 kHz
f_{rc}	Frequency	1.67 kHz	1.42 kHz

sampling frequency f_s. The lower limit is for avoiding common low-order harmonics present in the grid, which in most cases, is not a concern since f_r has intentionally been placed above $f_s / 6$, as demanded by (4.10). The upper Nyquist limit can also safely be avoided by designing f_r to be smaller than the Nyquist frequency when L_g = 0. As L_g increases in a real grid, f_r will then shift towards the left and away from the Nyquist frequency, as shown in Figure 4.5.

Another frequency range of interest is that related to f_{rc}, which in the case of parameter drift, will deviate from its nominal value. The deviation can be computed by assuming a +5% change for C_f, and a ±2% change for L_1 and L_f, according to the industrial filter tolerances specified in [101]. Substituting these tolerances to f_{rc} and it varies between 96.9% and 103% of its nominal value $f_{rc,nom}$. The design using (4.10) must hence consider 96.9% × $f_{rc,nom}$ rather than $f_{rc,nom}$. The parameters satisfying (4.10) and used for implementing the experimental *LLCL*-filter are given as Case I in Table 4.3. For comparison, Case II is designed without satisfying (4.10) and it is also given in the table. The non-optimized frequency relation of Case II is $f_{rc} < f_s / 6 < f_r$, which will gradually lead to instability, when f_r is pushed below $f_s / 6$ by a sufficiently large grid inductance.

4.4.3 Controller Design

The grid current is controlled by a PR controller G_c(s) with multiple resonant peaks at the 5th, 7th, 11th and 13th harmonics. The controller scheme is shown in Figure 4.1 in. For digital implementation, the open-loop transfer function in (4.4) is discretized by appling a zero-order-hold (ZOH) transform to give (4.13) in the *z*-domain for the analysis.

$$T(z) = K_p \cdot z^{-1} \cdot Z\left[\frac{1 - e^{-sT_s}}{s} G_1\right] \tag{4.13}$$
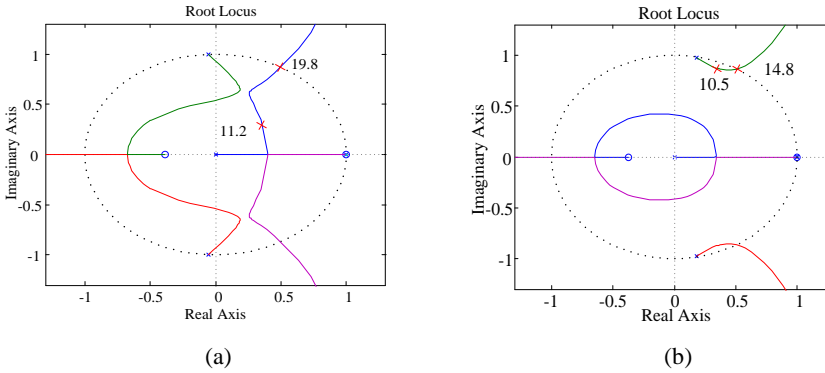
Figure 4.10: Root loci of the grid-current-controlled converter when filtered by parameters from (a) Case I and (b) Case II without damping.

Stability of the grid-current-controlled converter can then be analyzed by drawing root loci using filter parameters summarized in Table 4.3 for Case I and Case II.

Figure 4.10 shows the root loci drawn by increasing K_p, while keeping $L_g = 0$ and the relative low resonant gain at $K_{ih} = 500$. The figures clearly show that for Case I, the maximum K_p is 19.8, while for case II, it is 14.8. The values chosen are thus $K_p =$ 14.8 for Case I and $K_p = 10.5$ for Case II, based on the largest obtainable damping ratios. These values will be used for further test.

4.5 Experimental results

The experimental setup consists of a 5-kW Danfoss FC302 converter tied to the grid through a transformer and an *LLCL* filter. The power source to the converter is provided by a Delta Elektronika dc power supply.

The parameters used for experiments are summarized in Table 4.1 and Table 4.2, where the latter includes Case I and Case II designed with and without (4.9) considered. With this setup and the designed controller, Figure 4.11(a) shows the steady-state grid currents and voltage across the L_fC_f trap obtained with $L_g = 0$ mH and those properly designed *LLCL* parameters of Case I. Figure 4.11(b) shows the grid current spectrum, which clearly has dominant harmonics only at twice the switching frequency. This is expected since the dominant harmonics at the switching frequency have been diverted away by the L_fC_f trap. Harmonics compensation in experiments are set to $h = 5, 7, 11$ and 13.
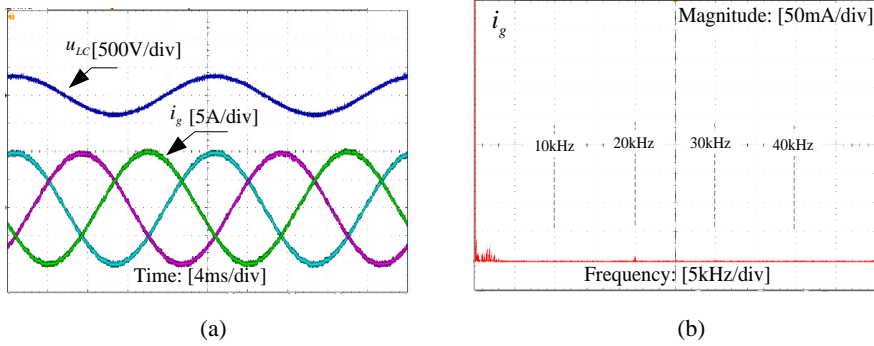
Figure 4.11: Experimental results of (a) voltage across *LC* trap and grid currents, and (b) grid current spectrum obtained with properly designed *LLCL* parameters from Case I with output power is 5 kW.
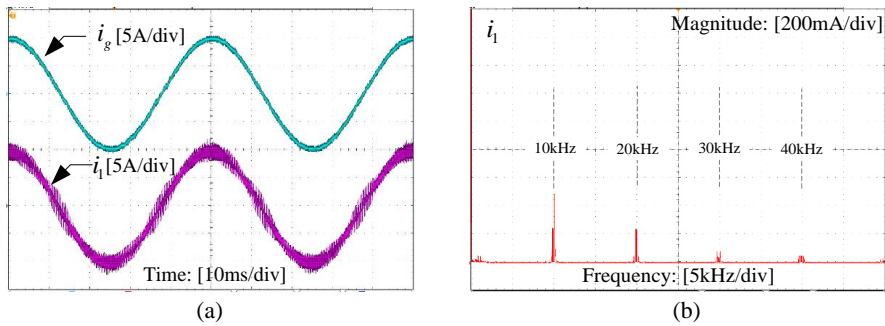
Figure 4.12: Experimental results of (a) grid- and converter-side currents, and (b) converter-side current spectrum obtained with properly designed *LLCL* parameters from Case I with output power is 5 kW.

Figure 4.12(a) shows the grid side and converter side currents with the properly designed *LLCL* parameters of Case I. The spectrum of the converter-side current is also given in Figure 4.12(b), which clearly has dominant harmonics at the switching frequency. This is expected since the dominant harmonics at the switching frequency will only be removed after passing through the L_fC_f trap. They will therefore only be removed in Figure 4.11(b), where the grid current spectrum has been plotted.

Figure 4.13(a) and Figure 4.13(b) show the grid currents for Case I and Case II, respectively. Both cases are dynamically comparable, even though Case I has a slightly less oscillatory response. However Case I is more robust as demonstrated by comparing Figure 4.14(a) for Case I with Figure 4.14(b) for Case II. Both figures show the same grid currents and voltage across the L_fC_f trap, but with L_g increased from 0 to 5 mH. The increase causes the resonance peak f_r to shift leftwards, as also seen from Figure 4.5. The shift is however always above f_s / 6 for Case I. Case I is

(a)   (b)
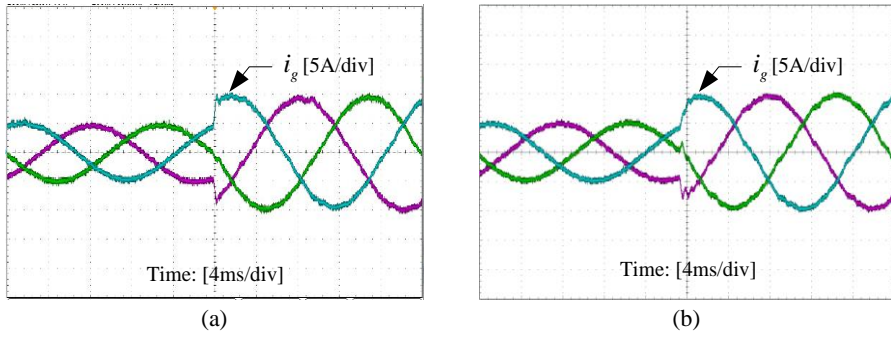
Figure 4.13: Experimental grid currents during transition from half to full load with $L_g = 0$ and filter parameters from (a) Case I and (b) Case II at 5 kW load.

(a)   (b)
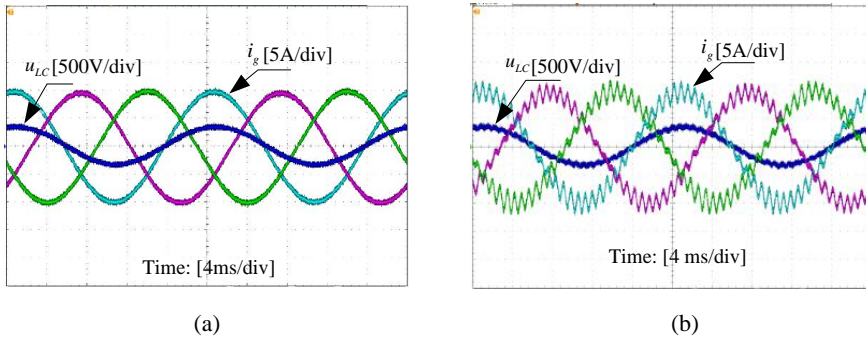
Figure 4.14: Experimental voltage across LC trap and grid currents with the same $L_g = 5$ mH, but different filter parameters from (a) Case I and (b) Case II at 5 kW load.

thus robust stable even with no passive and active damper used with the converter. On the other hand, case II is not robust since higher L_g has changed f_r to be below f_s / 6.

To further test the converter robustness with Case I, C_g in Figure 4.1 is set to a value of 6.7 μF, while L_g is set to 1.8 mH. The waveforms obtained are shown in Figure 4.15(a), which again are stable since the closed-loop output admittance G_{c2} in Figure 4.1 has been designed always to be passive. This robustness will obviously be lost in Figure 4.15(b) for Case II, since the chosen C_g and L_g have caused its resonance peak f_r to move between f_{rc} and f_s / 6. It is therefore important to design with (4.10), if a robust passivity of G_{c2} and stability of the system are to be ensured simultaneously.
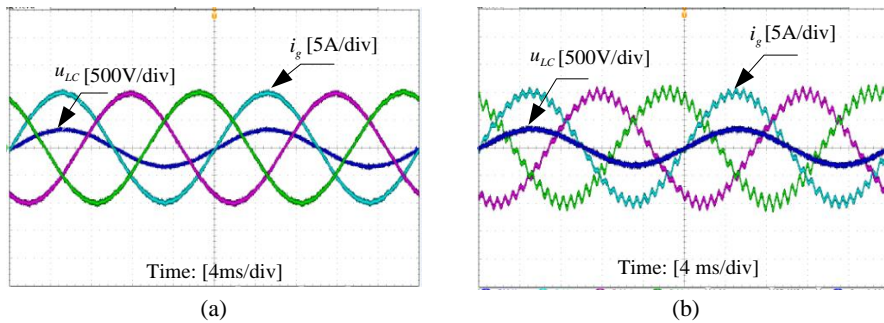
Figure 4.15: Experimental voltage across *LC* trap and grid currents with the same $L_g =$ 1.2 mH and $C_g = 6.7$ μF, but with different filter parameters from (a) Case I and (b) Case II at 5 kW load.

4.6 Summary

Based on the basic filter design method, a developed criterion is eventually used to improve the filter design procedure with both grid and filter parameter variations taken into consideration. The concept of passivity is applied to an *LLCL*-filtered converter with the purpose to derive an optimal condition, which when met, will guarantee system stability and robustness simultaneously. The criterion is also suitable for the *LCL* filter. If the situation is satisfied, it will ensure system stability and robustness simultaneously even without additional damping added to the system.

Chapter 5 Trap Filter Application for Current Source Converters

The resonant frequency characteristics of the filter used in a Current Source Rectifier (CSR) are analyzed. A filter design procedure is proposed based on the input power factor, filter capacitor voltage and the line current THD using Space Vector Modulation (SVM). The resonance of the input filter can be excited by the Pulse Width Modulation (PWM) and a simple passive damping method can damp the resonances. However, passive damping will bring system loss and instead impedance based active damping could be implemented. The analysis and design of the input filter have been verified by simulations in the MATLAB/Simulink. This chapter investigates also an LC + trap filter for the current source converters to improve the dominant harmonics filtering. Hence, a high power factor can be achieved and smaller passive components are required. A filter design procedure is proposed based on SVM modulation. Then active damping methods for current source converter are also proposed.

5.1 Introduction of current source converter

5.1.1 Description of current source converter

The traditional three-phase PWM CSR usually inserts an inductor as a dc-link to serve a constant current source, which has been successfully applied in high-power medium-voltage drives for their input power supply [102, 103]. The three phase CSR can also be regarded as a buck rectifier, which is applied in data center power supplies based on its step down conversion function and high efficiency [16, 104-106]. Current Source Inverter (CSI) is preferred in photovoltaics to generate ac power from the dc side with high conversion efficiency. CSI is capable to step up the voltage from dc side to ac side without using boost converter and also ride through grid faults such as voltage sags [107-110].

Compared to traditional thyristor rectifiers, the PWM current source rectifiers (CSRs) feature improved input power factor, reduced line current distortion and superior dynamic response [111]. The Gate-Turn-Off thyristors (GTOs) or Gate Commutated Thyristors (GCTs) can be used as switching device with low switching frequency, around several hundred Hertz [112, 113]. Three-phase CSR is also a promising solution for power supply system as front end buck-type rectifier. With the development of the SiC and GaN devices with lower resistance [16], SiC JFETs
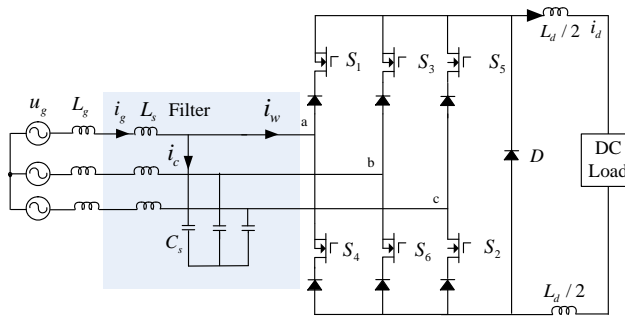
Figure 5.1: A PWM Current Source Rectifier (CSR) with an input *LC* filter.

and SiC MOSFETs have been applied for current source converters with high switching frequency to reduce the system loss [115, 114-115]. Figure 5.1 shows the diagram of a PWM CSR with an input *LC* filter.

There are various modulation techniques for the current source converters, which include Trapezoidal Pulse with Modulation (TPWM), Selective Harmonic Elimination (SHE), Carrier based Sinusoidal Pulse Width Modulation (CSPWM) and Space Vector Modulation (SVM) [111]. SHE has been widely used for high-power medium-voltage current-source drives and the switching frequency is usually several hundred Hz [116-119]. It is optimized to eliminate certain harmonics in the line current and motor current through the PWM pattern. It is usually implemented as an offline technique. CSPWM is suitable for analogue realization and easier to implement. SVM can offer a faster dynamic response, an instantaneous adjustment of the modulation index [111, 120-122]. A precise control of the dc and ac current magnitude and phase can also been achieved. For converters which switch at a relatively higher frequency carrier modulation the SVM is preferred to be implemented.

Different from the voltage source converter, open circuit should be avoided in the circuit and a diode is normally connected in series with a switch to block the reverse voltage. Overlap time is added in the gate signals of the current source converter to prevent any dc current interruption [113, 123]. The overlap time will cause error in the current control and increase the low-order harmonics in the input current. But switch or modulation fault could bring an open circuit when the dc link inductor carries current, thus the dc inductor could produce a high voltage spike which will destroy the switches [111, 113]. The freewheeling diode D is added in the rectifier to provide a path for the current of dc link inductor. There are some research papers focusing on the protection circuit [24, 25]. The overvoltage on the
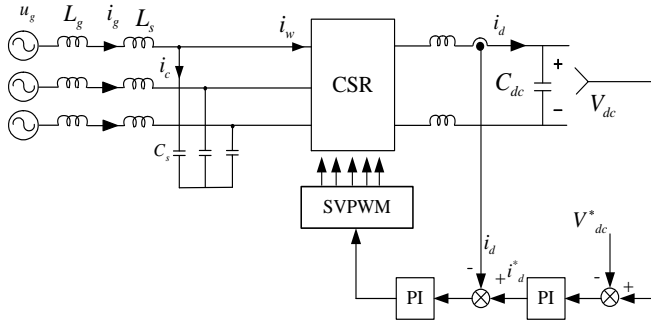
Figure 5.2: Two loop control scheme of three-phase current source rectifier.

devices can be detected and clamped by using a diode bridge and a transient-voltage-suppression (TVS) [24].

5.1.2 PWM CSR control and filter resonance problem

In the CSR, the PWM current waveform is discontinuous and has harmonic components at the multiples of the switching/carrier frequency. Traditionally, an *LC*-filter has to be inserted on the ac side to reduce the current harmonics in the current source rectifiers. In this chapter, SVM with a relative high switching frequency is investigated. When the switching frequency is several hundred Hertz, the SVM could generate high lower order harmonics (5th, 7th, 11th and 13th) and a high switching frequency to fundamental frequency ratio generates relative low harmonic distortion.

In some other dc power supply applications like uninterrupted power supply and power distribution architecture, a capacitor is connected after the inductor to convert the current source into a voltage source as shown in Figure 5.2. The dc-link current and voltage are controlled by modulation index regulation of space vector pulse width modulation. The controller has two control loops [124]. The outer loop is dc voltage control loop. The dc voltage (V_{dc}) of the dc capacitor is fed back to generate the dc current reference for the inner dc current control loop. In the dc current control loop, the dc current (i_d) in the output dc inductor is fed back to the current compensator to generate the duty cycle on the *d* axis in SVM [16].

In order to reduce the size of the passive components, the trap filter can also be applied in current source converters. This chapter investigates an *LC* + trap filter for a filter design procedure in combination with SVM modulation. A challenge in the PWM CSR systems is the possible resonance caused by the rectifier input *LC/LC* + trap filter. The filter resonances can be excited by the harmonics from the PWM modulation or from the background grid voltage distortion. What's more, the
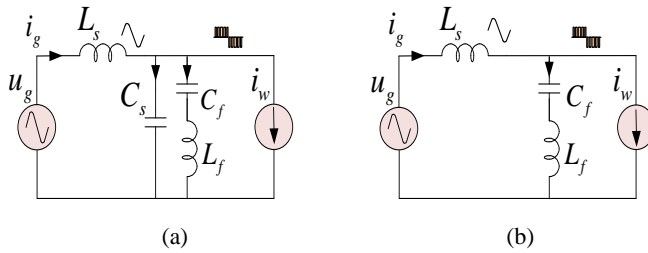
Figure 5.3: Equivalent of Current Source Rectifier. (a) *LC*+trap filter (b) *L*+trap filter.

variation of the line impedance could lower the filter resonance frequency and excite some resonances at the low order harmonics. There are many references talking about the active damping and passive damping of current source converters in high power application with low switching frequency [125-131], such as virtual impedance, feedforward control signal compensation [128], hybrid combination of a virtual resistor and a three step compensator [127]. [126] proposed an active damping method using both the filter inductor current and filter capacitor voltage as the feedback signals to the PWM generator. The impact of the dc side circuit on the CSR input *LC* resonance is related to the PWM switching pattern.

5.2 *LC*+trap filter for current source rectifier

It can be seen in Figure 5.1 that a smoothing reactor L_d is placed on the dc side, which forces a constant DC current. An *LC* filter has to be inserted on the ac side to reduce the current harmonics injected by the PWM operation. In practice, the dc-link inductor is usually split into two inductors placed on both positive and negative buses to reduce the common-mode noise or circulating current in the converters. In a CSR system, the line capacitor C_s is required to provide a path for the current to assist the PWM commutation. L_s is the inductor of the filter and L_g is the grid impedance. i_d is the dc current, i_w is the input PWM current, i_c is the current of the capacitor C_s, and i_g is the grid current. The investigated switching frequency of the CSR here is relatively high and the modulation index m is defined as the ratio of the peak value of the fundamental frequency component in i_w to the average dc link current which is $m = I_w / I_d$.

5.2.1 Trap circuit application

The *LC* trap has been applied in the filter for voltage source converter in order to get better attenuation at the dominant harmonics. For filter-based current source converter, an L_f-C_f series resonant circuit at the dominant harmonic frequency can be added to reduce the filter size as shown in Figure 5.3. Figure 5.3 (a) shows that the
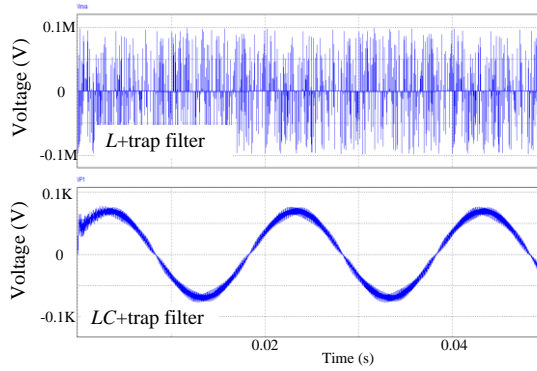
Figure 5.4: Example of voltage cross the $L_f C_f$ trap.

LC trap is additionally added and Figure 5.3 (b) shows the trap is constructed based on the capacitor like the *LLCL* filter for the voltage source converter. It can be seen from Figure 5.4 that the *L* + trap filter will bring voltage spike, which may damage the device if it is not properly handled. This is because the *LC* trap acts like an inductor when the frequency is higher than the switching frequency.

During the commutation of the current it could turn to zero and the trap circuit could excite a voltage spike. As shown in (5.1), $I_{h,k}$ is the *k*th harmonic current component, $V_{h,k}$ is the *k*th harmonic voltage component and f_i is the corresponding frequency. Hence, the capacitor is very necessary here to provide a current path for the energy trap. The capacitor acts as a harmonic filter and also assists the communication of the switching devices.

$$V_{h,k} = \frac{mI_{h,k}}{C_s 2\pi f_i \sqrt{2}} \tag{5.1}$$

Due to the input capacitor, a leading power factor could be produced, especially under light loading conditions [132]. It varies with the rectifier operating point. With the decrease of the capacitor size the power factor will increase and at the same time the system resonant frequency will be increased. The phasor diagram given in Figure 5.5 is obtained based on the assumption that the PWM current i_w is synchronized to the capacitor voltage u_c. The displacement angle between the grid voltage u_g and the grid current i_g can be calculated by:

$$\theta = tan^{-1} \frac{V_C}{I_w X_{Ceq}} - tan^{-1} \frac{X_{Leq} I_w}{V_C \left(1 - \dfrac{X_{Leq}}{X_{Ceq}}\right)} \tag{5.2}$$
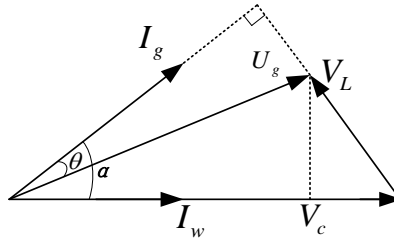
Figure 5.5: Phasor diagram of PWM rectifier.
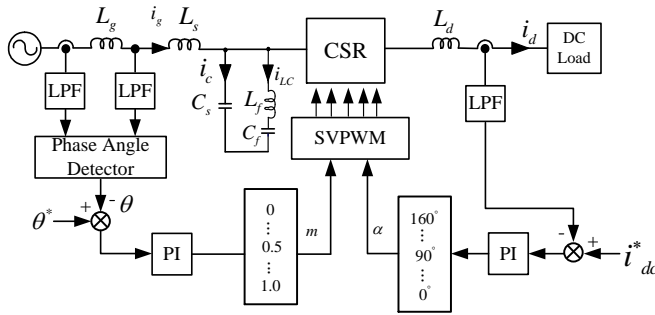
Figure 5.6: Power factor control scheme for CSR.

where V_c is the magnitude of voltage u_c of the capacitor C_f and I_w is the magnitude of i_w. X_{Leq} is the CSR grid inductive reactance due to the effects of filter inductance L_s and the grid impedance L_g. X_{Leq} is the paralleled reactance determined by the filter capacitor and the trap circuit impedance. It can be found that a unity power factor can be achieved when θ is zero. Normally the selection of the filter components requires the consideration (5.2) to obtain a good power factor performance at a reasonable filter cost. [113] shows a power factor scheme for current source rectifier, as shown in Figure 5.6. To achieve unity power factor control, the delay angle α should satisfy the following equation:

$$\alpha = sin^{-1} \frac{\omega_o C_s U_g}{mI_d} \tag{5.3}$$

ω_o is the fundermental frequency and U_g is the peak of fundermental frequency component of the grid voltage.

5.2.2 Space vector modulation

Figure 5.7 shows the space vector diagram for CSR. The current space vector is defined in (5.4). The PWM switching pattern must satisfy a constraint that two
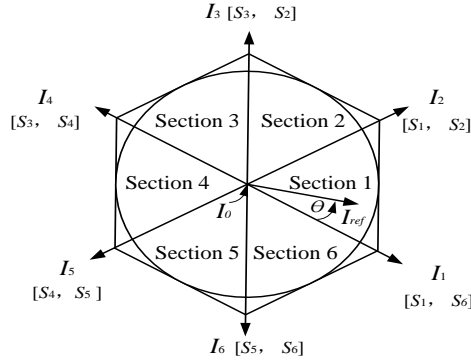
Figure 5.7: Space vector diagram for CSR.

switches conduct at any time instant, one in the top half of the CSR bridge and the other in the bottom half. There are six active and three zero vectors corresponding to nine switching states of the CSR. Six active vectors form a regular hexagon with six equal sectors (I_1, I_2... I_6). [S_1, S_6] refers to the switching state, when switches S_1 and S_6 are on. The zero vectors refer to when two switches on the same bridge are turned on and the dc current is bypassed. θ is the angular position of the average input current space vector with respect to the lagging vector or the first vector in the corresponding sector.

In one sampling cycle time T_s, the reference current vector I_{ref} can be synthesized by three stationary vectors, which are two adjacent active vectors and one zero vector. T_s is composed of time periods T_1, T_2, and T_0, as shown in (5.5).

$$I_{ref} = i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j-\frac{2\pi}{3}} \tag{5.4}$$

$$\begin{cases} T_1 = m\sin(\frac{\pi}{3} - \theta)T_s \\ T_2 = m\sin\theta T_s \\ T_0 = 1 - T_1 - T_2 \end{cases} \tag{5.5}$$

$$\Delta i_w = \sqrt{m\left(\frac{2}{\pi} - \frac{m}{2}\right)} I_d \tag{5.6}$$

The RMS of the input line current over one sampling cycle T_s can be obtained by (5.6), which is a function of the modulation index m [111].
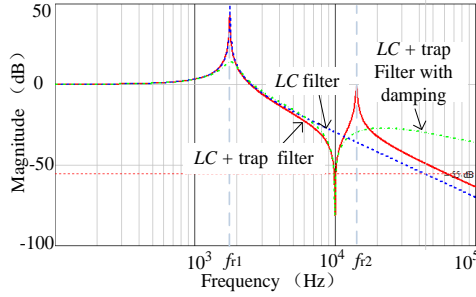
Figure 5.8: Bode plots of *LC* filter and *LC* + trap filter.

5.3 Characteristics of *LC* + trap filter for the current source rectifier

5.3.1 Resonances of *LC* + trap filter

The line current i_g is subjected to two disturbances: the supply voltage v_g and the rectifier input current i_w. Therefore, neglecting the influence of the grid impedance and the parasitic parameters, the open loop transfer function from the rectifier current i_w to the grid current i_g is expressed in (5.7) as:

$$G_{i_w \to i_g}(s) = \left. \frac{i_g(s)}{i_w(s)} \right|_{u_g(s)=0} = \frac{L_f C_f s^2 + 1}{L_s s \left(L_f C_f C_s s^3 + C_f s + C_s s \right) + L_f C_f s^2 + 1} \tag{5.7}$$

$$\omega_{r1} = \frac{1}{\sqrt{\left(L_s + L_f + L_g \right) \left(C_s + C_f \right)}} \tag{5.8}$$

$$\omega_{r2} = \sqrt{\frac{C_s + C_f}{L_f C_f C_s}} = \omega_{sw} \sqrt{1 + \frac{1}{\lambda}} \tag{5.9}$$

$$\omega_s = \frac{1}{f_{sw}} = \frac{1}{\sqrt{L_f C_f}} \tag{5.10}$$

Figure 5.8 shows the Bode plots of the *LC* filter and *LC* + trap filter. The *LC* + trap filter has a significant attenuation at the switching frequency but there is another resonance at a higher frequency caused by the *LC* and the capacitor. For the *LC* filter, $L_s = 1$ mH and $C_s = 8$ μF; For *LC* + trap filter, $L_s = 1$ mH, $C_s = 4$ μF, $L_f = 64$ μH and $C_f = 4$ μF. The two corresponding resonance frequencies are ω_{r1} and ω_{r2}, as shown in (5.8) and (5.9). λ is proportional relation between C_s and C_f, assuming $C_s = \lambda C_f$.
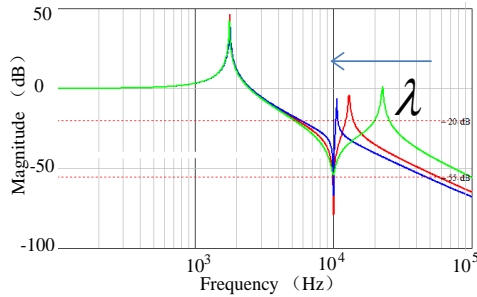
Figure 5.9: Bode plots of *LC* filter + trap with different λ .

ω_s is the sampling/switching frequency as shown in (5.10). The resonant frequency ω_{r1} of the *LC* + trap filter is similar to the one of *LC* filter under the condition of the same capacitance and inductance. The distribution of the C_s and C_f could be a problem. The resonances can be dampened by using passive or active damping methods. It can be seen from Figure 5.9, the second resonance frequency gets closer to the carrier frequency with λ increasing, but if it is too large, it could amplify the harmonics around the switching frequency and also bring a large L_f.

For the *LC* + trap filter, the resonance can be triggered by the side-band harmonics for CSCs. Damping methods are necessary to be investigated.

5.3.2 Damping circuit for the resonant peak in the filter

In order to avoid the amplification of the residual harmonics, a damping resistance may be needed to eliminate the oscillation at the *LC* resonant frequency and also to improve the stability. Figure 5.10 (a) shows the damping resistor placed in the branch of the filter capacitor C_s. Figure 5.10 (b) shows the damping resistor placed in the branch of the trap circuit.

It can be seen from Figure 5.11 (a) that there are two resonant peaks in the Bode plot of *LC* + trap filter and the corresponding frequencies are noted as f_1 and f_2. The resonant peaks may cause some system instability. The damping method can damp the resonance at both frequencies f_1 and f_2. The resistor can effectively damp the resonant peak and does not weaken the current harmonics attenuation at the selected frequencies, but it will bring higher losses. Figure 5.11 (b) shows the Bode plot of the transfer function i_g /i_w when R_d is in series with the *LC* trap circuit. The damping method has only the effect on the high frequency f_2 and could weaken the harmonics attenuation at the selected frequencies, but the power loss caused by the resistor is lower.
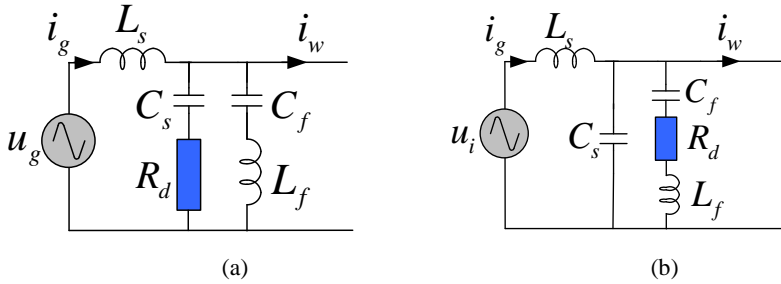
Figure 5.10: Passive damping circuits in the current source converters (a) R_d in series with the capacitor circuit, (b) R_d in series with trap circuit.
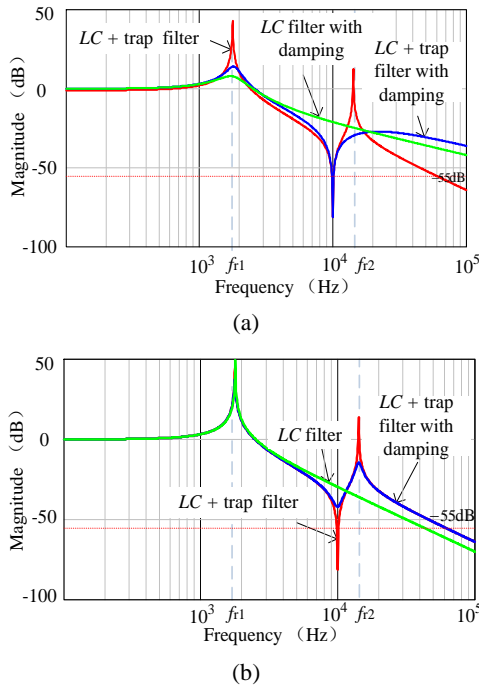
Figure 5.11: Bode plot of the transfer function i_g /i_w (a) when R_d is in series with capacitor circuit, (b) R_d is in series with LC trap circuit as shown in Figure 5.10.

5.3.3 Virtual impedance based control

The virtual impedance based control indicates the need of physical insight into different feedback or forward control methods, which has been increasingly used in active damping of the converter filter resonance, power flow control, harmonic compensation, and fault ride-through [130, 133 –135] operation to limit the current.
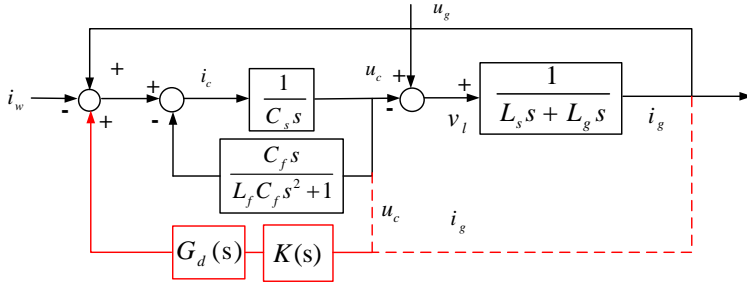
Figure 5.12: Control block diagram of active damping for *LC*+trap based current source rectifier.
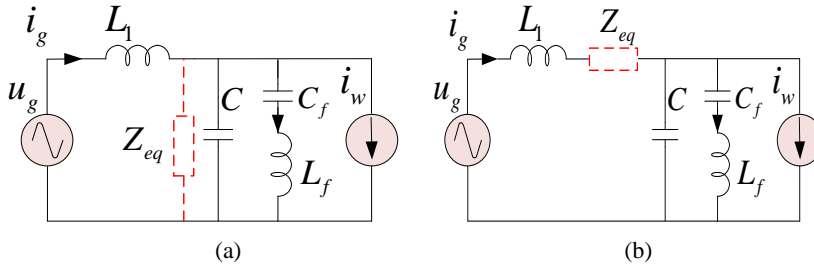
Figure 5.13: Equivalent virtual impedance circuits (a) the capacitor voltage is fedback (b) the grid current is fedback.

For *LC* + trap filter-based current source rectifiers, there are four feasible locations to add passive damping resistors, like resistors in parallel with the grid inductor L_s and resistors in series with capacitor C_s. Hence, active damping method is better to be implemented to damp the resonance for CSCs. Similar with *LLCL* filter-based voltage source converter, the capacitor voltage and grid current can be fedback to construct the vitual impedance, as shown in Figure 5.12. $G_d(s)$ is the delay. $K(s)$ is feedback equation. [126] illustrates and compares different variables feedback for *LC* filter-based current source rectifier.

Figure 5.13 shows the equilvalent virtual impedance circuit for active damping in Figure 5.12. $K(s)$ is expressed in this chapter as:

$$K(s) = \frac{ks}{s + \omega_h} \tag{5.11}$$

k is the proportional coefficient and ω_h is the cut off frequency. It can be regarded as a High Pass Filter (HPF) which should be applied to filter out the DC component. If the capacitor voltage feedback with high pass is used, it will mean a resistor across the capacitor.
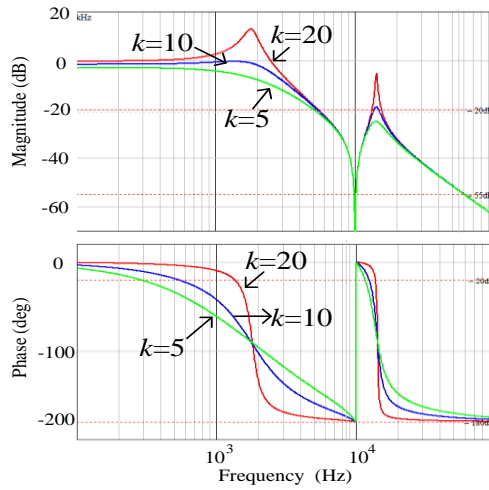
Figure 5.14: Bode plot of transfer function from current i_w to the grid current i_g with different k when $\omega_h = 2000$.
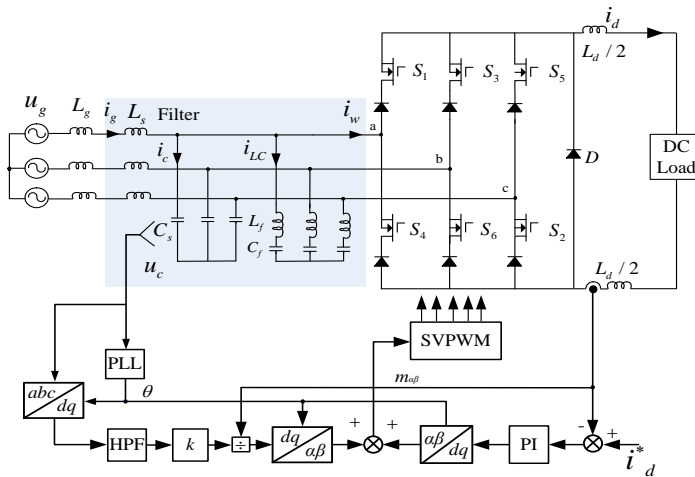
Figure 5.15: Virtual impedance control for a CSR system.

Figure 5.14 shows the transfer function from current i_w to the grid current i_g using active damping when $\omega_h = 2000$. It can be seen from the Bode plots that a lower k can exhibit a better damping effect.

Figure 5.15 shows the control block of a virtual impedance control for a CSR system. In the dc-link current control, a conventional PI algorithm is used. [124, 129] have shown that a more practical method of active damping for current source converter is to take effect at all frequencies except the fundamental frequency. The

damping current of fundamental components could occupy a large amount of the control variable, which may cause saturation of the modulation index and also interfere with the dc current control. The output of the DC side and AC side are controlled respectively and they are summed for space vector modulation. This HPF is applied in the stationary $\alpha\beta$-frame, which can also be used in the rotating dq-frame by using complex transfer functions.

5.4 *LC* + trap filter design for a three-phase current source converter

This section presents the design of the *LC* + trap filter for Space Vector Modulation. Due to Space Vector Modulation, the first group of dominant harmonic components in the current waveform appears to be around the equivalent carrier frequency $f_{sw} = 2\pi/\omega_s$. The other harmonic components occur at and around the multiples of the switching frequency. The base values of the total impedance, inductance, and capacitance are defined as:

$$Z_b = \frac{U_n^{\,2}}{P_{rate}}, \quad L_b = \frac{Z_b}{\omega_0}, \quad C_b = \frac{1}{\omega_0 Z_b} \tag{5.12}$$

where U_n is the line-to-line RMS voltage; ω_o is the grid frequency; P_{rate} is the active power absorbed by the converter in rated conditions. According to the IEEE 519 standard, the total THD in the grid current must be less than 5% of the fundamental current. The total equivalent line inductance on the CSR ac side is normally in the range of 0.1 to 0.15 per unit. However, the modulation techniques reported in the literature have been developed for higher switching frequencies (above 1 kHz) as they address low to medium power applications. One challenge in this design is that the rectifier system can have a large variation of total equivalent line inductance on the CSR ac side due to the variable inductance from the power system [136, 137].

5.4.1 Filter Design procedure

The *LC* filter should be designed to let the RMS of the ripple component of the grid current to be within a limit in order to maintain a particular THD. The first step in designing a filter is to identify the trap circuit position and the amplitude of the harmonics to be attenuated. The second step is to choose a suitable cross-over frequency for the filter. To achieve a desired attenuation of the dominant harmonic, which is at a multiple of the switching frequency. The second resonant peak should not be too close to the switching frequency to excite the bandside harmonics.

1) **Selection of the total capacitance**

Another consideration of the capacitor selection is the system power factor. It is necessary to limit the displacement angle. The value of capacitor is in the range of 0.3 to 0.7 per unit for the medium voltage high power current source drive with a resonance frequency of around 200 Hz [113]. The value can be reduced accordingly with the increase of the switching frequency. In this work, the switching frequency is chosen as 10 kHz and capacitor C_s is set to be 0.01 p.u. Therefore, it may increase the overall input power factor.

2) Design of capacitor C_s and C_f

The input filter capacitor voltage distortion is due to the current harmonics generated at the input side of the converter and flowing through the capacitor. The RMS value of the input voltage ripple can be expressed as:

$$\Delta v = \dfrac{\Delta i_w}{(\omega C_s + \dfrac{\omega C_f}{1 - L_f C_f \omega^2} - \dfrac{1}{\omega L_s})} = \dfrac{\Delta i_w}{\left[\omega C_f (\lambda + \dfrac{1}{1 - L_f C_f \omega^2}) - \dfrac{1}{\omega L_s} \right]} \qquad (5.13)$$

The value of λ should be large enough to keep the voltage ripple small and also cannot be too large to bring large inductance.

3) Design of Inductor L_s

The design for the filter inductor can be challenging due to the existence of the unknown grid impedance. It is important to avoid the situation that the resonant frequency is drifted to a place near the harmonic frequencies due to the variation of or the impact of the dc side circuit. The design of the filter components should follow the given maximum current harmonics limits defined by IEEE 519-1992.

To design the filter, the CSR as shown in Figure 5.2 has been modeled for the high-frequency component using the analytical estimation of the RMS current ripple. The RMS of the ripple current is obtained by subtracting the RMS of the fundamental component from the total input RMS current. THD in the grid current must be less than 5% of the fundamental current as shown in (5.14). Then the inductor L_s can be decided by this requirement.

$$\Delta i_g = \dfrac{\Delta i_w}{\left(\dfrac{1 - L_f C_f \omega^2}{1 - L_f C_f \omega^2 - L_s C_f \omega^2 - L_s C_s \left(1 - L_f C_f \omega^2 \right)} \right)} \qquad (5.14)$$

4) Design of resonant inductor L_f

P_{rate} , U_g , I_{dc}

Calculate i_g , modulation index m, base Impedance

Calculate the RMS of the converter current ripple i_w

Get λ , L_s , C_f by allowed voltage and current ripple

Get L_f and power factor

If power factor is ok — NO

YES

If voltage drop is ok — NO

YES

END
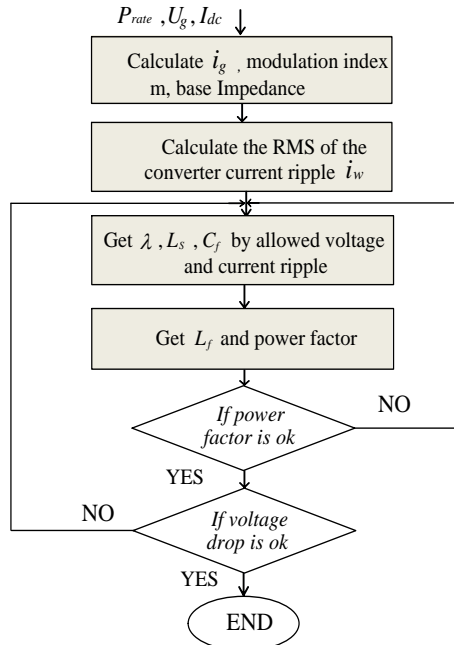
Figure 5.16: Flow-chart of the filter design in a current source converter.

In a CSR system, the capacitor C_s is required to provide a path for the current to assist the PWM commutation. At low frequencies, the filter is dominantly capacitive. The total capacitors include the capacitor C_s and the capacitor C_f in the trap circuit. The trap frequency is set at the switching frequency to calculate L_f. Figure 5.16 shows the flow-chart of the filter design.

5.4.2 Filter design example

Based on the design procedure proposed before, Table 5.1 shows the designed parameters. The rated power is 6 kW, switching frequency is 10 kHz and grid line to line voltage is 380 V/50 Hz. Z_b, C_b and L_b is 24 Ω, 132 μF and 76.6 mH respectively. Passive damping in series with C_s is used to damp the resonances and R_d is 5 Ω. The modulation index is 0.98. The peak value of the grid current is 12 A, which implies I_{dc} is 12A. According to (8), 10% voltage ripple and 5% THD of grid current is required to decide the capacitor C_s, C_f and L_s. The nominal operating conditions and other design specifications of the buck rectifier are given in Table 5.1.

5.5 Simulation Verifications

The simulation studies for the current source rectifier were carried out with the software of MATLAB/Simulink and done under ideal components without inductor

Table 5.1: Parameters for trap filter design in a current source converter.

Description	LC filter	LC + trap filter
Rated power P_{rate}	6 kW	6 kW
Rated grid voltage(line to line) U_g	380 V	380 V
Grid frequency	50 Hz	50 Hz
Input filter inductance L_s	0.08 p.u.	0.08 p.u.
Switching frequency f_{sw}	10 kHz	10 kHz
Trap circuit capacitor C_f	---	0.032 p.u.
Trap circuit inductor L_f	---	0.0008p.u.
Input filter capacitance C_s	0.08 p.u.	0.048 p.u.
DC link inductance L_d	0.06 p.u.	0.06 p.u.
DC load	1 p.u.	1 p.u.
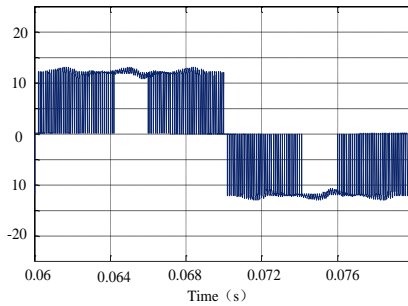
Figure 5.17: Waveforms of the rectifier side current i_w.

resistances. The aim of this section is to test the harmonics attenuation of LC + trap filter and compare with the traditional LC filter. The active damping effect is also investigated. The system parameters are given in Table 5.1. The total capacitance of the LC filter and LC + trap filter is same.

Figure 5.17 shows the simulated rectifier-side current of one phase of the CSR and Figure 5.18 shows the dc-link current with the designed LC + trap filter. The waveform of the rectifier side current is discontinuous PWM current with current ripple. The high frequency harmonics can be attenuated after the LC or LC + trap filter and the dc-link current has a maximum overshoot 20 A at beginning and reach the stable value 11.5 A after 0.1s.
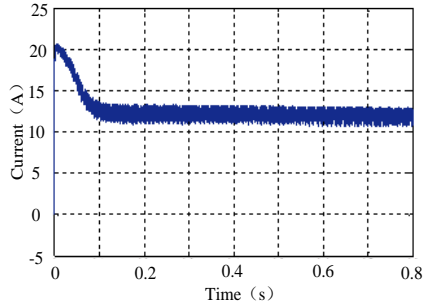
Figure 5.18: Waveform of dc-side current i_d.
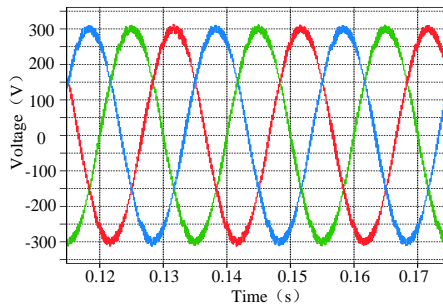
Figure 5.19: Phase voltage of the capacitor C_s for the CSR at $P = 6$ kW.
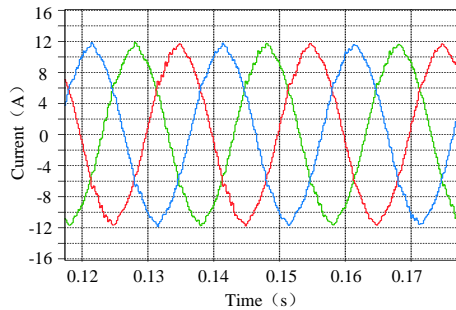
Figure 5.20: Waveforms of grid current i_g for the CSR at $P = 6$ kW.

Figure 5.19 shows the phase voltage of the capacitor C_s and Figure 5.20 shows the grid current waveforms with LC + trap filter at nominal load given in Table 5.1. The CSR system is stable with passive damping and the grid current is sinusoidal. The ripple of the voltage of the capacitor C_s is around 10%, which is the same as the designed value.

In respect to the waveform of the rectifier side current I_w, Figure 5.21 shows the simulated spectrum of the rectifier-side current i_w by using SVM modulation. There are significant harmonics at multiplies of the switching frequency. In order to

Fundamental (50Hz) = 12.24 , THD= 49.2%
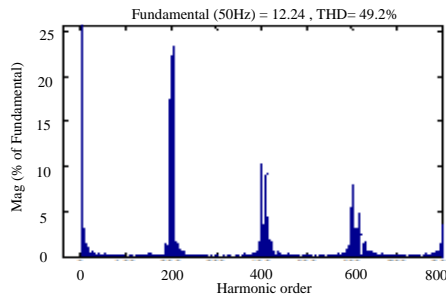
Figure 5.21: Simulated spectrum of rectifier-side current i_w of CSR at $P = 6$ kW.

Fundamental (50Hz) = 11.23 , THD= 3.99%

,

(a)

Fundamental (50Hz) = 11.27 , THD= 2.67%
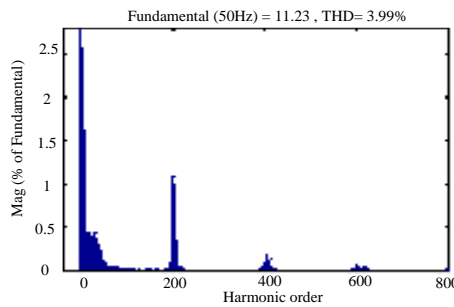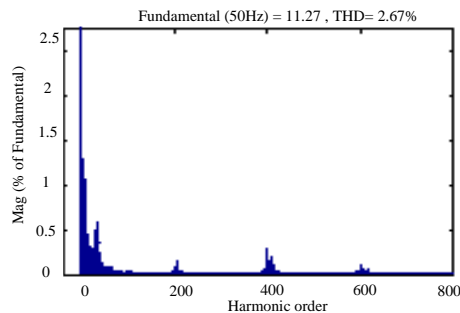
(b)

Figure 5.22: Grid current spectra of (a) *LC* filter,(b) *LC* + trap filter of CSR at $P = 6$ kW.

compare the filtering effect of different filters, Figure 5.22 shows the grid current spectra of the *LC* filter and *LC* + trap filter with the same capacitance and inductance, which are illustrated in Table 5.1. The grid current THD is 4.0% and 2.7% respectively to satisfy the IEEE standard of 5%. The dominant harmonics at the switching frequency can be significantly attenuated by using a trap circuit and the dominant harmonics appear around the double of the switching frequency for *LC* + trap filter.
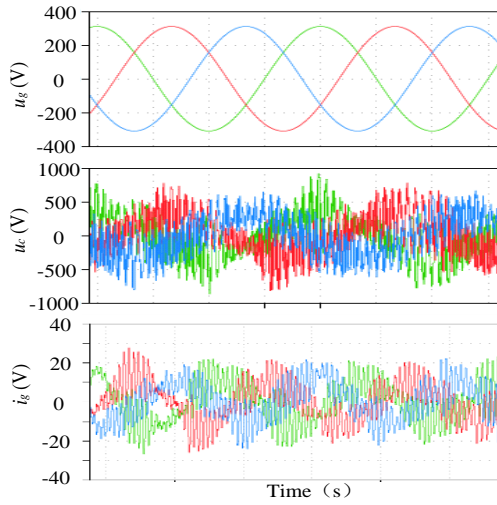
Figure 5.23: Simulation resuls without capacitor voltage feedback active damping at P = 6 kW.
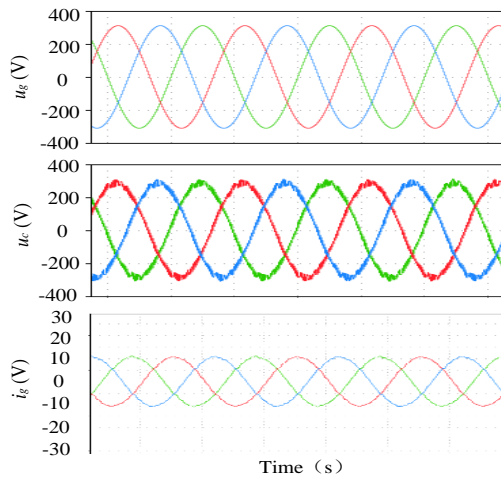
Figure 5.24: Simulation results with capacitor voltage feedback active damping (k = 5) at P = 6 kW.

Figure 5.23 shows the waveforms of the grid voltage u_g, the voltage cross the capacitor (C_s) u_c and the grid current i_g without capacitor voltage feedback active damping. The CSR system is not stable because of the triggered resonance of the LC filter and the system is undamped. If the capacitor voltage feedback active damping is enabled with k equal to 5 and ω_h is 2000, as shown in Figure 5.24, the CSR system is turned to be stable.

The ripple of the capacitor C_s is small, which can satisfy the commutation requirement. It should be noticed that the resonance around the swiching frequency can not be dampened by the active damping using the synchronous sampling method and a multisampling method should be applied for further investigations and improvements.

5.6 Summary

This chapter proposed a LC + trap filter and a design method of the filter used for current source converters. A proper selection of the filter parameters permits to reduce the current harmonics injected to the grid as well as to minimize the losses. The simulation results show the THD of the grid current can be improved by using a trap filter. Hence, the capacitor can be reduced to improve the power factor and reach the harmonics attenuation requirement according to the standards.

Chapter 6 Conclusions

The intent of this chapter is to summarize the work in the thesis and emphasize the main contributions. The main contributions of this project are concluded based on the achieved results and also potential applications. This chapter ends with several perspectives of the topic for future research.

6.1 Summary

To fulfill the research problems stated in Chapter 1, this thesis is devided into four parts. 1) Filter design and Stability Analysis for voltage source grid converters in distributed generation System. 2) Impedance-based active damping methods investigation for voltage source converters. 3) Design of *LLCL*-filtered grid converter with improved stability and robustness. 4) Trap filter application for current source converters.

Compared with the *L* filter, the *LCL* filter or *LC* filter has a higher attenuation of the switching frequency harmonics and allows typically a smaller total inductance. Similarly to the *LCL* filter, the purpose of using the *LLCL* filter resonance is to reduce the filter size and get a better harmonics attenuation. So this filter is studied both in the voltage source converter and current cource converter. A comparision is also given. At the same time, the high order filter resonance challenges the stability of a grid-connected system. At the beginning, the *LLCL* filter or high order filter design is proposed for the voltage source converter. Then the stability of the grid-connected converter with *LLCL* filter using different active damping methods is analyzed based on the virtual impedance method. The principle of virtual impedance of the *LC* circuit voltage and capacitor current with and without delay effect is presented by using the equivalent impedance functions and circuits. Inspired by trap filter idea, the application in current source converter is also investigated. The switching frequency can be increased when the power level of the current source converter is reduced.

In addition to the active damping method, the Proportional-Resonant controller using the Harmonic-Compensation (PR+HC) controller for voltage source converter is also used in this paper. The PR can provide larger gain at the fundamental frequency to eliminate the steady state error compared with PI regulator and the HC performs well to reject the grid harmonic distortion. For the harmonic compensation, the resonant controllers are only added for removing the 5th, 7th, 11th and 13th harmonics.

For current source rectifier, the PWM current waveform is discontinuous and has harmonic components at the multiple of the switching frequency. Due to the integration of power grid, the power quality is an important part. SVM is investigated at in a relative high switching frequency and filters are designed to reduce the harmonic distortion.

6.2 Main Contributions

This research work has focused on the design and control of the trap filter concept based filter for voltage source converter and current source converter. Although a number of research works have already been carried out in this area, most of them are focusing on the *LCL* filter or the *LC* filter. From the point of filter structure, this thesis investigates the relatively new type of filter and its characteristics. To the author's knowledge, the main contributions from this thesis are summarized as follows:

1. Switching harmonic attenuation of the filter will not be compromised because of the presence of the series *LC* trap tuned at the switching frequency. The developed criterion in the thesis may be used to improve the filter design procedure with both the grid and filter parameter variations taken into consideration. The theoretical expression of the equivalent phase voltage harmonics spectrum based on the Bessel functions is applied to determine the filter parameters in order to reduce the levels of the grid current harmonics. This thesis applies also the concept of passivity to an *LLCL*-filtered converter with the purpose to derive an optimal condition, which when met will guarantee system stability and robustness for parameter variations.
2. Based on the research results with the *LLCL* filter or trap filter for grid connected converter, it shows that the proposed higher order filter does not bring control and design problems for the system control.
3. Different active damping methods are analyzed based on their non-minimum-phase responses and their stability criteria. For the former, different circuit equivalences of the active dampers with and without considering delays are developed based on the impedance concept. The principle of the damping method is easier to follow. Normally, the capacitor current is used as a common signal dor dampers but the investigation has been expanded to include trap voltage feedback, which after the analysis is found to work properly with even a simple proportional damper.

4. Inspired by the trap idea of the voltage source converter the idea is also applied for the current source converter. The *LC* + trap circuit is proven efficient to get better harmonic attenuation and a higher power factor than *LC* filter.

5. Further, the current source converter is investigated at high switching frequency, which is different from the traditional low switching frequency used in high power application. The system can be modelled as a linear control system using the SVM method. Based on this, different damping methods for current source converter with trap filters are analyzed and they are demonstrated to be able to operate stably.

6.3 Future Work

Even though this research work has addressed several research subjects in the field of control of the trap filter based power converters, there are still a number of research area that could be interesting to be further explored. Based on the achievements and knowledge from this research work, several recommendations on the direction of the future work are given as follows:

1. Stability and robustness analysis of paralleled power converters with trap filter, where there are possible multi-resonances in the system. The investigation of the paralleled power converters should be carried out to see whether it has advantages or disadvanges as well as are they possible to solve.

2. The design method for the trap filter is a trade-off. Even though the value of the additional circuit is very small, but it is still interesting to investigate the power loss and the efficiency of the proposed trap filter compared to traditional *LCL*/*LC* filters.

3. It is also interesting to investigate the effect of trap filter with different modulation methods.

4. Also the filter components have not been physical optimized designed and only the shelf components have been applied.

5. The thesis does not explore all experimental cases which is a task for future work.

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Part II   Selected Publications

[J.1] M. Huang, X. Wang, P. C. Loh, F. Blaabjerg and W. Wu, "Stability analysis and active damping for *LLCL*-filter-based grid connected inverter," *IEEJ Trans. Industry App.*, vol. 4, no. 3, pp. 187-195, 2015.

[J.2] **M. Huang**, X. Wang, P. C. Loh, and F. Blaabjerg, "Active damping of *LLCL* filter resonance Based on *LC*-trap voltage or current feedback," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2337-2346, 2016.

[J.3] **M. Huang**, X. Wang, P. C. Loh, and F. Blaabjerg, "*LLCL*-filtered grid converter with improved stability and robustness," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3958-3967, 2016.

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