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Zhang, Chi; Coelho, Ernane A. A.; Guerrero, Josep M.; Quintero, Juan Carlos Vasquez

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Modular Online Uninterruptible Power System *Plug'n'Play* Control and Stability Analysis

Chi Zhang, *Student Member, IEEE*, Ernane A.A. Coelho, Josep M. Guerrero, *Fellow, IEEE*, Juan C. Vasquez, *Senior Member, IEEE*.

Abstract—in this paper, a *plug'n'play* control strategy proposed for modular online UPS system is presented, which allows to plug the UPS modules in or out randomly. This provides a lower difficulty for the maintenance of the whole system. A two level control scheme was proposed, including local controllers to achieve active and reactive power sharing and central controllers to maintain synchronization capability, which allows the online UPS modular system having faster dynamic performance according to the standard IEC 62040-3. A detailed small signal mathematical model was developed in order to analyze the proposed modular online UPS system. Experimental results and data are presented to validate the stability analysis and support the proposed *plug'n'play* control feasibility.

Index Terms—modular online UPS system, phase control, stability analysis.

NOMENCLATURE

k_{pv_sec}	Voltage proportional term in central controller
k_{iv_sec}	Voltage integer term in central controller
$k_{p\theta_sec}$	Phase proportional term in central controller
$k_{i\theta_sec}$	Phase integer term in central controller
ΔE_{mi}	RMS voltage of DC/AC #i
ΔE_{ri}	Amplitude reference of DC/AC #i
$\Delta \delta_{pi}$	Phase angle of DC/AC #i
$\Delta \delta_{ri}$	Phase reference of DC/AC #i
$\Delta \delta_{oi}$	Phase angle of output voltage of DC/AC #i
ΔQ_{avi}	Output reactive power of DC/AC #i
k_{ph}	Phase regulation coefficient based on reactive power
ΔE_{oi}	Output voltage of DC/AC #i
ω_{fm}	Cutoff frequency of equivalent low pass filter for RMS calculation
k_{pp}	PLL proportional term
k_{ip}	PLL integral term
ΔE_r	Matrix for amplitude reference
K_{pv}	Matrix for voltage proportional term in central controller
K_{iv}	Matrix for voltage integer term in central controller
ΔE_m	Matrix for RMS voltage
ΔE_o	Matrix for output voltage

$\Delta \delta_r$	Matrix for phase reference
$\Delta \delta_p$	Matrix for phase angle of DC/AC module
$K_{p\theta}$	Matrix for phase proportional term in central controller
$K_{i\theta}$	Matrix for phase integer term in central controller
K_{ph}	Matrix for phase regulation coefficient
K_{pp}	Matrix for PLL proportional term
K_{ip}	Matrix for PLL integral term
ΔQ_{av}	Matrix for output reactive power
ΔE_{δ_o}	Combined matrix of output voltage and phase
e_{odi}	d-axis component of output voltage of DC/AC #i
e_{oqi}	q-axis component of output voltage of DC/AC #i
E_{odq}	Matrix of output voltage dq component
e_{rdi}	d-axis component of reference voltage of DC/AC #i
e_{rqi}	q-axis component of reference voltage of DC/AC #i
ΔE_{δ_r}	Combined matrix of reference voltage and phase
E_{rdq}	Matrix of reference voltage dq component
I_n	n×n identity matrix
Z_{pi}	Line impedance for DC/AC #i
Z_L	Load impedance
Y_{pi}	Line admittances for DC/AC #i
Y_L	Line admittances
Y_o	Matrix for line and load impedance
i_{odq}	Matrix for dq component of output current
Z_{pi}	Line impedance for DC/AC #i
Δq_i	Reactive power oscillation of DC/AC #i
I_o	Matrix for dq component of output current
E_o	Matrix for dq component of output voltage
q_i	Reactive power after low pass filter of DC/AC #i
ω_f	Cutoff frequency of power low pass filter
Z_v	Matrix for virtual impedance
Z_{vr}	Matrix for virtual impedance in complex field

I. INTRODUCTION

NOWDAYS a large number of advanced electric equipment, such as medical equipment, communication facilities and data centers, are penetrating into our daily life [1]. Online UPS system is becoming an effective equipment to solve the concerns about the power quality and reliability [2], [3]. In [4] and [5], a kind of poor power factor UPS structure is proposed using rectifier and battery as the DC source of the UPS while a PFC is chosen to form the DC side in order to enhance UPS power factor performance in [6] and [7]. For the sake of smaller current and voltage stress and multi-output

C. Zhang, J. M. Guerrero, J. C. Vasquez are with Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark. (e-mail: zhc@et.aau.dk; joz@et.aau.dk; juq@et.aau.dk)

Ernane A.A. Coelho is with the Universidade Federal de Uberlândia, Uberlândia 38400-902, Brazil. (e-mail: ernane@ufu.br)

functionality, structures based on dual active bridge (DAB) converter are presented in [8] and [9]. Compared with the aforementioned structures, modular parallel online UPS systems are receiving more and more attention due to their high flexibility [10]. Due to the physical parameters differences that may cause high circulating currents among the paralleled DC/AC modules, parallel algorithms, like those proposed in [11]-[31], are becoming essential technology in the implementation of a modular online UPS system. Active and reactive power sharing, voltage amplitude, frequency and phase are common basic elements that most of parallel control algorithms are taken into consideration in modular UPS systems.

By considering the existence of intercommunications, parallel technology can be categorized into two main groups [11]. With these critical communications among the modules, active and reactive power are well controlled and equally shared among different modules. For instance, centralized control [12], master-slave control [13], [14] and average load sharing control [15] are three of the main techniques that rely on inter-communications. However, these critical intercommunications bring about some serious issues, such as reduced reliability, robustness and modularity.

As a consequence, parallel control based on droop methods have been proposed [16]-[23]. Basic type of droop control (mainly a *P-controller* for power regulation) is proposed in [16]-[20]. Hereby, it is assumed that the output impedance of the DC/AC in the UPS is mainly inductive. Thus, the active power of each DC/AC module is calculated in order to modify its own output voltage frequency, while reactive power is also required to regulate output voltage amplitude. Thus output voltage of different DC/AC modules is regulated to the same value, while contributing to both active power and reactive power sharing among them. In order to analyze droop controller impact on system performance, detailed mathematical models are established [20]. Moreover, by modifying the DC/AC output impedance, the control can be simplified and improved. So virtual impedance concept is introduced by [21]. Additionally, in [22], derivative component of the active and reactive power regulation is considered in order to enhance the parallel accuracy. Accurate small-signal analysis has been achieved on both stability impacts and controller parameters selection. However, droop-controlled UPS system output voltage frequency and amplitude are inherently load-dependent. Thus, serious frequency deviations may occur under heavy-load operation, being not acceptable for bypass operation in online UPS system. On the other hand, output voltage amplitude slightly changes according to different load currents. As a result, secondary controllers are proposed to compensate such a kind of voltage and frequency deviations [27].

Furthermore, in addition of the adjust of frequency, a phase loop can be included, which allows the increasing of the gain droops to get a faster response, but keeping the system damping level, that is, it is possible to accelerate the response without leading the system to a under-damped condition [24], [25]. Additionally, active power sharing among DC/AC modules

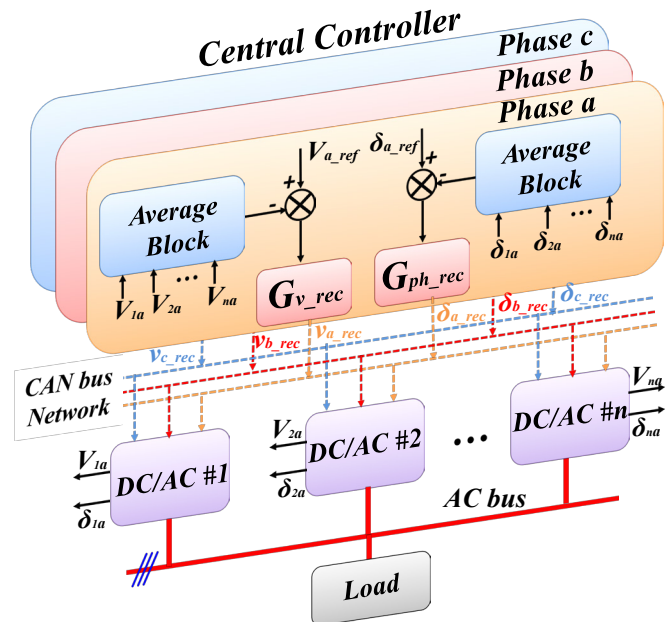


Fig. 1. Modular online UPS system structure.

should be also taken into consideration. Instead of using only active and reactive power as the feedback for power regulation, a power reference is inserted into the regulation loop in [28] to enhance a faster dynamic performance. Moreover, a cross combination of active and reactive power feedback is considered in [29]. In order to achieve a tight control on power, a PI or PD controller for power regulation is used in [30]. Virtual impedance, mentioned in [27], shows outstanding improvements on both power sharing and harmonic current sharing performance. Since in the proposed online UPS system, inductor current is measured to achieve inner current loop, a virtual impedance loop is inserted into the inner control loop to achieve both active power and harmonics sharing. Thus a voltage amplitude drop may occur due to the virtual impedance loop. Thus special efforts must be taken to compensate the output voltage phase shift and amplitude drop. As shown in Fig. 1, two conventional *PI* controllers, G_{v_rec} and G_{ph_rec} , are used to restore output voltage amplitude and to adjust the phase shift in order to keep the UPS system output voltage tightly synchronized with the utility grid voltage. In Fig. 1, different color lines in the CAN bus network denote different communication addresses for each phase. Each DC/AC module receives the amplitude and phase recover value through the CAN bus network. However, it can be seen that such kind of control architecture relies too much on the communication network. The central controller should be confirmed of the exact working numbers of the DC/AC modules in order to calculate the voltage amplitude and phase recovery reference. This will decrease the system reliability and increase the maintain cost of the system.

In order to achieve *plug'n'play* capability, an improved control architecture is proposed as shown in Fig. 2 by measuring voltage and frequency directly from the AC critical bus and removes the average blocks. Thus the central controller can operate at any time without knowing the exact numbers of

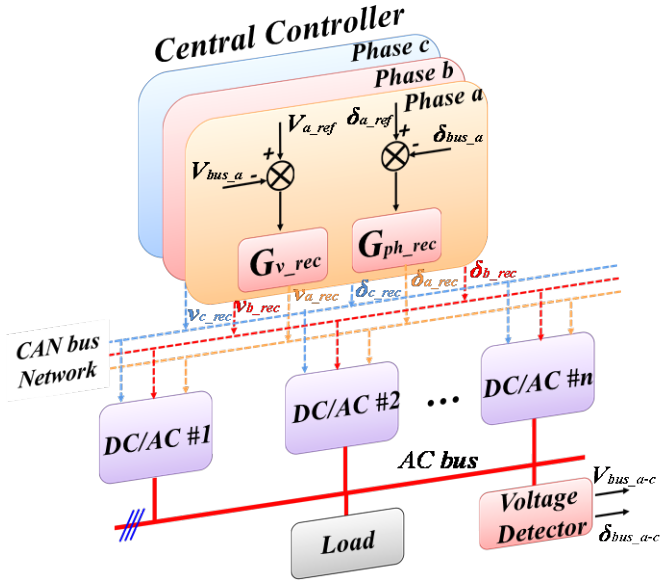


Fig. 2. Proposed Plug n' play control diagram.

DC/AC modules. Moreover, a small signal mathematical model is established to analyze critical parameters performance on the proposed online UPS system output voltage.

This paper is organized as follows. Section II depicts proposed *plug'n'play* control diagram. Section III shows the small signal modeling and the stability analysis with the experimental results is shown in Section IV. Section V presents the improved control experimental results. Finally, conclusions are given in Section VI.

II. PROPOSED CONTROL

The proposed *plug'n'play* control diagram is presented in Fig. 2. It can be observed that the central controller measures the AC bus voltage directly without using the average block $((V_{1a} + V_{2a} + \dots + V_{na})/n)$ used in Fig. 1. With the previous control, the exact number of the connected units must be refreshed in real-time to allow the correct calculation of the average value. For instance, if one DC/AC module plugs out and the n is kept the same, the output of average block will become smaller, which means that the feedback for the central controller will send an improper value for each unit in order to compensate the output voltage, which will affect the AC bus voltage controllability. Similarly, for phase regulation in the central controller, an improper average value calculation will imply a wrong phase compensation value, resulting in an abnormal system operation. In addition, average block depends too much on the communication network, which will decrease the system reliability.

Hereby two typical *PIs* are used to recover the voltage amplitude and phase,

$$G_{v_rec} = k_{pv_sec} + k_{iv_sec}/s \quad (1)$$

$$G_{ph_rec} = k_{p\theta_sec} + k_{i\theta_sec}/s \quad (2)$$

The inner loop for the DC/AC modules is considered in $\alpha\beta$ frame, which is shown in Fig. 3. References are modified in abc

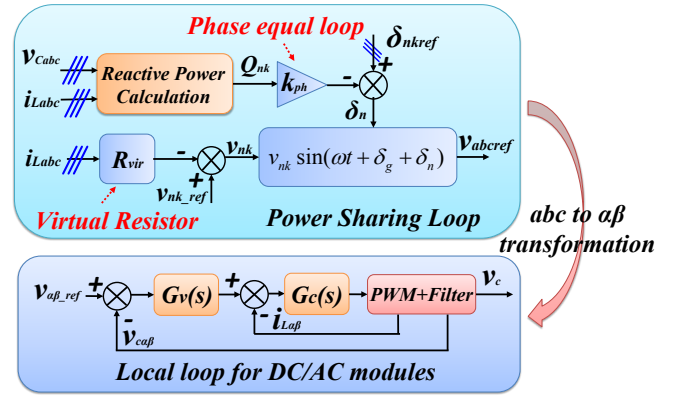
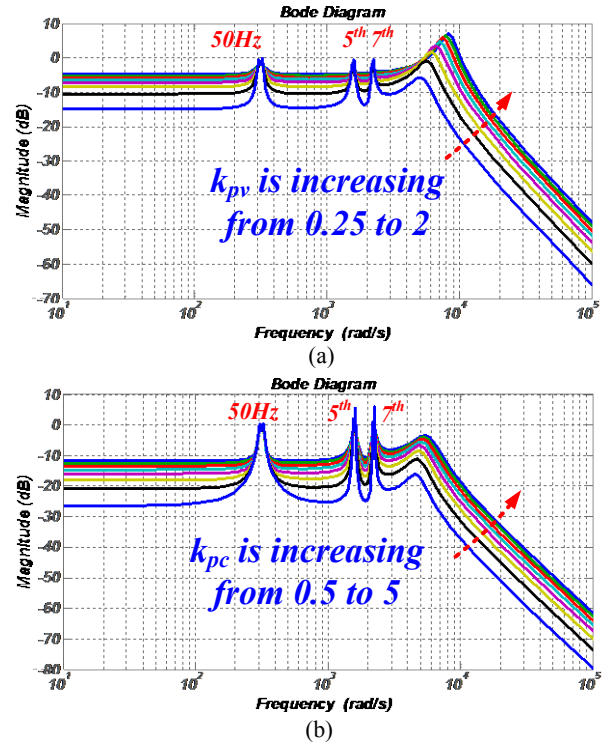


Fig. 3. DC/AC Module individual layer control loop diagram.

Fig. 4. Bode diagram of inner loop. (a) Bode diagram with variable k_{pv} . (b) Bode diagram with variable k_{pc} .

frame and then transferred to $\alpha\beta$ frame as shown in Fig. 3. Two conventional *PR* controllers are used for the voltage and current loop,

$$G_v(s) = k_{pv} + \frac{k_{rv}s}{s^2 + \omega_o^2} + \sum_{h=5,7} \frac{k_{hrv}s}{s^2 + (\omega_o h)^2} \quad (3)$$

$$G_c(s) = k_{pc} + \frac{k_{rc}s}{s^2 + \omega_o^2} + \sum_{h=5,7} \frac{k_{hrc}s}{s^2 + (\omega_o h)^2} \quad (4)$$

being k_{pv} , k_{rv} , ω_o , k_{hrv} , h , k_{pc} , k_{rc} and k_{hrc} as voltage proportional term, fundamental frequency voltage resonant term, fundamental frequency, the h^{th} harmonic voltage compensation term, harmonic order, current proportional term, fundamental frequency current resonant term and the h^{th} harmonic current compensation term respectively. The local controller has the ability of compensating harmonics due to nonlinear load, whose behavior in closed loop is shown in Fig. 4. Hereby the local controller bandwidth is designed to be around 1.5kHz

since the switching frequency is 10kHz. And the parameters range is chosen to be around the parameters shown in TABLE I- Control Parameters (DC/AC modules). At the same time, a bypass behavior is achieved at both 50Hz and harmonic frequency point (250Hz, 350Hz). Also 0dB is achieved at these frequency points.

As mentioned in [22], when the DC/AC output impedance is designed to be mainly resistance, the active power and reactive power that DC/AC module injects into the AC bus can be regulated by output voltage amplitude and phase angle respectively. Thus a virtual impedance loop and a Q - ϕ droop are embedded into the control scheme to realize parallel operation and power sharing as shown in Fig. 3,

$$\delta_{nk} = \delta_{nkref} - k_{ph} Q_{nk} \quad (5)$$

$$v_{nk} = v_{nkref} - i_{Labc} R_{vir} \quad (6)$$

where n is the number of DC/AC module (1, 2, 3...N), k is the phase order (a, b, c), V_{nkref} the nominal voltage reference, R_{vir} the virtual resistor, δ_{nkref} the nominal phase reference, k_{ph} the phase regulating coefficients, and Q_{nk} the reactive power of each phase of each DC/AC module. Hereby, instead of modifying frequency, the proposed control regulates the phase angle according to output power. Thus a better frequency behavior is achieved.

III. SMALL SIGNAL MODEL AND STABILITY ANALYSIS

This Section presents the small-signal model derivation process for the proposed online UPS system. Before modeling the system, some assumptions must be kept in mind, which are described as follows:

- 1) Consuming that the inner loop for DC/AC modules is well tuned and working well. Also the proposed controller presented in Fig. 5 presents a lower bandwidth compared to the PR internal controllers since they include low pass filters in the phase and voltage loops, as well, the PLL naturally presents a lower bandwidth compared to its central frequency. Thus the DC/AC modules can be considered as an ideal voltage source.
- 2) Since local controllers are carried out in the stationary-reference-frame ($\alpha\beta$), mathematical model is fully considered in $\alpha\beta$ frame as well.

A. Small Signal Model for the Proposed Controller

In Fig. 5, the small signal model for the proposed controller is presented, where the LC filters of the three DC/ACs are connected to the same AC critical bus.

Thus,

$$\Delta E_o = \Delta E_{o1} = \Delta E_{o2} = \Delta E_{o3} = (\Delta E_{o1} + \Delta E_{o2} + \Delta E_{o3})/3 \quad (7)$$

$$\Delta \delta_o = \Delta \delta_{o1} = \Delta \delta_{o2} = \Delta \delta_{o3} = (\Delta \delta_{o1} + \Delta \delta_{o2} + \Delta \delta_{o3})/3 \quad (8)$$

being ΔE_o , ΔE_{o1} , ΔE_{o2} and ΔE_{o3} the AC critical bus voltage, DC/AC #1 output voltage, DC/AC #2 output voltage and DC/AC #3 output voltage respectively and $\Delta \delta_o$, $\Delta \delta_{o1}$, $\Delta \delta_{o2}$ and $\Delta \delta_{o3}$ the AC critical bus phase, DC/AC #1 phase, DC/AC #2 phase and DC/AC #3 phase.

As a result, the ΔE_{m1} can be derived,

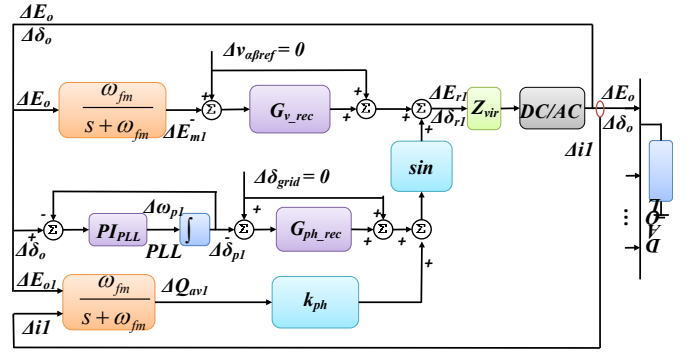


Fig. 5. Block diagram of the small-signal model for the proposed control.

$$\begin{aligned} \Delta E_{m1} &= \frac{\omega_{fm}}{s + \omega_{fm}} \Delta E_o = \frac{1}{3} \frac{\omega_{fm}}{s + \omega_{fm}} (\Delta E_{o1} + \Delta E_{o2} + \Delta E_{o3}) \\ &= \frac{1}{3} (\Delta E_{m1} + \Delta E_{m2} + \Delta E_{m3}) \end{aligned} \quad (9)$$

being ΔE_{m1} the RMS voltage value of DC/AC #1. Similar equation can be obtained in DC/AC #2 and #3.

Since voltage restoration is carried out in phase and amplitude respectively, the small-signal model can be derived by considering the two main loops, namely RMS voltage restoration loop and phase regulation loops,

$$\begin{bmatrix} \dot{\Delta E}_{r1} \\ \dot{\Delta E}_{r2} \\ \dot{\Delta E}_{r3} \end{bmatrix} = -\frac{1}{3} \begin{bmatrix} k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \\ k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \\ k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \end{bmatrix} \begin{bmatrix} \dot{\Delta E}_{m1} \\ \dot{\Delta E}_{m2} \\ \dot{\Delta E}_{m3} \end{bmatrix} \quad (10)$$

$$-\frac{1}{3} \begin{bmatrix} k_{iv_sec} & k_{iv_sec} & k_{iv_sec} \\ k_{iv_sec} & k_{iv_sec} & k_{iv_sec} \\ k_{iv_sec} & k_{iv_sec} & k_{iv_sec} \end{bmatrix} \begin{bmatrix} \Delta E_{m1} \\ \Delta E_{m2} \\ \Delta E_{m3} \end{bmatrix}$$

$$\begin{bmatrix} \dot{\Delta \delta}_{r1} \\ \dot{\Delta \delta}_{r2} \\ \dot{\Delta \delta}_{r3} \end{bmatrix} = -\frac{1}{3} \begin{bmatrix} k_{p\theta_sec} & k_{p\theta_sec} & k_{p\theta_sec} \\ k_{p\theta_sec} & k_{p\theta_sec} & k_{p\theta_sec} \\ k_{p\theta_sec} & k_{p\theta_sec} & k_{p\theta_sec} \end{bmatrix} \begin{bmatrix} \dot{\Delta \delta}_{p1} \\ \dot{\Delta \delta}_{p2} \\ \dot{\Delta \delta}_{p3} \end{bmatrix}$$

$$-\frac{1}{3} \begin{bmatrix} k_{i\theta_sec} & k_{i\theta_sec} & k_{i\theta_sec} \\ k_{i\theta_sec} & k_{i\theta_sec} & k_{i\theta_sec} \\ k_{i\theta_sec} & k_{i\theta_sec} & k_{i\theta_sec} \end{bmatrix} \begin{bmatrix} \Delta \delta_{p1} \\ \Delta \delta_{p2} \\ \Delta \delta_{p3} \end{bmatrix} \quad (11)$$

$$+ \begin{bmatrix} k_{ph} & 0 & 0 \\ 0 & k_{ph} & 0 \\ 0 & 0 & k_{ph} \end{bmatrix} \begin{bmatrix} \dot{\Delta Q}_{av1} \\ \dot{\Delta Q}_{av2} \\ \dot{\Delta Q}_{av3} \end{bmatrix}$$

RMS block is considered as a low pass filter, as shown in Fig. 5. Thus, output voltage dynamics can be expressed as,

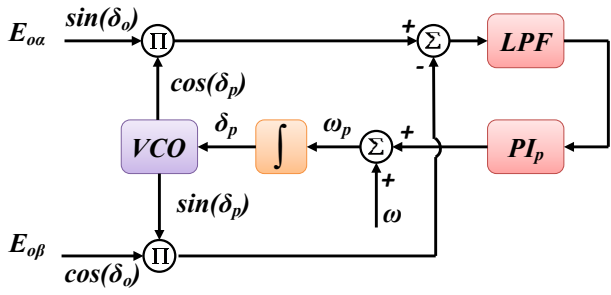


Fig. 6. PLL scheme diagram.

$$\begin{bmatrix} \dot{\Delta E}_{m1} \\ \dot{\Delta E}_{m2} \\ \dot{\Delta E}_{m3} \end{bmatrix} = - \begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix} \begin{bmatrix} \Delta E_{m1} \\ \Delta E_{m2} \\ \Delta E_{m3} \end{bmatrix} + \begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix} \begin{bmatrix} \Delta E_{o1} \\ \Delta E_{o2} \\ \Delta E_{o3} \end{bmatrix} \quad (12)$$

being ΔE_{oi} the output voltage of DC/AC #i and ω_{fm} the cutoff frequency of low pass filter. Thus (10) can be rewritten as,

$$\begin{bmatrix} \dot{\Delta E}_{r1} \\ \dot{\Delta E}_{r2} \\ \dot{\Delta E}_{r3} \end{bmatrix} = X_1 \begin{bmatrix} \Delta E_{m1} \\ \Delta E_{m2} \\ \Delta E_{m3} \end{bmatrix} - X_2 \begin{bmatrix} \Delta E_{o1} \\ \Delta E_{o2} \\ \Delta E_{o3} \end{bmatrix} \quad (13)$$

where,

$$X_1 = \begin{pmatrix} \frac{1}{3} \begin{bmatrix} k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \\ k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \\ k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \end{bmatrix} \begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix} \\ -\frac{1}{3} \begin{bmatrix} k_{iv_sec} & k_{iv_sec} & k_{iv_sec} \\ k_{iv_sec} & k_{iv_sec} & k_{iv_sec} \\ k_{iv_sec} & k_{iv_sec} & k_{iv_sec} \end{bmatrix} \end{pmatrix}$$

$$X_2 = \begin{bmatrix} k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \\ k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \\ k_{pv_sec} & k_{pv_sec} & k_{pv_sec} \end{bmatrix} \begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix}$$

According to the PLL scheme shown in Fig. 6, phase errors are derived as,

$$error_\alpha = \sin(\delta_o) \cos(\delta_p) = \frac{1}{2} (\sin(\delta_o + \delta_p) + \sin(\delta_o - \delta_p)) \quad (14)$$

$$error_\beta = \cos(\delta_o) \sin(\delta_p) = \frac{1}{2} (\sin(\delta_o + \delta_p) - \sin(\delta_o - \delta_p)) \quad (15)$$

So that the output of the detector is defined as,

$$error = error_\alpha - error_\beta \approx \delta_o - \delta_p \quad (16)$$

From the perspective of small-signal analysis, the output of the phase detector is considered as $(\Delta\delta_o - \Delta\delta_p)$. Consequently, based on (8), phase-signal equations are derived as,

$$\begin{bmatrix} \dot{\Delta\omega}_{p1} \\ \dot{\Delta\omega}_{p2} \\ \dot{\Delta\omega}_{p3} \end{bmatrix} = X_3 \begin{bmatrix} \dot{\Delta\delta}_{o1} \\ \dot{\Delta\delta}_{o2} \\ \dot{\Delta\delta}_{o3} \end{bmatrix} + X_4 \begin{bmatrix} \Delta\delta_{o1} \\ \Delta\delta_{o2} \\ \Delta\delta_{o3} \end{bmatrix} \quad (17)$$

$$- X_5 \begin{bmatrix} \Delta\omega_{p1} \\ \Delta\omega_{p2} \\ \Delta\omega_{p3} \end{bmatrix} - X_6 \begin{bmatrix} \Delta\delta_{p1} \\ \Delta\delta_{p2} \\ \Delta\delta_{p3} \end{bmatrix}$$

where,

$$X_3 = \begin{bmatrix} k_{pp} & 0 & 0 \\ 0 & k_{pp} & 0 \\ 0 & 0 & k_{pp} \end{bmatrix}, \quad X_4 = \begin{bmatrix} k_{ip} & 0 & 0 \\ 0 & k_{ip} & 0 \\ 0 & 0 & k_{ip} \end{bmatrix},$$

$$X_5 = \begin{bmatrix} k_{pp} & 0 & 0 \\ 0 & k_{pp} & 0 \\ 0 & 0 & k_{pp} \end{bmatrix}, \quad X_6 = \begin{bmatrix} k_{ip} & 0 & 0 \\ 0 & k_{ip} & 0 \\ 0 & 0 & k_{ip} \end{bmatrix}$$

being k_{pp} the proportional term and k_{ip} the integral term in PLL scheme, respectively. As a result, a series of differential equation system is derived in a symbolic way as shown in (18)-(21) by combining (11), (13) and (17) it yields,

$$\dot{\Delta E}_r = (K_{pv} \omega_{fm} - K_{iv}) \Delta E_m - K_{pv} \omega_{fm} \Delta E_o \quad (18)$$

$$\dot{\Delta\delta}_r = -K_{p\theta} \dot{\Delta\delta}_p - K_{i\theta} \Delta\delta_p + K_{ph} \dot{\Delta Q}_{av} \quad (19)$$

$$\dot{\Delta\omega}_p = K_{pp} \dot{\Delta\delta}_o + K_{ip} \Delta\delta_o - K_{pp} \Delta\omega_p - K_{ip} \Delta\delta_p \quad (20)$$

$$\dot{\Delta\delta}_p = \Delta\omega_p \quad (21)$$

Considering the vectors ΔX_r and ΔX_o represented by,

$$\Delta X_r = [\Delta E_{ri} \quad \Delta\delta_{ri} \quad \Delta\omega_{pi} \quad \Delta\delta_{pi}]^T \quad (22)$$

$$\Delta X_o = [\Delta E_{oi} \quad \Delta\delta_{oi} \quad \Delta\omega_{pi} \quad \Delta\delta_{pi}]^T \quad (23)$$

The differential equations (18)-(21) can be rewritten as,

$$\dot{\Delta X}_r = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & K_{pp} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \dot{\Delta X}_o + X_7 \Delta X_o$$

$$+ \begin{pmatrix} \begin{bmatrix} K_{pv} \omega_{fm} \\ 0 \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} K_{iv} \\ 0 \\ 0 \\ 0 \end{bmatrix} \end{pmatrix} \Delta E_m + \begin{bmatrix} 0 \\ K_{ph} \\ 0 \\ 0 \end{bmatrix} \dot{\Delta Q}_{av} \quad (24)$$

where

$$X_7 = \begin{bmatrix} -K_{pv}\omega_{jm} & 0 & 0 & 0 \\ 0 & 0 & -K_{p\theta} & -K_{i\theta} \\ 0 & K_{ip} & -K_{pp} & -K_{ip} \\ 0 & 0 & I_3 & 0 \end{bmatrix}$$

Here ΔX_r and ΔX_o are two vectors with 12 variables since ΔE_{ri} , $\Delta \delta_{ri}$, $\Delta \omega_{pi}$, $\Delta \delta_{pi}$, ΔE_{oi} and $\Delta \delta_{oi}$ represent 1x3 matrixes. Hence (24) can be rewritten as,

$$\dot{\Delta X}_r = M_1 \dot{\Delta X}_o + M_2 \Delta X_o + M_3 \Delta E_m + M_4 \dot{\Delta Q}_{av} \quad (25)$$

As for the DC/AC inner control loops, only phase and amplitude of output voltage should be taken into consideration. However, the reactive power is calculated in a Cartesian coordinate system. So that output voltage of DC/AC is represented,

$$\vec{E}_{oi} = e_{odi} + je_{oqi} \quad (26)$$

where, $e_{odi} = E_{oi} \cos \delta_{oi}$, $e_{oqi} = E_{oi} \sin \delta_{oi}$,

$$\delta_{oi} = \arctan(e_{oqi}/e_{odi}) \quad (27)$$

Linearizing (27) at the equilibrium point,

$$\begin{aligned} \Delta \delta_{oi} &= \frac{\partial \delta_{oi}}{\partial e_{odi}} \Delta e_{odi} + \frac{\partial \delta_{oi}}{\partial e_{oqi}} \Delta e_{oqi} \\ &= m_{odi} \Delta e_{odi} + m_{oqi} \Delta e_{oqi} \end{aligned} \quad (28)$$

where, $m_{odi} = -e_{oqi}/(e_{odi}^2 + e_{oqi}^2)$, $m_{oqi} = e_{odi}/(e_{odi}^2 + e_{oqi}^2)$

The amplitude of the output voltage is represented as,

$$E_{oi} = |\vec{E}_{oi}| = \sqrt{e_{odi}^2 + e_{oqi}^2} \quad (29)$$

Its linearization form around the equilibrium point is derived as,

$$\Delta E_{oi} = n_{odi} \Delta e_{odi} + n_{oqi} \Delta e_{oqi} \quad (30)$$

where $n_{odi} = e_{odi}/\sqrt{e_{odi}^2 + e_{oqi}^2}$, $n_{oqi} = e_{oqi}/\sqrt{e_{odi}^2 + e_{oqi}^2}$

Thus the vector \vec{E}_{oi} can be derived as,

$$\begin{bmatrix} \Delta E_{o1} \\ \Delta E_{o2} \\ \Delta E_{o3} \\ \Delta \delta_{o1} \\ \Delta \delta_{o2} \\ \Delta \delta_{o3} \end{bmatrix} = \begin{bmatrix} n_{od1} & n_{oq1} & 0 & 0 & 0 & 0 \\ 0 & 0 & n_{od2} & n_{oq2} & 0 & 0 \\ 0 & 0 & 0 & 0 & n_{od3} & n_{oq3} \\ m_{od1} & m_{oq1} & 0 & 0 & 0 & 0 \\ 0 & 0 & m_{od2} & m_{oq2} & 0 & 0 \\ 0 & 0 & 0 & 0 & m_{od3} & m_{oq3} \end{bmatrix} \begin{bmatrix} e_{od1} \\ e_{oq1} \\ e_{od2} \\ e_{oq2} \\ e_{od3} \\ e_{oq3} \end{bmatrix} \quad (31)$$

Rewriting (31) in symbolic form,

$$\Delta E \delta_o = T_o E_{odq} \quad (32)$$

Thus the vector ΔX_o (23) can be converted to its vertical coordinate form ΔX_{odq} as follows,

$$\Delta X_o = \begin{bmatrix} T_o & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{odq} = T_{odq} \Delta X_{odq} \quad (33)$$

and ΔX_{odq} is,

$$\Delta X_{odq} = \begin{bmatrix} \Delta e_{odq1} & \Delta e_{odq2} & \Delta e_{odq3} & \Delta \omega_{pi} & \Delta \delta_{pi} \end{bmatrix}^T \quad (34)$$

Furthermore, the same transformation process can be applied to the vector E_{ri} ,

$$\Delta \delta_{ri} = m_{rdi} \Delta e_{rdi} + m_{rqi} \Delta e_{rqi} \quad (35)$$

$$\Delta E_{ri} = n_{rdi} \Delta e_{rdi} + n_{rqi} \Delta e_{rqi} \quad (36)$$

where $m_{rdi} = -e_{rqi}/(e_{rdi}^2 + e_{rqi}^2)$, $m_{rqi} = e_{rdi}/(e_{rdi}^2 + e_{rqi}^2)$,

$$n_{rdi} = e_{rdi}/\sqrt{e_{odi}^2 + e_{oqi}^2}, \quad n_{rqi} = e_{rqi}/\sqrt{e_{odi}^2 + e_{oqi}^2}$$

Thus, it yields to,

$$\begin{bmatrix} \Delta E_{r1} \\ \Delta E_{r2} \\ \Delta E_{r3} \\ \Delta \delta_{r1} \\ \Delta \delta_{r2} \\ \Delta \delta_{r3} \end{bmatrix} = \begin{bmatrix} n_{rd1} & n_{rq1} & 0 & 0 & 0 & 0 \\ 0 & 0 & n_{rd2} & n_{rq2} & 0 & 0 \\ 0 & 0 & 0 & 0 & n_{rd3} & n_{rq3} \\ m_{rd1} & m_{rq1} & 0 & 0 & 0 & 0 \\ 0 & 0 & m_{rd2} & m_{rq2} & 0 & 0 \\ 0 & 0 & 0 & 0 & m_{rd3} & m_{rq3} \end{bmatrix} \begin{bmatrix} e_{rd1} \\ e_{rq1} \\ e_{rd2} \\ e_{rq2} \\ e_{rd3} \\ e_{rq3} \end{bmatrix} \quad (37)$$

Symbolically, (37) is rewritten as follows,

$$\Delta E \delta_r = T_r E_{rdq} \quad (38)$$

and the vector ΔX_r is derived as,

$$\Delta X_r = \begin{bmatrix} T_r & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{rdq} = T_{rdq} \Delta X_{rdq} \quad (39)$$

where

$$\Delta X_{rdq} = \begin{bmatrix} \Delta e_{rdq1} & \Delta e_{rdq2} & \Delta e_{rdq3} & \Delta \omega_{pi} & \Delta \delta_{pi} \end{bmatrix}^T \quad (40)$$

Substituting (33) and (39) in (25), it yields to,

$$\begin{aligned} T_{rdq} \Delta \dot{X}_{rdq} &= M_1 T_{odq} \dot{\Delta X}_{odq} + M_2 T_{odq} \Delta X_{odq} \\ &+ M_3 \Delta E_m + M_4 \dot{\Delta Q}_{av} \end{aligned} \quad (41)$$

which describes the small signal behavior of the controller presented in Fig. 5 around a certain equilibrium point by considering ΔE_m and ΔQ_{av} as the input variables.

B. Small Signal Model for the Whole System

The load impedance and line impedances of the system can be defined respectively as,

$$Z_{pi} = R_{pi} + jX_{pi} \quad (42)$$

$$Z_L = R_L + jX_L \quad (43)$$

which admittances are shown as follows,

$$Y_{pi} = 1/Z_{pi} \quad (44)$$

$$Y_L = 1/Z_L \quad (45)$$

Consequently, the output currents can be derived as,

$$\begin{bmatrix} i_{od1} \\ i_{oq1} \\ i_{od2} \\ i_{oq2} \\ i_{od3} \\ i_{oq3} \end{bmatrix} = \begin{bmatrix} G_{11} & -B_{11} & G_{12} & -B_{12} & G_{13} & -B_{13} \\ B_{11} & G_{11} & B_{12} & G_{12} & B_{13} & G_{13} \\ G_{21} & -B_{21} & G_{22} & -B_{22} & G_{23} & -B_{23} \\ B_{21} & G_{21} & B_{22} & G_{22} & B_{23} & G_{23} \\ G_{31} & -B_{31} & G_{32} & -B_{32} & G_{33} & -B_{33} \\ B_{31} & G_{31} & B_{32} & G_{32} & B_{33} & G_{33} \end{bmatrix} \begin{bmatrix} e_{od1} \\ e_{oq1} \\ e_{od2} \\ e_{oq2} \\ e_{od3} \\ e_{oq3} \end{bmatrix} \quad (46)$$

where

$$Y_{cij} = G_{ij} + jB_{ij} \quad (47)$$

Thus (46) can be expressed in symbolic form as,

$$i_{odq} = Y_o e_{odq} \quad (48)$$

and by linearizing (48), it yields,

$$\Delta i_{odq} = Y_o e_{odq} \quad (49)$$

Since reactive power is obtained through an orthogonal system as,

$$q_i = e_{odi} i_{oqi} - e_{oqi} i_{odi} \quad (50)$$

Then, the small signal form of the reactive power is presented as,

$$\begin{bmatrix} \Delta q_1 \\ \Delta q_2 \\ \Delta q_3 \end{bmatrix} = I_o \begin{bmatrix} \Delta e_{od1} \\ \Delta e_{oq1} \\ \Delta e_{od2} \\ \Delta e_{oq2} \\ \Delta e_{od3} \\ \Delta e_{oq3} \end{bmatrix} + E_o \begin{bmatrix} \Delta i_{od1} \\ \Delta i_{oq1} \\ \Delta i_{od2} \\ \Delta i_{oq2} \\ \Delta i_{od3} \\ \Delta i_{oq3} \end{bmatrix} \quad (51)$$

where

$$I_o = \begin{bmatrix} i_{oq1} & -i_{od1} & 0 & 0 & 0 & 0 \\ 0 & 0 & i_{oq2} & -i_{od2} & 0 & 0 \\ 0 & 0 & 0 & 0 & i_{oq3} & -i_{od3} \end{bmatrix},$$

$$E_o = \begin{bmatrix} -e_{oq1} & e_{od1} & 0 & 0 & 0 & 0 \\ 0 & 0 & -e_{oq2} & e_{od2} & 0 & 0 \\ 0 & 0 & 0 & 0 & -e_{oq3} & e_{od3} \end{bmatrix}.$$

Thus the symbolic form for (50) is derived as,

$$\Delta q = I_o \Delta e_{odq} + E_o \Delta i_{odq} \quad (52)$$

By substituting (49) into (52), it yields,

$$\Delta q = (I_o + E_o Y_o) \Delta e_{odq} \quad (53)$$

Considering the first order low pass filter used to calculate the reactive power, it can be obtained,

$$Q_{avi} = \frac{\omega_f}{s + \omega_f} q_i \quad (54)$$

and the linearization form of the filter is obtained as follows,

$$\begin{bmatrix} \Delta \dot{Q}_{av1} \\ \Delta \dot{Q}_{av2} \\ \Delta \dot{Q}_{av3} \end{bmatrix} = - \begin{bmatrix} \omega_f & 0 & 0 \\ 0 & \omega_f & 0 \\ 0 & 0 & \omega_f \end{bmatrix} \begin{bmatrix} \Delta Q_{av1} \\ \Delta Q_{av2} \\ \Delta Q_{av3} \end{bmatrix} + \begin{bmatrix} \omega_f & 0 & 0 \\ 0 & \omega_f & 0 \\ 0 & 0 & \omega_f \end{bmatrix} \begin{bmatrix} \Delta q_1 \\ \Delta q_2 \\ \Delta q_3 \end{bmatrix} \quad (55)$$

By combining (53), its symbolic form is,

$$\Delta \dot{Q}_{av} = -\omega_f \Delta Q_{av} + \omega_f (I_o + E_o Y_o) \Delta e_{odq} \quad (56)$$

Relating the vector e_{odq} with X_{odq} , we can rewrite (56) as,

$$\Delta \dot{Q}_{av} = -\omega_f \Delta Q_{av} + \omega_f (I_o + E_o Y_o) K_{xdq} \Delta X_{odq} \quad (57)$$

where

$$K_{xdq} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Considering (12) in a symbolic way and relating the vector ΔE_o with ΔX_o ,

$$\Delta E_o = K_x \Delta X_o = K_x T_{odq} \Delta X_{odq} \quad (58)$$

where

$$K_x = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (59)$$

Thus (12) can be rewritten as,

$$\Delta \dot{E}_m = -\omega_{fm} \Delta E_m + \omega_{fm} K_x T_{odq} \Delta X_{odq} \quad (60)$$

Finally, an equation system composed by (41), (57) and (60) is obtained. On the other hand, there is a virtual impedance loop between E_r and E_o that can be expressed as,

$$\vec{E}_{ri} = \vec{E}_{oi} + Z_v \vec{I}_{oi} \quad (61)$$

where

$$Z_v = \begin{bmatrix} R_{v1} + jX_{v1} & 0 & 0 \\ 0 & R_{v2} + jX_{v2} & 0 \\ 0 & 0 & R_{v3} + jX_{v3} \end{bmatrix}$$

Thus,

$$e_{rdqi} = e_{odqi} + Z_{vr} i_{odqi} \quad (62)$$

where

$$Z_{vr} = \begin{bmatrix} R_{v1} & -X_{v1} & 0 & 0 & 0 & 0 \\ X_{v1} & R_{v1} & 0 & 0 & 0 & 0 \\ 0 & 0 & R_{v2} & -X_{v2} & 0 & 0 \\ 0 & 0 & X_{v2} & R_{v2} & 0 & 0 \\ 0 & 0 & 0 & 0 & R_{v3} & -X_{v3} \\ 0 & 0 & 0 & 0 & X_{v3} & R_{v3} \end{bmatrix}$$

Substituting (48) in (62), it yields,

$$\begin{aligned} e_{rdqi} &= e_{odqi} + Z_{vr} Y_o e_{odqi} \\ &= (I_o + Z_{vr} Y_o) e_{odqi} = K_{ZY} e_{odqi} \end{aligned} \quad (63)$$

By linearizing (63), we can obtain the following small signal approximation,

$$\Delta e_{rdqi} = K_{ZY} \Delta e_{odqi} \quad (64)$$

Then, relating (64) with ΔX_{rdq} and ΔX_{odq} , it can be obtained:

$$\Delta X_{rdq} = \begin{bmatrix} K_{ZY} & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{odq} = K_{rdq} \Delta X_{odq} \quad (65)$$

$$\dot{\Delta X}_{rdq} = \begin{bmatrix} K_{ZY} & 0 \\ 0 & I_6 \end{bmatrix} \dot{\Delta X}_{odq} = K_{rdq} \dot{\Delta X}_{odq} \quad (66)$$

By combining (41) and (66), it yields,

$$T_{rdq} K_{rdq} \dot{\Delta X}_{rdq} = M_1 T_{odq} \dot{\Delta X}_{odq} + M_2 T_{odq} \Delta X_{odq} + M_3 \Delta E_m + M_4 \dot{\Delta Q}_{av} \quad (67)$$

Considering (57) and (67), we can rewrite (66) as,

$$\dot{\Delta X}_{rdq} = T_{km}^{-1} \left(M_2 T_{odq} + M_4 \omega_f (I_o + Y_o E_o) K_{xdq} \right) \Delta X_{odq} + T_{km}^{-1} M_3 \Delta E_m - T_{km}^{-1} M_4 \omega_f \dot{\Delta Q}_{av} \quad (68)$$

where

$$T_{km} = T_{rdq} K_{rdq} - M_1 T_{odq} \quad (69)$$

Based on (57), (60) and (68), we can write the following state-space equation,

$$\begin{bmatrix} \dot{\Delta X}_{rdq} \\ \dot{\Delta E}_m \\ \dot{\Delta Q}_{av} \end{bmatrix} = A \begin{bmatrix} \Delta X_{rdq} \\ \Delta E_m \\ \Delta Q_{av} \end{bmatrix} \quad (70)$$

which depicts the performance of the system around the equilibrium point under an initial condition by giving a disturbance, hereby

$$A = \begin{bmatrix} X_8 & T_{km}^{-1} M_3 & -T_{km}^{-1} M_4 \omega_f \\ \omega_{fm} K_x T_{odq} & -\omega_{fm} & 0 \\ \omega_f (I_o + E_o Y_o) K_{xdq} & 0 & -\omega_{fm} \end{bmatrix} \quad (71)$$

where $X_8 = T_{km}^{-1} \left(M_2 T_{odq} + M_4 \omega_f (I_o + Y_o E_o) K_{xdq} \right)$.

IV. STABILITY ANALYSIS

In order to achieve the stability analysis of the system, load step was carried out in the experimental setup, which is shown in Fig. 7. The critical parameters are shown in TABLE I. Through dSpace, experimental data are extracted from the experimental setup, plotted in Matlab and compared with poles movement obtained from the mathematical model in order to analyze the six critical parameters impacts on system performance.

Fig. 8(a) presents the system dynamics in case of changing k_{pv_sec} . Since the model is considered in $\alpha\beta$ frame, rms value of the AC critical bus is processed in $\alpha\beta$ frame, ie 230V rms means 281.69V in $\alpha\beta$ frame. It can be seen that, with k_{pv_sec} being 0.5,

TABLE I
PARAMETERS FOR MODEL TEST

Symbol	Parameter	Values
Load		
Z_{L1}	Load 1 (each phase)	230Ω
Z_{L2}	Load 2 (each phase)	230Ω//57Ω//27μF
Measure Parameters		
ω_f	Reactive power measuring cut-off frequency	6.28rad/s
ω_{fm}	RMS measure cut-off frequency	6.28rad/s
k_{pp}	Proportional PLL term	100
k_{ip}	Integral PLL term	1000
ω	Nominal frequency	314.16rad/s
Control Parameters (central controller)		
k_{pv_sec}	Proportional voltage term	2.5
k_{iv_sec}	Integral voltage term	20.5
$k_{p\theta_sec}$	Proportional phase term	0.2
$k_{i\theta_sec}$	Integral phase term	9
Z_{vir}	Virtual impedance	20+j0 Ω
k_{ph}	Phase control coefficient	0.0001rad/VAr
Control Parameters (DC/AC modules)		
k_{pv}	Proportional voltage term	0.55
k_{rv}	Resonant voltage term	70
k_{hrv}	5 th , 7 th resonant voltage term	100,100
k_{pc}	Proportional current term	1.2
k_{rc}	Resonant current term	150
k_{hrc}	5 th , 7 th resonant current term	30,30

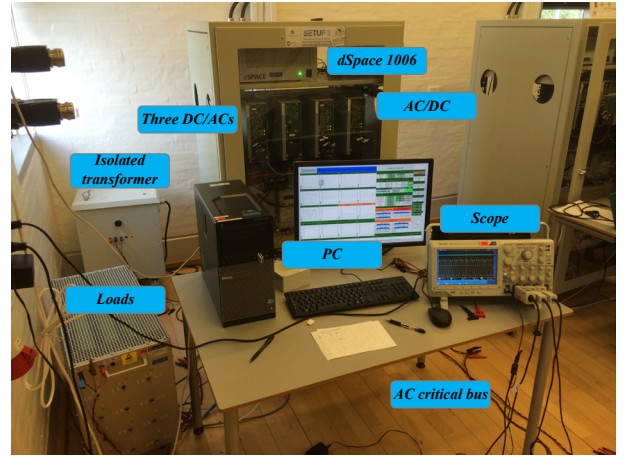


Fig. 7. Experimental setup.

2.5 and 5, the system transient performance including AC critical bus voltage, active power and reactive power, is becoming more and more damped. The poles movement is drawn with the same parameter changing range are shown in Fig. 9(a). It can be observed that the poles are moving towards the real axis, which also indicates that the system is becoming more and more damped.

The system performance when k_{iv_sec} is 5, 20.5 and 50 is presented in Fig. 8(b). It can be observed that AC critical bus voltage, active power and reactive power tend to have oscillations, which indicates a less damped system. Poles movements with the same changing range, is presented in Fig. 9(b), moving away from real axis. This means that the system is becoming less and less damped, which matches the experimental result.

Fig. 10(a) shows the system dynamics when k_{ph} is 0.0001, 0.0003 and 0.0005. Actually the dynamics are almost the same

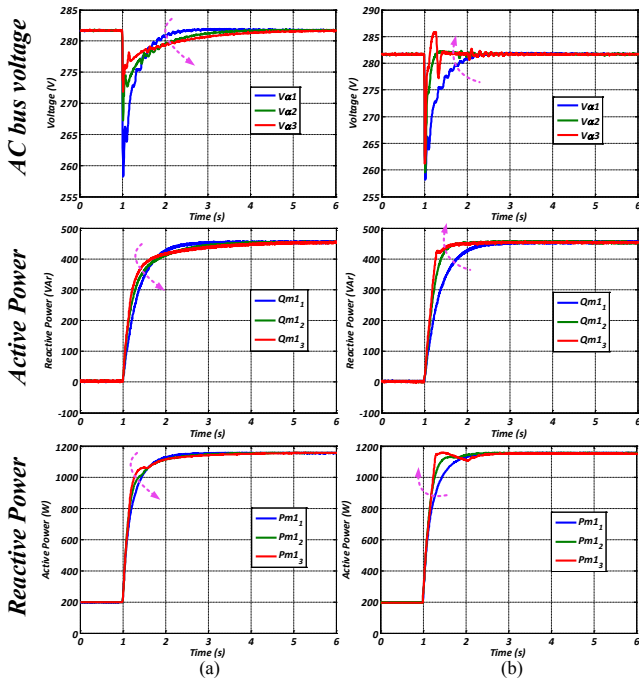


Fig. 8. Experimental data plot in Matlab under variable k_{pv_sec} and k_{iv_sec} . (a) Variable k_{pv_sec} (0.5, 2.5 and 5). (b) Variable k_{iv_sec} (5, 20.5 and 50).

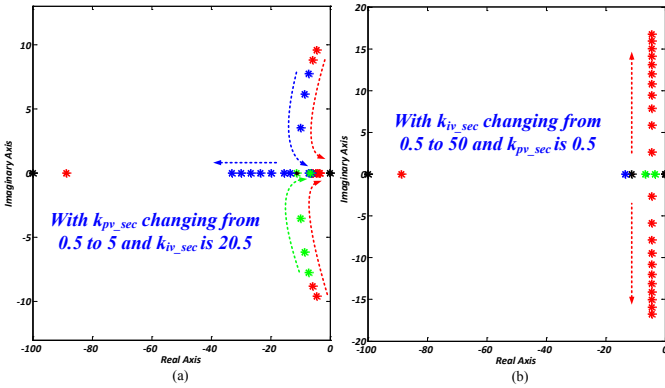


Fig. 9. Poles movements of the system. (a) k_{pv_sec} from 0.5 to 5. (b) k_{iv_sec} from 5 to 50.

in the experiment. But in order to show the process clearly, three curves are made manually a bit separated. And it can be seen that all the poles of the system is kept in the same position (Fig. 11(a)), which means that it has no impacts on system performance.

In Fig. 10(b), the impacts of the virtual resistor are depicted. Small impacts are observed on the active power and reactive power. However, it has significant impacts on the voltage sag amplitude in the transient process. With R_{vir} increasing, the voltage sag becomes bigger. Fig. 11(b) presents the poles distribution condition regarding the same R_{vir} variation range. The dominating poles have slight movements, which indicate that it has small impacts on the system performance. Based on IEC 62040-3, the voltage sags in the transient process should be controlled under 10% optimally,

$$\left| \frac{i_o R_{vir}}{V_o} \right| \leq 10\% \quad (72)$$

being i_o and V_o the maximum output current and nominal output voltage.

In Fig. 12(a), it can be observed that when the $k_{p\theta_sec}$ is 0.2, 1

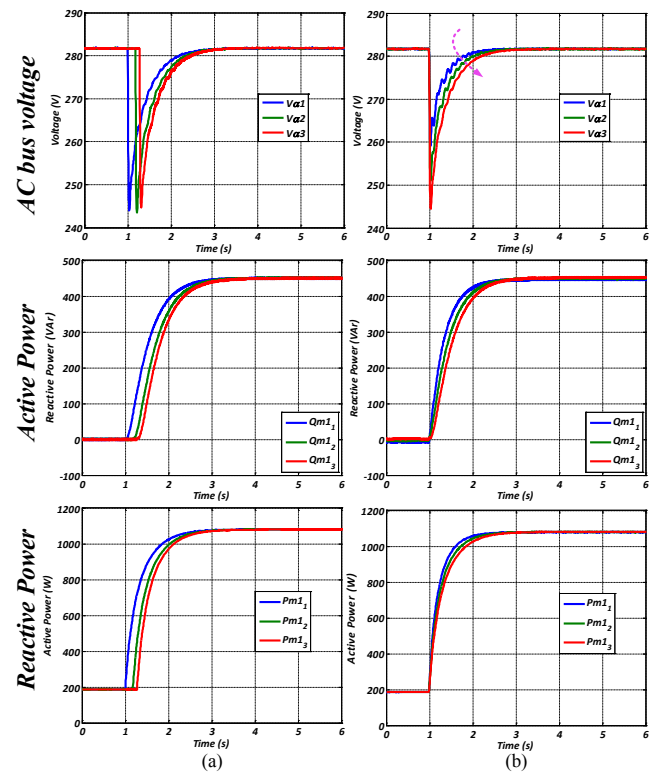


Fig. 10. Experimental data plot in Matlab under variable k_{ph} and R_{vir} . (a) Variable k_{ph} (0.0001, 0.0003 and 0.0005). (b) Variable R_{vir} (20, 30 and 40).

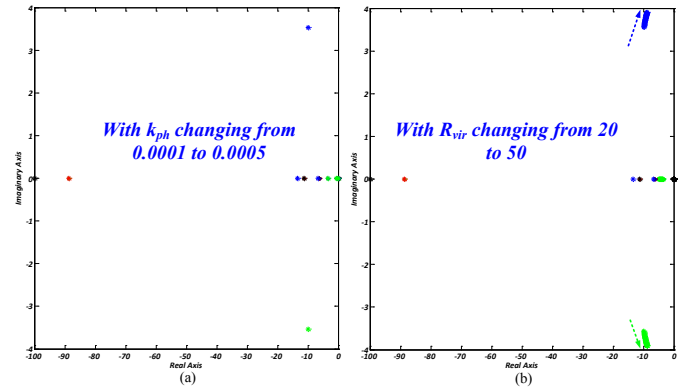


Fig. 11. Poles movements of the system. (a) R_{vir} from 20 to 30. (b) k_{ph} from 0.0001 to 0.0005.

and 2, small difference is able to be seen in AC critical bus voltage transient, active power transient and reactive power transient. Poles movement in this situation is presented in Fig. 13(a). One pole is moving away from original point in the real axis and its impact on the system is becoming more and more un conspicuous. And the remaining dominating poles doesn't move too much, which means that system performance is not affected too much. Fig. 13(b) shows the $k_{i\theta_sec}$ effects on the poles movement. Poles tend to remove away from real axis, which means that the system is less and less damped, as shown in Fig. 12(b) experimental data.

Besides its impacts on AC critical bus voltage transient process, $k_{p\theta_sec}$ and $k_{i\theta_sec}$ also has impact on the synchronization process divergence speed of the proposed online UPS system, which is shown in Fig. 14. In Fig. 14(a), the $k_{i\theta_sec}$ is 10, 20 and 30 respectively while $k_{p\theta_sec}$ is remained fixed. It can be

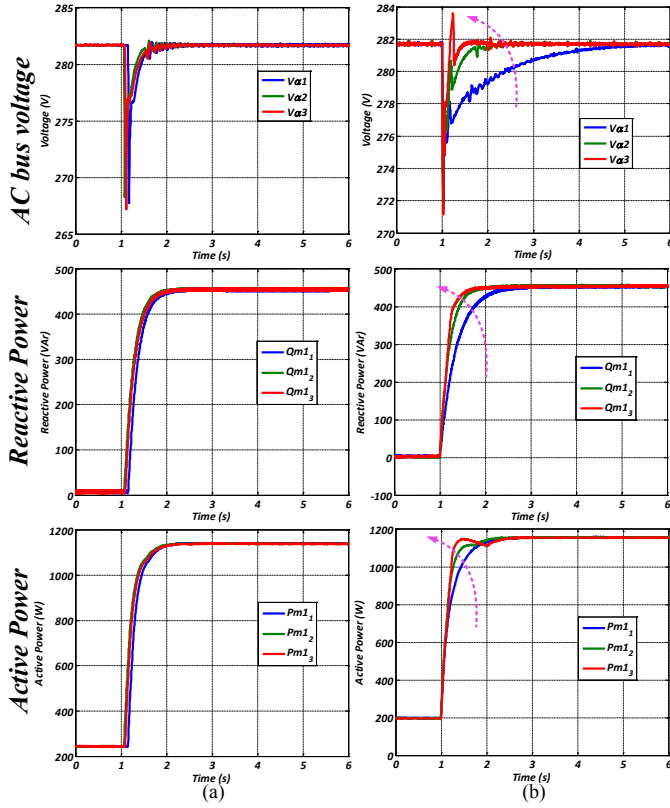


Fig. 12. Experimental data plot in Matlab under variable $k_{p\theta_sec}$ and $k_{i\theta_sec}$. (a) Variable $k_{p\theta_sec}$ (0.2, 1 and 2). (b) Variable $k_{i\theta_sec}$ (10, 20 and 30).

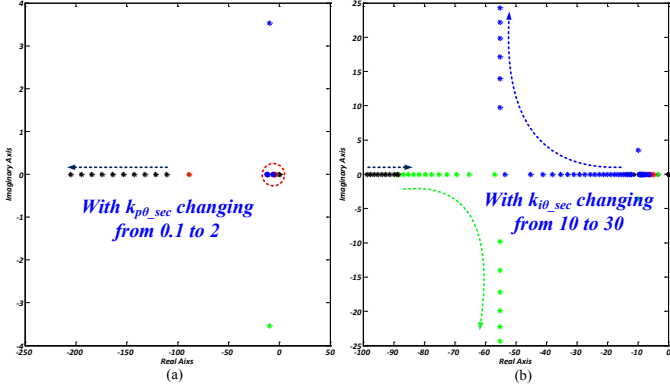


Fig. 13. Poles movements of the system. (a) $k_{p\theta_sec}$ from 0.2 to 2. (b) $k_{i\theta_sec}$ from 10 to 30.

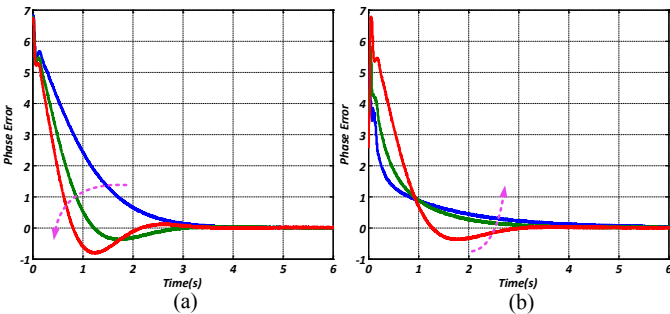


Fig. 14. Experimental data plot in Matlab under variable $k_{p\theta_sec}$ and $k_{i\theta_sec}$. (a) $k_{i\theta_sec}$ is 10, 20 and 30. (b) $k_{p\theta_sec}$ is 0.2, 1.2 and 2.2.

observed that the synchronization process tends to have oscillation with bigger $k_{i\theta_sec}$. Fig. 14(b) shows the synchronization process with variational $k_{p\theta_sec}$. While it increasing, the system is becoming more and more damped

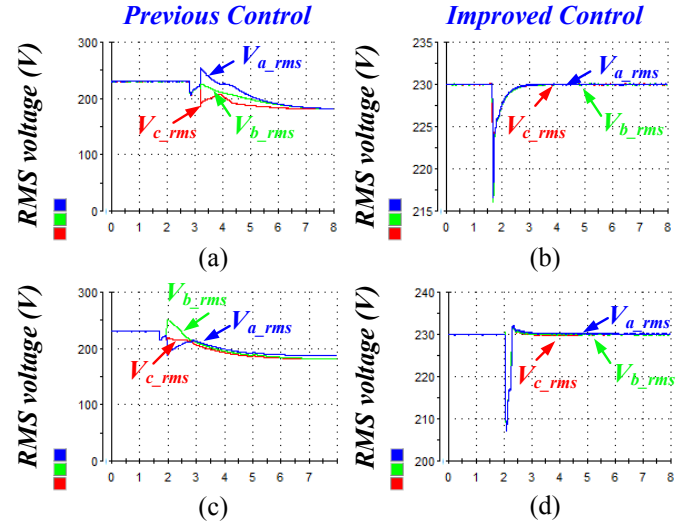


Fig. 15. AC critical bus voltage performance when one DC/AC breaks down. (a) Previous control under linear load condition. (b) Improved control under linear load condition. (c) Previous control under nonlinear load control. (d) Improve control under nonlinear control.

without any oscillation.

V. EXPERIMENTAL RESULTS

By using the control parameters shown in Table I, experiments were carried out to validate the feasibility of the proposed *plug'n'play* control strategy.

Fig. 15 presents the AC critical bus voltage restoration performance when one DC/AC is suddenly disconnected. It can be seen that the AC critical bus is tightly regulated to 230V_{rms}. During the transient, the voltage oscillation is kept under 15V, i.e. 8.6% of the nominal output voltage. In Fig. 15(a), the performance with previous control is presented. If one phase voltage of all modules are positive, for instance phase *a*, when one modules plug out without refreshing the DC/AC working number *n*, the average block output $((V_{1a} + V_{2a} + \dots + V_{na})/n)$ will become small. This means that the instantaneous input of the controller G_{v_rec} becomes bigger. As a result, the output of the controller v_{a_rec} is bigger, which means that a bigger voltage reference is generated. It can be observed that v_{a_rms} had an overshoot. After some transient process, it reaches a random value that is not equal to 230V. However, with the proposed control, the AC critical bus voltage can be recovered to 230V as shown in Fig. 15(b). Also, under nonlinear load conditions, a similar AC critical bus voltage performance is obtained as shown in Figs. 15 (c) and (d). Since the voltage variation is quite serve under previous control, the y axis in Fig. 15 between previous control and improved control are different.

Since there is a low pass filter in the RMS value calculation block, the voltage transient process is slowed and it cannot precisely reflect the UPS output voltage performance. So that real-time voltage performance is obtained through scope to evaluate the *plug'n'play* performance. At the same time, power sharing performance between modules is also presented in Fig. 16. At t_a , DC/AC #3 is order to plug in and plug out at t_b . The active power is well shared among the modules, as well as the reactive power. At t_c and t_d , a similar operation was carried out

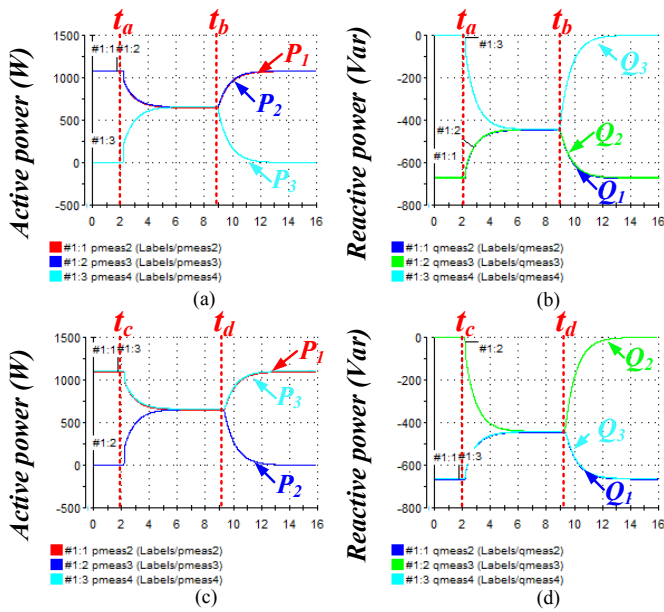


Fig. 16. Power sharing performance in case of module plugging in and out. (a) Active power sharing when module #3 plug in and out. (b) Reactive power sharing when module #3 plug in and out. (c) Active power sharing when module #2 plug in and out. (d) Reactive power sharing when module #2 plug in and out.

TABLE II
TRANSIENT TIME REQUIREMENT IN IEC-62040-3

	Voltage overshoot or sag (%)	Duration time (ms)
Linear Load	14% (overshoot or sag)	20-40
	12% (overshoot or sag)	40-60
	11% (overshoot or sag)	60-100
	10% (overshoot or sag)	100-1000
Nonlinear Load	12% (overshoot) / 27% (sag)	40-60
	11% (overshoot) / 27% (sag)	60-100
	10% (overshoot) / 20% (sag)	100-1000

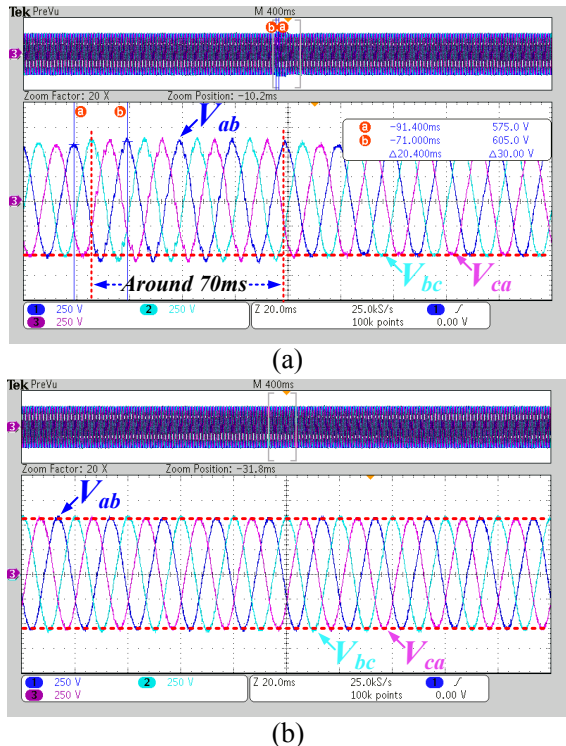


Fig. 17. System output voltage transient performance in case of DC/AC module plugging in and out. (a) Transient at t_a . (b) Transient at t_b .

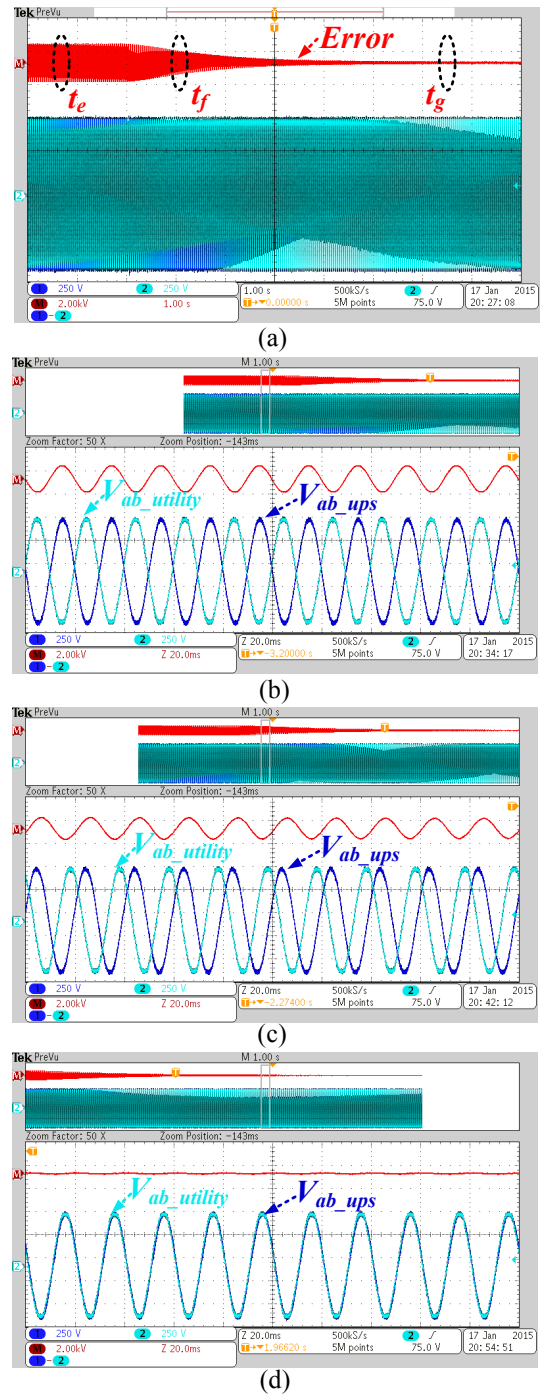


Fig. 18. Synchronization process. (a) Overall Process. (b) Transient at t_e . (c) Transient at t_f . (d) Transient at t_g .

for DC/AC #2. It can be observed that both active power and reactive power are well shared. AC bus voltage transient behaviors during this two modules operation are presented in Fig. 17 and evaluated according to IEC 62040-3 [2].

Fig. 17(a) depicts the UPS output voltage transient performance at t_a . It can be observed that the whole transient time duration is around 70ms. The voltage overshoot when DC/AC #3 is reconnected is around 40V, as shown in Fig. 17(a), which is around 5.21% ($(605V-575V)/575V$) of the nominal output voltage value. According to the standard shown in TABLE II, if the voltage overshoot is less than 10% of the nominal value, the transient duration time is in the range of

100ms – 1000ms when the load is either linear or nonlinear. Consequently, it can be concluded that the system performance meets the standard IEC 62040-3 [2].

Synchronization performance of the system was also tested as shown in Fig. 18. Line-to-line voltage of phase *a* and *b* of the utility and proposed online UPS system is presented. It can be observed that the phase errors are reduced smoothly without causing any voltage oscillation.

VI. CONCLUSION

This paper presents an improved control strategy for modular online UPS system, which aims at achieving *plug'n'play* capability. This control features allows the system to be maintained with less difficulty, such as serious AC critical bus voltage oscillation, unbalanced power sharing performance, synchronization problems with the utility and so on. The modules that need to be maintained can be stopped or started randomly without affecting the AC critical bus voltage. Besides the accurate active and reactive power sharing performance, the proposed control strategy presents a faster dynamic performance in case of module plugging out and in compared with the control methods proposed before according to IEC 62040-3. Moreover, a recovery and synchronization capability is achieved without using PLL. Experiments results are provided to validate the proposed control strategy. A detailed small signal model is derived to analyze the critical parameters impact on system performance using experimental data, which is able to be treated as a guidance to design the system.

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VII. BIOGRAPHIES



Chi Zhang (S'14) received the B.S degree in electronics and information engineering from Zhejiang University (ZJU), Hangzhou, China in 2012. Between 2012 and 2013, he works as a Master student in National Engineering Research Center for Applied Power Electronics in Zhejiang University. He is currently working toward his Ph.D in power electronic at the

Department of Energy Technology, Aalborg University, Denmark.

His research interests include power electronics converter design in modular uninterruptible power supply systems, active power filter systems and renewable energy generation systems.



Ernane Antônio Alves Coelho was born in Teofilo Otoni, Brazil, in 1962. He received the B.S. degree in electrical engineering from the Federal University of Minas Gerais, Belo Horizonte, Brazil, the M.S. degree from the Federal University of Santa Catarina, Florianopolis, Brazil, and the Ph.D. degree from the Federal University of

Minas Gerais in 1987, 1989, and 2000, respectively. In 1989, he joined the Electrical Engineering Faculty at Federal University of Uberlandia, where he is currently a Full Professor. In 2014, he was a Visiting Professor with the Microgrid Research Group, Institute of Energy Technology, Aalborg University, Aalborg, Denmark. He is a member of the Brazilian Power Electronic Society (SOBRAEP). He has been working with the Power Electronics Research Group at Federal University of Uberlandia, state of Minas Gerais, Brazil. His research interests are Power-factor Correction, PV and Fuel Cell Systems, Microgrid Modelling and Digital Control by microcontrollers and DSP's.



Josep M. Guerrero (S'01-M'04-SM'08-FM'15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. Since 2011, he has been a

Full Professor with the Department of Energy Technology, Aalborg University, Denmark, where he is responsible for the

Microgrid Research Program. From 2012 he is a guest Professor at the Chinese Academy of Science and the Nanjing University of Aeronautics and Astronautics; from 2014 he is chair Professor in Shandong University; and from 2015 he is a distinguished guest Professor in Hunan University.

His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, and optimization of microgrids and islanded minigrids. Prof. Guerrero is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and the IEEE Industrial Electronics Magazine, and an Editor for the IEEE TRANSACTIONS ON SMART GRID and IEEE TRANSACTIONS ON ENERGY CONVERSION. He has been Guest Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS Special Issues: Power Electronics for Wind Energy Conversion and Power Electronics for Microgrids; the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Special Sections: Uninterruptible Power Supplies systems, Renewable Energy Systems, Distributed Generation and Microgrids, and Industrial Applications and Implementation Issues of the Kalman Filter; and the IEEE TRANSACTIONS ON SMART GRID Special Issue on Smart DC Distribution Systems. He was the chair of the Renewable Energy Systems Technical Committee of the IEEE Industrial Electronics Society. In 2014 and 2015 he was awarded by Thomson Reuters as Highly Cited Researcher, and in 2015 he was elevated as IEEE Fellow for his contributions on "distributed power systems and microgrids."



Juan C. Vasquez (M'12-SM'14) received the B.S. degree in electronics engineering from the Autonomous University of Manizales, Manizales, Colombia, and the Ph.D. degree in automatic control, robotics, and computer vision from the Technical University of Catalonia, Barcelona, Spain, in 2004 and 2009, respectively. He was with the Autonomous University of Manizales working as a teaching assistant

and the Technical University of Catalonia as a Post-Doctoral Assistant in 2005 and 2008 respectively. In 2011, he was Assistant Professor and from 2014 he is working as an Associate Professor at the Department of Energy Technology, Aalborg University, Denmark where he is the Vice Programme Leader of the Microgrids Research Program. From Feb. 2015 to April. 2015 he was a Visiting Scholar at the Center of Power Electronics Systems (CPES) at Virginia Tech. His current research interests include operation, advanced hierarchical and cooperative control, optimization and energy management applied to distributed generation in AC and DC microgrids. He has authored and co-authored more than 100 technical papers only in Microgrids where 60 of them are published in international IEEE journals.

Dr. Vasquez is currently a member of the IEC System Evaluation Group SEG4 on LVDC Distribution and Safety for use in Developed and Developing Economies, the Renewable Energy Systems Technical Committee TC-RES in IEEE Industrial Electronics, PELS, IAS, and PES Societies.