Real Time Monitoring and Wear Out of Power Modules

Ghimire, Pramod

Publication date:
2015

Document Version
Publisher's PDF, also known as Version of record

Real Time Monitoring and Wear Out of Power Modules

Ph.D. Dissertation

Pramod Ghimire

September, 2015

Thesis submitted:	September, 2015
PhD Supervisor:	Prof. Stig Munk-Nielsen Aalborg University
Assistant PhD Supervisor:	Paul Thøgersen, Bjørn Rannestad KK Windsolutions A/S
PhD Committee:	Associate Prof. Erik Schaltz, Aalborg University Prof. Marco Liserre, University of Kiel Prof. Li Ran, The University of Warwick
PhD Series:	Faculty of Energy Technology, Aalborg University

Published by:
Aalborg University Press
Skjernvej 4A, 2nd floor
DK – 9220 Aalborg Ø

Printed in Denmark by

Preface

This dissertation is based on the experimental work carried out in Gurli I, an advanced active thermal cycling test setup located in the lab called garage. Later, the post-test failure analysis of the power cycled module is carried out separately.

Initially, I would like to thank Prof. Stig Munk-Nielsen for guidance, support, and the opportunity to work on the presented topics. Additionally, I would like to thank Dr. Paul Thøgersen and Bjørn Rannestad for significant assistance in defining real world problems, with experimental work, and their valuable suggestions over the last three years. I would like to thank sincerely Angle Ruiz de Vega for valuable support in experimental work, Dr. Szymon Beczkowski for making smart circuitry, and Dr. Ionut Trintis for helping in construction of the test setup. Furthermore, I am indebted to Kristian Bonderup Pedersen for carrying out post-test failure analysis and discussions regarding all presented topics. I admire Christian Uhrenfeldt and Peter Kjær Kristensen for their invaluable input during the investigation of IR thermography on open power modules. I would like to thank Klaus Olesen from Danfoss Silicon Power for providing open power module samples and also for the opportunity to stay at Danfoss Silicon Power, Germany. Discussions of relevant topics with engineers and production line personnel were especially helpful.

I would to like thank Prof. Frede Blaabjerg and Prof. Francesco Iannuzo for their encouragement and support throughout the period of study. I also thank all industrial colleagues from CORPE and IEPE projects for their discussion and tips during the workshops. I also thank all technical staffs in our department for their invaluable and timely support. I am also thankful to other departmental colleagues and secretaries. I am immensely grateful to Dr. Peter Freere and Ana Freere for their faith and thoroughly checking English in my thesis.

A special thanks goes to my beloved wife Sanchita for her patience, support and encouragement and also to my son Prasan. Finally, to my parents for being there.

Aalborg University, September 2015

Abstract

Power electronic devices have a wide range of applications from very low to high power at constantly varying load conditions. Irrespective of the harsh operating loads, including both internal and external, an improvement in a performance such as efficiency, power density, reliability and cost for power converter is a continuous research effort. Cost is a design limitation where the tendency is always to increase the rated power for the same price or decrease the price for same rated power.

Satisfying the above mentioned facts, a healthy operation of power devices is essential to meet the expected lifetime of converters. Real time monitoring of power modules is very important together with a smart control and a driving technique in a converter. This ensures to operate the device within a safe operating area and also to protect from a catastrophic failure. Furthermore, the inherent physical parameters that deviate by thermo-mechanical stress need to be identified and also measured during operation. Major stressors for high power multi-chip IGBT modules are identified as maximum junction temperature, temperature cycle, over-voltage, over-current, humidity, vibration etc. In addition, finding a root cause of failure is often difficult after a catastrophic failure.

This thesis proposes an on-state parameter measurement technique which is robust and easy to integrate into existing gate driver technology. The technique is suitable for the application in both normal converter operation and in a mission-profile oriented advanced power cycling test. The measurement technique is implemented in a full scale converter under field oriented test conditions.

Initially, a real time measurement technique and it's implementation in a converter are introduced. A full scale converter is also used as an advanced power cycling test setup, where both power module characterization and field emulated testing are proposed. As temperature is identified as a major stressor, transforming on-state forward voltage drop to die temperature for each individual chip is presented at a nominal rated power level. The wear out is monitored online and also the evolution of degradation in interconnects are studied extensively in order to understand the failure pro-

cess in high power modules under sinusoidal loading conditions. A number of power modules are tested in active power or thermal cycling for different number of cycles under similar loadings. Afterwards degradation evolutions in each power module are assessed and correlated with the results obtained from the online monitoring. Bond wire and solder fatigue are two major expected low thermal cycle fatigues. A data evaluation theory is proposed to separate two different fatigues in converter operation. A method which automatically re-calibrates each individual device is presented removing the effects from a difference in geometry of a power module. In order to map the degradation distribution, four-point probing results and micro-investigations are presented for aged power modules.

The presented online monitoring technique is implementable in real life applications. The measurement technique is also useful for fast overload protection, replacement of software based models for short overload control, etc.

Dansk Resume

Effektelektroniske apparater har bred vifte af anvendelser fra meget lav til høj effekt og deres belasting er ofte meget varierende. Belastning giver en del stress af apparaters effektmoduler som håndterer effekten hvilket har indflydelse på levetiden. Apparaternes ydelse måles på energieffektivitet, effekttæthed, levetid, pålidelighed og pris. Der sker en løbende udvikling for at forbedre effektelektroniske apparater. Prisen for teknologien er betydende og udviklingen går på at øge den nominelle effekt enten til samme pris eller mindske prisen for samme mærkeeffekt, vel at mærke med en forventning om høj pålidelighed.

Der arbejdes på at opfylde ovennævnte behov og belastningen af effektmodulerne er afgørende for at imødekomme den forventede levetid af konvertere. Sammen med en smart kontrol og forbedret elektronik der styrer effektmodulerne, har det vist sig muligt at lave en sandtids overvågning af effektmoduler som på sigt kan sikre at driften opretholdes og katastrofale fejl undgås. Igennem levetiden ældes effektmodulerne og det betyder at man skal tænke sig godt om når man forsøger at udlede noget om drifttilstanden af effektmodulerne. De mest betydende stressfaktorer for levetiden er identificeret som temperatur for halvledere, temperatur variation, overspænding, overstrøm, fugtighed og vibrationer. I tilfælde af katastrofale fejl opstår ødelægges modulet ofte hvilket gør det svært at finde en dybereliggende årsag til fejlen.

I denne afhandling foreslås en måleteknik metode som er robust og let at integrere i eksisterende elektronik der udgør gatedriveren. Teknikken er velegnet til anvendelse i både normal apparat drift ude i felten og i et laboratorie miljø hvor der realiseres en levetids test baseret på belasting der emulere

et driftpunkt. Måletekniken er implementeret i en fuldskala effektelektronisk konverter som eftergøre driftpunkt fra en vindmølle.

Indledningsvis i afhandling introduceres måleteknikker, realisering samt anvendelse i konverteren beskrives. En konverter som kan anvendes til eks. vindmøller anvendes til en levetidstest og effektmoduler karakteriseres. I forbindelse med levetid fokuseres på temperaturens indflydelse. Det er vigtigt at kende temperaturen og derfor præsenteres en metode som estimerer temperaturen i effektmodulet ud fra en måling af ledespænding og strøm. Under levetidstesten måles ledespænding hvilket muliggør at udvikling af det mekaniske slid internt i effektmodulet kan overvåges, ultimativt vil mekaniskslitage gøre at strømvejen afbrydes og der opstår en katastrofal fejlsituation. Et antal effektmoduler er testet til forskellige grader af ældning. Det gør det muligt at undersøge omfang af slitage på de tråde som lederstrømmen og de lodninger som forbinder halvledere med køling. Under ældning er det vigtigt løbende at kalibrere rutinen som estimerer temperaturen, da de nævnte ældningsfænomener påvirker estimeringen og en automatisk kalibrerings metode foreslås. For at forstå ældnings mekanismer laves der en laboratorieanalyse baseret på fire-punkts målinger og mikro-slib.

Den præsenterede sandtids overvågning teknik forventes anvendt i apparater inden for forskellige anvendelser. Måleteknikken er også nyttig til hurtig overbelastningsbeskyttelse herunder kan den forbedre overbelastnings modeller der baseres på designdata til at være baseret på målt information.

Thesis Details

Thesis Title: Real Time Monitoring and Wear Out of Power Modules
Ph.D. Student: Pramod Ghimire
Supervisors: Prof. Stig Munk-Nielsen, Aalborg University
Dr. Paul Bach Thøgersen
Bjørn Rannestad, KK Windsolutions A/S

The main body of this thesis consist of the following papers.

[A] P. Ghimire, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, P. Thøgersen, "A review on real time physical measurement techniques and their attempt to predict wear-out status of IGBT," *Proceedings of the 15th European Conference on Power Electronics and Applications, EPE 2013*, pp. 1-10, 2013.

[B] S. Beczkowski, P. Ghimire, A.R. de Vega, S. Munk-Nielsen, B. Rannestad, P. Thøgersen, "Online Vce measurement method for wear-out monitoring of high power IGBT modules," *Proceedings of the 15th European Conference on Power Electronics and Applications, EPE 2013*, pp.1–7, 2013.

[C] P. Ghimire, A.R. de Vega, S. Munk-Nielsen, B. Rannestad, P. Thøgersen, "A Real Time V-ce Measurement Issues for High Power IGBT Module in Converter Operation," *Proceedings of the 1st International Future Energy Electronics Conference, IFEEC 2013*, pp. 761–766, 2013.

[D] P. Ghimire, K. B. Pedersen, A. R. de Vega, B. Rannestad, S. Munk-Nielsen, P. Thøgersen, "A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application," *Proceedings of the 8th International Conference on Integrated Power Systems (CIPS), 2014 . VDE Verlag GMBH*, pp. 1–6, 2014.

[E] A. R. de Vega, P. Ghimire, K. B. Pedersen, I. Trintis, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, P. Thøgersen, "Test setup for accelerated test of high power IGBT modules with online monitoring of Vce and Vf voltage during converter operation," *Proceedings of the 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA)*, pp. 2547–2553, 2014.

[F] P. Ghimire, A. R. de Vega, S. Beczkowski, S. Munk-Nielsen, B. Rannested, P. Thøgersen, "An online Vce measurement and temperature estimation method

for high power IGBT module in normal PWM operation," *Proceedings of the 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA)*, pp. 2850–2855, 2014.

[G] P. Ghimire, A. R. de Vega, S. Beczkowski, B. Rannestad, S. Munk-Nielsen, P. Thøgersen, "Improving Power Converter Reliability: Online Monitoring of High-Power IGBT Modules," *I E E E Industrial Electronics Magazine*, vol. 8, No. 3, pp. 40–50, 2014.

[H] P. Ghimire, K. B. Pedersen, B. Rannestad, S. Munk-Nielsen, F. Flaabjerg, "Real time wear-out monitoring test setup for high power IGBT modules," submitted to *I E E E Transactions on Power Electronics*, 2015.

[I] K. B. Pedersen, L. H. Østergaard, P. Ghimire, V. Popok, K. Pedersen, "Degradation mapping in high power IGBT modules using four-point probing," *Microelectronics Reliability*, Vol. 55, Issue 8, PP 1196-1204, 2015.

[J] K. B. Pedersen, L. H. Østergaard, P. K. Kirstensen, P. Ghimire, V. Popok, K. Pedersen, "Degradation evolution in high power IGBT modules subjected to sinusoidal current load," *Journal of Materials Science: Materials in Electronics*, E-pub ahead of print 2015, doi: http://dx.doi.org/10.1007/s10854-015-3976-1.

[K] P. Ghimire, K. B. Pedersen, B. Rannestad, S. Munk-Nielsen, "Ageing Monitoring in IGBT Module Under Sinusoidal Loading," *Microelectronics Reliability*, Vol. 55, Issues 9-10, pp. 1945-1949, 2015.

[L] P. Ghimire, K. B. Pedersen, I. Trintis, B. Rannestad, S. Munk-Nielsen, "Online Chip Tempertaure Monitoring Using v_{ce}-Load Current and IR Thermography," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 6602-6609, 2015, doi: 10.1109/ECCE.2015.7310584.

[M] S. Munk-Nielsen, P. Ghimire, I. Trintis, B. Rannestad, P. Thøgersen, "Power Module Lifetime and State Monitoring," *IET Book-Chapter: Reliability of Power Electronic Converter Systems*, 2015, ISBN: 978-1-84919-901-8 (in Press).

[N] P. Ghimire, I. Trintis, S. Munk-Nielsen, B. Rannestad "On-state voltage drop based derating/uprating on MW converter to improve reliability," under peer review on *Microelectronics Reliability*, 2015.

In addition to the main papers, the following publications have also been made.

[1] S. Chaudhary, P. Ghimire, P. B. Thøgersen, P. de Place Rimmen "Field Data Logger Prototype for Power Converters," *IEEE Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1-4, Dec. 2014.

[2] A. Amoirdis, A. Anurag, P. Ghimire, N. Baker, S. Munk-Nielsen, "Online Junction Temperature Estimation Methods during Power Cycling of High Power IGBT Modules ," *IEEE European Conference on Power Electronics and Applications (EPE)*, pp. 1-9, 2015, doi: 10.1109/EPE.2015.7309449.

[3] S. Chaudhary, P. Ghimire, F. Blaabjerg, B. Rannestad, P. Thøgersen, P. de Place Rimmen, "Development of Field Data Logger for Recording Mission Profile of Power Converters," *IEEE European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, 2015.

[4] R. Wu, H. Wang, K. Ma, P. Ghimire, F. Iannuzzo, F. Blaabjerg "A Temperature-Dependent Thermal Model of IGBT Modules Suitable for Circuit-Level Simulations," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2901-2908, 2014.

[5] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo, F. Blaabjerg, "A 3D Lumped Thermal Network for Fast Estimation of Detail Thermal Dynamics in High Power IGBT Modules," *IEEE Transactions on Power Electronics*, 2015 (Submitted).

[6] K. B. Pedersen, M. Brincker, P. Ghimire, K. Pedersen "Monitoring of IGBT Modules - Temperature and Degradation Simulation," *International Conference on Integrated Power Systems (CIPS)*, 2016 (Accepted).

This present report combined with the above listed scientific papers has been submitted for assessment in partial fulfilment of the PhD degree. The scientific papers are not included in this version due to copyright issues. Detailed publication information is provided above and the interested reader is referred to the original published papers. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the faculty of Engineering and Science, Aalborg University.

Symbols

i_L	Load current
I_{ref}	Reference current
L	Inductor
F_{output}	Output Frequency
V_{DC}	DC Link Voltage
V_{ref}	Reference Voltage
V_{DUT}	Voltage at Device Under Test
V_{CTRL}	Voltage at Control Bridge
ϕ	Phase Displacement
V_{ge}	Gate-Emitter Voltage
$V_{ge,th}$	Gate-Emitter Threshold Voltage
v_{ce}	Collector-Emitter Voltage
$v_{ce,on}$	On-State Collector-Emitter Voltage
P_{cond}	Conduction Power Loss
P_{gate}	Gate Loss
P_{rec}	Recovery Power Loss
P_{sw}	Switching Power Loss
P_{tot}	Total Electrical Power Loss
$R_{g,on}$	On-State Gate Resistance
$R_{g,off}$	Off-State Gate Resistance
$T_{avg,j}$	Average Junction Temperature
T_{ref}	Reference Temperature
T_{cor}	Correction Temperature
$T_{cooloing}$	Cooling Temperature
q_c	Heat Dissipation
q_g	Heat Generation

Unit

A	Ampere
A_{peak}	Peak Current
Hz	Hertz
K	Kelvin
kV	Kilo-Volt
kA	Kilo-Ampere
mW	Milli-Watt
MW	Mega-Watt
$m\Omega$	Milli-Ohm
min	Minute
MC	Million Cycles
Ω	Ohm
$k\Omega$	Kilo-Ohm
$^{\circ}C$	Degree Centigrade
ϕ	Phase Displacement
Rad	Radian
sec	Second
V	Volt
W	Watt

Contents

List of Figures

Part I

Thesis

Chapter 1

Introduction

1.1 Introduction

Usage of power electronic devices is growing rapidly from very low to high power applications in various sectors: energy, auto-motives, defence, aerospace, medical etc. A continuous research effort has been improving the performances of semiconductor devices in terms of efficiency and power density since the development of transistors in 1947 [1]. The development is driven by the growing market for industrial applications, cost competitive market, and availability of new devices [2]. Power electronics reliability has been an important requirement in sensitive applications, such as aerospace and medical, to fulfil stringent constraints required by safety [3]. Nowadays, this is becoming of paramount important in industrial applications where the devices face high load fluctuations and fail much earlier than the expected lifetime, which is designed to meet up to 20-30 years lifetime [2]. Hence, the current research trend is focusing on improving power electronics reliability keeping it's cost low. Furthermore, reliable and efficient performance of power module or converter is the paramount important criteria to meet the recent announcement from the members of EU for climate change and energy sustainability. The target is to use 20% energy from renewable by increasing 20% in energy efficiency and reducing CO_2 emission by 20% by 2020 [4]. Reliability is defined as the ability of an item to perform a required function under stated conditions for a certain period of time, which is often measured by probability of failure, by frequency of failure or in terms of availability [5]. Reliability in power electronics can be improved by performing analytical analysis, design for reliability and verification and monitoring at different life-cycle management of components and converters [5], [6]. Life-cycle management is defined as the process of managing the entire life-cycle of a product from inception, through engineering design and manufacture,

to service and disposal of manufactured products [7]. Some important tests are required during life-cycle management of converters and power devices, see Table 1.1.

Table 1.1: TESTING DURING LIFECYLE MANAGEMENT of POWER DEVICES

Development phase	Functional and verification testing
Production	Fundamental and screening burn-in testing
Operation and maintenance	Monitoring/ Performance testing Smart control (derating/uprating) Mission profile logging Event logging (tripping, extreme events, failures etc) Predictive maintenance
End of life	Post mortem analysis

Analytical power electronics component failure models are developed based on stressors such as junction temperature and loading cycles [8], which are combined with a system level reliability model to give lifetime prediction of the overall system [9]. Such models are being improved over the year by including more design parameters and environmental conditions [10], [11]. For this, several active and passive thermal cycling test methods are developed for specific failures modes such as thermo-mechanical induced failure in interconnects [12]. In active thermal cycling, the thermal stress is induced in the active part of the components by applying a constant DC pulse for a given time followed by a cool down [2]. Accelerated test conditions are used by increasing the electrical and thermal stresses to reduce the test period thereby to collect large statistical data for lifetime investigation. Statistics are necessary to avoid uncertainty and variability in reliability. However, the variation is a function of time and operating conditions, hence statistics itself is not sufficient to interpret without the knowledge of technology, environment conditions, and POF of device [13] [14]. For this, lifetime models obtained from accelerated conditions are fitted and extrapolated with data from normal operating conditions [8], [15], [16], [17] [18], [19]. Although there is uncertainty in extrapolation, one can estimate the lifetime of components for making decision on preventive actions prior to failure. A bath tub curve is used in reliability to demonstrate the failure rate over time based on their decreasing, random, and increasing failure rate from early life to end of life [20]. The reliability in power converters can also be improved by using fault tolerant operation in control strategies [21]. Similarly, various power converter topologies are equipped with redundant capability which ruled out the case to shut down the overall system in any component failures at increasing cost [22], [23], [24].

This thesis is focused in high power multi-chip IGBT modules. The modules are designed to meet lifetime expectation around 20-30 years, which is not the case in reality [2], [25]. An advanced active thermal cycling is used where the device is handled as an active component and switched under normal operation. Accordingly, the switching losses constitute a significant part of the total power loss. In normal operation, the device is performed at ΔT of 20 K - 40 K compared to 100 K in active thermal cycling test. The big difference in thermal stress and surroundings changes the failure mechanisms. Especially high power IGBT modules face thermo-mechanical induced fatigue in interconnects for less than 100K [8], [25], [26].

Instantaneous values of system-energy-related variables such as temperature, voltage, current, flow, speed and system health related parameter values such as junction temperature and temperature sensitive electrical parameters (TSEP) are defined as state data [27]. On-state collector-emitter voltage is a key TSEP, which is not only used as an ageing indicator but also is used to estimate junction temperature [28]. Mainly, on-state v_{ce} at low current method is popularly used [29], [30]. Online measurement and logging of $v_{ce,on}$ in mV range is challenging in converter operation where the device is switched at kV and kA. Some measurement methods are introduced later but mostly limited to laboratory/offline measurements [28]. This thesis proposed a novel on-state v_{ce} measurement technique at mV accuracy in normal operation of converter. Needless to say, the monitoring is of paramount importance to reduce an operation and maintenance cost, to protect a system from catastrophic damages etc. For example, in onshore wind turbine applications, a survey based result shows that power electronic converters contributed to 13% failure rate as well as 18% downtime [31]. Here, power modules and capacitors are found as the most fragile components. Similarly, a reliability oriented industrial based survey shows that the power semiconductor devices ranked the most fragile components [9]. In addition, for offshore wind farms, currently the operation and maintenance cost includes 18-23% of total cost of energy. Hence, these data show an essence of real time measurement in component levels [32].

Online monitoring gives real time streaming of selected signals/variables from a system. The source of data can be a number of parallel sub-systems. Event-driven data logging involves typically high time-based resolution snapshots of important data for a pre-defined time-frame around an event. For a power converter, such logging could contain hundreds of signals, variables, and states for a few seconds. Such data logging with full information about all signals and states are the most important variables, and are crucial for an efficient post-event analysis [27], [33]. Often useful information is lost in catastrophic failure in power modules in both test and field operation. A time-based data logging history is essential to obtain a root cause of failure. Similarly, the degradation evolution in power modules needs to be investi-

gated at different life-stages to understand failure mechanisms. This thesis presents post-test failure analysis of power modules which are cycled to different degradation levels by a number of cycles.

1.2 Thesis Outline

The thesis consists of two parts: the monograph in part I and attached papers in part II. The first part contains 8 chapters including the introduction and conclusion. Selected publications are attached in part II. The structure of the thesis is organized as follows:

Chapter 1 presents a general introduction to the field under investigations including objectives and outline of the whole thesis.

Chapter 2 provides an overview of power module, electrical characteristics, and driving and monitoring techniques. Selected failure mechanisms including lifetime investigations and a brief overview on a few approaches of reliability data analysis are presented.

Chapter 3 introduces field emulated advanced power cycling tests implemented in converter operation. Power module characterization techniques while in converter are presented.

Chapter 4 describes online monitoring of on-state voltage of each component in a half-bridge power module. The measuring circuit principle and it's implementation in converter are highlighted. Similarly, load current and cooling temperature measurement techniques are illustrated.

In chapter 5 reliability stressors in power modules are considered. Knowing temperature as a major stressor, a brief overview on junction temperature measurement techniques is given. A high resolution IR camera is used and a temperature profile on chips during converter operation are presented. A $v_{ce,on}$-load current method is proposed to estimate the chip temperature. The calibration procedures, drawbacks and obtaining correction parameters to improve the accuracy in measurement are given.

Chapter 6 demonstrates wear out tests for a number of power modules at nominal rated power levels under similar loading conditions. The ageing parameters are measured using different approaches, and the trend of rise in those parameters are highlighted. A data evaluation theory to separate bond wire and chip solder degradation is presented.

Chapter 7 presents investigation of failure analysis for wear out power modules subjected to different number of loadings. Results obtained from four-point probing and micro-sectioning techniques are shown.

Finally in chapter 8, conclusion of thesis is given. In addition, some future prospectives of this work are also briefly discussed.

References

[1] Milestones: Invention of the first transistor at bell telephone laboratories, inc. IEEE Global History Network, 1947.

[2] J. Lutz, H. Schlangenotto, U. Scheuermann, and R.W. De Doncker. *Semiconductor power devices*. Springer, 2011.

[3] Patrick D. T. O'Connor and Andre Kleyner. *Practical Reliability Engineering*. John Wiley and Sons, Ltd, 5 edition, 2012.

[4] Europe 2020. $http : //ec.europa.eu/europe2020/europe - 2020 - in - a - nutshell/targets/index_en.htm$.

[5] German Electrical and Electronic Manufacturer's Association, www.zvei.org. *Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications*, third edition, May 2015.

[6] Huai Wang, Marco Liserre, and Frede Blaabjerg. Toward reliable power electronic. *IEEE Industrial Electronics Magazine*, 7(2):17–26, June 2013.

[7] Antti Saaksvuori and Anselmi Immonen. *Product Lifecycle Management*. Springer, Springer-Verlag Berlin Heidelberg, third edition, 2008.

[8] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech. Fast power cycling test of igbt modules in traction application. *Proc. of International Conference on Power Electronics and Drive Systems*, 1:425–430, May 1997.

[9] Shaoyong Yang, A Bryant, P. Mawby, Dawei Xiang, L. Ran, and P. Tavner. An industry-based survey of reliability in power electronic converters. *IEEE Transactions on Industry Applications*, 47(3):1441–1451, May 2011.

[10] J. Lutz. Igbt-modules: Design for reliability. In *Proc. of 13th European Conference on Power Electronics and Applications*, pages 1–3, 2009.

[11] U. Scheuermann and R. Schmidt. Impact of load pulse duration on power cycling lifetime of al wire bonds. *Microelectronics Reliability*, 53(9-11):1687 – 1691, 2013.

[12] Failure mechanisms and model for semiconductor devices (jep122f), jedec, Oct 2011.

[13] H. Wang, M. Liserre, F. Blaabjerg, P. De Place Rimmen, J.B. Jacobsen, T. Kvisgaard, and J. Landkildehus. Transitioning to physics-of-failure as a reliability driver in power electronics," emerging and selected topics in power electronics. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2(1):97–114, March 2014.

[14] W. Kanert. Active cycling reliability of power devices: Expectations and limitations. *Microelectronics Reliability*, 52(9-10):2336 – 2341, 2012.

[15] Raed Amro. *Power cycling capability of advanced packaging and interconnection technologies at high temperature swings*. PhD thesis, Electrical Engineering and Information Technology, Chemnitz University of Technology, 2006.

[16] Kristian Bonderup Pedersen. *IGBT Module and Reliabilty (Physics of Failure Based Characterization and Modelling)*. PhD thesis, Aalborg University, December 2014.

[17] C. Busca, R. Teodorescu, F. Blaabjerg, S. Munk-Nielsen, L. Helle, T. Abeyasekera, and P. Rodriguez. An overview of the reliability prediction related aspects of high power igbts in wind power applications. *Microelectronics Reliability*, 51:1903–1907, 2011.

[18] I.F. Kovacevic, U. Drofenik, and J.W. Kolar. New physical model for lifetime estimation of power modules. In *Proc. of International Power Electronics Conference (IPEC)*, pages 2106–2114, June 2010.

[19] Li Yang, P.A. Agyakwa, and C.M. Johnson. Physics-of-failure lifetime prediction models for wire bond interconnects in power electronic modules. *IEEE Transaction on Device and Materials Reliability*, 13(1):9–17, March 2013.

[20] How to measure lifetime for robustness validation - step by step, zvei - german electrical and electronics manufacturers' association e.v., 2012.

[21] Yantao Song and Bingsen Wang. Survey on reliability of power electronic systems. *IEEE Transactions on Power Electronics*, 28(1):591–604, January 2013.

[22] O. Wallmark, Lennart Harnefors, and O. Carlson. Control algorithms for a fault-tolerant pmsm drive. In *Annual Conference of IEEE Industrial Electronics Society (IECON)*, Nov 2005.

[23] Shengming Li and L. Xu. Strategies of fault tolerant operation for three-level pwm inverters. *IEEE Transactions on Power Electronics*, 21(4):933–940, July 2006.

[24] M.A. Parker, Li Ran, and S.J. Finney. Distributed control of a fault-tolerant modular multilevel inverter for direct-drive wind turbine grid interfacing. *IEEE Transaction on Industrial Electronics*, 60(2):509–522, Feb 2013.

[25] Mauro Ciappa. Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, 42:653 – 667, 2002.

[26] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani. Ageing and failure modes of igbt modules in high-temperature power cycling. *IEEE Transactions on Industrial Electronics*, 58(10):4931–4941, Oct. 2011.

[27] Paul Bach Thøgersen. Converter solutions for wind power. In *EWEA*, 2012.

[28] V. Smet, F. Forest, J. Huselstein, A Rashed, and F. Richardeau. Evaluation of vce monitoring as a real-time method to estimate aging of bond wire-igbt modules stressed by power cycling. *IEEE Transactions on Industrial Electronics*, 60(7):2760–2770, July 2013.

[29] R. Schmidt and U. Scheuermann. Using the chip as a temperature sensor; the influence of steep lateral temperature gradients on the vce(t)-measurement. In *13th European Conference on Power Electronics and Applications*, pages 1–9, September 2009.

[30] L. Dupont and Y. Avenas. Evaluation of thermo-sensitive electrical parameters based on the forward voltage for on-line chip temperature measurements of igbt devices. In *Energy Conversion Congress and Exposition (ECCE)*, pages 4028–4035, September 2014.

[31] Li Ran, Sylvia Konaklieva, Paul McKeever, and Philip Mawby. Condition monitoring of power electronics for offshore wind. *Engineering & Technology Reference*, 2014.

[32] P. Tavner. *Offshore wind tturbine reliability, availability and maintenance*. IET, 2012.

[33] M. Musallam, Chunyan Yin, C. Bailey, and M. Johnson. Mission profile-based reliability design and real-time life consumption estimation in power electronics. *IEEE Transactions on Power Electronics*, 30(5):2601–2613, May 2015.

Chapter 2

Power Modules

2.1 Power Module

A power module is defined as a power electronic module with some circuit topology, which is firmed by several power semiconductor components and packaging interconnections. Usually a power module is needed to increase total power rating of a device by sharing loads on each component of the device. For example, in an IGBT power module IGBT chips and diode chips for free-wheeling are used as semiconductor components and *cu* terminals, bond wires, *Al* metallization, and solders are used as interconnections. Key elements in a power module are voltage insulation, current capability, thermal design regardless of type of a switch such as MOSFET, IGBT, BJT, Thyristor [1].

In this work, a power module is preferred for IGBTs, which are popularly being used in today's market. There are several advantages of IGBTs over other devices. The IGBT makes it possible to have secondary charge carriers due to an extra doping region compared to MOSFETS. The IGBT has superior on-state characteristics, good switching speed and good safe operating area. The IGBT's are preferable in high voltage applications with lower conduction losses. Similarly, they possess comparable on-state voltage and current density at higher switching frequency with power BJTs [2].

2.1.1 Power Module Topology

Different standard designs by reverse blocking voltage and nominal current rating are demonstrated in Fig. 2.1. A half-bridge power IGBT module with 1.7 kV reverse blocking voltage with 1000 A current capability is used in this thesis.

The power module consists of six identical sections. Each section is com-

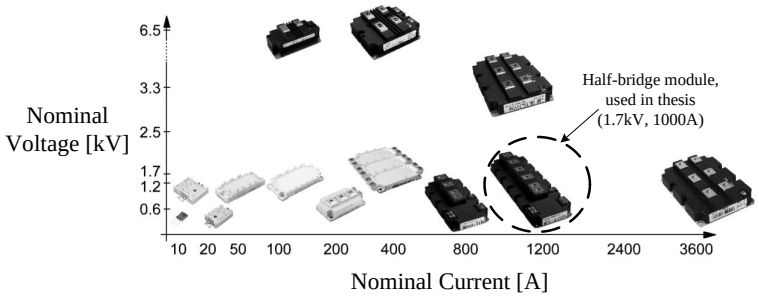


Fig. 2.1: Standard design based on blocking voltage anad nominal current rating, adapted from [3].

posed of two IGBT chips, two free-wheeling diodes, and 20 thick *Al* bond wires, see Fig. 2.3a. An image of an open IGBT power module without silicone gel and bus bar is shown in Fig. 2.2.

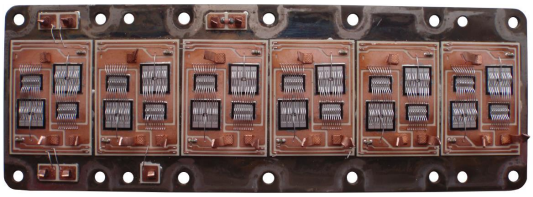


Fig. 2.2: Image of an open power module without silicone gel and bus bar, from [4].

Fig. 2.3a shows the physical layout and electrical equivalent of a single section of the half-bridge IGBT power module. The vertical cross-section of each layer on a single section is depicted in Fig. 2.3b. The section design, layer thickness/composition and physical parameters are presented in [4].

2.2 Electrical Characteristics

Electrical parameters of a power module are governed by material types, circuit topology, and packaging of devices. These are essential parameters in order to drive and switch the device properly.

2.2.1 IGBT Structure

The vertical cross-section of a half cell of one of the parallel cells in an n-channel IGBT is shown in Fig. 2.4a [2]. The $p+$ layer at the bottom forms the

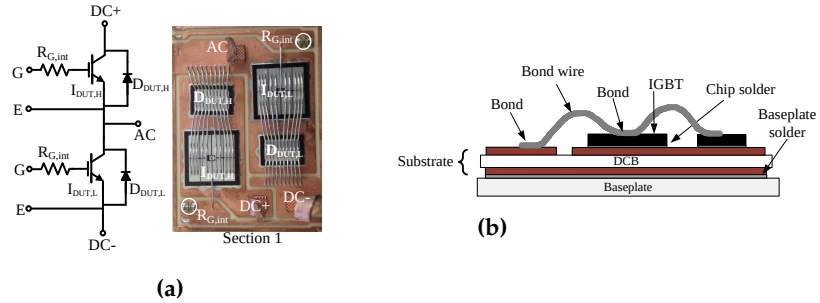
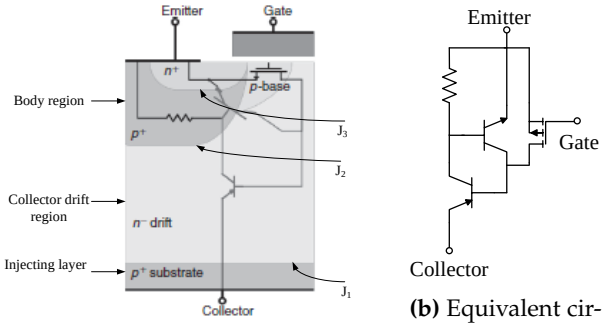


Fig. 2.3: Half bridge layout of IGBT module (a)Single section of half-bridge IGBT (2) vertical cross-sectional layer.

IGBT collector and a pn junction with $n-$ drift region, where conductivity modulation occurs by injecting minority carriers into the drain drift region of the vertical MOSFET. Therefore, the current density is much greater than a power MOSFET and the forward voltage drop is reduced. The $p+$ substrate, $n-$ drift layer, and $p+$ emitter constitute a BJT that cannot be forward biased, and therefore this transistor will not operate in saturation. But, when the potential drop across the inversion layer becomes comparable to the difference between the gate voltage and the threshold voltage, channel pinch-off occurs. The pinch-off limits the electron current and as a result the holes injected from the $p+$ layer. Therefore, base current saturation causes the collector current to saturate. If a positive potential is applied to the gate of the IGBT,



(a) IGBT structure.

(b) Equivalent circuit.

Fig. 2.4: Vertical cross section of IGBT structure and equivalent circuit (Adapted from [2]).

and exceeds the threshold voltage required to invert the MOS region under the gate, a conducting channel is formed and it changes over to forward conduction mode. Usually 15 V is used in such power modules. Similarly, if the gate emitter voltage is turned-off, the collector current is suddenly reduced,

because the electron from the channel is removed. Then, the excess carriers in the $n-$ drift region decay by electron-hole recombination, which causes a gradual collector current decay. In order to keep the on-state voltage drop low, the excess carrier lifetime must be large. Therefore, similar to the other minority carrier devices, there is a trade-off between on-state losses and faster turn-off switching times.

2.2.2 Static and Switching Characteristics

The power loss on an active component is governed by the temperature dependant conduction and switching characteristics of a device. Temperature dependent static (I-V) characteristics of IGBT and corresponding FWD are shown in Fig. 2.5, measured at V_{ge} on 15 V. Similarly, the IGBT performs

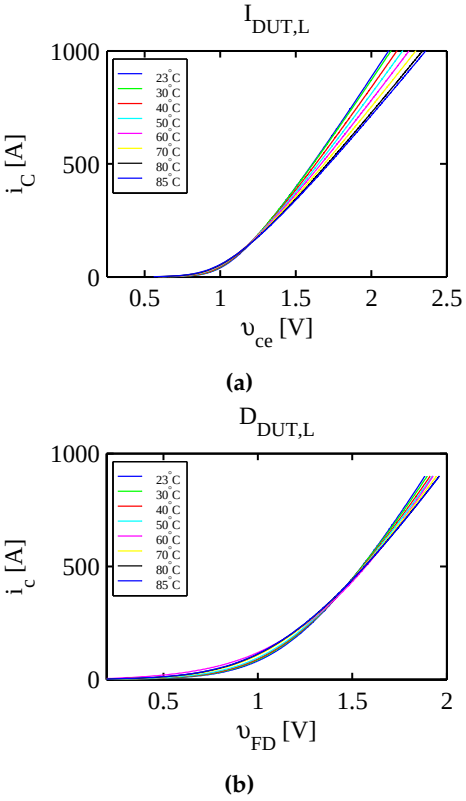
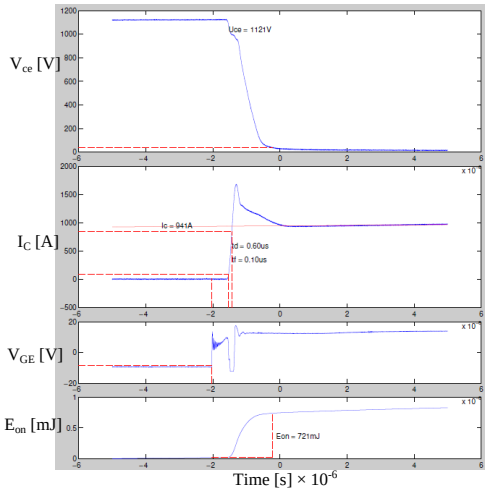
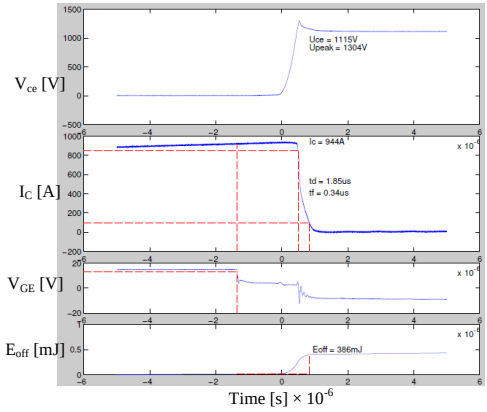


Fig. 2.5: Static IV characteristics of (a)IGBT and (b)FWD diode.

differently during turn-on and turn-off time as shown in Fig. 2.6.



(a)



(b)

Fig. 2.6: Switching characteristics of IGBT (a) during turn-on (b) during turn-off.

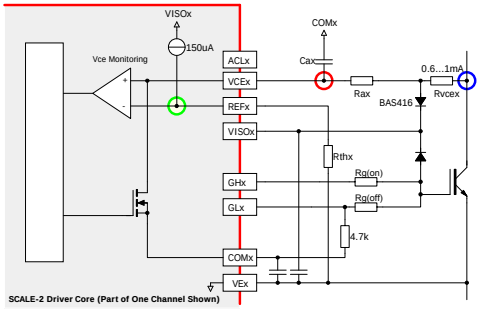
2.3 Gate Driving and Monitoring

Gate driving parameters are limited by current rise and fall times, turn-on delay, voltage and current overshoots, and parasitic components of the circuits. In general, an IGBT gate driver uses turn-on gate resistor $R_{g,on}$ during turn-on to limit maximum collector current, whereas turn-off gate resistor $R_{g,off}$ is used during turn-off to limit the maximum collector-emitter voltage [2].

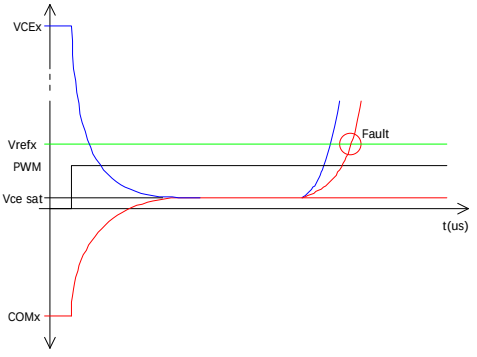
2.3.1 Gate Driving

The external gate capacitance is introduced only after V_{ge} reaches to $V_{ge,th}$ to reduce the initial delay required to reach the $V_{ge,th}$. Low gate impedance is needed to reduce the effect of noise on the gate. During off-state, negative gate voltage is used to prevent shoot through caused by transients during the on-period. The $R_{g,on}$ controls the collector current slope at the beginning and collector voltage slope during the miller effect, which ultimately determines the turn-on switching loss. However, selection of $R_{g,on}$ is a trade-off between a lower switching loss at smaller resistance or a lower EMI noises at higher resistance.

On the other hand, turn-off switching loss is governed by a tail current and a current slope, which mostly depends on the amount of stored charge and minority carrier lifetime. However, the turn-off loss can be reduced during the miller effect and MOS turn-off portion by reducing the $R_{g,off}$. But lowering $R_{g,off}$ increases the rate of change of collector voltage, which strongly affects the IGBT latching current and RBSOA.



(a) V_{ce} desaturation protection.



(b) V_{ce} desaturation.

Fig. 2.7: V_{ce} desaturation potection on IGBT with resistors(a)gate driver block diagram and (b)desaturation waveform, from [5].

2.3.2 Protection and Monitoring Parameters

Using a suitable control of V_{ge}, the IGBT has the ability to limit the current intrinsically under over-current and short circuit fault conditions. However, a fast response detection circuitry is required to limit the peak fault current, which reduces/turn-off V_{ge} during fault. Desaturation detection or collector voltage monitoring is one of the most common methods to detect the faults in an IGBT as shown in Fig. 2.7, where resistors are used to set the reference voltage.
During the turn-on and on-state period of an IGBT, the V_{ce} decreases, where C_{ax} is charged in Fig.2.7a from the COMx potential to the IGBT saturation voltage in Fig. 2.7b. The time required to charge Cax depends on the DC bus voltage, the value of the resistor Rax and the value of the capacitor Cax. The V_{refx} is set at typically around 7 V, which is valid in a short circuit condition for a minimum of DC link voltage of about 25 $V * Rvcex/Rax$. The response time will increase for lower DC link voltages. There are different methodologies introduced for desaturation monitoring [5].

2.4 Wear Out and Failures in Power Modules

In semiconductor devices, failure mechanisms are mainly differentiated as intrinsic and extrinsic [6]. The intrinsic failures are attributable to natural deterioration of materials, which is systematic in nature and shows wear out behaviour of materials. Whereas extrinsic failures are attributable to unintended defects or production deviations, which are random in nature and show early life failures and random failures. In power modules, several stressors cause intrinsic and extrinsic failures, however a final catastrophic failure can be a combination of many different processes [7]. This chapter focuses on thermo-mechanical induced failures in package interconnections, where an on-state electrical parameter shows an ageing effect in a long operation.

2.4.1 Selected Failure Mechanisms

Several mechanisms may cause an eventual device failure such as electromigration, cosmic rays, dielectric breakdown, corrosion etc. Fig. 2.8 shows a summary of the main sources of failures in IGBT power modules. Power modules suffer from fluctuating loads both with regards to environmental and electrical loadings. Both loadings are responsible for creating temperature oscillation inside a power module. The temperature cycle causes a thermo-mechanical loading due to material expansion and CTE mismatch. Both of these directly affect the module packaging and especially the interconnects: solder joints, bond wires, and metallization [7]. Fig. 2.9 shows a

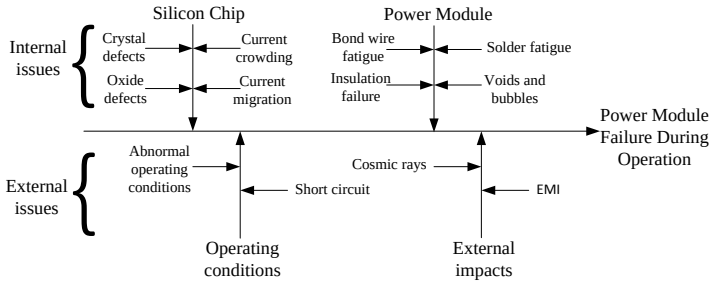


Fig. 2.8: Potential failure types in power modules insipred by [8].

vertical cross section of an IGBT geometry highlighting the weak region from A-TC.

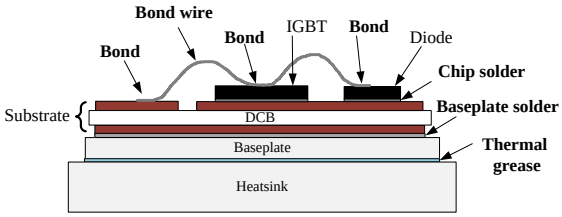


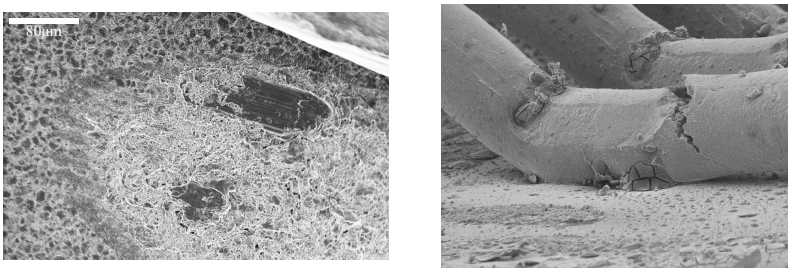
Fig. 2.9: Vertical cross section of a IGBT module geomtry highlighting weak interconnections.

Bond Wire Fatigue

Fundamentally, two major failure mechanisms heel cracking [9] and lift-off [10] are observed related to the bond wires or wire bonds, see Fig. 2.10. *Al* based bond wire has a relatively high CTE in comparison to copper and silicon which is together with stress induced by wire flexure, is the main stressor. An uneven wire length and wire bonding creates non-homogeneous current distribution causing additional stress on remaining wires [11]. After some cycles of operation, the degradation is increased in some wires, this is also observed as increase in on-state voltage [12]. Normally, the crack propagation path has been inside a wire itself, which is also observed as a significant amount of wire residue seen on top of the metallization after a wire lift-off,see Fig. 2.10a [13]. Details on bond wire fatigue are presented in chapter 7.

Metallization Reconstruction

A metallization layer is used to access electrical connection to all conducting channels of a semiconductor chip. The reconstruction seen on the metalliza-

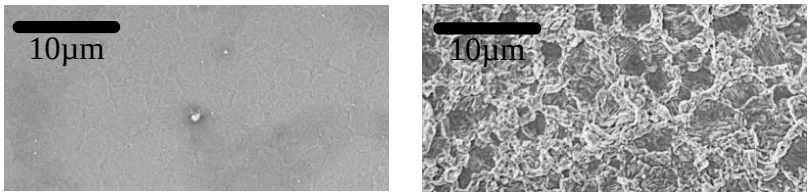


(a) **(b)**

Fig. 2.10: SEM Images for bond wire fatigue (a) bond wire lift off for A-TC module and (b) bond wire heel cracking, from [14]

.

tion, see Fig.2.11, is a well-known degradation process induced by the combined thermal induced stress which over time causes fatigue [7] and stress migration in the form of diffusion of Al along grain boundaries onto the surface [15]. Reconstruction occurs mainly due to mismatch of the CTE between Al metallization and the Si chip. The problem is the relatively low elastic limit of Al combined with the difference in CTE. The plastic deformation, such as sliding of grain boundaries and dislocations, occurs causing so-called reconstruction. Reconstruction affects the forward voltage of the section, if the metallization is losing contact to channels, becoming thinner, or causing the delamination or lift-off. The metallization mostly changes in the topmost 1-3 μm Al layer. Sometimes the reconstruction propagates down to the surface of the semiconductor chip through the entire metallization layer [11]. An increased degree of degradation is observed at the center of the chip compared to edges in the test which are discussed in chapter 7.

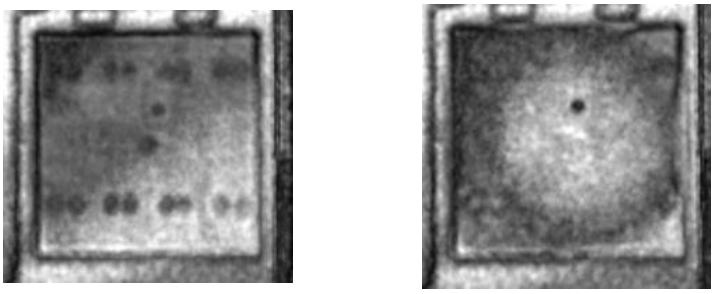


(a) Metallization of a new LS diode. **(b)** Metallization of a A-TC diode.

Fig. 2.11: SEM images of the metallization surface of (a) new low side diode and (b)A-TC diode after 3.5 million cycles of operation.

Solder Fatigue

Solder is used to attach a *Si* chip onto the DCB and DCB onto the baseplate. Solder layers experience significant temperature variation in converter operation, being the primary thermal path from the chip to the baseplate. The stress induced during temperature fluctuations causes crack formation in solders as shown in Fig. 2.12. Mainly, cracks are initiated from the solder edge, voids and impurities [7]. Especially in traction application the solder joints of DCB-substrates to the copper baseplate are a limiting factor [16]. *AlSiC* based baseplate was introduced to extend the lifetime of the solder joint to prevent the large mismatch of thermal expansion at all solder joints to improve reliability [17], [16].



(a) Unstressed solder layer.

(b) Stressed solder layer.

Fig. 2.12: A comparison of unstressed and stressed lead-free ship solder layer, from [18]).

2.5 Wear Out and Lifetime Investigation

Several factors affect power electronics reliability: electrical load, environmental (temperature, humidity), mechanical vibrations, etc. The stress levels are dependent on type and location of applications. For wear out and lifetime investigation of power modules, very severe test conditions are considered to ensure robustness and reliability for a given application within a limited time frame. Hence, severe stresses are generated under test methods, mainly based on A-TC and P-TC. Although increased stress levels under accelerated test conditions may induce unwanted failure modes.

On-state collector-emitter voltage, thermal resistance, and gate threshold voltage are used to define failure criteria under these tests, however the failure criteria are reported differently [19]. The rise in on-state voltage by 5% up to 20%, the rise in thermal resistance by 10% up to 20%, and the rise in gate threshold voltage by 10.5% are considered as failure criteria.

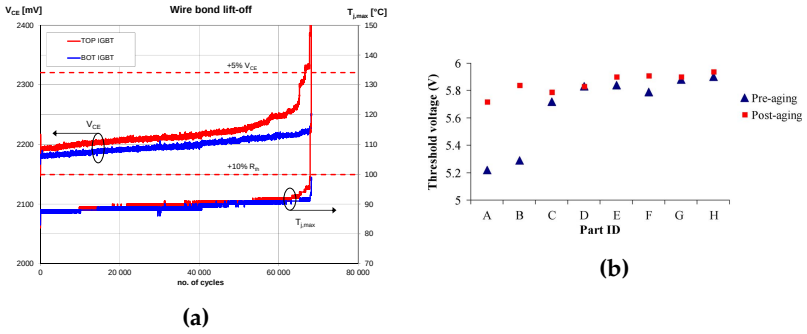


Fig. 2.13: Failure criteria and evolution on v_{ce}, R_{th}, $and V_{ge,th}$ [20] (a) v_{ce} and $T_{j,max}$ on a power cycling and (b)gate-emitter threshold variation with ageing.

2.5.1 Lifetime Investigation

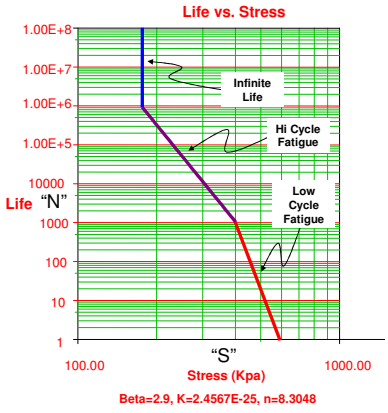
Empirical lifetime models based on thermal or power cycling tests are mainly based on Coffin- Manson only and Coffin-Manson including Arrhenius models [21]. Over the time period, contribution from other factors are taken into account such as frequency in the Norris-Landzberg model [22], [23] geometrical inputs like the Bayerer model [24], and the model including design and interface [7], [25].

Mathematical representations of such models are used to correlate physical changes of the device, which requires a detailed understanding of failure mechanisms. Such tests are carried out by A-TC/P-TC to obtain parameters for lifetime modelling, which is often selected for specific failure modes as a function of loading profile, geometry, material properties of power module, etc. [4]. It is unrealistic to build or simulate a test setup which can duplicate field conditions and run for the actual lifetime of a power module. Similarly, to build a model covering all failure modes is very complex, and may not be accurate. Hence, most lifetime models are based on the weakest parts such as: bond wire related fatigue and solder-layer related fatigue. Since the power module wear out process is complex with multiple physical processes, it is difficult to create an universal model applicable to various failure mechanisms [26]. An online wear-out process including loading profile monitoring technique is required to include real-time updated physical degradation into a model.

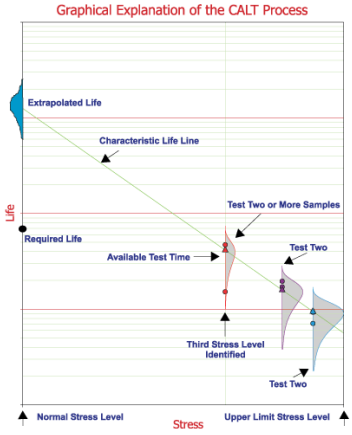
2.5.2 Reliability Test Data Analysis

In power semiconductors, acceleration models are developed based on major stressors such as temperature, voltage, current, humidity, and stress [27], [28], [29], [30]. In order to conduct a reliability test, first an appropriate failure mode need to be defined. The empirical acceleration models use em-

pirical constant values which have limited accuracy because their empirical equations are based on generic data [31]. In ALT, higher stress level is used, however below the upper limit to determine failure modes and also to estimate a product lifetime. Recently, CALT is proposed to reduce test time and sample size in ALT process. Using CALT, the life-stress relationship can be established at each stress level based on the characteristics of distribution at each accelerated stress level as described in Fig. 2.14. Then, appropriate sta-

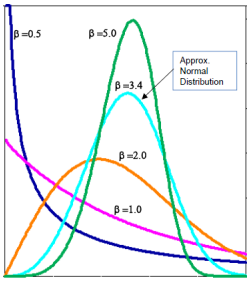


(a) S-N curve (Life as function of stress) [32].

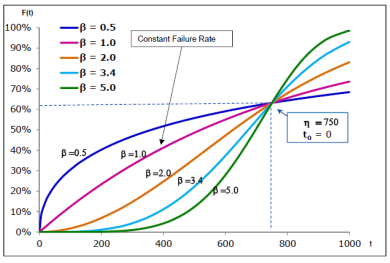


(b) CALT process illustration, taken from [33].

Fig. 2.14: Illustration of life-stress curve and CALT process.



(a) Probability density function (pdf).



(b) Cumulative failure plot (linear-linear).

Fig. 2.15: Influence of shape (β) parameter on Weibull distribution (a)Probability density function (pdf) and (b)cumulative failure plot, from [34].

tistical distribution can be selected. The Weibull distribution is a commonly used method for statistical analysis of the reliability test results. A main advantage of this method is that it doesn't require a large quantity of data. The

Weibull distribution and parameters are illustrated in Eq. (2.1).

$$F = 1 - exp\left[-\left(\frac{t - t_o}{\eta - t_o}\right)^{\beta}\right] \tag{2.1}$$

Where, F is probability of failure, t is test statistics such as number of cycles/time, η is characteristic life at $F = 63.2\%$, t_o minimum life without failure, and β is a shape parameter, see Fig. 2.15.
The Weibull parameters are obtained using median rank. The median rank is a non-parametric estimate of the cumulative distribution function based on ordered failures [35]. The median rank (x_i) is the value that the true probability of failure should have at the i^{th} failure for n samples at 50% confidence level, as given in Eq. (2.2).

$$x_i = \frac{i - 0.3}{n + 0.4} \tag{2.2}$$

Where, i is the failure order according to their lifetime and n is the total number of data points, both censored and uncensored.

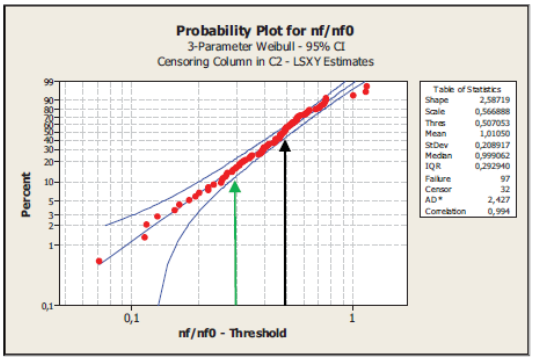


Fig. 2.16: The 3-paraemter Weibull analysis of the test data. The arroe mark the model prediction (black) and the prediction with a margin factor of 80% (green), from [36].

2.5.3 Fusion Prognostic Approach

Recently, a fusion approach to the prognostic method is proposed suitable for remaining useful life (RUL) estimation based on real time health-state monitoring, POF based models and data driven models. An accurate real time monitoring of the state parameter is essential in a such method, where anomaly detection is conducted from online monitoring. Fig. 2.17 shows a block diagram for a fusion prognostic approach.

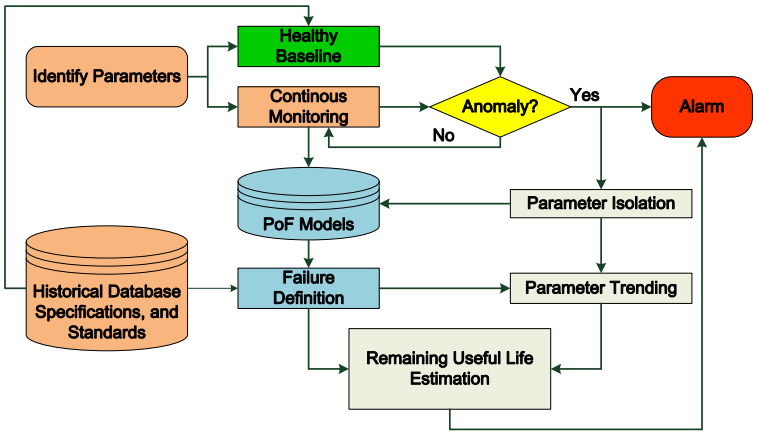


Fig. 2.17: Prognostic fusion approach for semiconductor devices, from [37].

References

[1] J. Lutz, H. Schlangenotto, U. Scheuermann, and R.W. De Doncker. *Semiconductor power devices*. Springer, 2011.

[2] Muhammad H. Rashid, editor. *Power Electronics Handbook (Devices, Circuits, and Applications)*. Elsevier Inc., third edition, 2011.

[3] A. Volke and M. Hormkamp. *IGBT Modules - Technologies, Driver and Applications*. Infineon Technologies AG, second edition, 2012.

[4] Kristian Bonderup Pedersen. *IGBT Module and Reliabilty (Physics of Failure Based Characterization and Modelling)*. PhD thesis, Aalborg University, December 2014.

[5] An 1101 application note application with scale - 2 gate driver cores, 2013.

[6] How to measure lifetime for robustness validation - step by step, zvei - german electrical and electronics manufacturers' association e.v., 2012.

[7] Mauro Ciappa. Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, 42:653 – 667, 2002.

[8] N. Y.A. Shammas. Present problems of power module packaging technology. *Microelectronics Reliability*, 43(4):519–527, April 2003.

[9] Y. Celnikier, L. Benabou, L. Dupont, and G. Coquery. Investigation of the heel crack mechanism in al connections for power electronics modules. *Microelectronics Reliability*, 51(5):965 – 974, 2011.

[10] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani. Ageing and failure modes of igbt modules in high-temperature power cycling. *IEEE Transactions on Industrial Electronics*, 58(10):4931–4941, Oct. 2011.

[11] Kristian Bonderup Pedersen, Lotter Haxen Ostergaard, Pramod Ghimire, Vladimir Popok, and Kjeld Pedersen. Degradation mapping in high power

igbt modules using four-point probing. *Microelectronics Reliability*, 2015. doi:10.1016/j.microrel.2015.05.011.

[12] Pramod Ghimire, Kristian Bonderup Pedersen, Bjorn Rannestad, and Stig Munk-Nielsen. Ageing monitoring in igbt module under sinusoidal loading. *Microelectronic Reliability*, 55(9-10):1945–1949, August- September 2015. doi:10.1016/j.microrel.2015.06.025.

[13] I. Lum, M. Mayer, and Y. Zhou. Footprint study of ultrasonic wedge-bonding with aluminum wire on copper substrate. *Journal of Electronic Materials*, 35(3), 2006.

[14] Raed Amro. *Power cycling capability of advanced packaging and interconnection technologies at high temperature swings*. PhD thesis, Electrical Engineering and Information Technology, Chemnitz University of Technology, 2006.

[15] H. Gao, L. Zhang, W.D. Nix, C.V. Thompson, and E. Arzt. Crack-like grain-boundary diffusion wedges in thin metal films. *Acta Materialia*, 47(10), 1999.

[16] Karsten Guth and Peter Mahnke. In *4th International Conference on Integrated Power System (CIPS)*, pages 1–6, June 2006.

[17] T. Schutze, H. Berg, and M. Hierholzer. Further improvements in the reliability of igbt modules. In *IEEE Industry Applications Conference*, volume 2, pages 1022–1025, Oct 1998.

[18] T. Herrmann, M. Feller, J. Lutz, R. Bayerer, and T. Licht. Power cycling induced failure mechanisms in solder layers. In *European Conference on Power Electronics and Applications*, pages 1–7, Sept 2007.

[19] P. Ghimire, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, and P.B. Thogersen. A review on real time physical measurement techniques and their attempt to predict wear-out status of igbt. In *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pages 1–10, Sept. 2013.

[20] Ralf Schmidt, Felix Zeyss, and Uwe Scheuermann. Impact of absolute junction temperature on power cycling lifetime. *15th European Conference on Power Electronics and Applications (EPE)*, pages 1–10, 2013.

[21] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech. Fast power cycling test of igbt modules in traction application. *Proc. of International Conference on Power Electronics and Drive Systems*, 1:425–430, May 1997.

[22] k. C. Norris and A. H. Landzberg. Reliabilty of controlled collapse interconnections. *IBM Journal of Research and Development*, 13(3):266–271, 1969.

[23] Kuan-Jung Chung, LiYu Yang, Bing-Yu Wang, and Chia-Che Wu. The investigation of modified norris-landzberg acceleration models for reliability assessment of ball grid array packages. In *5th International Microsystems Packaging Assembly and Circuits Technology Conference (IMPACT)*, pages 1–4, Oct 2010.

[24] Reinhold Bayerer, Tobias Herrmann, Thomas Licht, Josef Lutz, and Marco Feller. Model for power cycling lifetime of igbt modules- various factors influencing lifetime. In *Proc. of 5th International Conference on Integrated Power Systems (CIPS)*, pages 1–6, March 2008.

[25] K.B. Pedersen and K. Pedersen. Dynamic electro-thermo-mechanical simulation of material degradation in high power igbt modules. *IEEE Transactions on Power Electronics*, (99), 2015. DOI: 10.1109/TPEL.2015.2426013.

[26] George Vachtsevanos, Frank L. Lewis, Michael Roemer, Andrew Hess, and Biging Wu. *Intelligent Fault Daignosis and Prognosis for Engineering Systems*. John Wiley & Sons, Inc., 2006.

[27] Failure mechanisms and model for semiconductor devices (jep122f), jedec, Oct 2011.

[28] Eyring. Technical report, National Institute of Standards and Technology, Online Handbook, section 8.1.5.2, 2006.

[29] Peck D.Stewart. Comprehensive model for humidity testing correlation. In *24th Annual Reliability Physics Symposium*, pages 44–50, April 1986.

[30] Richard Bliash and Noel Durrant. Semiconductor device reliability failure models. Technical report, International SEMATECH, May 2000.

[31] Patrick D. T. O'Connor and Andre Kleyner. *Practical Reliability Engineering*. John Wiley and Sons, Ltd, 5 edition, 2012.

[32] Larry Edson. *The GMW3172 Users Guide (Electrical Component Testing)*. General Motors Corporation, 2008.

[33] John J. Paschkewitz. Calibrated accelerated life testing (calt) with time varying stress profiles. *Reliability Edge*, 2015.

[34] Peter de Place Rimmen. Reliability (conceptual day for reliability, corpe). Technical report, Danfoss Power Electronics A/S, 2012.

[35] Bryan Dodson. *The Weibull Analysis Handbook*. ASQ Quality Press, 2006.

[36] U. Scheuermann and R. Schmidt. Impact of load pulse duration on power cycling lifetime of al wire bonds. *Microelectronics Reliability*, 53(9-11):1687 – 1691, 2013.

[37] Shunfeng Cheng and M. Pecht. A fusion prognostics method for remaining useful life prediction of electronic products. In *IEEE International Conference on Automation Science and Engineering*, pages 102–107, August 2009.

Chapter 3

Field Emulated Testing and Charaterization Technique

3.1 Test methods for Power Module

Design lifetime capability of power modules is attributed to power cycling capability. Normally, two types of accelerated tests are used: A-TC and P-TC. A-TC is a common approach for evaluating design and performance under a given loading, as well as end of life tests at accelerated conditions [1], [2], [3], [4], [5]. In an A-TC setup, the DUT is normally heated through sheer conduction losses. However, in order to get test condition is closer related to real world stresses, the DUT in this setup is handled as an active component and switched under normal operation conditions. Accordingly, switching losses constitute a significant part of the total power loss. The proposed test method is categorised as an advanced A-TC method (which is also demonstrated in Fig. 3.1a). Conventional A-TC is carried out mainly to study degradation of bond wires and solder joints under a pulsating current.

3.1.1 Experimental Test Setup

The setup consists of the DUT and a control side (CTRL), where the latter is split into two separate legs of two devices in order to ensure the DUT fails first. A block diagram of the setup is shown in Fig. 3.2a and a picture of the physical setup in Fig. 3.2b. The benefit of this setup is that while large magnitudes of power are circulated by the switches only losses of the system are to be supplied.

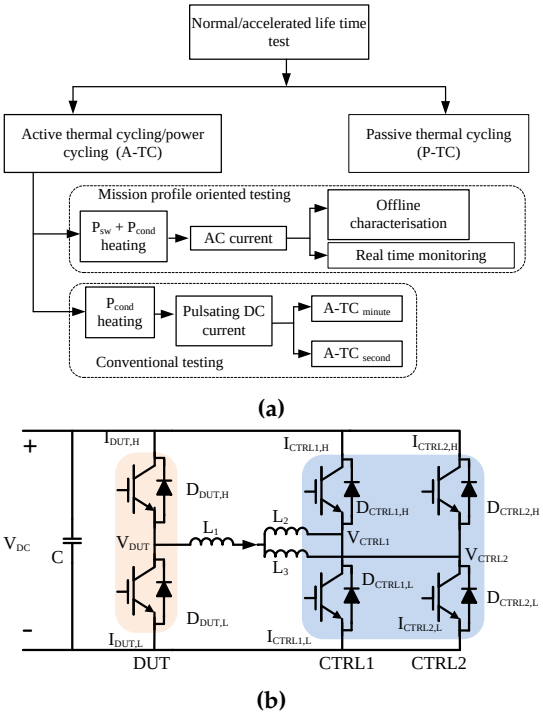
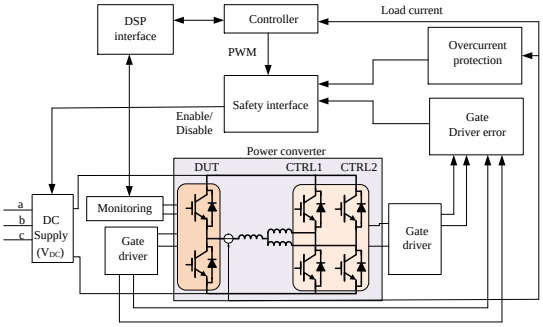


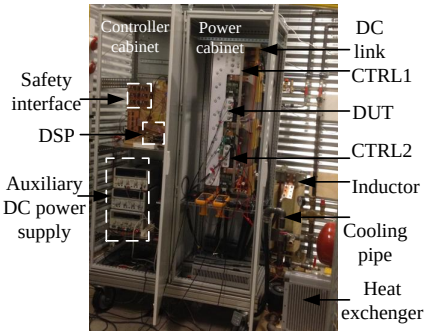
Fig. 3.1: Cycling of power modules (a)overview of methods (b) power converter for cycling of power modules.

3.1.2 Power Converter

A circuit diagram of the power converter is shown in Fig. 3.1b. Phase and magnitude of the two voltage sources V_{DUT} and V_{CTRL} are controlled by duty cycling each leg. The DUT leg is using an open loop space vector modulated (SVM) voltage (V_{DUT}), while the control side of the converter has a closed loop control in order to force sinusoidal current through the devices. In this measurement, the phase displacement (ϕ) of V_{DUT} to i_L is kept at 2.7 *Rad*. However, this can be chosen according to the need. By changing ϕ, the generating or drive mode of each leg can be controlled. Here, the DUT is operated at generating mode, where the diodes are more stressed, whereas on the control side IGBT's are more stressed. The equivalent inductance is given by Eq. (3.1). The parallel legs of the control side share similar current at the identical switching action, hence the voltages V_{CTRL1} and V_{CTRL2} are equal in phase and magnitude. For optimal cooling conditions a Danfoss Shower-Power is used by circulating a mixture of water and glycol [6]. The cooling temperature ($T_{cooling}$) is controlled by regulating heat dissipation through a



(a) Block diagram.



(b) Test setup.

Fig. 3.2: Experimental test setup (a) block diagram layout (b) picture of the test setup for field-oriented testing.

heat exchanger using PI control.

$$L_{eqv} = L_1 + \frac{1}{2}(L_2 + L_3), \tag{3.1}$$

Where, L_{eqv} is an equivalent inductor including series inductor L_1 and two similar magnitude current sharing inductors L_2 and L_3 in the converter.

3.2 Field Emulating Stressors on DUT

In the present setup, the primary operating parameters modulated to control the test conditions are the current amplitude (i_L), fundamental frequency (F_{out}), and cooling temperature ($T_{cooling}$). The primary effect controlled through i_L and F_{out} is the change in the junction temperature (ΔT). However, for increasing ΔT, this also affects the temperature gradient observed across the power module. $T_{cooling}$ is primarily controlled to increase the electrical and thermal resistance of the power module and thereby increasing the effect of

the current amplitude on the switching loss.

IGBT and diode chips are the primary contributors to the total power loss in the module. The total electrical power loss (P_{tot}) is comprised of conduction (P_{cond}), switching (P_{sw}), and gate losses (P_{gate}), where the latter normally can be neglected, see Eq. (3.2).

$$\begin{aligned} P_{tot} &= P_{cond} + P_{sw} + P_{gate}, \\ &\approx P_{cond} + P_{sw}, \end{aligned} \tag{3.2}$$

In this example, conduction losses include all forward losses during steady state which affects all current carrying components of the module (Cu, wires, chips, and solders). As illustrated in Eqs. (3.3) and (3.4), the power dissipation in the semiconductor chips during conduction depends on the on-state period (t_{on}), on-state (v_{ce}), and the load current (i_c).

$$P_{cond,I} = \frac{1}{t_{out}} \int_0^{t_{on}} v_{ce}(t) i_c(t) dt, \tag{3.3}$$

$$P_{cond,D} = \frac{1}{t_{out}} \int_0^{t_{on}} v_{FD}(t) i_c(t) dt, \tag{3.4}$$

Switching losses include the energy required to turn on and off the semiconductor components. For the diode this is limited to recovery loss, see Eq. (3.5). In Eq. (3.6) the IGBT switching loss is presented.

$$P_{rec,D} = F_{sw} E_{rec} \left(\frac{V_{DC}}{V_{ref}} \right)^{K_{v,D}}, \tag{3.5}$$

$$P_{sw,I} = F_{sw} E_{sw} \frac{i_c}{I_{ref}} \left(\frac{V_{DC}}{V_{ref}} \right)^{K_{v,I}}, \tag{3.6}$$

Where, I_{ref} and V_{ref} are the current and voltage at the manufacturer specified switching loss E_{sw} and recovery loss E_{rec}.

As illustrated in the power loss relation in Eqs. (3.2)-(3.6), the stress can be controlled through the load current, DC-link voltage, switching frequency, fundamental frequency and modulation index. The latter controls the stress between the IGBT and the diode. Fig. 2.9 shows a vertical cross section of the geometry showing the layers constituting the IGBT module. Similarly, a layout of a single section of an open DUT is depicted in Fig. 2.3a.

3.3 Characterization of a Power Modules

Manufacturer provide typical characteristics of power modules, which does not necessarily match with all devices even in the same batch of production.

Especially, the static characteristics of a power module at initial phase and during test/run give health status as well as shift in state parameters during the ageing process. The static characteristics are measured offline. Similarly, the state parameters are also measured online (during normal converter operation), the shift in parameter due to the ageing process can be deduced from these measurements. Here, the wear out is monitored using three strategies: real time in normal converter operation, offline and recalibration when converter is in an off-state.

3.3.1 Measurement in Normal Operation

On-state v_{ce}, v_{FD} and the corresponding i_L are measured at the center of a PWM pulse in converter operation. Hence the measurement is not affected by the transients in settling time required by the circuit and packaging of the module [7]. In addition, this technique also makes the implementation into the converter control simple. The measurement routine is illustrated in [7], where the online measurement is routined at every 5 min of operation to reduce the amount of data. During one measurement, the on-state v_{ce}, i_C and corresponding $T_{cooling}$ are sampled and recorded for 2.5 cycles. The measurements of current, corresponding v_{ce}, and v_{FD} for one cycle are shown in Fig. 3.3.

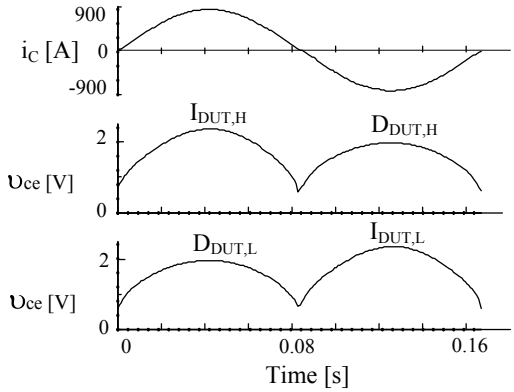
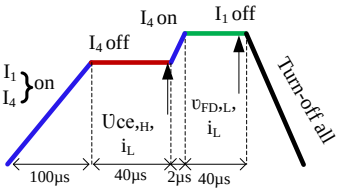


Fig. 3.3: Real time monitoring of on-state v_{ce} and i_C for one cycle.

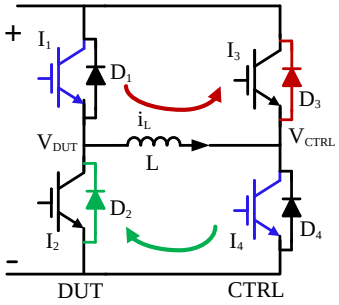
3.3.2 Offline Characterization

Offline characterization produces forward characteristics of all IGBT's and diodes in a power module. Two approaches could be used for characterization: current-ramp method and current-plateau method. The characterizing process of devices are completed in μS time frames in order to minimize or

eliminate the effect of self-heating at load current, see Figs. 3.4a and 3.5a.



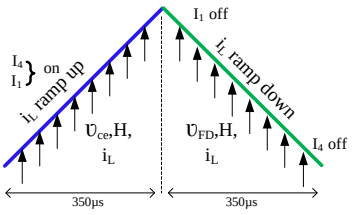
(a) Current waveform in a current-plateau method.



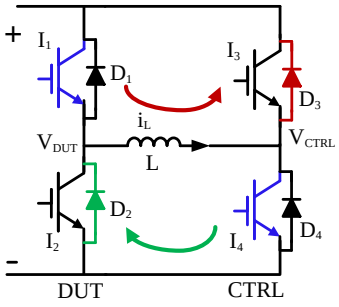
(b) Converter switching sequence in a current-plateau method.

Fig. 3.4: A current-plateau method to characterize power modules in a converter.

Fig. 3.4 shows a current-plateau method for characterization of each component of a power module in converter, see Figs. 3.4a and 3.4b. Similarly, Fig. 3.5 shows a current-ramp method for characterization of each component of a power module in converter, see Figs. 3.5a and 3.5b.



(a) Current waveform in a current-ramp method.



(b) Converter switching sequence in a current-ramp method.

Fig. 3.5: A current-ramp method to characterize power modules in a converter.

In offline characterization, the power dissipation occurs mainly due to conduction losses which are limited by shortening the on-state period. The I_1/D_2 and I_2/D_2 pairs are conducting in DUT, when the current is positive and negative, respectively. The measured v_{ce} is a function of current, gate voltage (V_{GE}), and chip temperature. To study the change in v_{ce} due to ageing, V_{GE} is kept constant at 15 V and the $T_{cooling}$ is maintained steady at 80°C.

Table 3.1: THE I-V CHARACTERIZATION STRATEGIES

1. Current-ramp method	
v_{ce} and i_L	Active components
v_{ce} at I_1, i_L	I_1 is ON, I_4 is ON (Current ramp) I_4 is OFF
v_{FD} at D_1, i_L	I_3 is ON, I_2 is ON (Current ramp) I_3 is OFF
v_{ce} at I_2, i_L	I_2 is ON, I_3 is ON (Current ramp) I_3 is OFF
v_{FD} at D_2, i_L	I_4 is ON, I_1 is ON (Current ramp) I_1 is OFF I_2 is OFF
2. Current-plateau method	
v_{ce} at I_1, Ic	I_1 is ON, I_4 is ON (Current ramp) I_4 is OFF(Plateau)
v_{FD} at D_1, I_c	I_4 is ON, (Second current ramp) I_1 is OFF (Plateau)
v_{ce} at I_2, Ic	I_2 is ON, I_3 is ON (Current ramp) I_3 is OFF(Plateau)
v_{FD} at D_2, I_c	I_3 is ON, (Second current ramp) I_2 is OFF (Plateau)

The conduction time is in microseconds, hence v_{ce} is mainly a function of applied current. Table 3.1 shows the switching sequences for characterization of IGBT modules in converter.

3.4 Post-Mortem Test Analysis

After the wear out test, the power modules are subjected to a post-mortem process for a physics of failure analysis. Two major approaches are used: four-point probe measurement and micro-sectioning.

3.4.1 Four-Point-Probe Method

Four-point-probing is a commonly used technique for measuring electrical properties of semiconductor devices, as well as fracturing or degradation in various conducting structures [8], [9]. The concept is based on having two current carrying terminals attached to the sample while placing two probes in between for measuring the potential difference across the region of interest.

This technique is used for electrical measurements on individual semiconductor chips, and interconnections: bond wires, solders, and metallizations in power cycled and fresh modules. This process allows assessment of degradation type and distribution through different components as a function of stress and time.

3.4.2 Microscopy Based Investigations

Electro-thermal degradation of interconnections is investigated using different microscopy based methods. Metallization reconstruction is characterized using a Zeiss 1540 XB SEM/FIB. The wire/chip interfaces are studied using a micro-sectioning approach combined with optical microscopy. By investigating the microscopical structure the information regarding quality as well as lifetime may be obtained. In this work, the quality of wire interfaces are investigated for A-TC modules.

References

[1] P. Cova and F. Fantini, "On the effect of power cycling stress on igbt modules," *Microelectronics Reliability*, vol. 38, no. 6-8, pp. 1347–1352, June-August 1991.

[2] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of igbt modules in traction application," *Proc. of International Conference on Power Electronics and Drive Systems*, vol. 1, pp. 425–430, May 1997.

[3] A. Morozumi, K. Yamada, T. Miyasaka, and Y. Seki, "Reliability of power cycling for igbt power semiconductor modules," in *Proc. of Industry Applications Conference*, vol. 3, Sept 2001, pp. 1912–1918.

[4] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, pp. 653 – 667, 2002.

[5] U. Scheuermann, "Reliability challenges of automotive power electronics," *Microelectronics Reliability*, vol. 49, pp. 1319 –1325, 2009.

[6] K. Olesen, R. Bredtmann, and R. Eisele, "Shower power new cooling concept for automotive applications," in *Automotive Power Electronics*, June 2006.

[7] P. Ghimire, A. de Vega, S. Beczkowski, S. S.Munk-Nielsen, B. Rannestad, and P. B. Thgersen, "Improving power converter reliability: Online monitoring of high-power igbt modules," *IEEE Industrial Electronics Magazine*, vol. 8, no. 3, pp. 40–50, Sept 2014.

[8] L. Valdes, "Resistivity measurements on germanium for transistors," in *Proceedings for the IRE*, 1954, pp. 420–427.

[9] K. Pedersen, P. Kristensen, V. Popok, and K. Pedersen, "Degradation assessment in igbt modules using four-point probing approach," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2405–2412, may 2015.

Chapter 4

Monitoring On-State Electrical Parameters

4.1 On-state Electrical Parameters

On-state $v_{ce,on}$ is mainly influenced by intrinsic parameters such as device structure, materials and doping level, and extrinsic parameters such as gate emitter voltage V_{GE} , I_c and T. Effectively, the total v_{ce} drop across a conducting IGBT chip is contributed by three dominant behaviours itemized as follows.

- The voltage drop across J_1, see Fig. 2.4a, follows the exponential law of a pn junction.
- The drain drift resistance, which is considerably lower compared to a MOSFET due to strong conductivity modulation by the injected minority carriers from the collector.
- Channel resistance.

While in modules, the additional voltage drop appears from packaging such as bond wires, cu layers, metallization, etc. On top of this, the effective resistance will be higher during switching, because of temperature gradients in layers and in series components.

The $v_{ce,on}$ is a dominating parameter for detecting the degradation of power modules. The $v_{ce,on}$ is influenced by all electrical and thermal effects at all times but not necessarily at the same level, as outlined in Fig. 4.1. The former could be due to degradation of interconnections (wire bond, solder, metallization) or semiconductor chips, where the latter is primarily due to thermal resistance. Several methods are proposed to measure $v_{ce,on}$, when

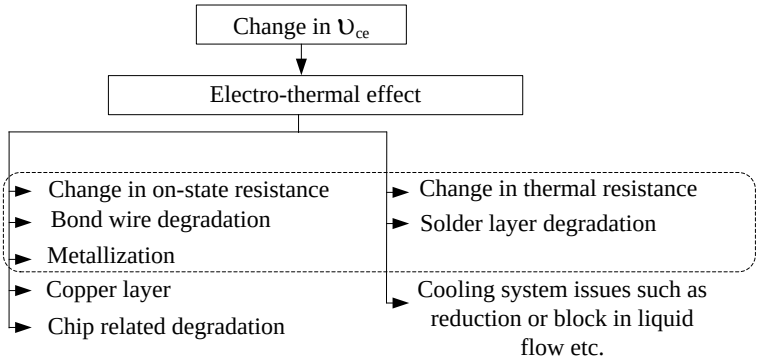


Fig. 4.1: Diagram illustrating how degradation affect the collector emitter voltage of a power module.

the converter is active and is in an off-state [1]. However, most of them are confined to a laboratory test only. An online $v_{ce,on}$ monitoring method [2], [3] is suitable, which is also similar in technique, known as desaturation protection in modern IGBT gate drivers. However the desaturation protection is different in nature and in desaturation the voltage across the IGBT may get very high.

4.2 Real Time Monitoring of On-State Voltage

Primarily, online monitoring of $v_{ce,on}$ topology should fulfil the following criteria when the converter is active.

- Voltage blocking capability: The voltage blocking components should withstand module rated collector-emitter voltage level.
- Voltage insulation: Minimum physical (clearance and creepage) distance requirement as defined on standard IEC60950-1, UL60950-1.
- Self-protection capability: Protect low voltage/current components in measurement circuit from high di/dt and dV/dt that originated during switching of the device.
- Isolate circuit during fault (avoid fusing): Self islanding capability if fault occurs in the measurement unit.
- Rugged on temperature fluctuation: No/minimize error in the voltage measurement due to change in the ambient temperature.
- Less offset voltage: Minimal offset in the measurement from amplifiers to improve accuracy of the measurement.

- Low impedance: Measurement circuit should not influence the gate switching performance such as oscillations in the gate signal.

4.2.1 Circuit Principle

The $v_{ce,on}$ measurement circuit uses a similar technique known as desaturation protection, as explained in chapter 1. Fig. 4.2a shows the basic principle

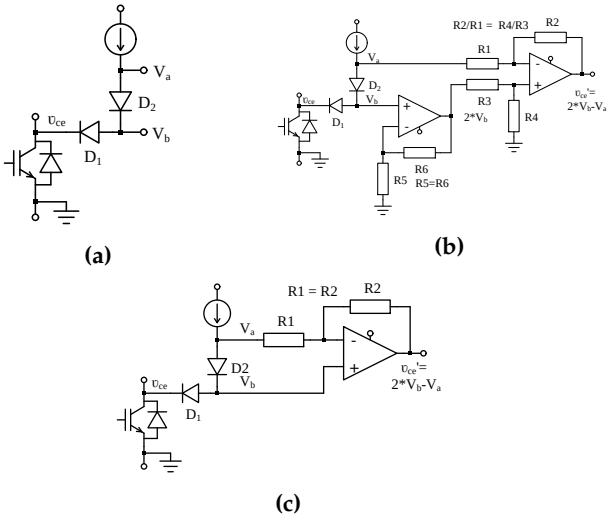


Fig. 4.2: The on-state collector-emitter voltage measurement circuit (a) basic measurement circuit, (b) $v_{ce,on}$ calculation using differential amplifier, and (c) simplified measurement circuit with gain equal to one.

of v_{ce} measurement circuit operation. Two diodes are connected in series and a current source forward-biases them during the transistor on-time. When the transistor is off, the D_1 is blocking the v_{ce} voltage, protecting the measurement circuitry from damage. An additional low-leakage diode anti parallel to diode D_2, is required so that only D_1 blocks the high voltage. Assuming the two diodes are identical ($V_{D_1} = V_{D_2}$), the v_{ce} may be measured by subtracting the voltage drop on diode D_2 from the V_b.

$$v_{ce} = V_b - V_{D_2} = V_b - (V_a - V_b) = 2V_b - V_a, \tag{4.1}$$

Mathematical Eq. 4.1 is realized using a circuit as shown in Fig. 4.2b. First, the V_b is amplified with a gain of two. A differential amplifier subtracts the V_a from the $2V_b$. In this circuit, there is a possibility of changing the gain of the differential amplifier to fully utilize the ADC voltage range. If the gain of the amplifier is set to one, then the $R3$ and $R4$ resistors form a voltage divider with a ratio of 0.5. Because of this, the voltage on the non-inverting

pin of the operational amplifier is equal to V_b, therefore the circuit can be simplified to the form as shown in Fig. 4.2c. The output voltage of the amplifier is tracking the v_{ce}. If the amplifier is supplied with the bipolar voltage, the circuit will operate for both positive and negative voltage, therefore, the FWD voltage can also be measured.

4.2.2 Selection of Diodes

In order to meet the desired specifications for the measurement, two diodes: D_1 and D_2 need to meet the following criteria:

- The current through the diodes should be equal. Connecting diode's common terminals to high impedance input of the amplifier fulfil this condition.
- The diodes should be thermally coupled to keep the junction temperatures at a similar level.
- The two diodes still need to have similar forward voltage temperature coefficients.

Two BY203 2 kV diodes were chosen due to a low reverse recovery and a high blocking voltage. The I-V characteristics of two randomly chosen diodes were compared. Their I-V characteristics were compared at a range of ambient temperatures. Fig. 4.3 demonstrates the difference in forward voltage dependency to the measured current. Based on these results 10 mA test current is chosen, where it exhibits similar dependencies with the temperatures, see [2].

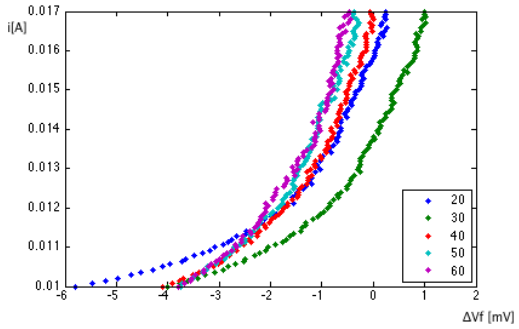


Fig. 4.3: Voltage difference between two measurement diodes at various ambient tempertaures.

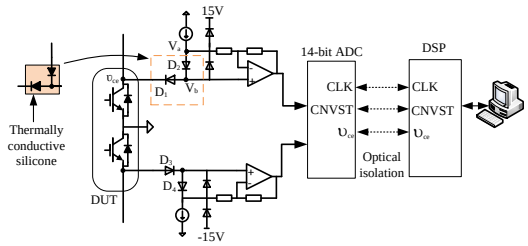


Fig. 4.4: v_{ce} measurement circuit.

4.2.3 A Full Measurement Circuit

The measurement circuit has been designed to achieve accuracy approximately 1 mV. A ± 5 V, 14-bit ADC with resolution of 0.61 mV has been chosen. Analogue circuitry has been designed so that ageing and temperature effects will be lower than $1/2$ of the LSB. A MAX9633 amplifier has been chosen so that the v_{ce} temperature variation and the settling time are satisfied. A MAX5490 100 K precision voltage divider has been used to assure thermal and time stability. Adding a 25 $k\Omega$ series resistor on the non-inverting input compensates the amplifier's bias current. The ADC works with an external voltage reference REF5025 capable of maintaining half-bit accuracy within the desired temperature range. The outputs of the two amplifiers (4.4) are connected to two-channel bipolar ADC 7367, with ± 5 V input range. A circuit capable of measuring the voltages on IGBTs and diodes of a half-bridge converter is shown in Fig. 4.4.

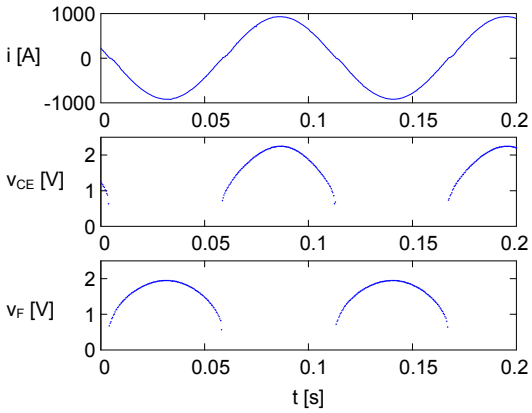


Fig. 4.5: Measured current and corresponding $v_{ce,on}$ and v_F for high side components.

Fig. 4.5 demonstrates the measurement of $v_{ce,on}$ and v_F at the 6 Hz sinusoidal load current.

4.2.4 Influence of Ambient Temperature

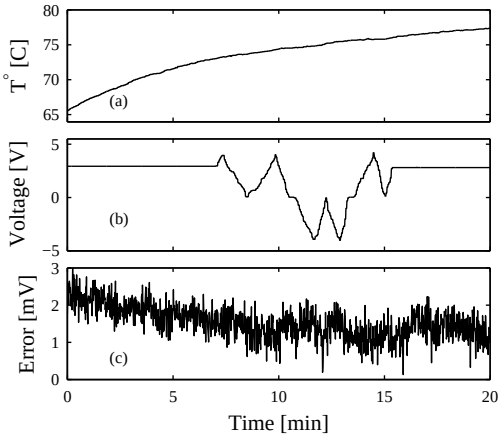


Fig. 4.6: Prototype board test measurement: (top) ambient temperature input, (middle) v_{ce}, and (bottom) error voltage = v_{ce}-v_{out}.

An effect of large ambient temperature on the output of a prototype board was investigated. Fig. 4.6 (Top) image shows the input voltage, Fig. 4.6 (middle) shows a locally created high temperature around the prototype board and (bottom) shows error in the output voltage for the worst case condition. The error in voltage is about 2 mV when ambient temperature is close to 90 $^{\circ}C$, which is most unlikely to occur in the applications.

4.3 Current Measurement

A DSP TMS320F2812 is used to build a control platform. A 12-bit ADC built-in inside the DSP is used to sample a load current using a LEM LF 1005-S current transducer, as shown in Fig. 4.7b. The output signal is also used for the control and over-current protection. An interface circuit is built to protect the DSP, which should be operated in between 0 and 3.3 V. Here, the interface circuit adds the voltage shift of 1.5 V and limits the voltage at 3.3 V during positive and negative peak of the load current. In Fig. 4.7a, R_m is a measuring resistor and V_{meas} is the output voltage for actual current. The current signal has a 1.5 V DC offset and current to voltage ratio of 0.00135 V/A. Hence, maximum $\pm$1000 A will yield the measurement signal in between 2.85 V and 0.15 V. The over-current protection is also built based on these measurement signals. An offset correction technique is included in the control or calibration sequence in the measurement. The offset by the transducer

and the circuit is measured during converter stops or before starting and compensated during operation.

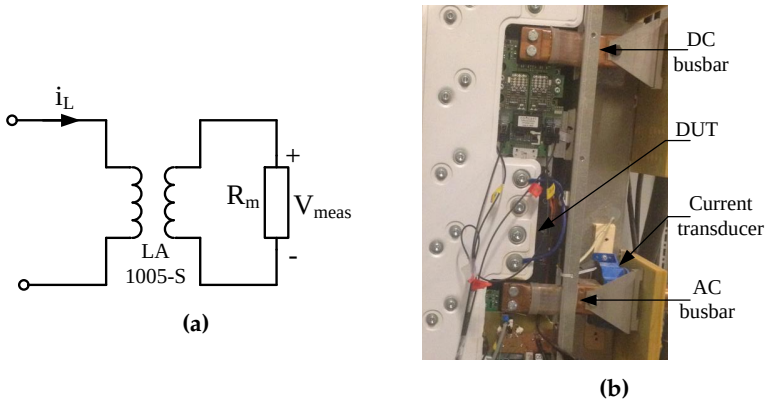
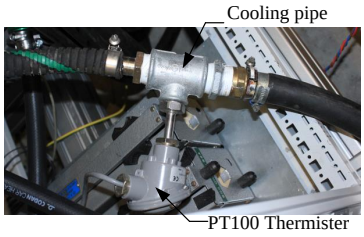


Fig. 4.7: A load current measurement using (a) a layout of current measurement technique, and (b) an image of current measurement in the setup.

4.4 Temperature Measurement

The lower baseplate temperature of power modules is controlled by using a Danfoss Shower Power where liquid (water mixed glycol) is circulating on a pressurized cooling pipe. A heavy-duty Pt100 thermister, shown in Fig.4.8a, is used as a temperature transducer for the cooling temperature measurement. The thermister is inserted into a cooling pipe as shown in Fig. 4.8b. The output of the transducer is fed into a National Instrument (NI) data acquisition system (USB-6215). The output is used for the control and for the data logging during normal operation of a converter.

(a)



(b)

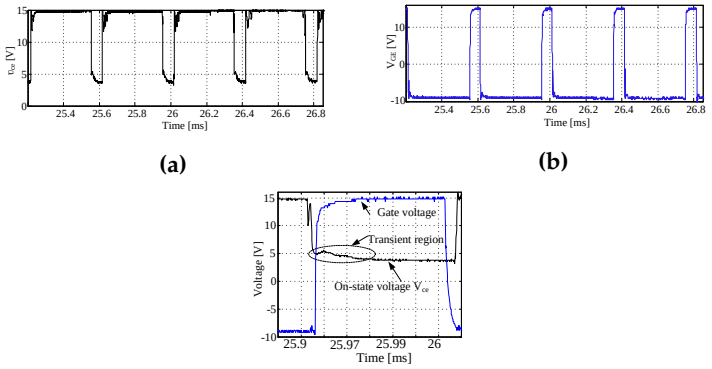
Fig. 4.8: Cooling temperature measurement using (a) a PT100 thermister, and (b) an image of a temperature transducer inserted in a cooling pipe.

4.5 Implementation in a converter

The turn-on time for transistors and diodes varies with the space vector PWM. The following criteria are needed to be fulfilled in order to measure the $v_{ce,on}$ accurately.

- Allow enough turn-on time for the transistors to enter into a saturation region.
- Wait until gate voltage stabilizes at a certain level 15 V, in this case.
- Allow enough settling time required by the measurement circuit, and packaging of a power module.
- Sample the $v_{ce,on}$ and the load current at the same time.

In order to track the changes of $v_{ce,on}$ in a full cycle, sampling of the voltage and the current on each switching modulation is essential. However, the minimum turn-on time during modulation should be larger than the settling time required by the measurement circuit. Therefore, enabling the measurement signal at the middle of a switching pulse makes both integration of the measurement technique in a control simpler and can sample the v_{ce} on the high side IGBT and the low side FWD on converter at the same time. Fig. 4.9 demonstrates an example of v_{ce} voltage waveforms and initial transients in the $v_{ce,on}$ after turn on of a device. Fig. 4.9a shows the v_{ce} clamped at 15 V by the measurement diodes. Similarly, Fig. 4.9b shows the gate-emitter voltage during switching operation. Transients in the voltage waveforms shows the time required by the monitoring circuits to avoid this region. However, in the shown figures the transients are also included originating from the high voltage active probes.



(c) v_{ce} transients.

Fig. 4.9: Switching waveforms (a) collector-emitter voltage waveform clamped at 15 V, (b) gate-emitter voltage waveform and (c) expanded waveforms (both) for a single pulse.

4.6 On-State Voltage Measurement Issues

Increase in gate bias voltage will increase di/dt. The reverse recovery of the diode is also a function of the di/dt. Consequently, the reverse recovery creates the over current stress on IGBT and over-voltage stress on FWD. The transients are also the source of EMI in converter operation. At positive current peak, when a low side IGBT is suddenly turned off, the current starts flowing through a diode on the upper side with a forward voltage drop. This voltage is negative for a high side IGBT. The voltage is recorded up to -80 V in the worst cases, as shown in Fig. 4.10. The emitter stray inductance and commutating current are responsible for these voltage transients.

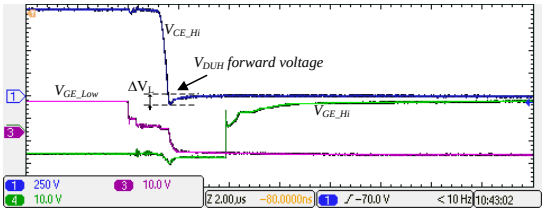
$$\Delta V_L = -L\frac{di}{dt} \tag{4.2}$$

During turn off, the v_{ce} reaches up to 1.2 kV when DC link voltage is at 1 kV caused by the miller capacitance and the stray inductance. However this voltage level is not critical for the 1.7 kV module.

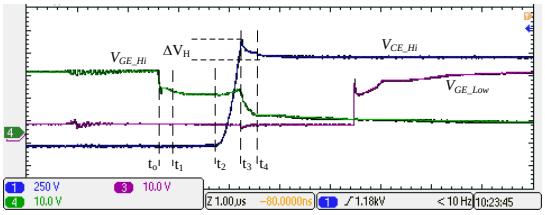
$$\Delta V_H = -L\frac{di}{dt} + V_{ce_H i} \tag{4.3}$$

References

[1] P. Ghimire, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, and P.B. Thogersen. A review on real time physical measurement techniques and their attempt to predict wear-out status of igbt. In *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pages 1–10, Sept. 2013.



(a) Voltage transient during turn on period.



(b) Voltage transient During turn off period

Fig. 4.10: Valtage transients in IGBT during switching on (a) turn on time and (b) turn off time, from [4].

[2] S. Beczkowski, P. Ghimire, AR. de Vega, S. Munk-Nielsen, B. Rannestad, and P. Thgersen. Online vce measurement method for wear-out monitoring of high power igbt modules. In *Proc. of 15th European Conference on Power Electronics and Applications (EPE)*, pages 1–7, Sept 2013.

[3] P. Ghimire, A de Vega, S. Beczkowski, S. S.Munk-Nielsen, B. Rannestad, and P. B. Thgersen. Improving power converter reliability: Online monitoring of high-power igbt modules. *IEEE Industrial Electronics Magazine*, 8(3):40–50, Sept 2014.

[4] P. Ghimire, A Ruiz de Vega, S. Munk-Nielsen, B. Rannestad, and P. B. Thgersen. A real time vce measurement issues for high power igbt module in converter operation. In *Future Energy Electronics Conference (IFEEC), 2013 1st International*, pages 761–766, Nov 2013.

Chapter 5

Stressors on Power Modules

5.1 Introduction

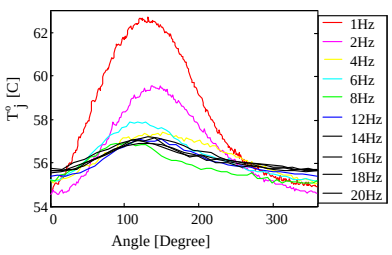
The stressors that have the highest contribution to the ageing of power electronic devices are: ΔT, T_{avg}, voltage, humidity, pollution and vibration [1]. Humidity, pollution and vibration are usually created by external equipment and environment. Field-experience investigation conducted on two different wind turbine converters show condensation during long standstill of wind turbines, insufficient protection against environment, and deterioration of thermal grease between a heat sink and a power module are root causes of failures [2]. Typically, the lifetime of power modules is estimated based on the A-TC capability of a device, where the temperature is a key stressor. This section presents an investigation of chip temperature in power modules during converter operation. A new $v_{ce,on}$-load current method to estimate the chip temperature is also proposed.

5.1.1 Temperature as a Stressor

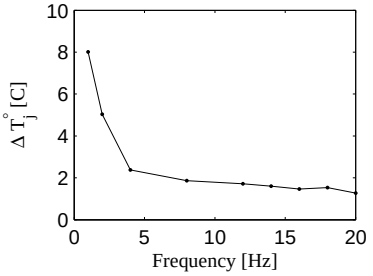
The failure mechanisms in power modules are not dominated by semiconductor die failure, this is implied since the temperature of the junction defines the stress level. The main advantage of an A-TC test setup is that the power loss is created by both switching and conduction loss in both transistors and diodes. Depending on the chosen stress conditions, the focus can be on IGBTs or diodes, as the sign of the current can be chosen as well as the power factor. The effective temperature stresses in converter operation are highlighted below.

Junction Temperature Swing

There are more degrees of freedom to vary junction temperature in such AC power cycling to create accelerated test conditions. The reference AC frequency of the current and the voltage can be adjusted for this purpose. In Fig. 5.1, an example of such variation is shown for the following conditions: $T_{cooling} = 50\ °C$, $f_{sw} = 2.5\ kHz$, $V_{DC} = 450\ V$, $i_{ref} = 150\ A_{peak}$. Similarly, the switching frequency can be adjusted to increase the switching loss.



(a) Junction tempertaure variation at different fundamental frequency.



(b) ΔT_j at different fundamental frequency.

Fig. 5.1: Juncation tempertaure variation changes with fundamental frequency keeping other parameter constant.

Average Junction Temperature

The T_{avg} in an AC power cycling system is adjusted using a combination of both baseplate temperature and the electrical operating points (V_{DC}, V_{AC}, i_L, f_{ref}, f_{sw}). The baseplate temperature is controlled by using a type of cooling system. For example, by controlling the coolant temperature in the case of liquid cooling [3] or by controlling the heat sink temperature in the case of air cooling [4].

5.1.2 Overview of Junction Temperature Monitoring Methods

Modern devices have a built-in NTC thermistor on top of a baseplate, which is placed far from a chip location, hence is not able to detect the chip temperature. Thus, two major approaches, such as analytical (electro-thermal models of devices) and physical (measurement) are used for estimating a chip temperature [5]. An accurate $3D$ structure FEM could give an accurate temperature field, but it requires a post-processing, and often takes a long computational time [5]. In the second method, direct and indirect measurements can be done. In a direct method, a temperature sensor can be integrated directly

on a chip surface such as thermocouple and fibre optic (with/without temperature sensor). Similarly, the temperature field can also be measured by an IR thermal camera. However, these methods require modification on a device packaging, which often poses functional limitations. In an indirect method, several temperature sensitive electrical parameters (TSEPs) can be used. This approach is more suitable to apply in converter operation. Hence, innovative measurement methods have been introduced lately. Mainly, dynamic and static characteristics of a PM can be utilized to find chip temperature dependencies with a function of V_{ge}, I_C and forward voltage drop [6]. In dynamic characteristics, IGBT turn-on, turn-off, peak gate current and rise time are used where gate resistors and capacitors are dominating parameters.

In static characteristics, $v_{ce,on}$ is used in both low-current and high-current methods. In a low-current method, a small current runs through the device when the converter is offline. Therefore, it has a negligible contribution to heat-up. However, it requires a modification to the converter control, halting normal operation for a short period of time during the measurement. On the other hand, a high-current method introduces self-heating, if the calibration is not conducted in a short time. In addition, $v_{ce,on}$ changes due to the temperature gradient in series interconnection. Nonetheless, this method is regarded as a suitable and cheaper technique in real time operation, though maintaining accuracy and implementing while in operation are still challenging. A key benefit is that this method does not require any functional or structural modifications in the converter. However, the measurement circuitry has to fulfil certain requirements to estimate chip temperature [7] as listed below.

- Sensitivity: Minimum of $1mV\ /^{\circ}C$ would be best.
- Measurement accuracy: Minimum of 1 mV would be best.
- Measurement resolution: 0.61 mV.
- Calibration time: As short as possible, in the case of the P3 module (used in this thesis) for less than 200 uS.
- Homogeneous temperature field across module during calibration.
- Ageing compensation: varies with the packaging, typically 20 mV from normal ageing in the P3 module.
- Failure compensation: varies with the packaging mainly from bond wire lift-off, typically 5 mV to 7 mV in the $P3$ module.

5.2 Tempertaure Profile Monitoring

An IR thermography method is used because it can capture the temperature profile across a chip and the surroundings. A new generation thermal camera (FLIR $X8400SC$) with a higher resolution is used. It is able to capture frame size up to 1280×1024 at 1.3 million pixels. The camera has an adjustable frame rate; up to 106 Hz at full frame and close to 3 kHz at 48×4 window frame.

5.2.1 IR Thermography

Thermal heat transfer by radiation follows the Stefan-Boltzman law, which in terms of power can be expressed as:

$$P = \varepsilon \sigma A T^4 \tag{5.1}$$

Where, the ε is the emissivity which varies between 0 and 1, A is the emitting area and T is the temperature in K. In thermography, the power radiated from a selected area is measured by a detector. The detector collects radiated power from an angular span determined by the optics in the device. If no other sources of radiated power are influencing the measurements and also the true emissivity (ε_t) of the surface under investigations is known, the true temperature (T_t) of the test sample can be determined directly from the measured power (P_m) by ignoring the geometrical details, see Eq. (5.2).

$$P_m = \varepsilon_t \sigma A T_t^4 \tag{5.2}$$

Hence in practical measurements the ε has to be known from other sources or has to found from calibration. For most devices, the ε is set to a given input value ε_{in} either in a single detector device or in software made for an IR camera. However, the above assumption that no other sources of power are affecting the power measurement is rarely met, since any material above $-273.15^{\circ}C$ will emit some radiation. The additional contributions to the measured power is shown in Eq. (5.5).

$$P_m = \varepsilon_t \sigma A T_t^4 + P_{air} + P_{reflection} \tag{5.3}$$

Moreover, the intensity and thereby also the detected power may be attenuated by absorption (A_t) in the air or in the optics on the way from sample to the detector. For simplifying, if all this absorption occurs just before the detector, the following equation can be determined.

$$\begin{aligned} P_m &= (1-A)(\varepsilon_t \sigma A T_t^4 + P_{air} + P_{reflection}), \\ &= (1-A)\varepsilon_t \sigma A T_t^4 + (1-A)(P_{air} + P_{reflection}), \\ &= \varepsilon_{eff} \sigma A T_t^4 + P_{back,true} \end{aligned} \tag{5.4}$$

This latter absorption effect will result in an effectively lower emissivity, $\varepsilon_{eff} = (1 - A)\varepsilon_t$, which will depend on the distance to the sample under investigation and the optics. If the setup is fixed, and the ambient atmosphere is kept the same, a well calibrated ε should prove it's robustness.

5.2.2 IR-Temperature Calibration

For a given measurement, the detector will give a temperature output T_m, which depends on the parameter input. For a well calibrated detector i.e. the internal power measurement in the Charge Coupled Device(CCD) array is correct, it can be assumed that the true power received by the detector P_m as expressed in Eq. (5.1) equals the power P_m read by the detector, which is used via Eq. (5.2) to get the T_m. Thus, the Eq. (5.5) can be realized.

$$\begin{aligned} P_m &= \varepsilon_t \sigma A T_t^4 + P_{back}\left(T_{air,reflection,abs} in \frac{air}{optics}, distance\right), \\ &= = \varepsilon_t \sigma A T_t^4 + \left[P_{back}\left(T_{air,reflection,abs} in \frac{air}{optics}, distance\right)\right]_{input} \end{aligned} \tag{5.5}$$

Calibration can be done by measuring the T_t by some other means under a well-defined steady state condition. In the following, an ideal thermocouple (calibrated) is used to measure the true surface temperature and assumes that the local thermocouple measurement T_c is representative of the temperature of the surface imaged in the camera during passive heating.

By measuring pairs of T_m and T_c over the temperature range of interest, the ε can be obtained from Eq. (5.6).

$$T_m^4 = \frac{\varepsilon_{eff}}{\varepsilon_{in}} + \frac{(P_{back,tru} - [P_{back}]_{input})}{\varepsilon_{in}\sigma A} \tag{5.6}$$

Where, as mentioned, it is assumed that $T_t = T_c$. By plotting T_m^4 as a function of T_c^4, a straight line can be obtained as shown in Fig. 5.2. If the data does not display a straight line, it indicates that some of the assumptions above should be reconsidered. But, if a straight line is obtained, this confirms the formal validity of the above analysis and also indicates that the assumption of a constant background contribution is reasonable. The true effective emissivity (ε_{eff}) is obtained from the input value ε_{in} and the fitted slope of the line which equals the ration $\frac{\varepsilon_{eff}}{\varepsilon_{in}}$. With the new correct emissivity one or more background parameters are adjusted until the T_m agrees with the T_c. In this later step, there is no need to adjust the absorption/transmission setting for the air or optics in the software, because this will change the ε_{eff} and not just the background.

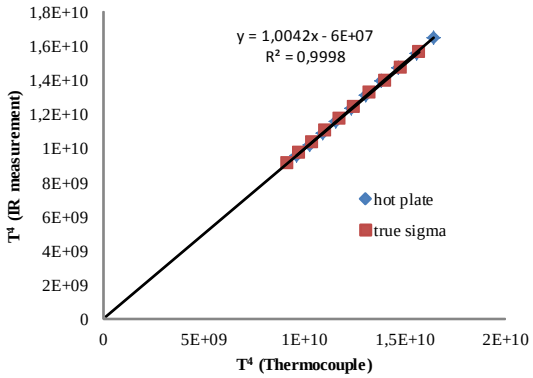


Fig. 5.2: Calibration of IR camera and temperature to obtain correct emissivity.

5.2.3 Test Setup and Sample Preparation

The visibility of a chip area in PMs is covered by a low inductance bus bar in a converter stack, as shown in Fig. 3.2b. Hence, the DUT is relocated outside of a converter stack in the same test rig, see Fig. 5.3a. This allows direct visibility on the chip area through an IR camera. Furthermore, the test setup is interchangeable between liquid cooling, see Fig. 5.4a and an externally controlled hot plate, see Fig. 5.4b. The later method is used during $v_{ce,on}$-T calibration of a power module, up to 125°C.

Power terminals of internal bus-bars of the open module are inclined out-

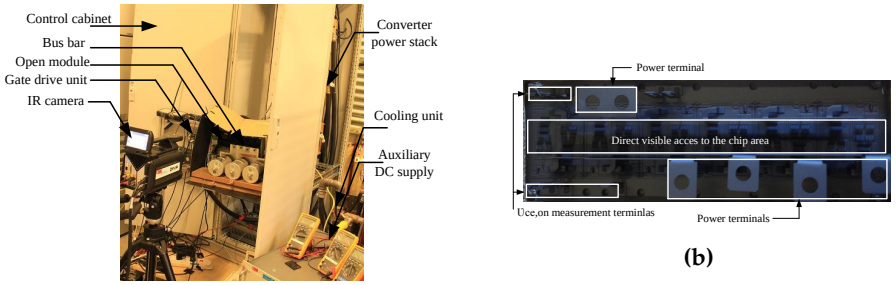
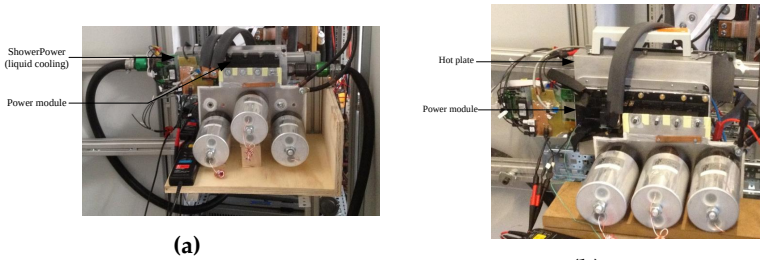


Fig. 5.3: IR thermography (a) a test setup and (b) an open device under test power module.

wards, see Fig. 5.3b. A high temperature (400°C) matte black paint is coated with around 50 μm thickness on the top surface. The emissivity is calibrated using the method introduced in section 5.2.2 and found 0.954 for a wide temperature range starting from 25°C to 125°C. The suitable thickness of paint is investigated using an IR spectrometer, details are presented in [7]. A high voltage insulation Mylar sheet is used in between positive and negative bus

bar for the voltage insulation.

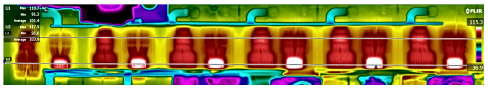


(a) **(b)**

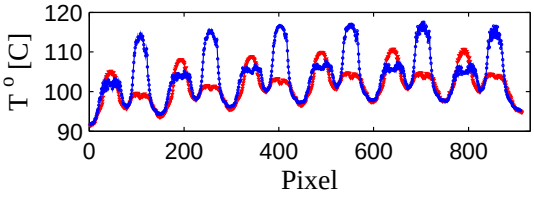
Fig. 5.4: IR thermography test setup on (a) liquid cooling and (b) a hotplate.

5.2.4 Temperature Profile on a Power Module

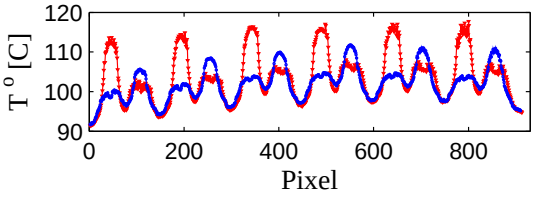
The temperature field on a chip surface is studied in three different levels, focusing only on a half-section of a bridge, a full-section of a bridge and a full module. Upon increasing a window size, the frame rate is reduced and also the temperature on the far edges of the selected window is less accurate. Hence, the investigation is conducted on each section at a time. Fig. 5.5a



(a) A image for a full module.



(b) Tempertaure profile on two lines.



(c) Tempertaure profile on two lines.

Fig. 5.5: IR thermography on a full module.

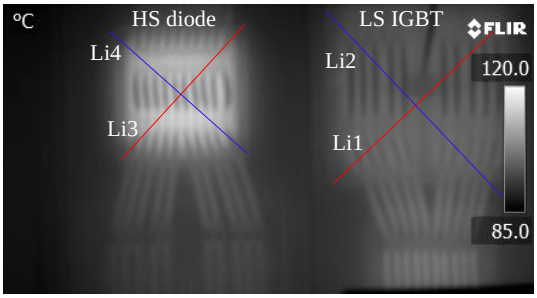
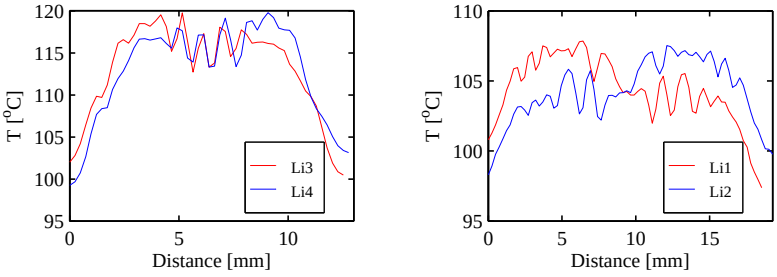
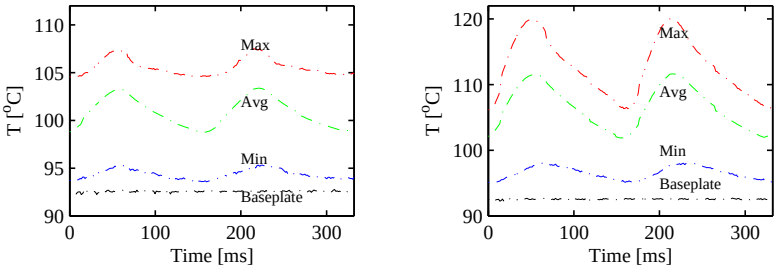


Fig. 5.6: Spatial tempertaure profile from corner to cornr on the LS IGBT and the HS diode.



(a) HS diode. **(b)** LS IGBT.

Fig. 5.7: Spatial temprature distribution on IGBT and diode chips.



(a) LS IGBT. **(b)** HS diode.

Fig. 5.8: Temporal temprature distribution on IGBT and diode chips.

shows an image captured for a full size of a PM at 500 $Apeak$, 450 VDC and 6 Hz. Temperature profiles using two isothermal lines across the module from left to the right are shown in Figs. 5.5b and 5.5c. In Fig. 5.5b the LS diode/ HS IGBT are conducting, while in Fig. 5.5c, the HS diode/ LS IGBT are conducting.

The spatial distributions of temperature on a single IGBT and diode from corner to corner, see Fig. 5.6, are shown in Figs. 5.7b and 5.7a. Similarly, the temporal distributions of temperature in two fundamental load cycles for an IGBT and a diode are shown in Figs. 5.8a and 5.8b. Fig. 5.9a shows the tem-

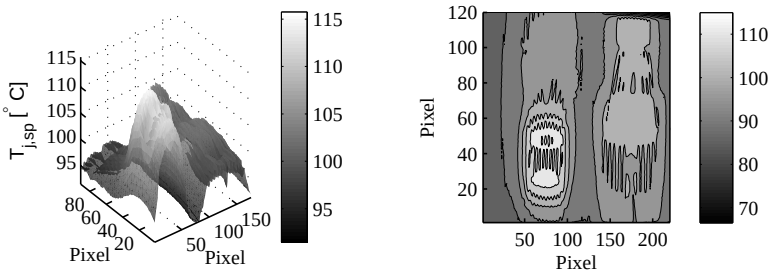


Fig. 5.9: IR measurement in spacial temperature distribution at 500 A peak for one section when $D_{DUT,H}$ is hotter, (a) temperature field, and (b) a temperature contour.

perature field in a single section, as shown in Fig. 5.11 when the $D_{DUT,H}$ is at maximum temperature. Fig. 5.9b shows the temperature gradient contour on the corresponding surface.

Similarly, Fig. 5.10a shows the temperature field when the $D_{DUT,L}$ is at maximum temperature. Fig. 5.10b shows the temperature gradient contour on the corresponding surface.

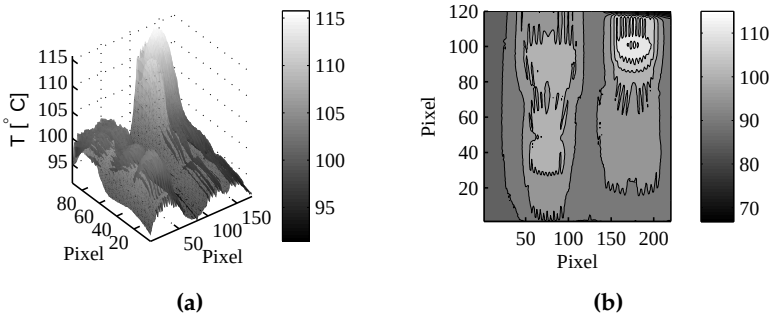


Fig. 5.10: IR measurement in spacial temperature distribution at 500 A peak for one section when $D_{DUT,L}$ is hotter, (a) temperature field, and (b) a contour.

5.3 Vce-Load Current Method

This method includes two major steps in estimating chip temperature. First, a calibration of $v_{ce,on}(T)$ is required at different load currents for varying cooling temperature. Generally, a manufacturer provides characteristic curves for $25°C$, $125°C$ and $150°C$. These are typical values, which may vary largely between the modules. Hence, the calibration of $v_{ce,on}$-T on each measuring sample is required. The individual calibration also eliminated the discrepancies in physical parameters from production. Nearly, 20 mV variation is observed between four power modules for identically located chips [8]. The second step includes a real-time $v_{ce,on}$ measurement, when the converter is active, but with a higher accuracy, as specified in section 4.2.

Calibration of $v_{ce,on}(T)$

Calibration is a process to obtain static characteristics $I - v_{ce,on}(T)$ of individual components of a PM. As outlined in the previous section, short calibration time is an essential requirement to avoid self-heating. Hence, two approaches are developed to calibrate the module at the load current in converter. The switching sequences and the current waveforms are outlined in section 3.3.

- Current-ramp method
- Current-plateau method

In a current-ramp method, the current is ramped up through the device within 350 μs, as shown in Fig. 3.5a. Here, $v_{ce,on}(T)$ is measured for a wide range of I_c and T at constant DC link voltage. Whereas, in a current-plateau method, the current is ramped up at 100 μS and maintained at a steady level, as shown in Fig. 3.4a. Thereafter, $v_{ce,on}(T)$ is measured for a wide range of I_c and T. The latter method is good for calibrating at a smaller current step in comparison to the former. In both methods, the temperature field is monitored continuously and the uniform temperature field on the chip surface is verified using an IR thermography. However, during the calibration at higher temperature ($125°C$), the surface temperature is also affected by the ambient air flow around the open module, see Fig. 5.11, where nearly 2-3$°C$ variation is observed from the IR measurement in a single half-bridge section.

Fig. 5.12 shows $I - v_{ce}(T)$ characteristics for $I_{DUT,H}$ (Fig. 5.12a) and $D_{DUT,H}$ (Fig. 5.12b) at 25^0C to 125^0C in a $5°C$ and a 5 A steps. The characteristics are modelled by a Shockley model together with a series resistor as given by Eq. 5.7.

$$v_{ce,on} = \eta.V_T.ln(\frac{i_C}{I_S} + 1) + i_C \times R + V_o \tag{5.7}$$

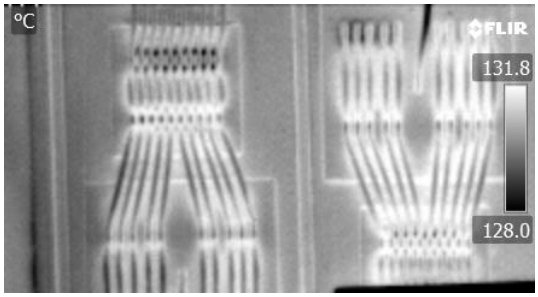
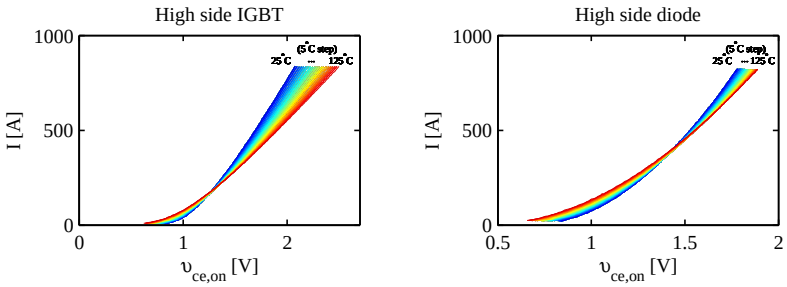


Fig. 5.11: IR image of a single section of module during calibration at 125°C.



(a) IV curve for $I_{DUT,H}$. **(b)** IV curve for $D_{DUT,H}$.

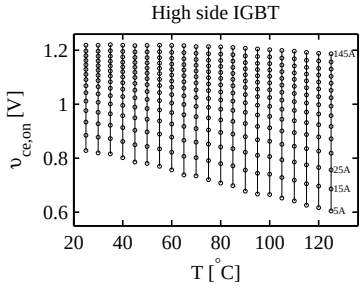
Fig. 5.12: Calibrated IV curve from 25 °C to 125 °C for (a) a high side IGBT and (b) high side diode.

Where, η is a ideality factor and V_T is a thermal voltage found as $V_T = \frac{k_B T_j}{q}$. i_C, I_S and V_o are collector current, saturation current and offset voltage respectively. The model is fitted using Newton-Raphson iteration to measure the internal resistance from the static characteristics.

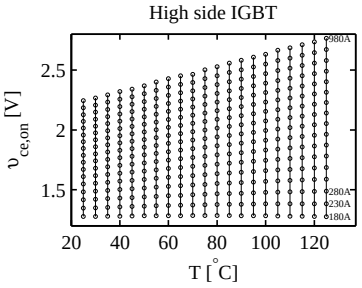
From those characteristics, a voltage and temperature dependency is shown for a high side IGBT, see Fig.5.13 and for a high side diode, see Fig. 5.14. For both components, the voltage and the temperature dependency for both NTC and PTC region is separated. The cross-over current from NTC to PTC for the diode chip is much higher, close to 416 A and for the IGBT chip, close to 215 A in the used PM.

Using the calibrated curve, as shown in Fig.5.13 and 5.14, the current dependencies temperature calibration factor (K-factor) $(°C/mv)$ is formulated [9]. The K-factor is used to transform the load information to the temperature in converter operation. The K-factor is formulated as follows,

$$\text{K-factor} = \frac{(T_H - T_L)}{(v_{ce,on,H} - v_{ce,on,L})} \tag{5.8}$$

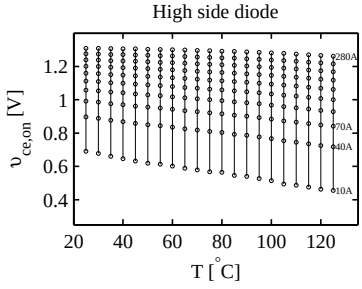


(a) Voltage and temperature dependency at NTC region.

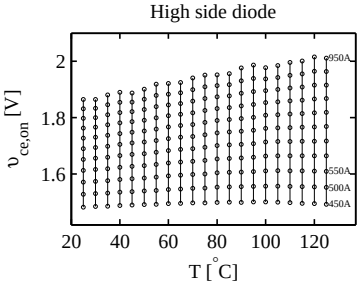


(b) Voltage and tempertaure dependecy at PTC region.

Fig. 5.13: Voltage and temperature dependency for a high side IGBT.



(a) Voltage and temperature dependency at NTC region.



(b) Voltage and tempertaure dependency at PTC region.

Fig. 5.14: Voltage and temperature dependecy for a high side diode.

Where, $v_{ce,on,H}$ and $v_{ce,on,L}$ are calibrated on-state voltage for the high chip temperature T_H and for the low chip temperature T_L correspondingly. The turn on time is limited to 140 μs to avoid a rise in temperature from self-heating. The rise in temperature is also monitored by using the IR camera during the calibration. For 200 μs turn on time the rise in temperature on the chip surface is observed as less than 0.5°C [7]. In addition, taking the voltage difference at two different temperatures for the same current further reduces the effect of self-heating. Here, the temperature sensitivity shall be updated using recalibration after a certain degradation level, which depends on the load applied. Figs. 5.15 and 5.16 show the K-factor for $I_{DUT,H}$ and $D_{DUT,H}$.

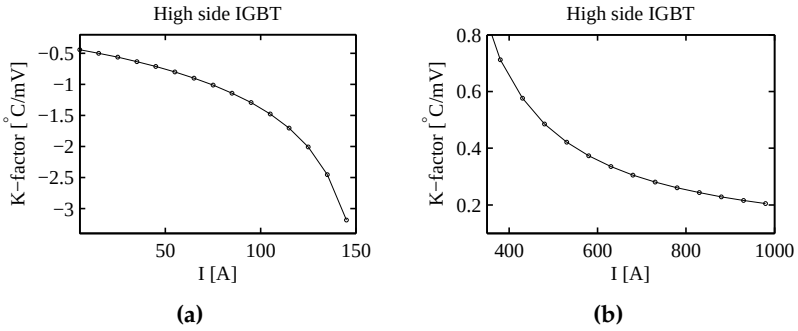


Fig. 5.15: Current and temperature dependency (K-fcator) for high side IGBT at (a) NTC current and (b) PTC current.

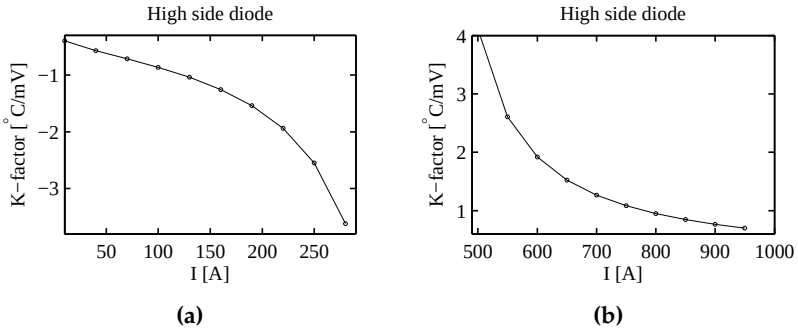


Fig. 5.16: Current and temperature dependency (K-factor) for high side diode at (a) NTC current and (b) PTC current.

5.3.1 Real Time Measurement

The real-time $v_{ce,on}$ measurement technique is presented in chapter 3. Fig. 5.17a is shown for current and forward voltage drop measured at 500 A_{Peak}

and at 6 Hz frequency for a single cycle.

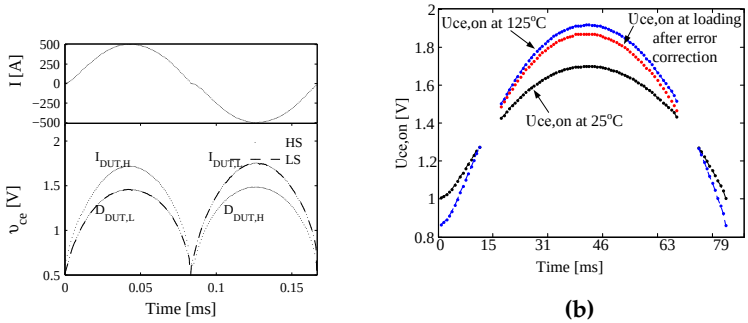


Fig. 5.17: Juntion temperature estimation (a) I_L, $v_{ce,on}$ and v_{FD} measurement for one cycle at 500Apeak and (b) calibrated and measured $v_{ce,on}$ to estimate $T_{avg,space}$.

5.3.2 Estimating Temperature in a Converter Operation

During a converter operation, the $v_{ce,on}$ is monitored continuously with 2-3 mV accuracy. The K-factor is used to obtain chip junction temperature from the TSEPs as given in Eq. (5.9).

$$T_{avg,j} = T_{ref} + T_{cor} + K(v_{ce,meas} - v_{ref}(T_{ref}) + \Delta v_{err}) \tag{5.9}$$

Where, T_{ref} is the reference temperature used for the calibration (in this case 25°C), v_{ref} is the on-state voltage at T_{ref} and $T_{cor}/\Delta v_e rr$ are corrections for the calibration approach.

5.3.3 Correction Parameters

The temperature estimation process involves two major steps, calibration and loading where dynamics of the temperature profile differ from each other. Two correction parameters are introduced, $T_{cor}/\Delta v_e rr$ to compensate the error. T_{cor} is the heat up during calibration, see Fig. 5.18, which has to be added to the reference temperature. The effect is negligible for turn on time 140 μs in the current-plateau method. The temperature error during calibration is verified based on simple 1D finite difference approach which is validated using a full FEM and IR thermography. Eq. (5.10) introduces the equation used for estimation of temperature increase:

$$\delta T = \delta T(t_o) + \int_{t_o}^{t_1} \frac{q_g - q_c}{c_p \nu \rho} dt \tag{5.10}$$

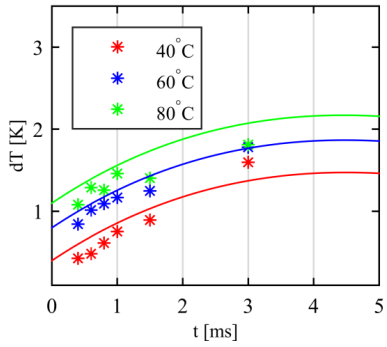


Fig. 5.18: Calibration heat-up error on high side IGBT for different turn-on time. The asterisk indicates experimental values measured by IR thermography and the solid curves are simulated, from [10].

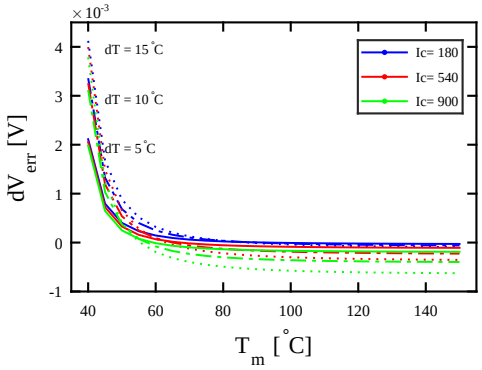


Fig. 5.19: Δv_{err} at different current and ΔT on a IGBT.

Where, q_g is the generated heat by the current load, q_c is the heat dissipating away from the chip, and $c_p \nu \rho$ are material/ geometry parameters. The heat dissipation is calculated using direct copper bonded (DCB) thermal impedance and capacitance. Generated heat is derived from a Shockley model with a series resistor, see Eq. (5.7), in order to remove the contribution from interconnections its' contribution is subtracted. Another major correction parameter is Δv_{err}.

Δv_{err} is the correction in forward voltage from a homogeneous temperature field to inhomogeneous field. This correction depends on the difference in chip temperature from center to edge, see Fig. 5.9-b. Fig. 5.19 shows Δv_{err} as a function of current, temperature at different ΔT obtained from a full FEM simulation.

Fig. 5.20 shows the rise in interconnection resistance as a function of temperature, which is obtained from the static calibration. A Shockley together

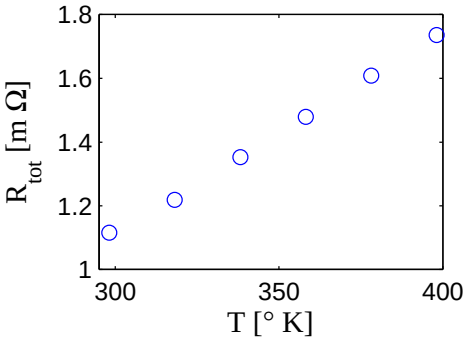
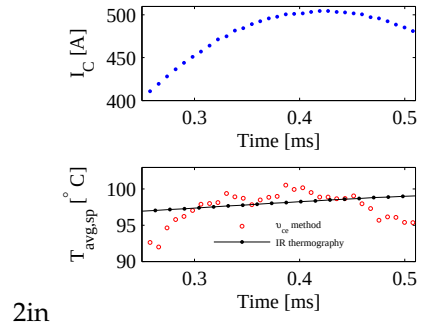


Fig. 5.20: Tempertaure dependency of interconnection resistance obtained from calibration for IGBT.



2in

Fig. 5.21: Estimated $T_{avg,sp}$ from v_{ce}-I_c method and IR thermography at $500A_{Peak}$ for $I_{DUT,H}$.

with a resistor model, see Eq. (5.7), is used. The forward temperature coefficient is $0.0042/K$, which is close to the temperature coefficient for Al. This confirms that the total resistance is mainly contributed by bond wires and chip metallization. The total resistance to use for the correction parameter is $6.27e^{-6}\ \Omega/K$. The resistance may change for different modules, hence a calibration is must for each power module. A typical value of R_{int} per section is $0.25m\Omega$ at $25^{\circ}C$ from the manufacturer. This is close to the measurement and FEM simulations [7]. On-state voltage correction from homogeneous to inhomogeneous temperature distribution is also obtained using FEM simulations under required circumstances, deriving from on-state voltage, and compared to an homogeneous case.

5.3.4 Results

Fig. 5.9 shows the spatial temperature field ($T_{j,sp}$) measured from the IR thermography, when $D_{DUT,H}$ and $I_{DUT,L}$ are at maximum temperature in the

first section of DUT. The spatial temperature variation along a diagonal on IGBT and diode chips are shown in Fig. 5.7 at maximum temperature. The $T_{avg,sp}$ measured with the IR camera and the estimation from v_{ce}- load current method are shown in Fig. 5.21 for $I_{DUT,H}$ when the current is at peak. Table 5.1 gives temperature measurements at different I_c at peak for 6 Hz output frequency and at corresponding tabulated baseplate temperatures for $I_{DUT,H}$. Similarly, the peak temperature variation for the IGBT at 6 Hz to 20 Hz load

Table 5.1: Temperature measurement from $v_{ce,on}$-load current and IR thermography (The peak temperature shown in table reaches nearly after 20ms of current peak)

Current	Proposed method	IR thermography on $I_{DUT,H}$			
$I_{c,peak}$	T_{est}	$T_{baseplate}$	T_{avg}	T_{max}	T_{min}
(A)	($^\circ C$)	($^\circ C$)	($^\circ C$)	($^\circ C$)	($^\circ C$)
500	100	88	99.5	102.6	92.9
450	81	71	79.6	82	74.8
400	110	101.6	110.4	113.7	104.5
350	88	82	89	92	85

frequencies are compared to the estimated die temperature based on $v_{ce,on}$ and FEM simulation and shown in Fig.5.22 [9]. The peak temperatures are very close.

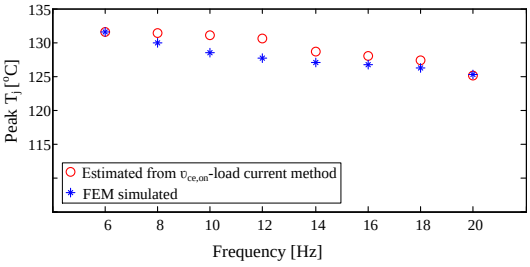


Fig. 5.22: A comparison of peak temperature between measured and simulation, from [9].

References

[1] Miguel Sanz Bobi. *Operation and Maintenance of Renewable Energy Systems: Experiences and Future Approaches (Green Energy and Technology)*. Springer, 2014.

[2] Katharina Fischer, Thomas Stalin, Hans Ramberg, jan Wenske, Goran Wetter, Robert Karlsson, and Torbjorn Thiringer. Field-experience based root-cause anal-

ysis of power-converter failure in wind turbines. *IEEE Transactions on Power Electronics*, 30(5):2481–2492, May 2015.

[3] A.R. de Vega, P. Ghimire, K.B. Pedersen, I. Trintis, S. Beczckowski, S. Munk-Nielsen, B. Rannestad, and P Thgersen. Test setup for accelerated test of high power igbt modules with online monitoring of vce and vf voltage during converter operation. In *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA)*, 2014.

[4] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani. Ageing and failure modes of igbt modules in high-temperature power cycling. *IEEE Transactions on Industrial Electronics*, 58(10):4931–4941, Oct. 2011.

[5] Y. Avenas, L. Dupont, and Z. Khatir. Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters: A review. *IEEE Transactions on Power Electronics*, 27(6):3081–3092, 2012.

[6] N. Baker, M. Liserre, L. Dupont, and Y. Avenas. Improved reliability of power modules: A review of online junction temperature measurement methods. *IEEE Industrial Electronics Magazine*, 8(3):17–27, Sept. 2014.

[7] P. Ghimire, K. B. Pedersen, I. Trintis, B. Rannestad, and S. Munk-Nielsen. Online chip temperature monitoring using vce-load current and ir thermography. in Press ECCE 2015.

[8] P. Ghimire, K. B. Pedersen, S. Rannestad, B.and S.Munk-Nielsen, and F. Blaabjerg. Real time wear out monitoring test setup for high power igbt modules. Submitted.

[9] Pramod Ghimire, Kristian Bonderup Pedersen, Angel Ruiz de Vega, Bjorn Rannestad, Stig Munk-Nielsen, and Paul Bach Thgersen. A real time measurement of junction temperature variation in high power igbt modules for wind power converter application. In *Proc. of 8th International Conference on Integrated Power Systems (CIPS)*, pages 1–6, Feb 2014.

[10] K. B. Pedersen, M. Brincker, P. Ghimire, and K. Pedersen. Monitoring of igbt modules - temperature and degradation simulation. Peer reviewed and accepted for International Conference on Integrated Power Systems (CIPS), 2016.

Chapter 6

Wear Out of Power Modules

Wear out is a process of material fatigue due to both electrical and environmental loadings. The loadings create temperature oscillations, which causes thermo-mechanical fatigue due to material expansion and coefficient of thermal expansion (CTE) mismatch [1]. This directly affects the module packaging especially the interconnects: solder joints, bond wires and metallization. Usually information after catastrophic failure events is lost. Hence, in order to investigate the degradation process, the power modules are subjected to different numbers of loading cycles and their post test characterization with the online measurement are assessed. This chapter presents the ageing monitoring for four power modules that are subjected to A-TC for different numbers of cycles. The monitoring strategies for advanced power cycling/converter operation are presented. Also a data evaluation method to separate wire degradation and solder degradation are presented.

6.1 Wear Out Monitoring

The wear out on power modules is monitored using three strategies: static calibration, offline characterization and real time monitoring as given in Fig. 6.1. The I-V characteristic of each power module is measured after nearly 24 hours of operation by halting and allowing sufficient time for natural cooling.

The **static calibration** is conducted at different cooling temperatures and current levels. This test shows a rise in $v_{ce,on}$ caused by a rise in internal resistance from material degradation mainly in bond wires, metallization, and Cu during the test. The **offline characterization** at constant temperature is carried out for every 5 min of operation, where the interconnections ageing is perceived as a function of the number of cycles.

In **real time measurement**, ageing parameters are monitored in every switching cycle without interruption of the converter operation. This mea-

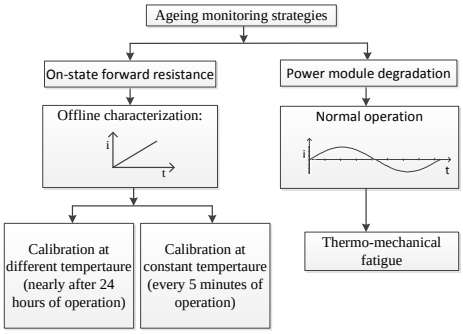


Fig. 6.1: Ageing monitoring strategies on power modules in a converter.

surement demonstrates the effects caused by thermo-mechanical induced fatigue in PMs.

Fig. 6.2 shows an I-V curve measured at 80°C and V_{ge} at 15 V for an IGBT and diode. In the offline characterization process, the measurement is conducted at one test temperature level, while in real-time, the measurement is routinely-done as described in the previous chapter 5. In real-time mea-

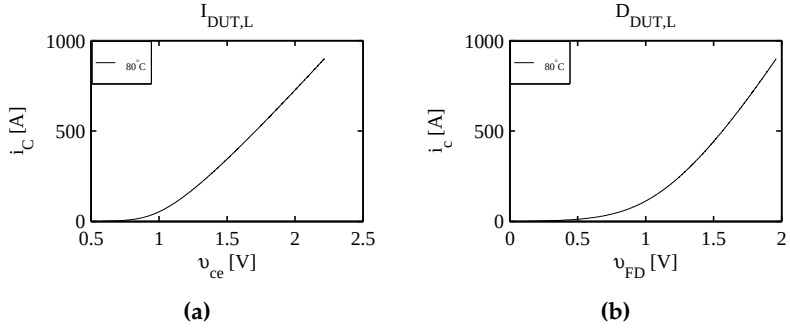


Fig. 6.2: An offline IV charctarization for (a) a low side IGBT, and (b) a low side diode at 80 °C.

surement, v_{ce}, v_{FD} and the corresponding i_C are measured at the center of a PWM pulse. Hence, the measurements are not affected by the transients during the settling time required by the circuit and packaging of a power module [2]. The measurement routine is illustrated in [2], where the online measurement is routinely-done at every 5 minutes of operation to reduce the amount of data to be processed. During one measurement, the v_{ce}, i_L, and the corresponding $T_{cooling}$ are sampled and recorded for 2.5 load cycles. The measurements of current, the corresponding v_{ce}, and the v_{FD} for the whole life and a zoom in image for one-cycle are shown in Fig. 6.3.

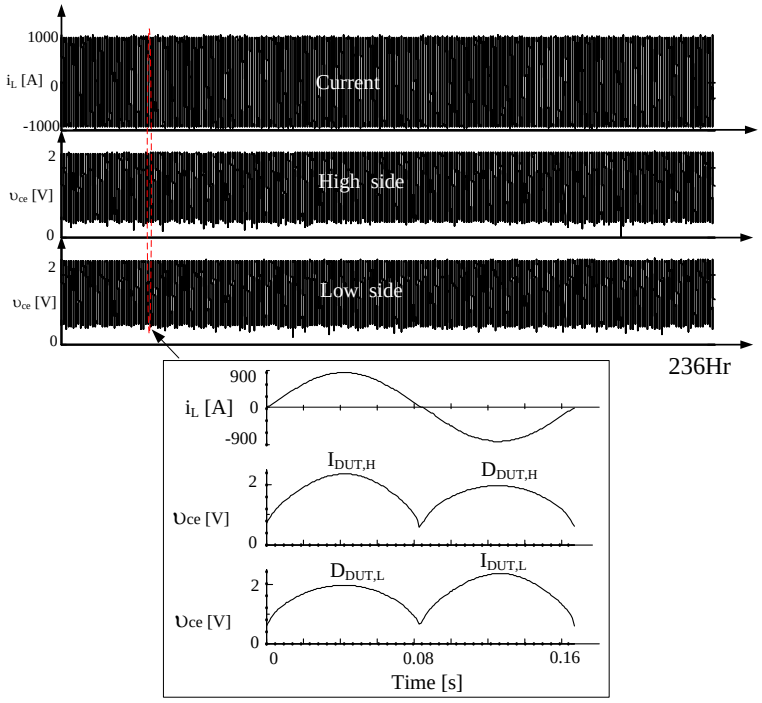


Fig. 6.3: Real time monitoring of on-state v_{ce} and i_C for all cycles during lifeitme and expanind image for a single cycle.

6.1.1 Separating Degradation Mechanisms

As shown in Fig. 4.1, the rise in v_{ce} is affected by thermo-mechanical degradation in wires, metallization and solder layers. The degradation can be realized by continuous measurement of the falling and rising sides of the sinusoidal current. Although the measurement is conducted for a full cycle, the rise in voltage can be analysed at one current level. Any measurement point could in principle be chosen except at the crossover current, where the behaviour of the IGBT and FWD changes from NTC to PTC. Here 900 A is chosen for investigation. Table 6.1 presents the sampling points for analysis and the corresponding active components as shown in Fig. 6.4. By comparing the forward voltage v_{ce}/v_{FD} at point P_{1+} and P_{2+}, one obtains an indication of the thermal response of the active components, and similarly at P_{1-} and P_{2-}. The wear out of the tested modules is demonstrated using the v_{ce}/v_{FD} evolution at P_{1+}/ P_{1-}. For this analysis, a reference voltage $V_{P_{ref}}$ is obtained from the average of the initial 100 healthy current cycles, as given in Eq. (6.1). The average voltage of the first 100 cycles is 2.35 V with a standard deviation below 0.13 mV for the sample PM1. Eq. (6.2) measures the wear of the DUT

Table 6.1: THE ACTIVE COMPONENTS and THEIR SAMPLING.

	Positive half cycle		Negative half cycle	
	P_{1+} (Rising)	P_{2+} (Falling)	P_{1-} (Rising)	P_{2-} (Falling)
IGBT	$I_{DUT,H}(V_{ce,P1+})$	$I_{DUT,H}(V_{ce,P2+})$	$I_{DUT,L}(V_{ce,P1-})$	$I_{DUT,L}(V_{ce,P2-})$
Diode	$D_{DUT,L}(V_{FD,P1+})$	$D_{DUT,L}(V_{FD,P2+})$	$D_{DUT,H}(V_{FD,P1-})$	$D_{DUT,H}(V_{FD,P2-})$

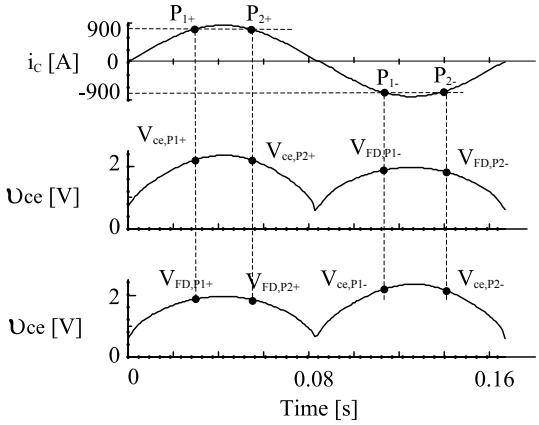


Fig. 6.4: Observation points are chosen at 900 A for studying wear out process in IGBT modules.

by displaying ΔV_1. The change in thermal response is similarly measured regarding the increase in forward voltage from P_{1+}/ P_{1-} to P_{2+}/ P_{2-}, namely ΔV_2 as given in Eq. (6.3). It is expected that the module will display a slow steady wear in the beginning of the testing followed by an accelerated wear closer to the end of life.

$$V_{P_{ref}} = \frac{1}{N}\sum_{i=1}^{100} V_{P_1}(n_i), \tag{6.1}$$

$$\Delta V_1(n) = V_{P_1}(n) - V_{P_{ref}}, \tag{6.2}$$

$$\Delta V_2(n) = V_{P_2}(n) - V_{P_1}(n), \tag{6.3}$$

Where, n is the number of cycles.

Considering half a fundamental cycle, the temperature cycle is expected to follow the current cycle because of the electrical power dissipation [3]. The temperature rise has a delayed response due to the thermal time constant in the system. As a result, the v_{ce} is higher at P_{2+}/ P_{2-} at the same current, regardless of the material degradation.

6.2 Wear Out Test Case

6.2.1 Test Strategies

The converter operating parameters are listed in Table 6.2 to generate A-TC. Four modules are power cycled for different numbers of cycles and stopped at different times. PM1 is tested continuously until it fails, which is after 5.1 *MC* of operation. This test is regarded as a threshold to designate the number of test cycles for the other modules under similar stress and loadings. The whole test is summarized for all modules in Table 6.3. Three PMs (PM2,

Table 6.2: CONVERTER OPERATING PARAMETERS

Symbol	A-TC parameters	Offline
V_{DC}	1000 V	1000 V
V_{DUT}	257 V_{rms}	257 V_{rms}
i_L	922 A_{peak}	890 A_{peak}
θ	2.7 Rad	-
F_{out}	6 Hz	-
F_{SW}	2.5 kHz	-
C	4 mF	4 mF
L	380 μH	380 μH
$T_{cooling}$	80 ± 0.5°C	80 ± 0.5°C

PM3, PM4) are stopped cycling long before than their end of life, hence were still regarded as operational.

Cooling Temperature Variation

Fig. 6.5 shows the average water temperature $T_{cooling,m}$ measured on each fundamental cycle for all power modules. The test setup is kept in a closed room, where the ambient temperature varies periodically during day and night. As a result, the converter cooling temperature deviates approximately $\pm 0.5°C$ from the reference temperature. Furthermore, in the initial test period of PM1, the $T_{cooling}$ dropped approximately $0.5°C$. This is influenced by an open heat exchanger in the setup. The exchanger is used to control the $T_{cooling}$ through a liquid circulating pipe. Later, the exchanger was separated by a wall to divert the hot air which reduced the temperature fluctuations significantly in the other three tests.

Table 6.3: POWER MODULE SAMPLES USING THE TEST SYSTEM FOR WEAR OUT TEST.

Power Module	Number of cycles	Status	Bond wire lift-off
0 (PM0)	0 cycle	Operational	No
1 (PM1)	5103000 cycle	Critical failure	All sections damaged
2 (PM2)	4500000 cycle	Operational	No
3 (PM3)	3526200 cycle	Operational	Section 1 diode HS wire 1 and 8 section 3 diode LS wire 6 to 10 Section 4 diode LS wires 8 to 10
4 (PM4)	2512800 cycle	Operational	No

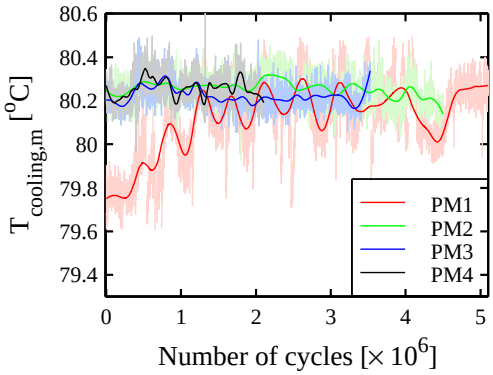
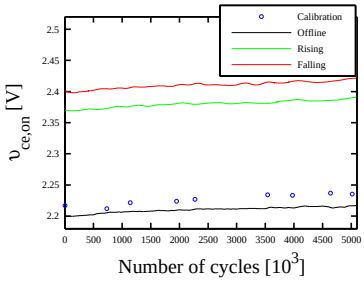


Fig. 6.5: Liquid cooling temperature variation during the wear out test of four power modules.

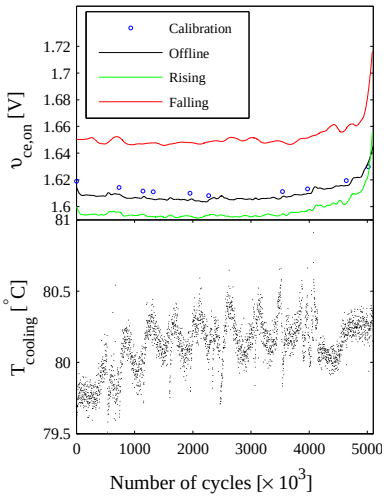
6.2.2 Wear Out Monitoring Results

A summary of the $v_{ce,on}$ rise in the failed module for $I_{DUT,L}$ and $D_{DUT,L}$ measured using three strategies (see 6.1) at 80 ± 1 °C cooling temperature are demonstrated in Fig. 6.6.

In the calibration and the offline characterization methods, the power dissipation is minimal in comparison to the normal operation, hence the voltage drop is lower. However, a trend of rise in voltage due to ageing is similar irrespective of the measurement methods. Fig. 6.6 includes the evolution in voltage in both rising and falling sides of the sinusoidal current, where the voltage is higher on the falling side because of a higher chip temperature, resulting in a bigger thermal resistance.



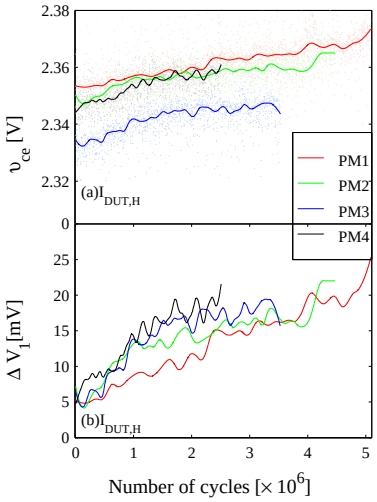
(a) LS IGBT measured at 900A.



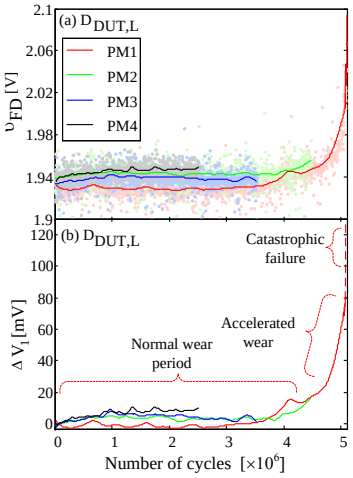
(b) LS diode measured at 550A.

Fig. 6.6: Ageing measurement using three strategies: calibration, offline characterization, and normal operation for LS IGBT and diode at 900 A, 80 ± 1 °C.

The on-state voltage evolution and ΔV_1 for $I_{DUT,H}$ are shown in Fig. 6.7a. Similarly, Fig. 6.7b shows the on-state voltage evolution and ΔV_1 for $D_{DUT,L}$. Figs. 6.6-6.9 show the variation in conduction voltage drop for A-TC modules at similar working conditions as presented in Table 6.2. The difference in off-set of the forward voltage observed between the test modules may be appeared from the variations in the module production. The initial on-state $v_{ce,on}$ varies by nearly 20 mV to 30 mV in both HS and LS IGBTs. However, it is clear from ΔV_1 in Figs. 6.7a and 6.7b, that the voltage rise follows a similar trend with a number of cycles. Similarly, HS and LS diodes have 20 mV variation between the four modules. Fig. 6.7b shows the change in ΔV_1 for $D_{DUT,L}$, which also shows that the increased offset does not indicate potential early failures. In Fig. 6.7b, the v_{FD} increases significantly between 4 MC and 5 MC giving an indication of a large change in resistance of PM1. The voltage drop was increased by 135 mV just before the explosion, which is nearly a 7 % rise in the initial voltage drop. The $v_{ce,on}$ on the LS IGBT is also increased by nearly 20 mV, which is close to a 1 % rise indicating the IGBT did not fail initially. Step increments in v_{FD} are observed after 4.5 MC cycles of operation, indicating a possible bond wire lift-off during the operation. Nearly, 7-10 mV step increments are witnessed for the LS diode of PM1. This is consistent with the micro-sectioning results presented in Chapter 7. Here, the bonded interfaces were identified as clear weak spots in the module geometry, and several lifted or delaminated wires were observed. Fig. 6.8



(a) HS IGBT measured at 900A.



(b) LS diode measured at 900A.

Fig. 6.7: Power cycling at a cooling tempertaure at 80 $^{\circ}C$ on $D_{DUT,L}$.

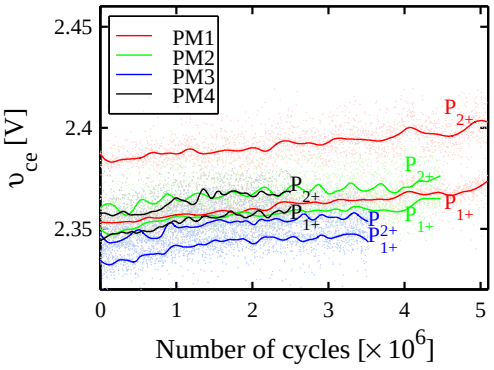
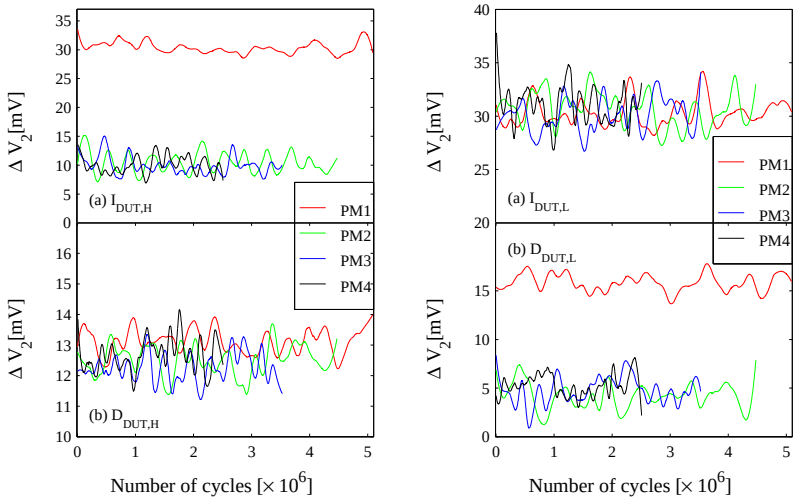


Fig. 6.8: On-state $v_{ce,on}$ comparing $I_{DUT,H}$ (Vce, P_{1+}) and $(Vce, P_{2+}$ at 900 A.

demonstrates the on-state voltage evolution at P_{1+} and P_{2+} on $I_{DUT,H}$. Fig. 6.9a demonstrates the ΔV_2 for $I_{DUT,H}$ and $D_{DUT,H}$ respectively as described in Eqs. (6.2) and (6.3). Similarly, Fig. 6.9b demonstrates ΔV_2 for $I_{DUT,L}$ and $D_{DUT,L}$. Fig. 6.9 shows the thermal response of the HS and LS components of the module. The sample with a mean value above the others appear to be the same sample displaying a higher variation in baseplate temperature in the cooling, see Fig. 6.5. This could indicate the difference in cooling conditions. The amplitude of oscillations appears on the scale of 5-8 mV, which is expected to be due to the standard noise during the measurement. The



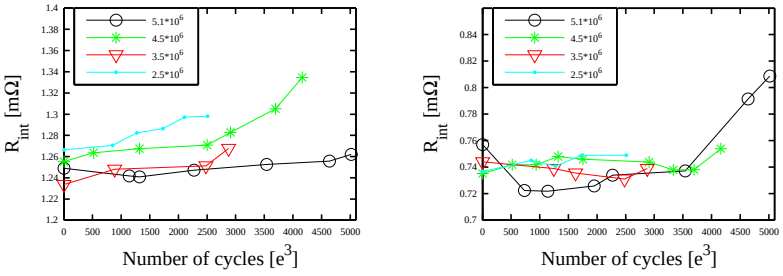
(a) ΔV_2 at $I_{DUT,H}$ and $D_{DUT,H}$. **(b)** ΔV_2 at $I_{DUT,L}$ and $D_{DUT,L}$.

Fig. 6.9: Power cycling at a cooling tempertaure at 80 $^{\circ}C$ and at 900 A.

lack of change in thermal response shows that the solder is not degrading on a large scale, which changes the signal above the standard deviation. The reason for this is also proven in [4] where a four point probing is to single out degrading elements.

6.2.3 Rise in Interconnection Resistance

The interconnection resistance represents a total equivalent resistance during turn-on. This is contributed by interconnects such as copper terminals, bond wires, chip metallization, and chip solder. A Shockley together with a resistor



(a) LS IGBT. **(b)** LS diode.

Fig. 6.10: Rise in interconnection resistance from progressive degradation of materials in a module.

model is used and is fitted using Newton-Raphson iteration to the resistance from the calibration, given by Eq. (5.7) in chapter 5. Fig. 5.20 shows a change in the resistance as a function of calibrated temperature. Using this model, the temperature coefficients found were $0.0042/K$, which is close to the coefficient for Al. This suggests that the resistance is mainly contributed by bond wires and metallization. From the repetitive calibration conducted at different lifetimes, the evolution in R_{int} is extracted. Especially, in the LS diode, the R_{int} is increased largely as expected from the $v_{ce,on}$ measurement. The resistance is increased by nearly 7.8 % from the calibration conducted at 5 MC, which failed at 5.1 MC.

References

[1] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, pp. 653 – 667, 2002.

[2] P. Ghimire, A. de Vega, S. Beczkowski, S. S.Munk-Nielsen, B. Rannestad, and P. B. Thgersen, "Improving power converter reliability: Online monitoring of high-power igbt modules," *IEEE Industrial Electronics Magazine*, vol. 8, no. 3, pp. 40–50, Sept 2014.

[3] P. Ghimire, K. B. Pedersen, A. R. d. Vega, B. Rannestad, S. Munk-Nielsen, and P. B. Thgersen, "A real time measurement of junction temperature variation in high power igbt modules for wind power converter application," in *Proc. of 8th International Conference on Integrated Power Systems (CIPS)*, Feb 2014, pp. 1–6.

[4] K. B. Pedersen, L. H. Ostergaard, P. Ghimire, V. Popok, and K. Pedersen, "Degradation mapping in high power igbt modules using four-point probing," *Microelectronics Reliability*, 2015, doi:10.1016/j.microrel.2015.05.011.

Chapter 7

Physics of Failure Analysis of Power Modules

Understanding of physics behind given failures of power modules is important to optimize a reliability oriented design [1], [2]. Generally, failure investigations are conducted on damaged components, rather than the process itself destroying the components catastrophically [3], [4]. Hence, the investigation of degradation evolution in power modules prior to a catastrophic failure yields the possibility of enhancing a lifetime estimation model and improving the present design of the component layout [5].

In this chapter, post-mortem investigations of A-TC power modules subjected to different numbers of load cycles are presented. The brief results obtained from two approaches: four-point probing and micro-sectioning are presented [5], [4]. Four-point probing is used to characterize the A-TC modules in a non-destructive manner, whereas micro-sectioning is used for analysing wire/chip interface and bond wire degradation. This investigation also ensures the validity of online monitoring in operation, presented in chapters 4 and 6.1. The post-mortem measurement methods and the test setup preparations are already discussed in the thesis [6] and also included in the papers [5], [4].

7.1 Four-Point Probing

Four-point probing is a common technique for high resolution measuring of local electrical properties in semiconductor chips, as well as fracturing or degradation in various conducting structures [5], [7], [8]. The concept is based on having two current carrying terminals attached to the sample, while placing two probes in between for measuring the potential difference across

the region of interest. The different measurement schemes are shown in Fig. 7.1. All measurements are performed by applying a current from 0 to 5 A in

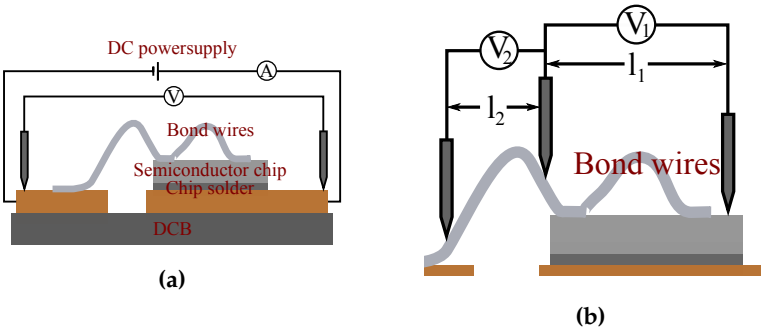


Fig. 7.1: Illustration of the different probing configurations for (a) measuring on the section terminals, and (b) bond wire measurements, from [9].

steps of 0.4 A to the section terminals. The details of the measurement are presented in [5].

Only selected sections are used to conduct the four-point probing approach. It was clearly observed that the HS and LS of the modules are degraded differently. This is in accordance with the temperature field experienced by the HS and LS, see [10]. It was found that the LS diodes experience higher thermal stresses affecting the bond wires and failed initially as presented in chapter 6.1.

7.1.1 Four-Point Probing Results

Measurements conducted through the terminals to the chip surface shows a gradual rise in differential voltage for the HS diode and the LS diode as shown in Fig 7.2. In the LS diode, maximal change is observed for PM2. This rise in voltage with increased power load can be related to either solder degradation, metallization reconstruction, or production variation [9].

The bond wire degradation is observed by monitoring a current distribution in ten wires in all sections of the power modules. The current is well distributed in the diodes except at the edge wires see Fig. 7.3a, which also explains the similar length of bond wires. As expected from online monitoring during the test, the current distribution for stressed modules in LS diodes differed significantly from that of new modules compared to the HS diode as shown in Fig. 7.3a. In IGBTs, central wires carry higher current for both LS and HS, see Fig. 7.3b. However, compared with LS diodes, the current distribution through the IGBT wires does not change in A-TC modules. Four-point probing is conducted through metallization including chips, solder and bond wires, and used to calculate bond wire effective resistance using bond

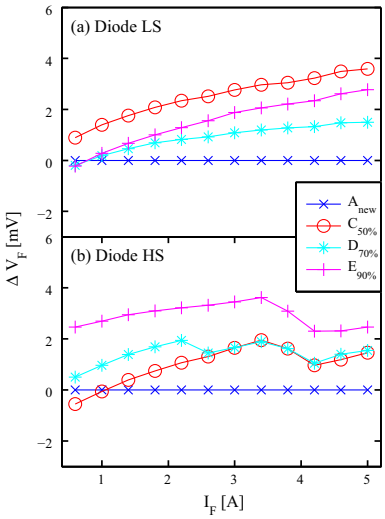
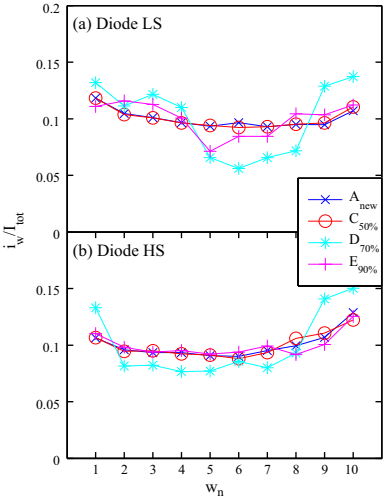
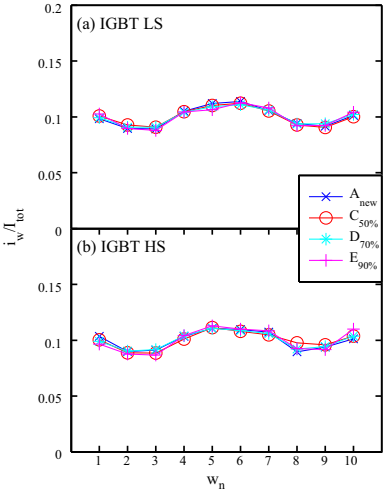


Fig. 7.2: Differential voltage as function of current measured from terminal to metallization for the (a) LS and (b) HS diodes, for a fresh and active thermal cycle power modules, see [9].[In legend A_{new}: fresh module, $C_{50\%}$: 2.5 MC, $D_{70\%}$:3.5 MC, $E_{90\%}$:4.5 MC]



(a) The current distribution for LS and HS diode bond wires.

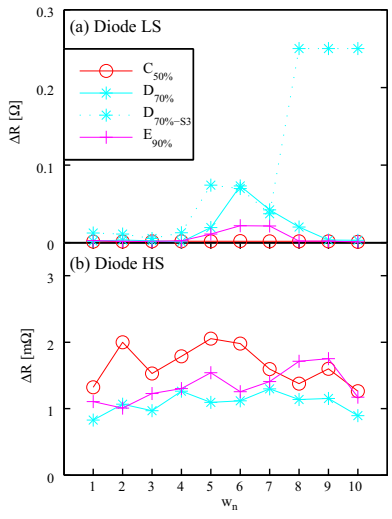


(b) The current distribution for the LS and HS IGBT bond wires.

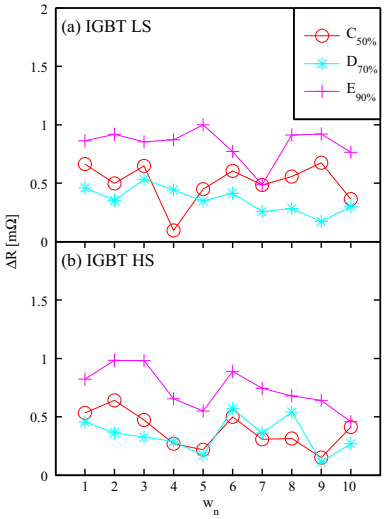
Fig. 7.3: The current distribution for the LS and HS diode and IGBT bond wires for fresh and active thermal cycle power modules. First axis shows wire numbering. Second axis presents fractional current, i.e. the ratio of the current going through the wire to the total current applied to the device, from [9].[In legend A_{new}: fresh module, $C_{50\%}$: 2.5 MC, $D_{70\%}$:3.5 MC, $E_{90\%}$:4.5 MC]

wire current with a voltage drop across the wires. Here, the changes in effective resistance of bond wires on the LS and HS are presented, see Figs. 7.4a and 7.4b. It is observed that the wire resistance of the stressed modules for both the diodes and IGBT's has a small increase (on the scale of $m\Omega$), except for the LS diodes. A clear tendency of increased wear in the LS diodes is observed, where resistance change is in Ω compared to $m\Omega$ on the HS. The increase in the effective resistance for the A-TC modules is significant especially for the central wires in the LS diode. The degradation pattern in Fig.7.4a is not proportional to the number of A-TC, which is suspected to be related to fabrication variation. This can be illustrated by excluding sample $D_{70\%} - S_3$, where severe damage was observed on a specific section.

Change in resistance of the IGBT chip's wire bonds is consistent with numbers of cycles and the degree of degradation between LS and HS of IGBT is on the same level, see Fig.7.4b.



(a) Change in effective wire resistance for the LS diode and HS diode.



(b) Change in effective wire resistance for the LS and HS IGBT.

Fig. 7.4: Change in effective bond wire resistance for IGBT and diode of new and power modules subjected to different numbers of cycles, from [9].[In legend $C_{50\%}$: 2.5 *MC*, $D_{70\%}$:3.5 *MC*, $E_{90\%}$:4.5 *MC*]

7.2 Microscopy Analysis

This section presents results obtained using microscopy analysis using two approaches: micro-sectioning and scanning electron microscopy (SEM) combined with focused ion beam milling (FIB) for A-TC power modules. The

method is used to analyse the current state of stressed power modules. The wire/chip cross section is obtained through micro-sectioning combined with optical microscopy, see [4].

7.2.1 Micro-Sectioning

The Micro-sectioning approach, as described in [4], is used for characterizing the microscopical processes occurring at interfaces of A-TC modules. High resolution images of metallization surfaces and cross-sections of interfaces are obtained using a Zeiss 1540 Xb SEM/FIB.

7.2.2 Results

Bond Wire Degradation

Normally, heel cracks and wire lift-off are two major failure mechanisms in wire bonds. Both are induced by thermo-mechanical stress because of CTE mismatch and wire flexure. Wire lift-off is observed in the step rise of an on-state voltage drop [11]. Lifting of a wire creates a domino effect, where surrounding wires are stressed more because of a non-homogeneous current distribution after initial lift-off. This causes an additional lift-off resulting in a catastrophic failure at an accelerated rate [12]. Fig. 7.5 shows a cross-sectional image of the wire and chip interface on a top side of a fresh diode. It is seen that the stitch bonds tend to be poorly terminated on the right hand side, which displays a possible source of fracture initiation.

A cross sectional cut of an IGBT bond wire interface from a sample sub-

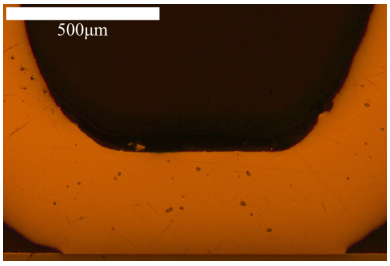


Fig. 7.5: Wire/chip interface on diode of a fresh module, from [13].

jected to 4.5 *MC* is presented in Fig. 7.6. A clear tendency of wire lift-off through partial wire fracturing and wire delamination is observed. The delamination is observed between the wire and the metallization as normally observed. The fracture is propagating inside the wire itself due to bond wire fracture strength. The wire lift-off process in the modules subjected to different numbers of cycle are presented detail in [13]. Initially, fractures tend to

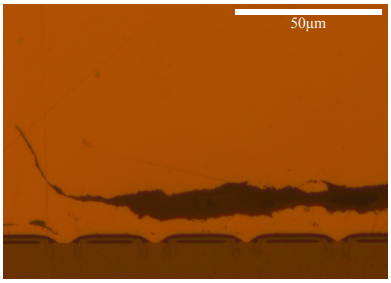


Fig. 7.6: A cross sectional cut of IGBT bond wire interface, from [14].

propagate between wire and metallization. At later stages the crack moves inter-granularly inside the wire itself combined with trans-granular fracture across certain ranges. Fig. 7.7 shows a wire and chip interface of end bond on IGBT subjected to 4.5 *MC* highlighting a fracture area, position of the crack tip and an trans-granular fracture [13]. The observed phenomenon of com-

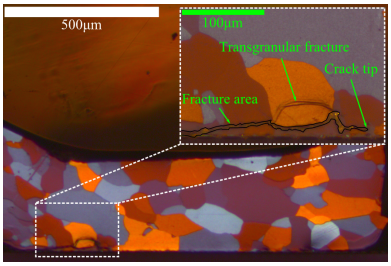


Fig. 7.7: Wire/chip interface end bond on IGBT from 3.5MC module. The insert illusartes the fractured area, poistion of the crack tip, and and transgranular figure. from [13].

bined delamination and fracturing was observed in the majority of samples, both IGBTs and diodes, subjected to a high number of cycles. Fig. 7.8 shows an image of a lifted wire with a clear indication of the bond footprint, wire residue from the fracture process, and discharge spots created in the final steps of lift-off.

Metallization Reconstruction

Metallization reconstruction is a gradual ageing process affected by temperature peak and variation [12]. In parallel with bond wire degradation, the severe diode chip metallization reconstruction was observed in A-TC power modules. Figs. 7.9 and 7.10 present topographic images of the surface metallization. A clear difference between the IGBT and diode metallization is observed. This is in accordance with the power loss distribution and on-line monitoring. While the IGBT metallization seems unaffected after 3.5 *MC*, the

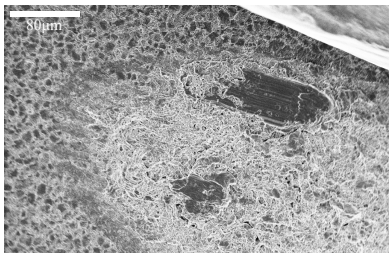
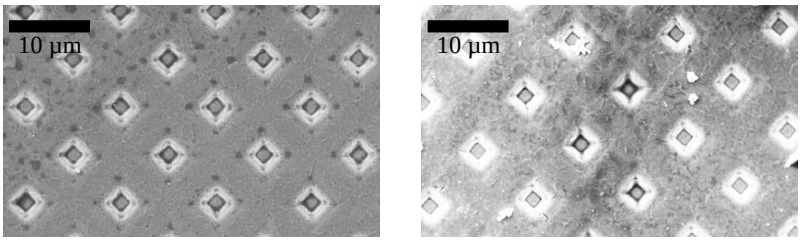
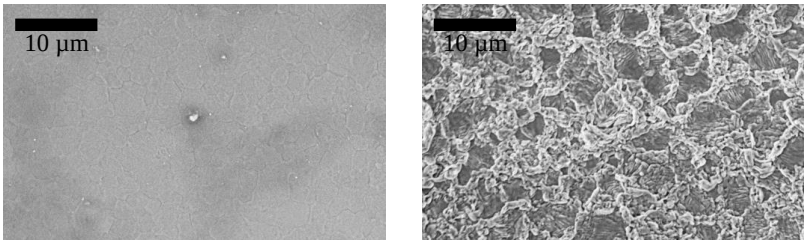


Fig. 7.8: A SEM image of lifted bond wire, from [14].



(a) A new IGBT. **(b)** 3.5MC IGBT.

Fig. 7.9: SEM images of the metallization surface of IGBT on power modules (a) for a fresh IGBT and (b) after 3.5MC of operation on a IGBT, from [11].



(a) A new low side diode. **(b)** 3.5MC low side diode.

Fig. 7.10: SEM images of the metallization surface of IGBT on power modules (a) for a fresh LS diode and (b) after 3.5MC of operation on a LS diode, from [11].

diode metallization is severely reconstructed. Fig. 7.11 presents an SEM image of a focused ion beam cut into the LS diode metallization. As indicated in the image, in the later stages of its lifetime the reconstruction changes from surface effects to creation of cavities. This will affect sheet resistance and thereby on-state resistance. Additionally, a tendency of *Si* diffusion into the metallization is observed in the sample subjected to a higher number of cycles. There was only limited reconstruction in the IGBT chips indicating the temperature load is not high enough to activate the reconstruction process. The metallization reconstruction process between edge and centre of

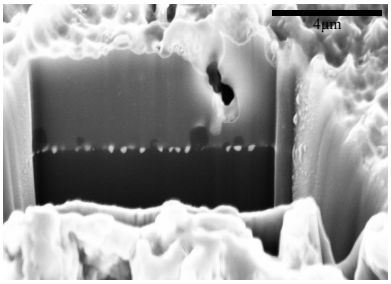


Fig. 7.11: Diode metallization SEM/FIB cross-sectional image, from [14].

the diode chip surface is compared and presented in [13]. A significant difference is observed between center and edge and the degree of degradation observed is proportional to the function of the number of cycles. This suggests that the metallization reconstruction is a thermally induced low cycle fatigue process.

References

[1] Mauro Ciappa. Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, 42:653 – 667, 2002.

[2] W. Kanert. Active cycling reliability of power devices: Expectations and limitations. *Microelectronics Reliability*, 52(9-10):2336 – 2341, 2012.

[3] Jens Goehre, Martin Schneider-Ramelow, Ute Geibler, and klaus Dieter lang. Interface degradation of al heavy wire bonds on power semiconductors during active power cycling measured by the shear test. In *Conference on Integrated Power Elctronic Systems (CIPS)*, 2010.

[4] Kristian Bonderup Pedersen, Peter Kjær Kristensen, Vladimir Popok, and Kjeld Pedersen. Micro-sectioning approach for quality and reliability assessment of wire bonding interfaces in igbt modules. *Microelectronics Reliability*, 53(9-11):1422 – 1426, 2013.

[5] K.B. Pedersen, P.K. Kristensen, V. Popok, and K. Pedersen. Degradation assessment in igbt modules using four-point probing approach. *IEEE Transactions on Power Electronics*, 30(5):2405–2412, may 2015.

[6] Kristian Bonderup Pedersen. *IGBT Module and Reliabilty (Physics of Failure Based Characterization and Modelling)*. PhD thesis, Aalborg University, December 2014.

[7] L. Valdes. Resistivity measurements on germanium for transistors. In *Proceedings for the IRE*, pages 420–427, 1954.

[8] S. Pietranico, S. Lefebvre, S. Pommier, M. Berkani Bouaroudj, and S. Bontemps. A study of the effect of degradation of the aluminium metallization layer in the case of power semiconductor devices. *Microelectronics Reliability*, 51(9-11):1824 – 1829, 2011.

[9] Kristian Bonderup Pedersen, Lotter Haxen Ostergaard, Pramod Ghimire, Vladimir Popok, and Kjeld Pedersen. Degradation mapping in high power igbt modules using four-point probing. *Microelectronics Reliability*, 2015. doi:10.1016/j.microrel.2015.05.011.

[10] K.B. Pedersen and K. Pedersen. Dynamic electro-thermo-mechanical simulation of material degradation in high power igbt modules. *IEEE Transactions on Power Electronics*, (99), 2015. DOI: 10.1109/TPEL.2015.2426013.

[11] P. Ghimire, K. B. Pedersen, S. Rannestad, B.and S.Munk-Nielsen, and F. Blaabjerg. Real time wear out monitoring test setup for high power igbt modules. Submitted.

[12] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani. Ageing and failure modes of igbt modules in high-temperature power cycling. *IEEE Transactions on Industrial Electronics*, 58(10):4931–4941, Oct. 2011.

[13] Kristian Bonderup Pedersen, Lotter Haxen Ostergaard, Peter Kjær Kristensen, Pramod Ghimire, Vladimir Popok, and Kjeld Pedersen. Degradation evolution in high power igbt modules subjected to sinusoidal current load. *Journal of Material Science: Materials in Electronics*, pages 1–8, October 2015.

[14] Pramod Ghimire, Kristian Bonderup Pedersen, Bjorn Rannestad, and Stig Munk-Nielsen. Ageing monitoring in igbt module under sinusoidal loading. *Microelectronic Reliability*, 55(9-10):1945–1949, August- September 2015. doi:10.1016/j.microrel.2015.06.025.

Chapter 8

Conclusion and Future Perspectives

8.1 Conclusion

In a life-cycle management of power electronic devices and a full converter, several tests starting from production to end of life are mandatory. This thesis proposes a measurement and field emulated characterization technique for high power modules in the operation of a converter. This work is carried out to optimize end of life investigation of power modules for a laboratory as well as for field applications. Initially, a field emulated advanced power cycling method is shown, where active thermal cycling is performed in a normal converter operation. Normally, it is not possible to simulate real life conditions including all stressors and also cause a failure in a reasonable time-frame. Therefore, accelerated test conditions are employed. In A-TC, there are more degrees of freedom to imply field emulated stress conditions in comparison to P-TC. Furthermore, the power modules can be tested at a nominal rated power in operation.

An online monitoring method to acquire on-state voltage and corresponding load in every switching cycle of a power module is proposed and validated in normal operation. In switching operation, the voltage across the device swings from V to kV in a power converter. There are many challenges implementing measurement during operation mainly: to protect the measurement circuit from high voltage and to maintain the accuracy within a 1 mV are of paramount importance. The measurement resolution in the proposed method is 0.61 mV and the precision is less than ± 2 mV even at high ambient temperatures above $80^{\circ}C$. The measurement of on-state voltage as a function of load cycles gives ageing in real time. Similarly, the trend

of a rise in voltage can be employed as precursor parameter detection and preventive maintenance. The proposed monitoring technique is suitable for well-known state of health monitoring in wide applications including offshore/onshore wind turbines, automotives, aviations, etc. The precursor parameters can be used to generate an alarm signal to make smart decisions on power de-rating/uprating, operation and preventive maintenance, removal of the faulty part to avoid catastrophic failures, etc.

Knowing the temperature of a chip is a key parameter to optimize electrical, thermal design and reliability studies of power module and converters. A combination of average chip temperature and its cycle induces thermo-mechanical stress in power module interconnects, which limits their power cycling capability. Furthermore, thermal design and power density of converters are designed based on the thermal capability of semiconductor devices. The monitoring of temperature in operation could enable the operation of the converter within a safe limit. Although various temperature measurement methods are identified, a $v_{ce,on}$ - load current measurement method is proposed. One can use this method in converter without modification of structure and control. However, several parameters need to be considered to ensure accuracy in the measurement such as rise in voltage from ageing in interconnection, contribution in voltage drop from internal resistance, and discrepancies in power module from production. Hence, a calibration process and finding of correction parameters are presented and the method is also validated using IR thermography in an open module. The investigation of temperature distribution in an open module in a full scale converter is presented in detail.

Often, understanding of failure mechanism is difficult, as information is usually lost in catastrophic events. Hence, online monitoring in converter operation facilitates investigations of the ageing and assists with indicating root cause of failures. This could give valuable insight in field applications to identify the root cause of failures and also to make a smart decision for preventive maintenance. Wear out tests are performed where four power modules are subjected to different numbers of cycles at similar loadings. An online monitoring, offline characterization and repetitive calibration are conducted during the test. On-state voltage and rise in interconnection resistance are used as ageing parameters. A data evaluation theory is proposed to separate two different failure mechanisms: bond wire fatigue and solder layer degradation. The method automatically re-calibrates on each individual device which is essential removing the effects from a difference in a geometry of power module. Usually bond wire and solder fatigue are two major known low thermo-mechanical failures.

In order to validate the online monitoring results as well as map the degradation distribution, four-point probing and micro-investigations using micro-sectioning approaches are presented for active thermal cycled mod-

ules. Typically, interconnection related failures are the most common in active thermal cycled devices. The four-point probing indicates the bond wire interfaces are the weakest points. A clear tendency of wire-lift off related failure mechanisms are observed. The process is observed as a hybrid of wire de-lamination and actual fracturing. A severe metallization reconstruction appears on the diode in comparison with IGBT showing it is thermally induced. The mean chip temperature in diodes is higher than the IGBTs. Furthermore, reconstruction is significantly increased near the chip center than the edges. At the later stages of their lifetime the reconstruction changes from surface effects to creation of cavities, which will affect sheet resistance and thereby on-state resistance.

8.2 Future Perspectives

Response time of on-state voltage measurement circuits can be improved by using faster response SiC diodes. The fabrication of two diodes in the same packaging could enhance thermal coupling between the two. For higher frequency applications, the settling time required by the circuit should be reduced. The integration of such measurement circuitry in a gate driver broadens the applications and the capability of existing gate drivers.

The thermal dynamics of chip and packaging can be investigated and integrated with other parameters such as cooling temperature, gate-emitter voltage turn on or off characteristics to ensure accuracy in estimating the junction temperature.

The monitoring technique can be integrated with a field data logger. Together with ageing performance, the chip temperature information would increase the robustness of a system. There are wide area of applications where the method can be used.

Intelligent new functions like lifetime control and marginal operation cost calculators could target optimal operation and future real time market response [1]. Integration of smart monitoring in other parts of the system such as blades, tower, gearbox, generator, pitch and yaw drives in wind turbines, enables production reduction cleverly during high wind periods with low energy prices. In future, wind power plants based on modern wind turbines will have high market penetration, where control, communication and monitoring of overall systems play a significant role.

8.2.1 Performance Improvement

Smart control functions can be built using smart monitoring systems in operation. The control functions are applicable to several applications:

- Derating/ uprating control of power converters in real application,

- Preventive maintenance, generate alarms and warning signals,
- Power limit detection,
- Short term overload control.

8.2.2 Reliability

Such measurement systems can be employed directly in reliability studies as well as reliability improvement in power converters.

- Field monitoring,
- Prognostic and health monitoring,
- Generate ageing or lifetime models,
- Failure investigation, obtain a root cause of failure,
- Advanced active thermal cycling in advanced power modules including Wide Band Gap (WBG) devices and their characterizations during the test period.

References

[1] Paul Bach Thøgersen. Converter solutions for wind power. In *EWEA*, 2012.