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High Performance Design of 100Gb/s DPSK Optical Transmitter

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Abstract – High performance communication systems require high performance devices for exchanging information at a faster rate. These devices are experiencing several challenges e.g. bandwidth limitations, power limitations, design limitations and etc. The existing techniques are lacking in providing high performance output simultaneously by maintaining actual parameters of device. In this work, high performance 100Gb/s optical DPSK transmitter design is realized in Field Programming Gate (FPGA) using time constraint technique. Before applying the proposed technique actual FPGA's frequency was 0.2 GHz and optical transmitter have taken plenty of time for transmitting signal. When proposed design is operated at 1 GHz, 5 GHz, 10 GHz and 20 GHz using time constraint technique, it is observed that among all these frequencies, at 10 GHz high performance output is achieved for designed optical transmitter. This high performance design of optical transmitter has zero timing error, low timing score and high slack time due to synchronization between input data and clock frequency. It is also determined that 99% timing score is reduced in comparison with 1 GHz frequency that has high jitters, high timing error, high time score and low slack time. The high performance design is realized without disturbing actual bandwidth, power consumption and other parameters of the design. The proposed high performance design of 100Gb/s optical transmitter can be used with existing optical communication system to develop high performance communication system for future generation networks.

Keywords – Differential Phase Shift Keying (DPSK), High performance devices, Laser Signal, NRZ modulator, Optical transmitter, Synthesis constraints.

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I. INTRODUCTION

An optical transmitter is an initiation device, which play significant role in high-speed communication systems. Normally, optical transmitter is configured using either direct modulation or external modulation scheme [1]. External modulation scheme is preferred in Gb/s communication systems [1]. External modulation based optical transmitter requires electrical signal, laser signal and modulator to produce optical signal [1]. External modulation is further classified in modulation type and modulation format such as; Non-Return-to-Zero (NRZ) and Return-to-Zero (RZ), On-Off Keying (OOK) schemes with modulation formats i.e. amplitude, (OOK) or phase format, Phase Sift keying (PSK) [1]. Among these, PSK format with NRZ scheme is widely used because it provides the high resilience to noise with 3 dB sensitivity of receiver [2]. Although, PSK based NRZ scheme is widely utilized but these techniques are not capable enough to produce high performance output for high-speed Gb/s transmission system [2].

High performance optical transmitter are required to fulfill the demand of efficient, reliable and quick communication system design [3]. High performance design of optical transmitter is restricted due to power consumption, bandwidth, design and other issues [3]. Because as high-speed transmission demand increase high power components, high bandwidth and complex design of device is required to achieve high performance design goal [3]. This confined to lower down the system performance. In communication system design, high performance device is ultimate goal for designers in achieving the reliable communication [3]. However, several efforts have been taken to design high performance based communication devices.

For example, by optimizing optical modulation amplitude [4], green routing [5], IP forwarding [5], queening theory [5], stochastic process [5], energy efficient network access [5], high-speed current controllers [5], sleep mode techniques [5] and many more in [5]. These techniques are helpful for performing transmission of 10Gb/s data rate [5]. Nevertheless, high performance limitation is still wandering devices in designing the high-speed communication system. In this regard, using Field Programming Gate Array (FPGA) based

Very Large Scale Integration (VLSI) many systems are acknowledged that are designed using chip [6]. For instance, 100Gb/s Ethernet systems [7], power optimization of pseudo noise based optical transmitter [8]. The high performance issue is recently investigated using clock gating and others [9]. Nevertheless, to the best of this study none of the techniques promise for high performance operation of 100Gb/s communication devices.

In this work, high performance 100Gb/s optical DPSK transmitter is designed in FPGA using timing constraints technique. For proposed design different timing parameters for 100Gb/s optical transmitter are calculated to produce high performance output using time constraint technique. The proposed design delivers proficient, consistent and speedy transmission of Gb/s data rate. The developed design will be utilized in high speed communication systems as high-end feature device for fiber optic networks.

II. RESEARCH FRAMEWORK FOR HIGH PERFORMANCE DESIGN OF 100Gb/s OPTICAL DPSK TRANSMITTER

High performance design of 100Gb/s optical DPSK transmitter (target device) is demonstrated as shown in Fig. 1.

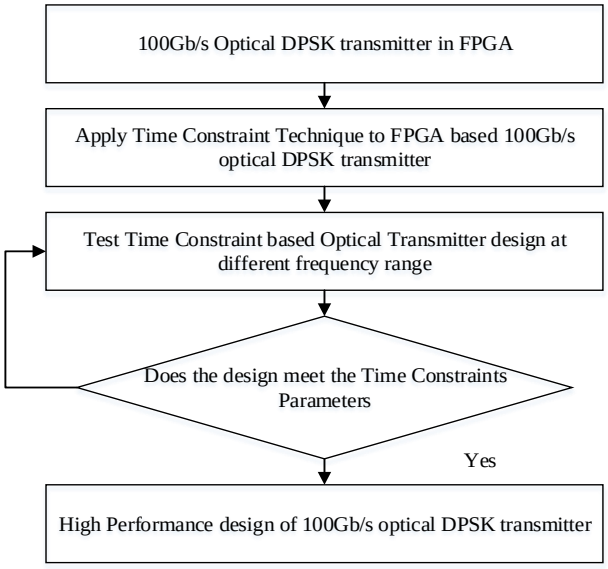

Fig. 1. Research frame work of high performance design of 100G/s optical DPSK transmitter

The research frame work is executed in different steps. In first design step, numerical model of target device is modeled and after that design is realized in FPGA using vhdl coding. In second design stage, time constraint technique [10] is applied over FPGA based design of target device. High performance design of target device is achieved that can produce minimum time score, zero timing error, zero phase error and zero discrete jitter at applied input frequency. In third design step, 100Gb/s optical DPSK transmitter design using time constraint is tested at different frequencies, 1 GHz, 5 GHz, 10 GHz and 20 GHz. Frequency at which time constraint based 100Gb/s optical DPSK transmitter is producing minimum time score, zero timing error and minimum jitters will produce high performance output for target device. Finally, high performance design of 100Gb/s optical DPSK transmitter is developed using proposed technique.

III. NUMERICAL MODEL OF 100GB/S OPTICAL DPSK TRANSMITTER AND ITS FPGA BASED DESIGN

FPGA based 100Gb/s optical DPSK transmitter is designed in two stages. In first stage, the optical transmitter is designed numerically. In second stage, FPGA based 100Gb/s optical DPSK transmitter is implemented using vhdl coding along with Register Transfer Logic (RTL) schematic design of target devices is created in Xilinx Vivado

A. Numerical Model of 100Gb/s Optical DPSK Transmitter

100Gb/s optical DPSK transmitter is designed using external modulation scheme with 100Gb/s Pseudo Random Binary Sequences (PRBS), Fabry-Perot laser diode and NRZ modulator. The numerical model is developed by generating the 100Gb/s DPSK signal using DPSK sequence and PRBS and modulating this signal with laser signal. Fig. 2 describes model for 100Gb/s optical DPSK transmitter.

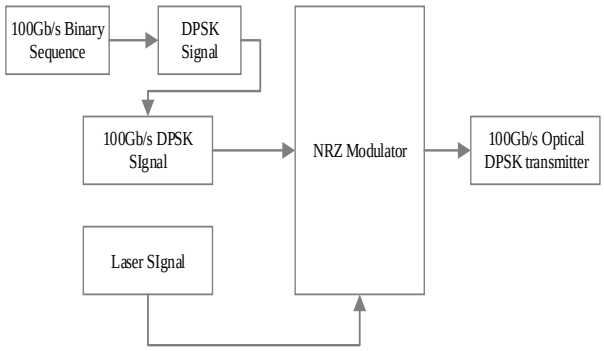

Fig. 2. 100Gb/s Optical DPSK transmitter model

Input binary sequence is generated using 8 bit bn at sample rate of 100Gb/s. The DPSK format signal is expressed as shown in (1) [2]. Where DDPSK(t) is DPSK format signal, K is constant and fc is carrier frequency.

$$D_{DPSK}(t) = kb_n(t)\cos 2\pi f_c t \tag{1}$$

100Gb/s DPSK signal is generated by exclusive-OR operation of input binary sequences and DPSK format signal of current value and pervious value so that phase relation can be incurred for sequence. 100Gb/s DPSK signal for 8 bit binary sequence is described in (2).

$$B_{DPSK}(t) = b_n D_{DPSK}(t) \oplus \overline{b_{n-1}}\,\overline{D_{DPSK}(t)} \tag{2}$$

After that, laser signal will be generated and it will be modulated with 100Gb/s DPSK signal to generate the optical transmitter for 8 bit transmitted sequence. Laser signal is generated using Fabry-Perot laser diode. Transfer function of Fabry-Perot laser diode is shown in (3) [11]. Where Lfp is laser signal f is laser frequency given (4) [11], β is dumping frequency given (5) [11];

$$L_{fp} = \frac{f^2}{f^2 - 4\pi^2 f^2 + i\beta 2\pi f} \tag{3}$$

$$f = \frac{I_o - I_{in}}{\tau_c \tau_p I_R} \tag{4}$$

$$\beta = \frac{I_o}{\tau_c I_R} \tag{5}$$

100 Gb/s optical DPSK transmitter is developed by applying NRZ modulation scheme to laser signal in (3) and binary DPSK signal in (2). For this a carrier signal i.e. *Lfp* laser signal is phase modulated in (7). Θ is instantaneous phase of carrier signal and sinusoidal varying in proportion to original signal.

$$E_o(t) = L_{fp} Sin\theta \tag{6}$$

Therefor after NRZ modulation, the instantaneous phase of laser signal will be as in (7).

$$\theta = 2\pi ft + AB_{DPSK}(t)\cos 2\pi f_c(t) \tag{7}$$

In (7) $A{\cdot}B_{DPSK(t)}$ is termed as modulation m and will be rewritten as m= $A{\cdot}B_{DPSK(t)}$, insert in (7) will yield (8);

$$\theta = 2\pi ft + m\cos 2\pi f_c(t) \tag{8}$$

Insert (8) in (6), will formulate (9);

$$E_o(t) = L_{fp} Sin(2\pi ft + m\cos 2\pi f_c(t)) \tag{9}$$

100Gb/s optical DPSK transmitter signal is generated by NRZ modulation of DPSK signal and laser signal as in (9). In next stage, 100Gb/s optical DPSK transmitter is developed in FPGA.

B. RTL Schematic of 100Gb/s Optical DPSK transmitter in Xilinx

The FPGA design of 100Gb/s optical DPSK in (9) is realized by developing the vhdl code for each module developed numerically as in (2) for DPSK signal, in (3) for laser signal, in (7) for NRZ modulated signal. Furthermore, RTL schematic is also developed for numerically modeled 100 Gb/s optical DPSK modulator. The top view of designed 100Gb/s optical DPSK transmitter of RTL schematic in FPGA is shown in Fig. 3. RTL schematic diagram of 100Gb/s optical DPSK transmitter consist five inputs Clk pulse of 0.2 GHz; 100Gb/s DPSK signal as generated in (2); laser signal generated using (3); NRZ modulated signal generated in (7); shiftEn pulse of enabling and disabling the modulation operation.

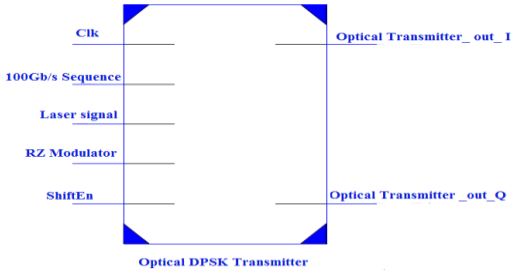

Fig. 3. 100Gb/s optical DPSK transmitter RTL schematic top view

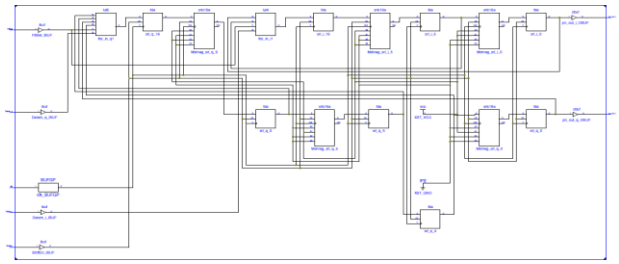

Fig. 4. Complete RTL schematic of 100Gb/s optical DPSK transmitter

FPGA design of 100Gb/s optical DPSK transmitter has two outputs; one is amplitude signal optical transmitter_output_I and other is quadrature signal optical transmitter_output_Q. However, both signal can be combined to produce unified 100Gb/s optical DPSK signal. The inside layout of RTL diagram as described in Fig. 4 is very complicated and composed of several components that includes input output buffer, shift registers and memory blocks due to complexity the diagram may not visible clearly.

IV. APPLY TIME CONSTRAINT TECHNIQUE OVER FPGA BASED 100GB/S OPTICAL DPSK TRANSMITTER

In FPGA, there are various constraints are available such as; synthesis, implementations, grouping, logical, physical, placement and etc. constraints [10]. These constraints are attribute that affects an instantiated design's functionality and are defined in the design using vhdl coding [10]. In high-performance applications, synthesis constraints based timing constraint is used widely in communication system. Because, it provides direct synthesis tool optimization technique for a particular design to improve the response time of the signal [10]. Timing Constraint enables you to specify any nets or paths in your design by define the start and end points can be flip-flops, I/O pads, latches, or RAMs [10]. Timing constraints provides timing analysis for your design that includes the several parameters, such as launched clock, data, hold stack, setup slack and etc. as discussed in [10]. All these parameters can be accessed using timing analyzer in Xilinx suite.

In this work, timing constraints in the UCF file of Xilinx based design of 100Gb/s optical DPSK transmitter are defined, using OFFSET_IN and OFFSET_OUT. OFFSET_IN constraint is used to specify timing requirements of an input interface to FPGA that specifies clock and data timing relationship at the external pads of the FPGA [10]. OFFSET_OUT constraint is used to specify the timing requirements of an output interface from the FPGA. It specifies time from the clock edge at the input pin of the FPGA, until data becomes valid at the output pin of the FPGA [10]. The timing constraints provide detailed information of several parameters, in this case only important parameters are considered for analyzing high performance design [10]. These parameters includes such as; slack time, frequency period, timing error, timing score, step hold values [10]. From these parameters slack time is the most important one because it is difference of time required for data and arrival time of data as illustrated in (10) [10].

$$Slack\ Time = Data\ Required\ Time - Data\ Arrival\ Time \quad (10)$$

High slack time will result high performance design for low slack time provides slow output for the design [10].

V. TESTING OF TIMING CONSTRAINT BASED DESIGN OF 100GB/S OPTICAL DPSK TRANSMITTER IN XILINX

Timing constraints based design is realized by specifying different clock frequency. 100Gb/s optical DPSK transmitter Xilinx design is operated at 1 GHz, 5 GHz, 10 GHz and 20 GHz frequencies. Before this, standard frequency was 0.2 GHz for 100 Xilinx based 100Gb/s optical DPSK transmitter. The target device is operated at these frequency to achieve high performance transmission using timing constraints. At each frequencies 1 GHz, 5 GHz, 10 GHz and 20 GHz timing constraints parameters values such as; slack time, frequency period, minimum are recorded. Timing constraints based 100Gb/s optical DPSK transmitter developed in Xilinx is considered to be high performance design if any of input frequencies is fulfilling the criteria shown in Table 1.

TABLE I. CRITERIA FOR HIGH PERFROMANCE DESIGN

Parameters	Values
Slack time	**High**
Frequency period (input frequency period)	**Variable**
Minimum period (time required to execute task)	**Min. +ve**
Timing error (time of delay for task)	**Zero**
Timing score (total time inc. timing error)	**Min. +ve**
Step Hold values	**S=0 , H=0**

A. Testing of Timing constraint based design of 100Gb/s optical DPSK transmitter in Xilinx for 1 GHz

Timing constrain based design of designed optical transmitter is operated at 1 GHz frequency. Table. 2 shows timing constraints parameters for designed optical transmitter at 1 GHz frequency. It is observed that when, designed transmitter is operated at high time period the timing error is around 200 and time score is also high. In this case, this frequency does not fulfill the basic criteria as discussed in Table. 1.

TABLE II. TIMING CONSTRAINTS PARAMETRS AT 1 GHZ

Parameters	Values
Slack time (delay time for task)	**-5.66 ns**
Frequency period (input frequency period)	**1 ns**
Minimum period (time required to execute task)	**6.66 ns**
Timing error (time of delay for task)	**200**
Timing score (total time inc. timing error)	**153269**
Step Hold values	**S=2, H=2**

B. Testing of Timing constraint based design of 100Gb/s optical DPSK transmitter in Xilinx for 5 GHz

It is observed that timing error is reduced from 200 to 85 and also timing score is also reduced for 5 GHz in comparison with, operating the transmitter at 1 GHz as described in Table. 3. It is determined that at 5 GHz basic criteria for high performance design is still not achieved.

TABLE III. TIMING CONSTRAINTS PARAMETRS AT 5 GHZ

Parameters	Values
Slack time (delay time for task)	**-6.566 ns**
Frequency period (input frequency period)	**0.2 ns**
Minimum period (time required to execute task)	**6.66 ns**
Timing error (time of delay for task)	**85**
Timing score (total time inc. timing error)	**42690**
Step Hold values	**S=1, H=1**

C. Testing of Timing constraint based design of 100Gb/s optical DPSK transmitter in Xilinx for 10 GHz

When designed transmitter is operated at 10 GHz, the basic criteria for high performance design is achieved as mentioned in Table. 4. Timing error is zero and minimum timing score with minimum step and hold values. 10 GHz is providing high performance output for design optical transmitter because the given input frequency is completely, synchronized with clock pulse and data, and producing very minimum hold for data. Furthermore, the glitch is minimum because of efficient synchronization. At 10 GHz, slack time is very high because slack time is equal to data required Time – data arrival time. Due to fast arrival of data at output, terminal high performance design of optical transmitter is achieved.

TABLE IV. TIMING CONSTRAINTS PARAMETRS AT 10 GHZ

Parameters	Values
Slack time (delay time for task)	**4.1 ns**
Frequency period (input frequency period)	**0.1 ns**
Minimum period (time required to execute task)	**6.66 ns**
Timing error (time of delay for task)	**0**
Timing score (total time inc. timing error)	**102**
Step Hold values	**S=0, H=1**

D. Testing of Timing constraint based design of 100Gb/s optical DPSK transmitter in Xilinx for 20 GHz

It is extracted from Table. 5 that timing constraint parameters for high performance design are not achieved using 20 GHz. Because timing error is high enough to produce the synchronization between clock and data.

TABLE V. TIMING CONSTRAINTS PARAMETRS AT 20 GHZ

Parameters	Values
Slack time (delay time for task)	**6.2 ns**
Frequency period (input frequency period)	**0.05 ns**
Minimum period (time required to execute task)	**8.66 ns**
Timing error (time of delay for task)	**1105**
Timing score (total time inc. timing error)	**22547**
Step Hold values	**S=3, H=2**

VI. RESULTS AND DISCUSSION

Timing constraint based 100Gb/s optical DPSK transmitter designed in Xilinx is producing high performance output for 100Gb/s optical transmitter. The designed transmitter is producing high performance output at 10 GHz. The timing error is removed 100% with very small timing score and with no jitters and delays. The developed design will produce fast output for optical transmitter in comparison with operating the transmitter at other frequencies. Fig. 6 describes the percentage of parameters used for each frequency. It is defined that at 1 GHz, timing error and slack timing is high. At 5 GHz, the slack time is reduced but timing error is high. At 10 GHz, there is high slack time and zero timing error with low time score. At 20 GHz, slack time is very low with high timing error. The high slack time is producing high performance output for optical transmitter. It is also determined that 99% timing score is reduced due to timing constraint technique.

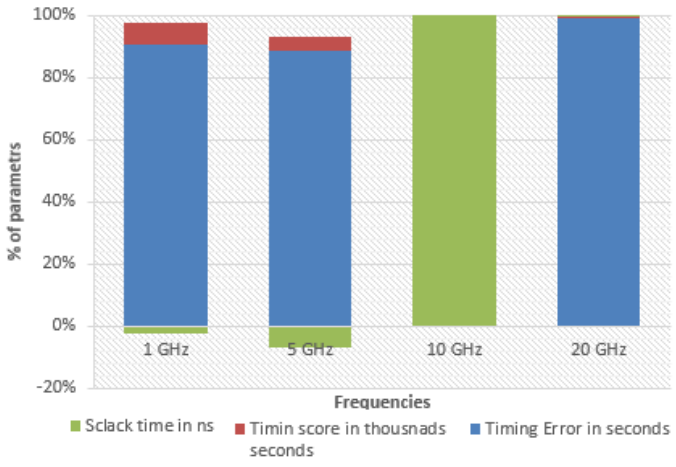

Fig. 5. Tming constaints parametrs

VII. CONCLUSION AND FUTURE SCOPE

In this paper, high performance design of 100Gb/s optical DPSK transmitter is demonstrated using time constraint technique in Xilinx FPGA. It is concluded that using proposed design system is 99% efficient in removing timing error. Furthermore, deigned transmitter provides faster data transmission in comparison with optical transmitter design without implementing the time constraint. The designed optical transmitter can be integrated with other components in optical communication system to provide high performance optical communication system for future generation network. In future, the designed system can be further enhance by implementing the energy efficient high performance transmitter using UltraScale FPGA device that provides the power efficient output for designed system this design with for 100Gb/s optical DPSK transmitter.

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