# Evidence of Gate Voltage Oscillations during Short Circuit of Commercial 1.7 kV/ 1 kA IGBT Power Modules

Paula, Diaz Reigosa, Aalborg University, Denmark, pdr@et.aau.dk
Rui, Wu, Aalborg University, Denmark, rwu@et.aau.dk
Francesco, Iannuzzo, Aalborg University, Denmark, University of Cassino and Southern Lazio, Italy, fia@et.aau.dk
Frede, Blaabjerg, Aalborg University, Denmark, fbl@et.aau.dk

## Abstract

This paper analyzes the evidence of critical gate voltage oscillations in 1.7 kV/1 kA Insulated-Gate Bipolar Transistor (IGBT) power modules under short circuit conditions. A 6 kA/1.1 kV Non-Destructive Test (NDT) set up for repeatable short circuit tests has been built with a 40 nH stray inductance. A large amount of measurements have been acquired on commercial IGBT modules evidencing gate voltage oscillations under short circuit conditions. To tackle this problem, similar tests have been performed on a modified version of the same modules with two parallel sections and one single section. Mutual oscillations between two parallel sections have been evidenced, whereas single section configuration does not exhibit such instability. According to the experimental observations, it can be concluded that these oscillations are initiated by the paralleling of IGBT chips and sustained by a positive feedback involving the stray impedances of the module itself.

## 1. Introduction

Intensive research activities have been done to improve the short circuit robustness of Insulated-Gate Bipolar Transistor (IGBT) modules. During short circuit events, IGBTs have been designed to withstand both high current and high voltage conditions for few microseconds (i.e., typical value is 10 $\mu$s), allowing the gate driver to turn-off the IGBT before destruction. However, under specific operational conditions (i.e., non-negligible stray inductance) commercial 1.7 kV/ 1 kA IGBT power modules exhibit high-frequency gate voltage oscillations, that in the case of exceeding the maximum rated Vge, typically $\pm$ 20 V, could cause the device failure and therefore drastically limit the expected short circuit robustness.

Among different IGBT failure mechanisms during short circuit, critical high-frequency gate voltage oscillations have previously been presented in the literature and different interpretations have been given. It has been systematically observed that gate voltage oscillations are more prone to occur in parallel-chip configurations than single-chip configurations [1], [2], even if it is well-known that IGBT chips are inherently unstable at high collector voltages and high temperatures due to the presence of a negative gate capacitance [3–7]. Therefore, one of the possible explanations is that the oscillations are initiated by the IGBT chip and enhanced by the internal stray impedances of the module itself. Indeed, research efforts have been devoted in improving the layout design to suppress the oscillations [1, 8–10]. Moreover, Infineon [11] has discussed high frequency oscillations occurring for different types of short circuits (i.e., short circuit type 1 and type 2). They have highlighted the factors triggering these oscillations (i.e., internal module layout, IGBT characteristics and application conditions) and the countermeasures to suppress such oscillations. However, barely details are given and there is no discussion of the type of devices tested. Other research activities discuss Plasma Extraction Transit Time (PETT) effect as the excitation mechanism for high frequency oscillations during the turn-off of paralleled IGBT chips [12], whereas the researches in [13, 14] discuss that a couple of mechanisms, namely, Dynamic Impact Ionization Transit Time (IMPATT) and the PETT effect can lead to turn-off oscillations. So far, no definitive interpretation of gate voltage oscillations occurring during the short circuit period has been given.

Previous experimental observations conducted thanks to a 6 kA/1.1 kV Non-Destructive Tester (NDT) [15], lead to conclude that there are three major aspects which play an important role in limiting the short circuit robustness of 1.7 kV /1 kA IGBT modules: a) non-negligible external loop stray inductance, b) internal layout design: distribution of stray parameters inside the module, and c) IGBT chip: amplification behavior under certain conditions.

The present challenges to predict the root-cause of the observed oscillations in commercial 1.7 kV/ 1 kA IGBT power modules are: a) it is necessary to differentiate various triggering mechanisms for different specific conditions (i.e., DC-link voltage, temperature, gate-emitter voltage), b) each manufacturer has its own limitations due to the applied IGBT technology in their modules (i.e., doping profile, IGBT generation) and different internal module construction (i.e., stray impedance distribution), and c) 2D/3D finite-element simulations, including highly accurate semiconductor physics models, complex stray elements coupling effects and simulation of several number of chips in parallel, may not be feasible.

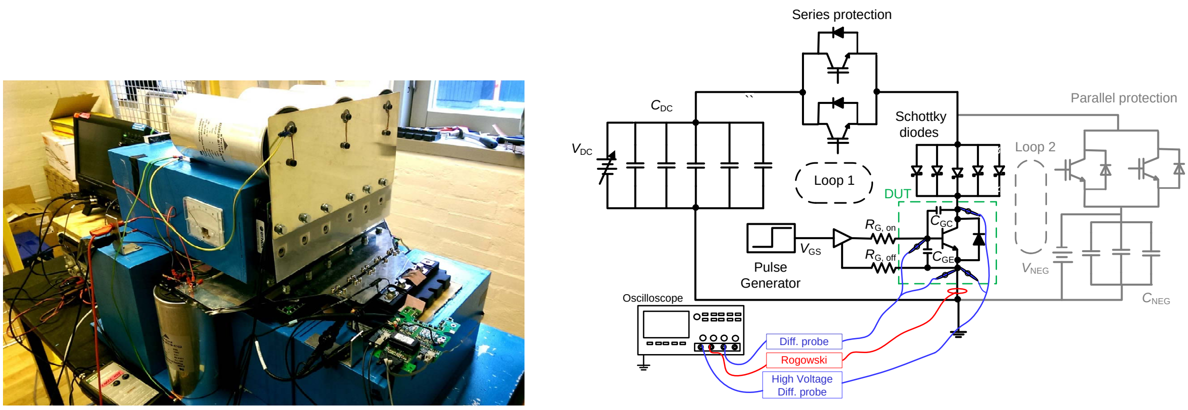
This paper gives an interpretation of critical high-frequency oscillations that may appear when commercial 1.7 kV/ 1 kA IGBT power modules are operated under short circuit conditions. The problem will be tackled from an experimentally point of view: i) closed-package 1.7 kV/ 1 kA IGBT power modules from three different manufacturers will be tested under short circuit conditions and non-negligible stray inductance (40 nH), ii) two parallel sections and one single section of open-package 1.7 kV/ 1 kA IGBT power module will be tested under the same conditions.

## 2. Description of the Experimental Setup and Device Under Test

### Non-Destructive Test Setup for Short Circuit Operation

The experimental setup is a 6 kA/ 1.1 kV Non-Destructive Tester (NDT) system built in the laboratory of the Energy Technology Department at Aalborg University, Denmark. The basic idea is to perform repetitive short circuit tests of several IGBT power modules, while avoiding catastrophically damages. As it can be seen in Fig. 1 , the NDT consists of a high-voltage power supply, $V_{DC}$, a high-voltage capacitor bank, $C_{DC}$, a series protection switch, a parallel protection switch, schottky diodes and a negative-voltage capacitance $C_{NEG}$ with the corresponding negative voltage supply $V_{NEG}$ [15]. Since the type of short circuit test conducted is the well-known *hard switch load* or type 1 [11], where no significant inductance is present in the circuit, only the first loop of the NDT has been used. More details and the specifications of the NDT components can be found in [15].

The operating principle is the following: the capacitor bank, which is made of 5 parallel capacitors, is first charged up to the desired DC-link voltage, then the series protection switch, which consists of 2 IGBT power modules (3 kA /3.3 kV), is turned on before the short circuit experiment. In this way, the DUT is connected directly to the $C_{DC}$ capacitors for a short circuit at the




(a) A photo of the test setup.    (b) A simplified schematic of the NDT.

Fig. 1: 6 kA/ 1.1 kV Non-Destructive Test (NDT) setup.

IGBT turn-on. The DUT is fired then and short circuit occurs. The series protection is switched off right after the short circuit period, by means of a precise time controller implemented by a 100 MHz FPGA board, and finally save the DUT. The total inductance including busbar, intrinsic inductances of the series protection and capacitors is 40 nH, which is larger than the external inductance that manufacturers use to test their devices, however a realistic value for the end-users applications. A Personal Computer (PC) is used for the data acquisition and remote control, which is connected via an Ethernet link to the LeCroy HDO6054-MS oscilloscope and via an RS-232 bus to the FPGA board.

## Device Under Test for Short Circuit Operation

The first set of experiments have been conducted with commercial 1.7 kV/ 1 kA closed-package IGBT power modules from three different manufacturers (manufacturer A, B and C in the following). Each module has 6 identical sections in parallel containing two arms (upper-arm and lower-arm), whose specifications are shown in Table 1. The gate and emitter terminals of the upper-arm IGBT were connected with a gate driver from Concept and those of the lower-arm IGBT were shorted. The second set of experiments have been conducted with a modified version of commercial 1.7 kV/1 kA open-package IGBT power module from manufacturer A, where two parallel sections and a single section of the DUT were tested. Both set of experiments have been done for gate-emitter voltage equal to +15/-10V and the temperature of the module cases were about 25°C.

| | Manufacturer A | Manufacturer B | Manufacturer C |
|---|---|---|---|
| Collector-emitter voltage, $V_{CES}$ | 1.7 kV | 1.7 kV | 1.7 kV |
| Collector current, $I_{C,nom}$ | 1 kA | 1 kA | 1 kA |
| Turn-on energy loss, $E_{on}$ | 390 mJ | 400 mJ | 240 mJ |
| Turn-off energy loss, $E_{off}$ | 295 mJ | 270 mJ | 360 mJ |
| Collector saturation voltage, $V_{CE(sat)}$ | 2.35 V | 2.35 V | 2.40 V |
| Gate threshold voltage, $V_{GE(th)}$ | 5.8 V | 5.8 V | 6.5 V |

Tab. 1: Device Under Test (DUT) specifications extracted from datasheets.

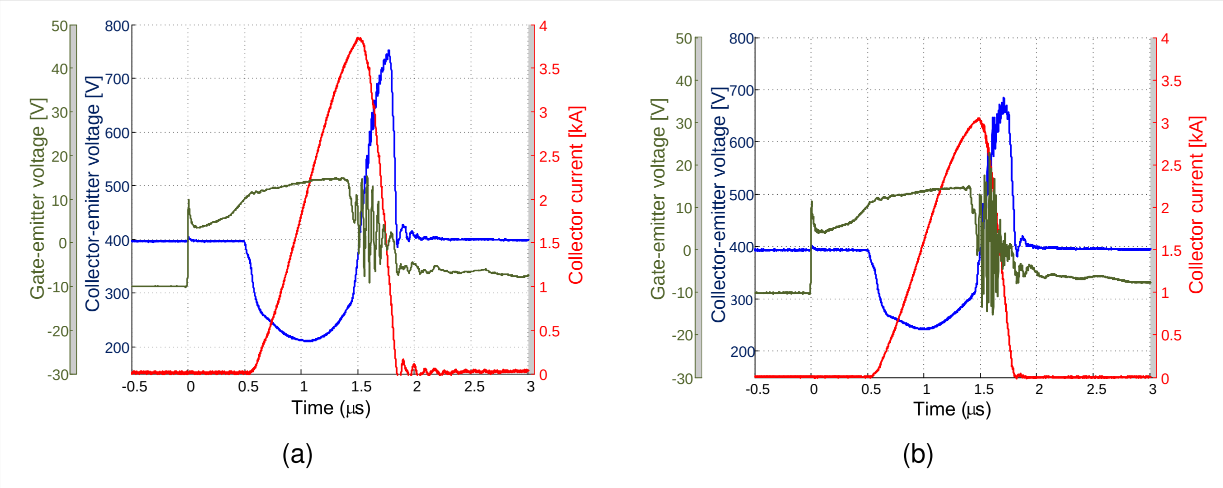



Fig. 2: Gate voltage oscillations observed during 400 V/ 1.4 $\mu$s short circuit test of 1.7 kV/ 1 kA IGBT power module: (a) manufacturer A, and (b) manufacturer B.

# 3. Evidence of Gate Voltage Oscillations under Short Circuit Conditions

## 3.1. Comparison among Different Manufacturers

Fig. 2 shows the typical short circuit waveforms with evidence of gate voltage oscillations ($V_{ge}$) for manufacturers A and B, respectively. The short circuit test was conducted on the upper-arm IGBTs at 400 V DC-link voltage and 1.4 $\mu$s short circuit time. Higher DC-link voltages were tested as well, however these waveforms are not included because the oscillation amplitude increased significantly and appeared earlier and earlier. Even though the oscillations occur at the same time in both tested IGBTs, the peak of gate voltage oscillations differs significantly among them - 15.2 V and 22.8 V for manufacturer A and B, respectively. Both samples oscillate with a similar frequency range - 20 MHz, and the wave shape is not sinusoidal but a composition of different frequencies in the MHz range.

Short circuit tests have also been performed on devices from Manufacturer C. Fig. 3(a) shows the upper-arm IGBT tested at the same test conditions (400V and 1.4 $\mu$s short circuit) whereas Fig. 3(b) illustrates the short circuit test at 900 V DC-link voltage up to 10 $\mu$s, differently from devices from manufacturer A and B, oscillations were not observed.

## 3.2. Layout Influence on Gate Voltage Oscillations under Short Circuit Conditions

To better understand the factors triggering the evidenced gate voltage oscillations, similar tests have been performed on a modified version of the same modules tested, where two sections or one section have been used instead of six parallel sections, with the aim of proving whether the IGBT chip itself and/or the internal package layout are the root-cause of the instability of the device.

Fig. 4 shows the experimental results performed on two sections of the upper-arm of the DUT from Manufacturer A, at 200 V DC-link voltage and 10 $\mu$s short circuit. The turn-on and turn-off gate resistances were increased accordingly to the number of sections tested, however,

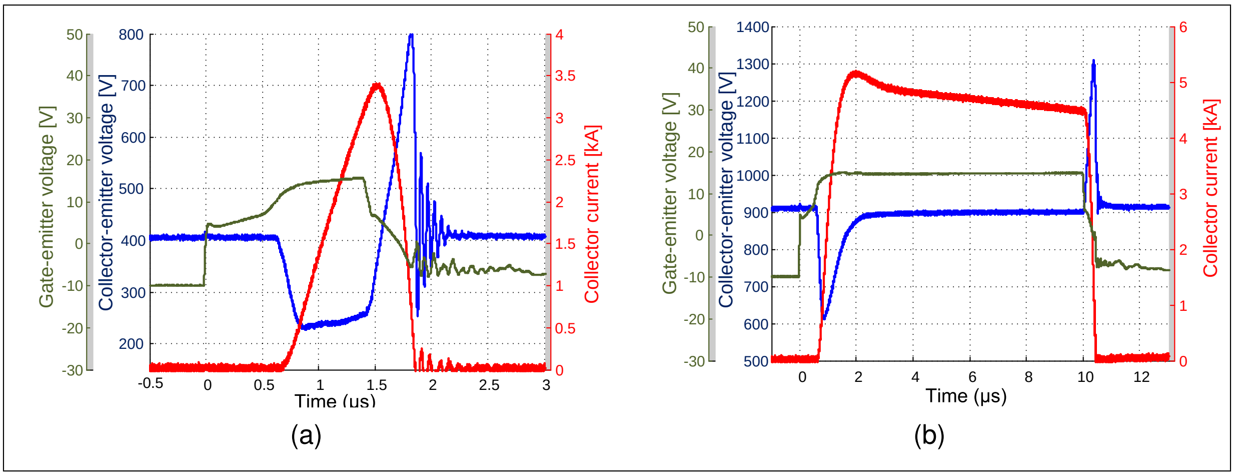



Fig. 3: Short circuit test of 1.7 kV/ 1 kA IGBT power module from Manufacturer C: (a) 400 V/ 1.4 $\mu$s short circuit, and (b) 900V / 10 $\mu$s short circuit.

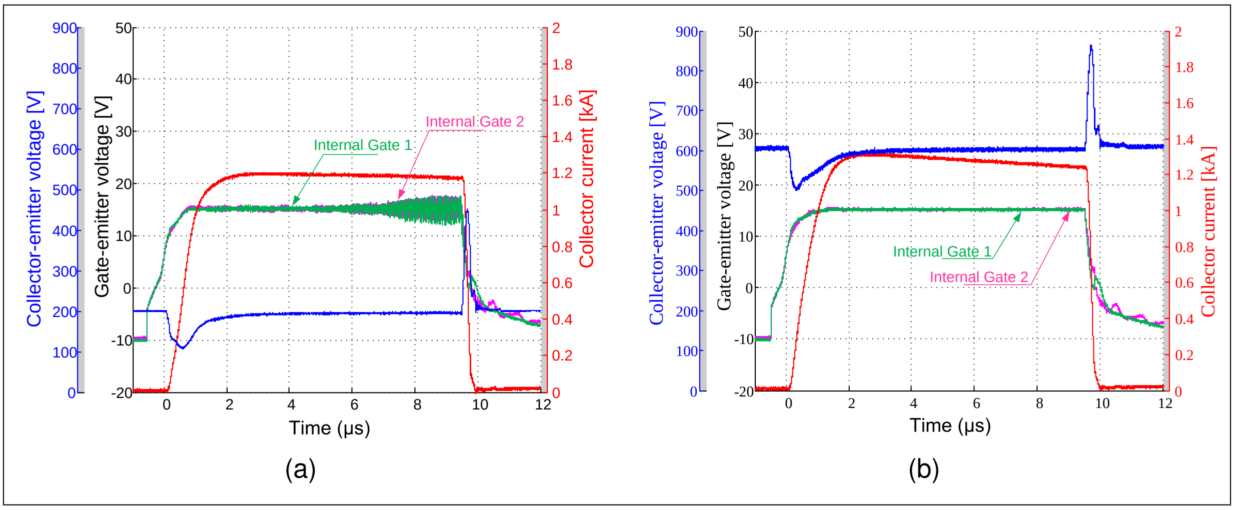



Fig. 4: Two parallel sections tested under short circuit conditions of open-package 1.7 kV/ 1 kA IGBT Power Module from Manufacturer A: (a) 200 V/ 10 $\mu$s short circuit, and (b) 600V / 10 $\mu$s short circuit.

the external stray inductance (40 nH) remained unchanged, resulting in a decreased $di/dt$. The amplitude of the oscillations were of the same level between the two chips but each chip oscillated in opposite phases, again in the frequency range of 20 MHz. It is worth to point out, that the oscillations do not occur at higher DC-link voltages (i.e. from 400V - 900V), as shown in Fig. 4(b).

Fig. 5(a) shows the short circuit test results when the upper-arm of a single section was tested at 200 V DC-link voltage and 10 $\mu$s and Fig. 5(b) when the same section was tested at 600 V and 10 $\mu$s. The gate voltage did not oscillate and there was not found any oscillation behaviour for different DC-link voltages.

## 4. Discussion

Experiments highlighted that gate oscillations appear for two or more paralleled chip configurations, which have not been observed for a single chip configuration of the same module. Fig. 6(a) shows a zoomed view of the internal gate voltage terminals in the case of the experiments

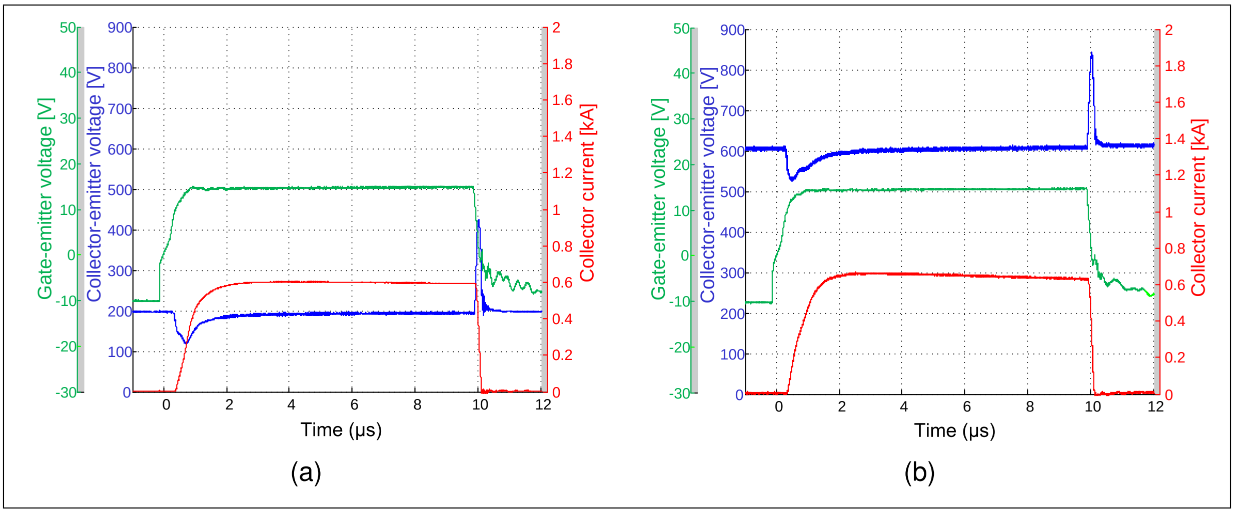



Fig. 5: Single section tested under short circuit conditions of open-package 1.7 kV/ 1 kA IGBT Power Module from Manufacturer A: (a) 200 V/ 10 $\mu$s short circuit, and (b) 600V / 10 $\mu$s short circuit.

with two parallel sections at 200 V and 300 V respectively, which confirms that the oscillations occur between the two chips.

Some interesting considerations can be made if the starting time of the oscillation is considered. With reference to Fig. 2, it can be observed that the oscillations begin when the current reached the saturation value. Plenty of other experiments have been done to confirm this observation, whose results have not been reported for the sake of brevity. This results also helps to give an interpretation about the dependence on the collector voltage. In fact, if the following equation ($V_{ce}$ = $V_{DC-link}$ - $L_{stray} \cdot \frac{di}{dt}$) is considered, it is obvious that higher DC link voltages lead to earlier oscillation as also illustrated in Fig. 6(b).

A significant result comes out from the observation of the oscillation frequency. With reference to Fig. 6(a), the measured oscillation frequency increases with the applied DC-link voltage - 18 MHz at 200 V and 22 MHz at 300 V. An interpretation arises from the influence of the transfer Miller capacitance (Fig. 7). During the short circuit period, the gate alternating current flows through the Miller capacitance, $C_{gc}$, and since the Miller capacitance, has a non-linear characteristic with the applied collector-emitter voltage, the value of $C_{gc}$ decreases if the collector-emitter voltage is increased, hence a higher oscillation frequency is expected. Because the $C_{gc}$ depends on the collector-emitter voltage, the results at 200 V and 300 V explain the collector-emitter voltage dependence with the oscillation frequency.

Thanks to a comparison among different manufacturers, experiments have demonstrated that the devices coming from manufacturer C show higher short circuit robustness than devices coming from manufacturers A and B. However, according to the experimental results, the *di/dt* and *dv/dt* slopes of the device from manufacturer C shows a slower switching characteristic (hence higher energy loss), if compared with those from manufacturers A and B. This fact is also confirmed when looking at the datasheet specifications shown in Table 1; devices from manufacturer C have higher turn-off energy loss. Therefore, a compromise between fast switching devices and short circuit ruggedness appears evident by this analysis.

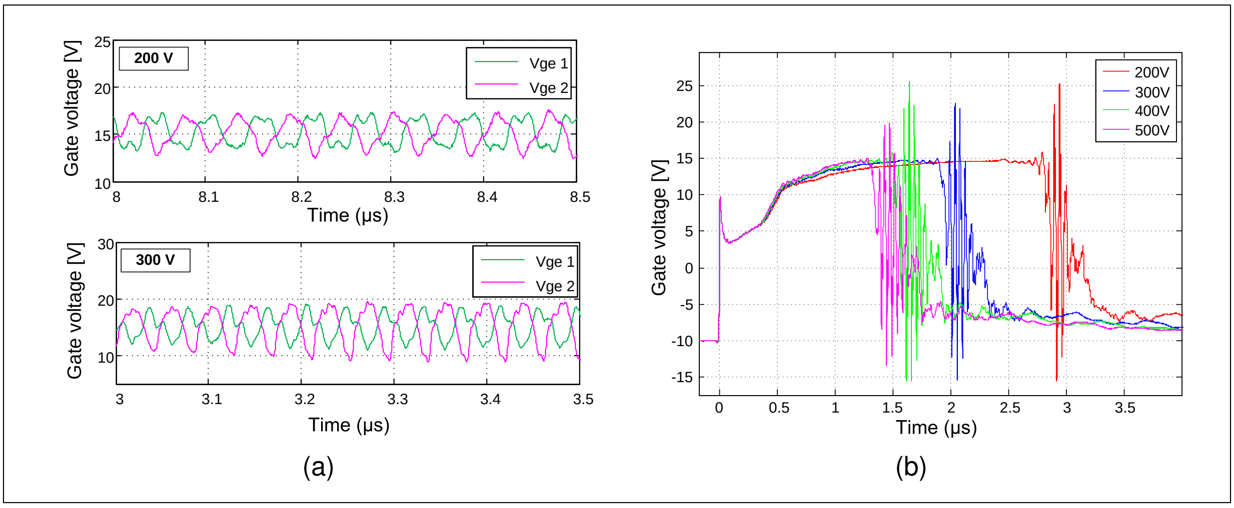



Fig. 6: Gate voltage oscillations of 1.7 kV/ 1 kA IGBT power module from manufacturer A ($V_{ge,1}$ - internal gate voltage terminal from section 1, and $V_{ge,2}$ - internal gate voltage terminal from section 2): (a) two parallel sections for $V_{DC-link} = 200V$ and $V_{DC-link} = 300V$ , and (b) six parallel sections for $V_{DC-link} = [200V - 500V]$.

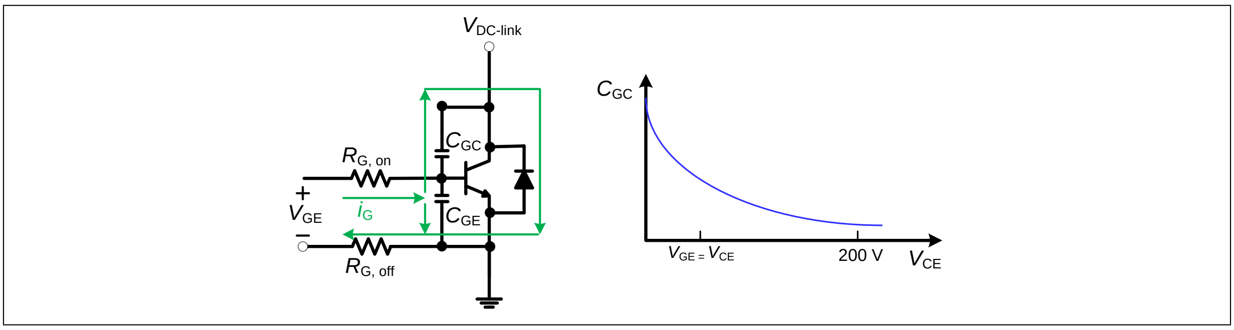



Fig. 7: Equivalent circuit used to explain the oscillation frequency dependency with the applied collector-emitter voltage.

## 5. Conclusion

Gate voltage oscillations during short circuit of commercial 1.7 kV/ 1 kA IGBT power modules have been presented in this paper. In contrast to the oscillations presented in the prior-art literature, these oscillations appear during the short circuit event with frequencies in the range of a few tens of MHz - about 20 MHz. A comparison among three different manufacturers concluded that two of the them exhibit a limitation in the short circuit capability due to critical gate voltage oscillations, whereas the other manufacturer shows a better short circuit ruggedness, but with the trade-off of higher turn-off switching times, and hence higher losses. In the efforts to understand the root-cause of the observed oscillations, a modified version of the same modules, with two sections and one section, have been tested instead of six. The results show gate oscillations in phase opposition between the two chips in parallel for low DC-link voltages; on the other hand, a single section has no evidence of such oscillations. It is concluded that these oscillations may be initiated by the paralleling of IGBT chips and sustained due to a positive feedback involving the stray impedances of the module itself.

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