Advanced Power Cycling Test for Power Module with On-line On-state V_{CE} Measurement

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***Abstract*—Recent research has made an effort to improve the reliability of power electronic systems to comply with more stringent constraints on cost, safety, predicted lifetime and availability in many applications. For this, studies about failure mechanisms of power electronic components and lifetime estimation of power semiconductor devices and capacitors have been done. Accelerated power cycling test is one of the common tests to assess the power device module and develop the lifetime model considering the physics of failure. In this paper, a new advanced power cycling test setup is proposed for power module. The proposed concept can perform various stress conditions which is valid in a real mission profile and it is using a real power converter application with small loss. The concept of the proposed test setup is first presented. Then, the on-line on-state collector-emitter voltage V_{CE} measurement for condition monitoring of the test device is discussed. Finally, a characterization method of test device regarding on-state V_{CE} for junction temperature estimation is proposed. The experimental results of the prototype confirm the validity and the effectiveness of proposed test setup.**

I. Introduction

The accelerated power cycling test is one of the common tests to assess power device modules and develop lifetime models considering the physics of failure [1]-[3]. The power cycling test setup plays an important role because the test setup simulates the stresses and operating conditions and they are directly related to the results. However, the issues of designing and building the power cycling test setup have not been taken up in previous works in detail [4]. Most power cycling tests have been performed with simple designed test setup, where the load pulse with constant DC current source is applied to the test module in order to obtain the specific junction temperature swing ΔT_j and mean junction temperature T_{jm} [4]-[8]. Besides ΔT_j and T_{jm}, other factors like power cycling frequency will also affect the lifetime significantly [9]. Therefore, they should be considered in a lifetime model of the power module. However, the applied stresses by a simple test setup are different with the stresses in real applications such as adjustable speed drives, grid-connected inverter, traction application, wind turbine and so on. Even though much higher temperature stresses are applied to the power device module compared with the real applications during power cycling test, it is important to apply the similar operating conditions with the real applications as much as possible. Therefore, an advanced test setup for power cycling test is needed to perform the active power cycling test and to develop a more reliable and acceptable lifetime model.

Some features are required in the advanced power cycling test. The test setup should easily emulate the real application conditions like motor driving condition, grid connected condition and so on. Further, it should be possible to apply various stresses without difficulties. Finally, the loss in the test setup should be kept low during the test because power cycling tests are lasted for long periods until the test module reaches a certain degradation level and maybe even failure.

In this paper, advanced power cycling test setup for three phase power converter which can fulfill the requirements that are mentioned above is proposed. First, the concept and operation principle are explained. Afterwards an on-line on-state V_{CE} measurement method to monitor the degradation of the test device module is introduced. Next, the characterization of the test devices regarding the on-state V_{CE} for the junction temperature estimation is proposed. Finally, the experimental results of the prototype are presented.

II. Advanced Accelerated Power Cycling Test Setup

A. *Configuration of Power cycling Test setup*

Fig. 1 shows the configuration of the proposed power cycling test setup. Two converters are connected through load inductors. One is the test converter and another is the load converter. The IGBT modules that will be tested are used for the test converter. In the load converter, the IGBT modules have much higher rated power than the test modules in order to reduce the effect of the power cycling stress on the load of

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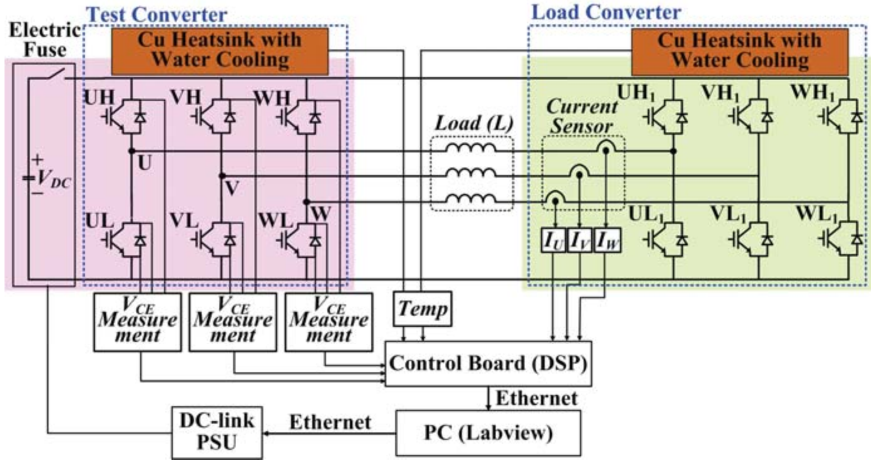

Fig. 1. Configuration of power cycling test setup with a test converter and a load converter.

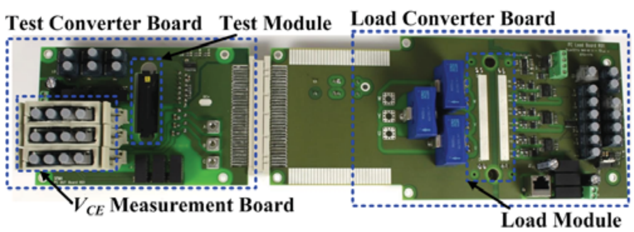

Fig. 2. Prototype of power circuit board.

the IGBT module. By using this, the load converter can run for a long time although the test IGBT modules are changed after a certain number of power cycling tests.

These two converters are connected with a DC source (V_{DC}) via an electric fuse (see Fig. 1). If there is short circuit current during the test, the electric fuse disconnects the two converters from the DC source to protect the overall system. The on-state collector-emitter voltages (V_{CE}) of the IGBTs and forward voltages (V_F) of diodes are measured in real time by a on-line V_{CE} measurement circuit to monitor the condition of the IGBT modules under test. The on-state V_{CE} is a good indicator to determine the degradation of the power device module and the junction temperature of the power device can also be estimated by the on-state V_{CE} because it is one of Temperature Sensitive Electrical Parameter (TSEP) [10]-[12] in IGBT module. The two converters are controlled by DSP and Labview interface communicates with a DSP to manage and monitor the overall system. Water cooling is used to keep the heat sink temperature of the IGBT module as a constant during the test. The heat sink temperature can be changed by the heater. The heater heats the heating element which is contacted with heat sink up to change the heat sink temperature according to test conditions. By the water cooling equipment and heater, the heat sink temperature is kept as constant during power cycling test.

Fig. 2 shows the prototype of power circuit board. It consists of three parts; Test Converter Board, Load Converter Board and V_{CE} Measurement Board. The IGBT module for test will be replaced with a new one after power cycling test and the test converter board will sometimes also be replaced

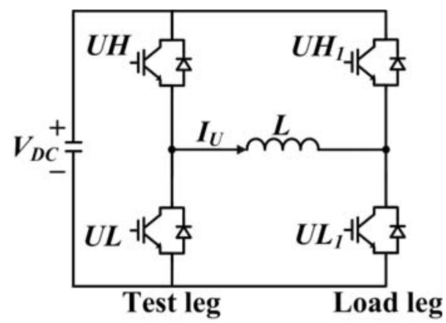

Fig. 3. Diagram of a single phase converter in test and load.

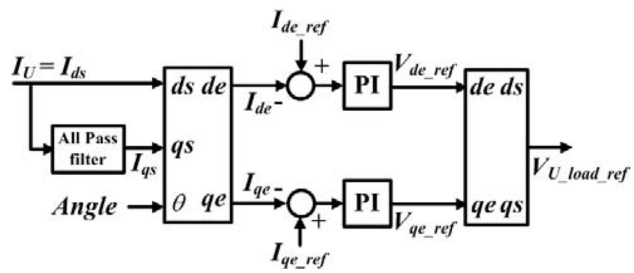

Fig. 4. Block diagram of converter control to control the current in the module.

with a new one as degradation also will happen with test IGBT module. Therefore, the power circuit board has been designed by applying the plug-and-play concept to be able to change module. The boards can be separated from each other easily and the components, which are put on the Test Converter Board are minimized to avoid the unnecessary replacement of components. In this topology, there are only losses by the test and the load IGBT modules, which are the switching and the conduction losses and losses from the load inductor, because the current is circulated between the two converters. Further, only a small value of inductors is needed for the loads in order to get acceptable ripple currents. Therefore, although, the rated output currents are generated, the losses by the test setup can be kept low.

B. Operation Principle of Test Setup

Each phase of the test converter and each phase of load converter are connected through the inductors and the 3-phases are not connected to each other. Therefore, this topology can be considered as 3 single-phase H-bridge converters as shown in Fig. 3.

Phase U, for example, the Test leg generates the output voltage that fulfills the required test condition like modulation index, power factor, output frequency and so on. Then, the load leg is controlled as a single phase converter to generate the output current by the current controller.

The real current is placed along the d-axis and the imaginary current is the q-axis in this paper. The q-axis current can be made using an all-pass filter as shown in Fig. 4. The d- and q-axis currents in the stationary frame are converted to the currents in the synchronous frame with a phase angle which then becomes the input of the current controllers. The output of current controllers becomes the reference of the output voltages in the synchronous frame. By inverse transformation, the output reference voltages are converted to voltages in the stationary frame and the d-axis reference voltage becomes the reference voltage of the load leg. The output current flows by the difference between the output voltages of test leg and load leg. It means that a DC voltage is applied to the inductor during a very short period which is the difference of the duty between the test leg and load leg. Therefore, only small inductors are needed for loads in this test setup in order to obtain the acceptable current ripple. The controls for the other phases are same but there are only 120 and 240 degree shifting in phase angle, respectively to simulate a 3-phase converter system. The parameters like output frequency, modulation index, current magnitude, power factor, switching frequency can be set to apply various thermal stresses on the test module and simulate the various conditions of the test converter.

III. ON-LINE ON-STATE V_{CE} MEASUREMENT

The on-state voltage V_{CE} of IGBT and diode is a good indicator to determine the degradation level of the power device module [1], [12]. By measuring the on-state V_{CE} and V_F on-line, the degradation level of the test module can be monitored during the power cycling test. Usually, from 5% to 20 % increases\ in on-state V_{CE} voltage is considered as a degradation failure of power device module [13]-[14]. Further, the junction temperature of the test module can be estimated.

Fig. 5 shows the schematic of the V_{CE} measurement circuit which is described in [15], [16]. Two diodes D_1 and D_2 are connected in series and these diodes are forward-biased by the current source when the transistor is turned on. When the transistor is turned off, the D_1 blocks the high V_{CE} voltage, which comes from DC-link to protect the measurement circuitry. Assuming diodes D_1 and D_2 have the same characteristics, the forward voltage of D_1 and D_2 can be represented as (1)

$$V_{D1} = V_{D2} = V_a - V_b \tag{1}$$

For example UH, the V_{CE1} can be expressed by the difference between the voltage potential V_b and V_{D1} as given below

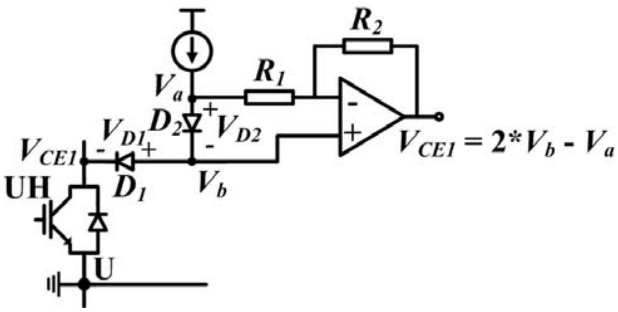

Fig. 5. Diagram of the on-line on-state V_{CE} measurement circuit [13].

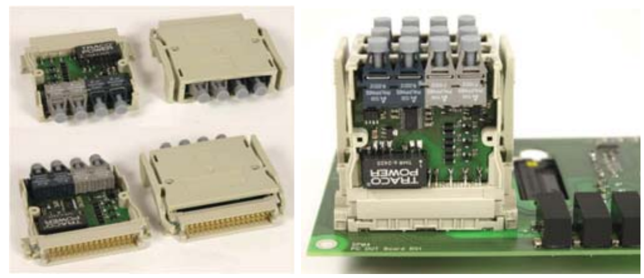
Fig. 6. Prototype of on-state V_{CE} measurement circuit with optic fiber communication.

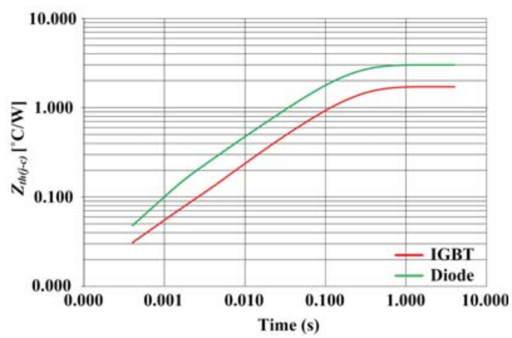

Fig. 7. The transient thermal impedance of a SPM4 power module (V_{DC} : 400 V, I_{rated} : 30A).

$$V_{CE1} = V_b - V_{D2} = V_b - (V_a - V_b) = 2V_b - V_a \tag{2}$$

The above result can be realized by choosing properly the gain of the amplifier. If $R_1 = R_2$, the output of amplifier can be expressed as

$$V_{op\text{-}amp} = V_b - ((V_a - V_b)\cdot R_2 / R_1) = 2V_b - V_a = V_{CE1} \tag{3}$$

The output of the amplifier is the same with V_{CE1} as described above. The on-state V_{CE} of the transistor can be measured during the positive current. The V_F of the diode can be measured during negative current.

Fig. 6 shows prototype of the on-state V_{CE} measurement circuit where galvanic isolation is provided by optic fibers. To improve the resolution of the measured data, an external 14 bit Analog to Digital Converter is used for this circuit. It is designed compactly and it can easily be separated from the Test Board.

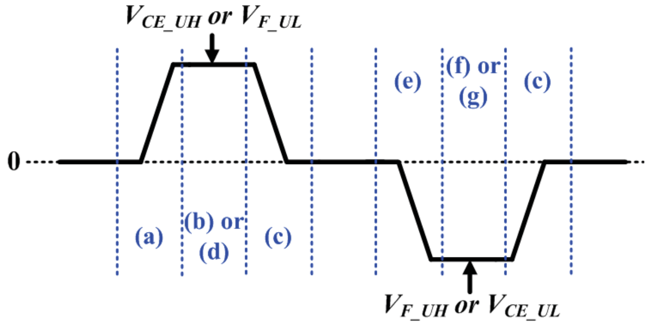

Fig. 8. The output current for device characterization.

IV. CHARACTERIZATION OF TEST DEVICE

This circuit can also characterize the test device regarding on-state V_{CE} according to specific current and junction temperature. By characterization of the test device, the junction temperature can be estimated, when the V_{CE} and the current are given. Further, it is also needed for calibration during the power cycling test because the on-state V_{CE} voltage is changed as the device module wear-out. This means that the applied stress on the test device module is changed during the wear-out.

Fig. 7 shows the transient thermal impedance of an SPM 4 power module. If the transient time is short, the thermal impedance is very small. Therefore, the losses during a short transient time are also very small which means that the junction temperature increase by the losses is negligible.

The characterization of the test device is performed using the principle above explained. The characterization of each transistor and diode can be achieved by a simple switching sequence. Fig. 8 shows the output current for the characterization of the test device and Fig. 9 shows each switching sequence, which corresponds with the output current. The measurement of the on-state V_{CE_UH} for example; first, the heat sink temperature is changed to reference temperature by a heating element. When the junction temperature becomes equal with heat sink temperature after a while, the transistors of UH and UL_1 are turned on until the output current reaches the desired value as shown in Fig 8.

The current level can be adjusted by changing the dwell time of sequence shown in Fig. 9 (a). Then, the transistor of UL_1 is turned off and the transistor of UH_1 is turned on. The current is circulated through transistor of UH and diode of UH_1 as shown in Fig 9 (b). The output current and the V_{CE_UH} are measured at this point as shown in Fig. 8. Finally, the transistor of UH is turned off. The output current flows through diodes of UL and UH_1 as shown in Fig. 9 (c) and it decreases to zero. This sequence is performed by changing the current level from the minimum to the rated current of the power device module with fixed temperature. It is performed again under different temperature. The test device can be characterized in respect to on-state V_{CE} at various currents and temperatures, which will be the criteria for junction temperature estimation, when the current and the on-state V_{CE} are given. The switching sequences for characterization of the power devices are arranged in Table I.

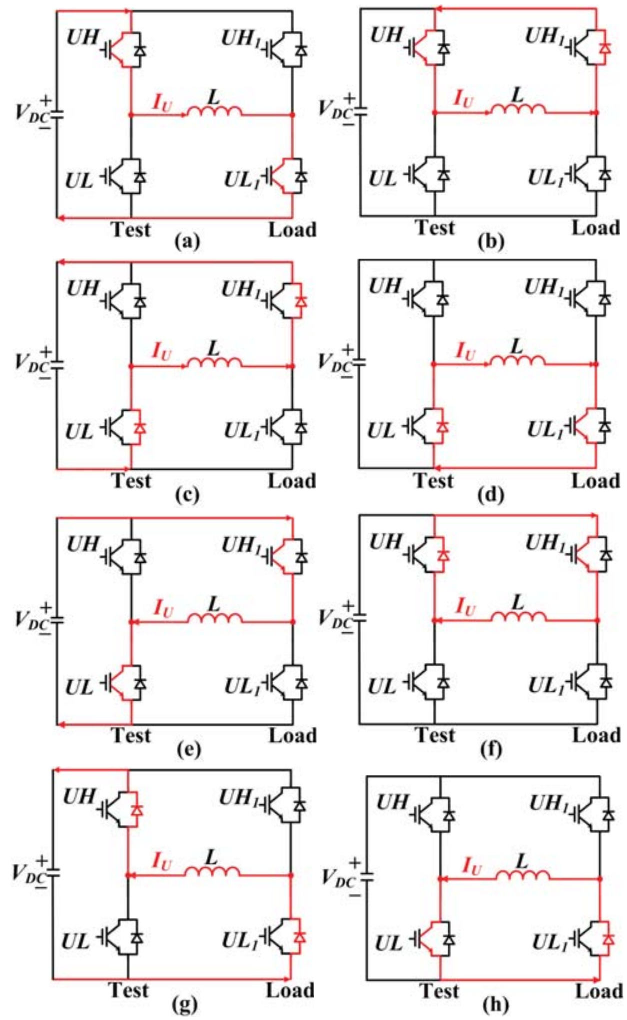

Fig. 9. Switching sequences (a)-(h) for test device characterization.

TABLE I. SWITCHING SEQUENCE FOR CHARACTERIZATION OF POWER DEVICES IN MODULE

Device	Switching Sequence
Transistor of UH	(a)-(b)-(c)
Diode of UH	(e)-(f)-(g)
Transistor of UL	(e)-(h)-(g)
Diode of UL	(a)-(d)-(c)

V. EXPERIMENTAL RESULTS

To demonstrate the proposed concept of the advanced power cycling test setup, a prototype system containing on-line V_{CE} measurement circuit has been built. Fig. 10 shows the prototype of the overall test setup, which consists of a power circuit (Test board and Load board), V_{CE} measurement circuits, control board, load inductors, electrical fuse with DC-link, heating and water cooling systems. The FNCS 3060L (SPM 4) Fairchild module is used for test module and the 6MBI75VA-120-50 Fuji module is used on load module. The inductors of 0.5 mH are used for loads.

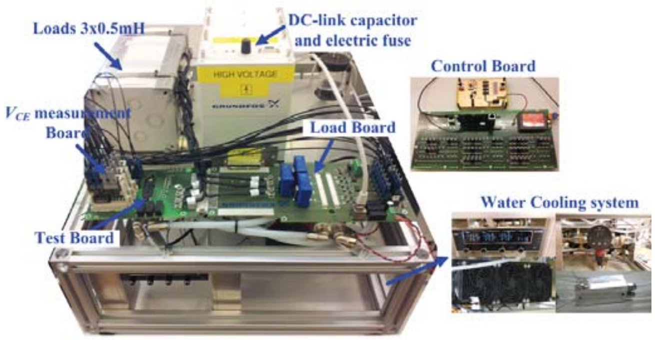

Fig. 10. Prototype of the overall power cycling test setup.

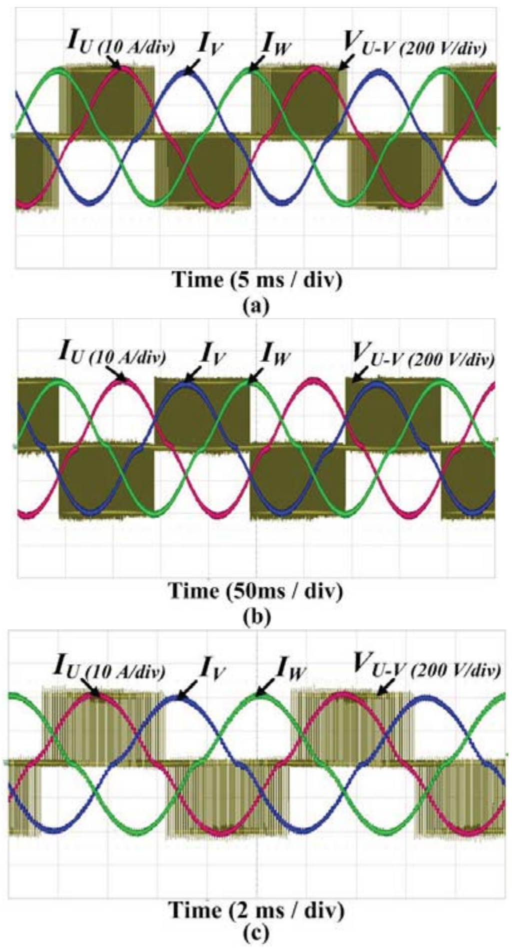

Fig. 11. Outputs of test setup under various operating conditions when I_{ref} = 20A, V_{DC} = 400 V (a) f_{out} = 50 Hz, PF =1, (b) f_{out} = 5 Hz, PF = -1, (c) f_{out} = 100 Hz, PF = 0.8.

Fig. 11 shows the outputs of the test setup under various conditions. Fig. 11 (a) shows the outputs when the test setup is operated as grid connected inverter. The output frequency is 50 Hz and the PF is 1. The line-to-line voltage ($V_{U\text{-}V}$) leads I_U to be 30˚. Fig 11 (b) shows the outputs when the test setup is controlled as converter with unity power factor and 5 Hz output frequency. Fig. 11 (c) shows the output waveforms when the test setup is simulated under the capacitive load condition with 100 Hz output frequency.

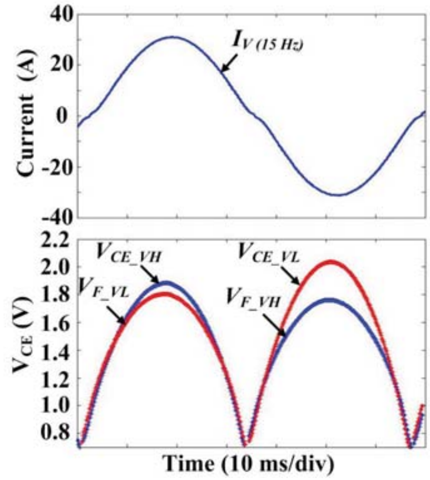

Fig. 12. Measured V_{CE} and V_F of phase V under the inverter operation.

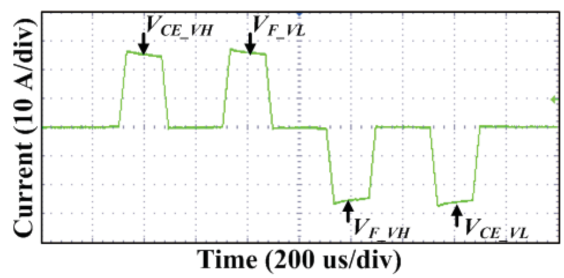

Fig. 13. Measured output current under the characterization sequence.

The outputs of test setup are controlled with various operating conditions as shown in Fig. 11. Although, the 30 A_{peak} current flows with 400 V_{DC}, the total loss by the test setup is 400 W. It means that various stress conditions can be applied to the converter under test like in real application conditions with small losses.

Fig. 12 shows the measured V_{CE} and V_F voltages under the inverter operation. According to the current direction and status of the switch, V_{CE} and V_F voltages are measured complementary. If positive current direction is from the test leg to the load leg, the V_{CE} of lower IGBT (V_{CE_VL}) and V_F of upper diode (V_{F_VH}) are measured when the current is negative. The V_{CE} of upper IGBT (V_{CE_VH}) and V_F of lower diode (V_{F_VL}) are measured, when the current is positive.

Fig. 13 shows the output current under the characterization sequence. By the characterization sequence under the various current levels, the characterization curves of the device can be obtained as shown in Fig. 14.

Fig. 14 shows the characterization curves of the lower side switch of phase V. From these curves, the junction temperature can be estimated, when the V_{CE} and current are measured as shown in Fig. 12. In this test setup, the characterization of the power devices is performed from 30 ˚C to 80 ˚C for safety reason. However, as shown in Fig. 14, the relation between V_{CE} and junction temperature under certain current point is linear. Therefore, even though, the characterization is performed until 80 ˚C, the junction temperature can be estimated above 80 ˚C.

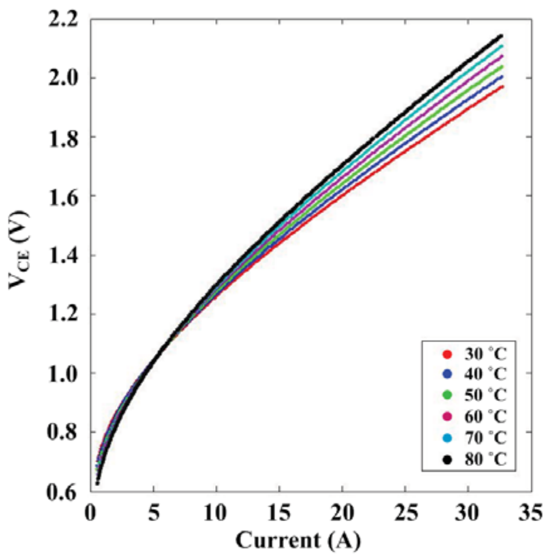

Fig. 14. Characterization curves of lower side switch of phase V at different temperatures.

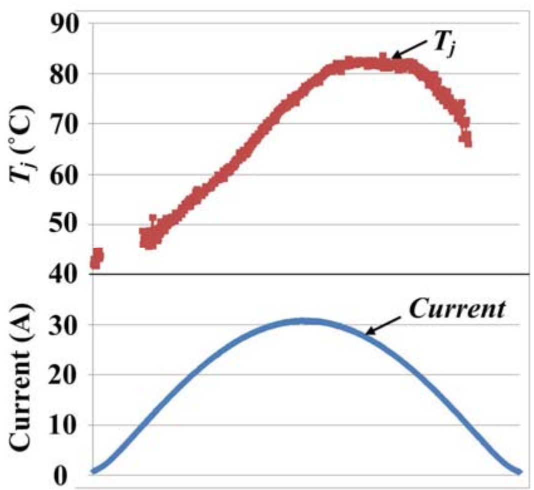

Fig. 15. Estimated junction temperature of lower side switch of phase V under the following conditions; V_{DC} : 400 V, f_{out} : 3 Hz, I_V : 30 A.

Fig. 15 shows the estimated junction temperature of the lower side switch of phase V when the test module is operated under the following conditions; V_{DC} = 400 V, I = 30 A, f_{sw} = 10 kHz, f_{out} = 3 Hz, PF=1. From the estimated value, the important factors for development of lifetime model like ΔTj, T_{jm}, $f_{\Delta Tj}$ and etc can be obtained. In this operating condition, ΔTj is 40˚C, T_{jm} is 62˚C and the $f_{\Delta Tj}$ is 3 Hz.

VI. Conclusion

In this paper, an advanced concept for power cycling has been proposed. The proposed concept can easily emulate the real application conditions like adjustable speed drive, grid connected converter and other 3-phase applications. Further, it can apply various thermal stresses by changing the output current and frequency without difficulty. Under the accelerated power cycling test, much higher thermal stresses than the thermal stress under normal operating condition are applied to the test module to reduce the test time. However, the test module can be operated like real applications as similar as possible by the proposed power cycling test setup. Further, the losses by the test setup can also be kept low during the power cycling test.

An on-line V_{CE} measurement concept is also discussed. By applying the on-line V_{CE} measurement circuit, the degradation of the power device module can be monitored in real time. Further, the characterization method of the test module is proposed. By characterization of the power device, the junction temperature can be estimated when the V_{CE} and current are measured. The experimental results of the prototype validate the functions of the proposed test setup.

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