Grid Connected Power Supplies for Particle Accelerator Magnets

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Grid connected Power Supplies for Particle Accelerator Magnets

Ph.D. Dissertation

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Abstract

Power supplies play a large role in particle accelerators, for creating, accelerating, steering and shaping the beam. This thesis covers the power supplies for steering and shaping the beam, namely the magnet power supplies. These power supplies have a special set of requirements regarding output current stability and accuracy, typically allowed drift over 8 hours is down to 10 parts per million of the maximum output current.

After an introduction to the topic several topologies are discussed and compared for different power ranges. Hereafter a topology is proposed. A converter based on this topology is constructed using a single power module on the grid side of the transformer, consisting of a boost rectifier and a dual half-bridge isolated DC/DC converter. It is shown that it is possible to create a power supply using a single module and that this approach can lead to improved layout and smaller converter size.

A high efficiency converter based on Silicon Carbide switching devices is also presented exhibiting above 96 % efficiency for the entire power range.

Finally reliability issues are considered as the reliability of a particle accelerator supply is of utmost importance. Particle accelerators requires large up time and many power supplies, magnets etc. must function in parallel for the particle accelerator to operate. A method for increasing the reliability of the proposed converter is shown. This is done by creating a lifetime model for the power module converter together with a mission profile.

Resume

Strømforsyninger spiller en stor rolle i partikelacceleratorer. De bruges til at lave, accelererer og forme partikelstrømmen. Denne tese omhandler strømforsyningerne til at styre og forme partikelstrømmen, magnetstrømforsyninger. Disse strømforsyninger har specielle krav hvad angår udgangsstrømsstabilitiet og præcision. Typisk tilladt ændring i strømmen over 8 timer er 10 ppm af den maksimale udgangsstrøm.

Efter en introduktion til emnet bliver flere forskellige topologier, for en sådan strømforsyning, diskuteret og sammenlignet i forskellige effektområder. Ud fra dette bliver en topologi foreslået. Denne topology bliver implementeret i en konverter ved hjælp af et enkelt power modul før skilletransformatoren. Topologien består af en boost ensretter efterfulgt af en isoleret dobbelt halvbro DC/DC konverter. Det vises at en enkelts moduls løsning fungerer og at det er muligt at lave et kompakt design med forbedret printudlægning.

En konverter baseret på Siliciumkarbid halvledere bliver også præsenteret. Denne konverter præsterer en effektivitet på over 96 % over hele effektområdet.

Til slut bliver pålidelighedsudfordringer diskuteret. I partikelacceleratorer er pålidelighed meget vigtigt, da oppetiden skal være høj og mange strømforsyninger skal fungerer samtidigt for at acceleratoren virker. En levetidsmodel for konverteren baseret på et enkelt modul bliver sammen med en missionsprofil præsenteret. Baseret på dette foreslås en metode til at forbedre levetiden på den undersøgte konverter.

Contents

Thesis Details

Thesis Title:	Grid connected Power Supplies for Particle Accelerator Magnets
Industrial Ph.D. Student:	Rasmus Ørndrup Nielsen
Supervisors:	Prof. Stig Munk-Nielsen, Aalborg University Dr. Arnd Baurichter, Danfysik A/S

This is an industrial Ph.D. project made in collaboration with Danfysik A/S, project no. 0604-00494. The work was also sponsored by the Innovation fund Denmark. The project was conducted in the period between January 2011 and December 2013. The main body of this thesis consist of the following papers.

[A] Rasmus Ørndrup Nielsen, Alexander Elkiær, Stig Munk-Nielsen, Benoît Bidoggia, Lajos Török, RamKrishnan Maheshwari, "Innovative use of Power Integrated Modules for DC Power Supplies," *15 th. Conference on Power Electronics and Applications (EPE-ECCE)*, pp. 1–6, 2013.

[B] Rasmus Ørndrup Nielsen,Benoît Bidoggia, RamKrishan Maheshwari, Lajos Török, "Innovative Digitally Controlled Particle Accelerator Magnet Power Supply," *39th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, pp. 7086–7090, 2013.

[C] Rasmus Ørndrup Nielsen, Lajos Török, Stig Munk-Nielsen, Frede Blaabjerg, "Efficiency and Cost Comparison of Si IGBT and SiC JFET Isolated DC/DC Converters," *39th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, pp. 693–697, 2013.

[D] Rasmus Ørndrup Nielsen, Stig Munk-Nielsen, "Optimizing design of converters using power cycling lifetime models," *Submitted for: 17th Conference on Power Electronics and Applications (EPE-ECCE)*, 2015.

In addition to the main papers, the following publications have also been made.

[E] Rasmus Ørndrup Nielsen, Jens Due, Stig Munk-Nielsen, "Innovative Measuring System for Wear-out Indication of High Power IGBT Modules," *Energy Conversion Congress and Exposition (ECCE)*, pp. 1785–1790, 2011.

[F] Jens Due, Stig Munk-Nielsen & Rasmus Nielsen, "LIFETIME INVESTIGATION OF HIGH POWER IGBT MODULES," *14 th. Conference on Power Electronics and Applications (EPE-ECCE)*, pp. 1–8, 2011.

[G] Benoit Bidoggia, RamKrishan Maheshwari, Rasmus Ørndrup Nielsen, Stig Munk-Nielsen, Frede Blaabjerg, "Steady-state analysis of dead-time effect on bidirectional buck converters," *38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, pp. 792–797, 2012.

This present report combined with the above listed scientific papers has been submitted for assessment in partial fulfilment of the PhD degree. The scientific papers are not included in this version due to copyright issues. Detailed publication information is provided above and the interested reader is referred to the original published papers. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty of Engineering and Science, Aalborg University.

Preface

This industrial PhD study was carried out during the period between January 2011 and December 2013. It was conducted under the supervision of Prof. Stig Munk-Nielsen from Aalborg University and Arnd Baurichter from Danfysik A/S.

The purpose of this project is to study the grid connected power supplies for particle accelerator magnets. Different power converters have been proposed, designed and verified in the laboratory. I hope that this work will give others inspiration and that the methods developed will be helpful in other projects.

I would like to show grateful thanks to my supervisor Prof. Stig Munk-Nielsen for faithful and professional supervision during the project. For excellent suggestions and help during the project.

I would also like to thank Danfysik and especially my company supervisor Arnd Baurichter for giving me this great opportunity to learn and grow. I really feel that I have been included in the company and that I have learned a lot from being part of this great company. Also thank you to my other colleagues at Danfysik for excellent sparring and help during the project.

I appreciate my colleagues at Aalborg University and our collaboration during the project. I would like to thank Frede Blaabjerg, Benoit Bidoggia, RamKrishnan Maheshwari, Lajos Török and Szymon Bęczkowski.

Finally I would also like to thank my family, friends and my girlfriend, Katrine Damsgaard Boye, for loving support during my project. I could not have done this without the support and the understanding from home that I had to be away so much.

Rasmus Ørndrup Nielsen
Aalborg University

Part I

Introduction

Introduction

1 Introduction

The first particle accelerator intentionally perceived as such came to life in the early 1930s, constructed by John D. Cockcroft and E.T.S. Walton at the Cavendish Laboratory in Cambridge, England [1]. The first accelerator was made using 200 kV generated by a voltage multiplier in order to accelerate protons. Since then the industry moved on, from Van der Graff generators, to RF accelerated Linacs, Cyclotrons and Synchrotrons. Common for these particle accelerator types is the need to steer and shape the charged particle beam.

In most cases when steering or shaping a particle beam a magnetic field is applied to the charged moving particles. This control of moving charged particles is governed by Lorentz force, as seen in Equation 1.

$$\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B}) \tag{1}$$

From the equation it can be seen that the magnetic field gives a force acting perpendicular to the speed of the charged particle. Thus by shaping the magnetic field in a proper manner it is possible to steer or shape the beam. This is illustrated in Figure 1 where a dipole acting upon a charged particle beam is shown.

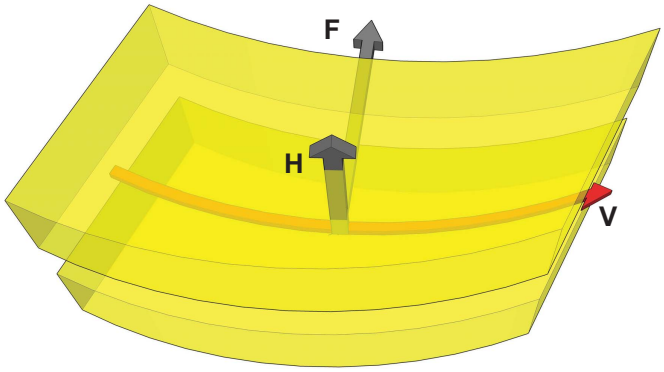
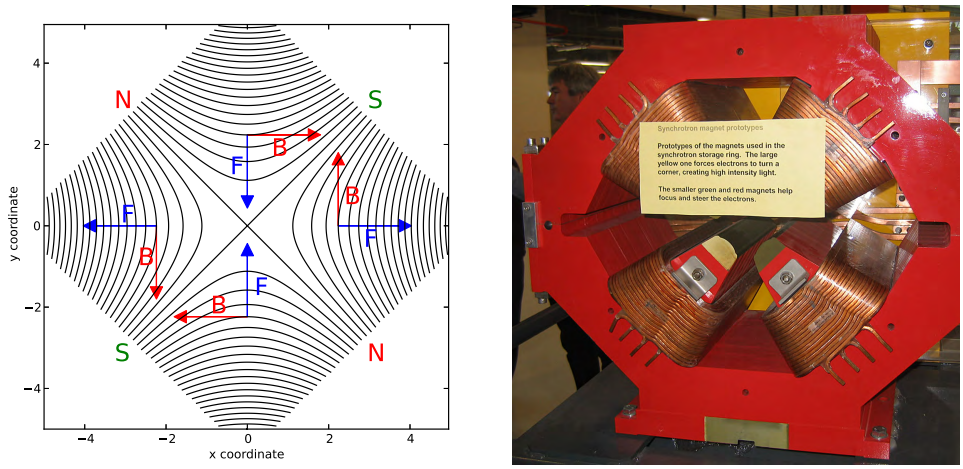


Fig. 1: The magnetic field acting upon a charged particle beam acting with an inward force [2].

Another example of a magnet acting upon a particle beam is the quadrupole magnet. This acts as a focusing device pushing stray particle towards the center in one direction and pushing the away from the center in the perpendicular directions. An illustration of this is shown in Figure 2.



(a) (b)

Fig. 2: (a)Magnetic field lines of a quadrupole and the force acting on a charged particle. In this case the charged particle is moving into the image. (b) Quadrupole from the storage ring of the Australian Synchrotron [3].

All these magnets, di-, quadru-, sixtu-, octupoles etc. are utilized to steer and

shape the beam. These elements can be used in several different accelerator types, from Linacs (Linear Accelerators) to synchrotron storage rings. An example of a synchrotron storage ring is shown in Figure 3. The red magnets shown in the figure are dipoles, and the green magnets are quadrupoles.

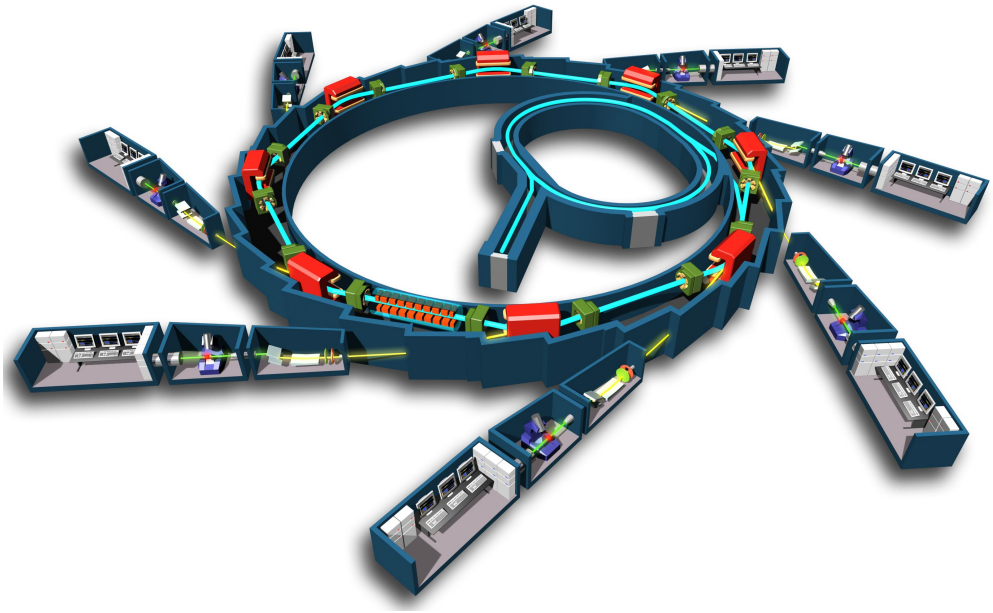


Fig. 3: Overview of the Synchrotron Soleil [4].

In Figure 3 an overview of the Synchrotron Soleil light source is shown. The charged particles, in this case electrons, are moving around the ring at near the speed of light. This means that all the magnetic fields from the magnets must be very accurately set and from this point also be very stable. Any drifting in the current from the power supply will quickly alter the path of the electrons thus shifting them out of the vacuum tube in which they are moving. As the magnetic fields from these electromagnets are directly proportional to the current sent through the windings this puts very high demands to the current delivered from the power supplies. Typically these demands are stability over 8 hours of 10 parts per million of the maximum current and ability to set the current with similar accuracy.

Although generic from their basic principles, DC power supplies for accelerator magnets applications are often specifically designed for matching the loads in each

application. Depending on the characteristics of the load to which the power is delivered, the power supply must meet different requirements. A Magnet Power Supply (MPS) is basically consisting of an input stage and an output stage. This is illustrated in Figure 4 where a block diagram of an MPS is shown.

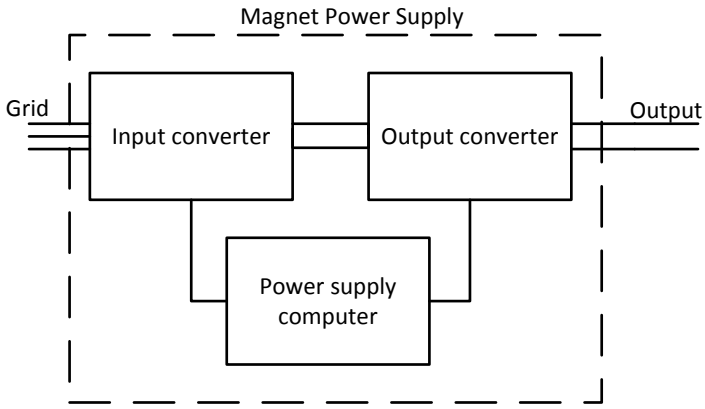


Fig. 4: Block diagram of a magnet power supply

Normally such a MPS is created with both the input and the output stage in order to reach the required current precision, which often is specified in ppm and have galvanic isolation. The converter must have galvanic isolation either at the input or at the output stage. The job of the input converter is to control the voltage to the output converter and at the same time to ensure a line current, which is compliant with the grid codes. The optimization criteria are compactness, cooling method, reliability and price. The output converter must deliver the current to the magnet.

Conventional MPS utilize a large and bulky 50 Hz transformer in order to obtain the galvanic isolation. One way to make the converter more compact is to utilize a higher frequency transformer. However there are challenges with this solution. The skin effect and proximity effects are major problems in high frequency transformer design, because of induced eddy currents in the core material. Leakage inductance and unbalanced magnetic flux distributions are two further obstacles for the development of high frequency transformers.

However, the semiconductor and magnetic technology are in constant progress. Therefore larger and larger power converters are moving towards technology with high frequency transformers. This leads to the following hypothesis:

- ***With the existing and future components it is possible to built a power supply for particle accelerator purposes which is more compact and efficient***

The hypothesis gives rise to the following questions:

- How does the different topologies scale in power, from W, to kW and MW range?
- Where is the limit for compactness and efficiency with existing components and future semiconductors and magnetic materials?

As described the converter consists of both an input and an output converter. This dissertation will consider the input converter of such a power supply. The input converters considered will in all cases include galvanic isolation in order to ensure operational safety, while the output converter will ensure the desired stability and accuracy needed in the output current.

In the following section the state of the art of such galvanic isolated input converters is considered. Each section is started with a small discussion of harmonic standards to be met by the input converter, in order to determine whether it is possible for the given topologies.

2 Thesis outline

1. Part 1: Introduction and state of the art.
   The first part will consist of an introduction to the subject of this thesis. This will be followed by a state of the art examination, which is divided into two power cases.

2. Part 2: Converter design, Si IGBT converter, SiC JFET converter.
   The second part will consider two converters. First a complete converter with grid interface and galvanic isolation, made with Silicon (Si) IGBTs. This is followed by the design of an isolated DC/DC converter with Silicon Carbide (SiC) JFET semiconductors and a comparison with the Si converter.

3. Part 3: Reliability considerations. In the third part converter reliability is considered, in particularly power module power cycling. A lifetime model with a given mission profile is presented for the Si IGBT converter and a method for improving the expected lifetime of the power module is presented.

4. Part 4: Conclusion and future work.

5. Part 5: Papers.

3 State of the art

In order to evaluate different topologies and possibilities the literature for galvanic isolated converters is studied both for single stage and two stage converters. The power capability of the converters is also considered in order to be able to find the proper candidate for the converters described in this thesis. In this section two different cases have been studied, a small power case study and a large power case study; this document will be divided accordingly. The two cases are listed below:

- Small power cases: 100 W - 1 kW class. Only single phase solutions will be studied.

- Large power cases: 2 kW - 25 kW. Only three phase input converters will be studied.

The next two sections will consider the cases. Some of the proposed solutions will be unique for each case; others will be applicable in both cases.

3.1 Large Case study

The converter must comply with current standards of the country or regional area. In Europe the EMC standards apply. One of the main standards determining the design/topology of the input converter is IEC-61000-3-12 (11 kW - 52 kW for a 400 V system), "Limits for harmonic currents produced by equipment connected to public low-voltage with input current >16 A and <75 A per phase" [5]. This standard lists the maximum harmonic components in the current under different circumstances. These values are listed in Table 1. The standard is in this case used down to 2 kW

converters as there is no provision in IEC 61000-3-2 for professional equipment above 1 kW [5].

Table 1: Current harmonics for balanced three-phase equipment [5].

Minimal R_{sce}	Admissible individual harmonic current %				Admissible harmonic current distortion factors %	
	I_5	I_7	I_{11}	I_{13}	THD	PWHD
33	10.7	7.2	3.1	2	13	22
66	14	9	5	3	16	25
120	19	12	7	4	22	28
250	31	20	12	72	37	38
$\geq$350	40	25	15	10	48	46

As can be seen the maximum allowable harmonic content increases with the short circuit ratio (R_{sce}). R_{sce} is determined as given in the following equation:

$$R_{sce} = \frac{S_{sc}}{S_{equ}} \tag{2}$$

Where S_{sc} is the short circuit power in the grid at the consumer and S_{equ} is the rated apparent power of the equipment.

This means that the larger the short circuit power available at the consumer the more harmonic current distortion can be allowed. However if no demands to the consumers grid are to be specified in the product manual, the product must comply with the harmonic levels corresponding to a R_{sce} of 33.

For a demanded $R_{sce} < 33$ this means that the input converter in some way must be power factor corrected. Classically the way to do this is to utilize a 50 Hz transformer with 6 or 9 phase outputs in order to connect each three phases to one 6-pulse rectifier, giving 12 or 18 pulse rectification. However this solution requires a large and bulky transformer. By switching at a higher frequency using switching semiconductors it is possible to minimize the size of the transformer, as the size of transformer is approximately inversely proportional to the frequency.

However it is possible, while still complying with the standard, to demand a higher R_{sce}. This is done by stating the following in the documentation of the product:

"This equipment complies with IEC 61000-3-12 provided that the short-circuit power is greater than or equal to xx at the interface point between the user's supply and the public system. It is the responsibility of the installer or user of the equipment to ensure, by consultation with the distribution network operator if necessary, that the equipment is connected only to a supply with a short-circuit power S_{sc} greater than or equal to xx." [5]

In the following two different approaches for the input converter are described; the single stage and two stage converters.

Two stage converters

The two-stage consists of two parts as the name suggests; a rectifier, and an isolated DC-DC converter. The job of the rectifier is to supply the DC-DC converter with a rectified grid voltage. A block diagram of a two-stage converter is shown in Figure 5.

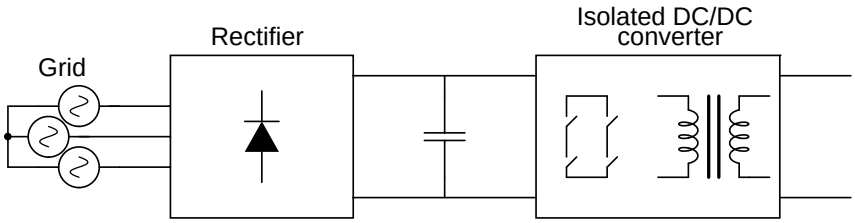


Fig. 5: Block diagram of two-stage converter

An often chosen rectifier by power supply manufactures is a six-pulse three phase rectifier. The six pulse rectifier has its advantages in cost, compactness and efficiency. The disadvantage of a six-pulse rectifier is that it is impractical to reach THD below 30 %, and comply with the 61000-3-12 without using the provision for higher R_{sce}, as the filter inductors then needs to be very large. An ordinary six-pulse rectifier also has the disadvantage of not being able to regulate its output voltage and thus an interface with different grid voltages must be done by the second converter in a two stage concept.

The rectifier could also be some kind of power factor corrected rectifier in order to reach low THD in the grid currents. An example of this type of converters is presented in [6]. In this work, a topology based on the Vienna Rectifier is proposed. The converter shown in Figure 6 can handle an output power of up to 35 kW and the efficiency is higher than 97 % at full load. The power factor is above 0.990 when the power exceeds 20 % of the maximum power.

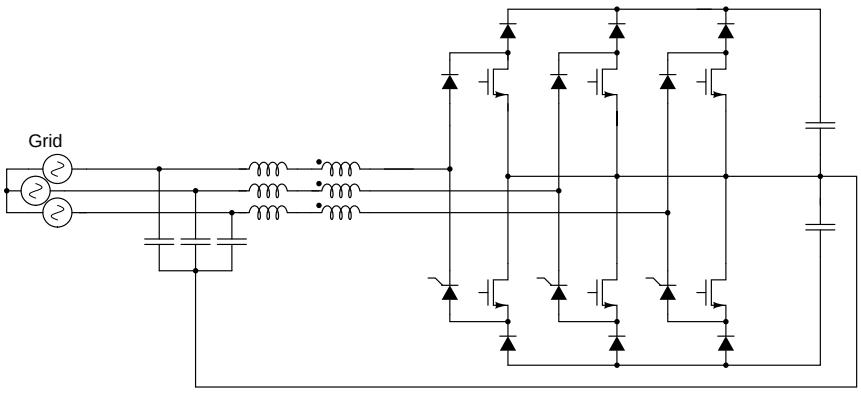


Fig. 6: Unidirectional three-phase Vienna rectifier [6].

There are many other kinds of improved power factor rectifiers. A review is given in [7].

The rectification stage must be followed by an isolated DC-DC converter. The job of this converter is more or less to give the galvanic isolation and lower the output voltage to an appropriate level. There are many topologies available for this conversion, however only a few of them are applicable in this power range. Among those are full bridge converters, both hard switched and multiphase DC-DC converters.

Often a full-bridge converter is used for DC-DC conversion using a high frequency transformer for higher power levels (>3 kW). An example of this topology is shown in Figure 7 [8].

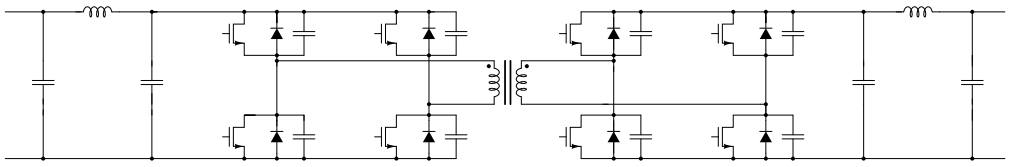


Fig. 7: Full bridge high frequency isolated bi-directional DC-DC converter [8].

In the example shown in Figure 7, zero voltage and quasi zero current switching are used. In full bridge topologies usually soft switching is used. This is accomplished by either combined zero current and zero voltage switching or by zero voltage switching only. The rationale behind this is to reduce switching losses and

thereby enable high switching frequencies. However there are examples where switching frequencies at up to 200 kHz are reached with hard switching for a 5 kW converter using MOSFETs and SiC Schottky diodes [9]. The converter depicted in Figure 4 could also be realized with a diode bridge on the secondary side if only unidirectional operation is needed.

Another solution could be to use multiphase DC-DC converters. An example of such a converter is shown in Figure 8.

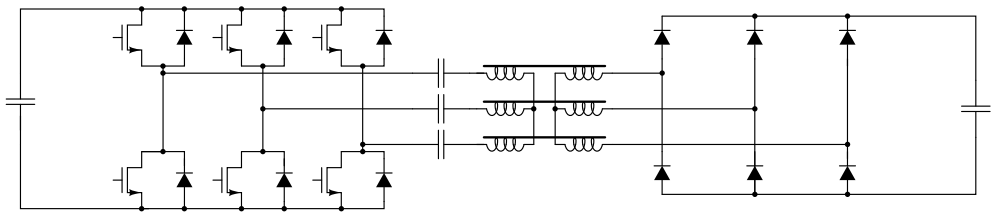


Fig. 8: Multi phase high frequency transformer isolated DC-DC converter [10].

This concept has been realized as a 5 kW prototype with a switching frequency of between 100-140 kHz with an efficiency of 97 %. Also another source reports efficiencies of above 96 % for an extension of the concept [11].

In [12], a three-phase galvanic isolated AC-DC converter is presented. It consists of three full-bridge converters with a DC regulated output as shown in Figure 9. As galvanic isolation is required, a high-frequency transformer is included. The converter provides high power factor and low THD. This converter avoids current loops to control the power factor as it is corrected by a polyphase autotransformer. The switches of this topology are commutated using the ZVS-PWM technique. The high power factor is ensured by the polyphase autotransformer which shifts the current drawn in each phase. The converter is proven up to 12 kW with an efficiency of 90%.

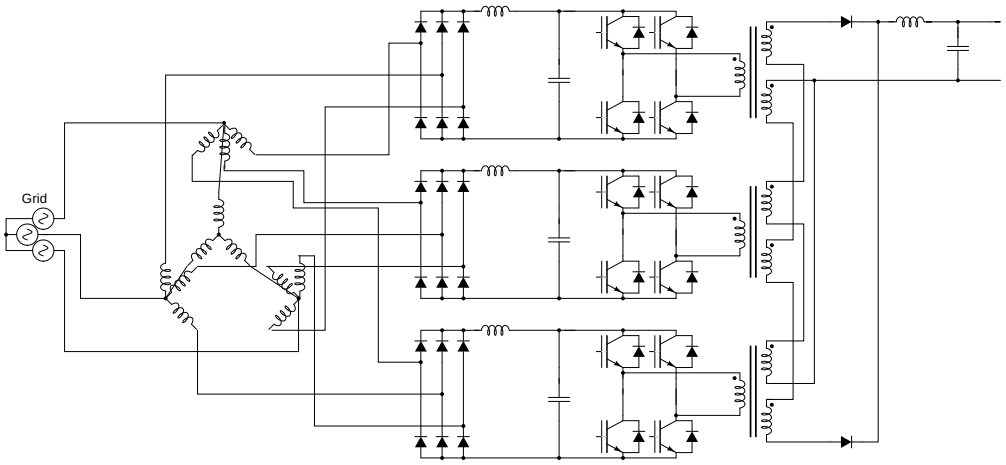


Fig. 9: Three-phase AC-DC converter with high-frequency isolation [12].

Sometimes power flows from the load side to the grid side is also desired with the inductive nature of the load of the particle accelerator magnets. In this case, bidirectional converter topologies are required. In [13], an AC-DC-DC isolated converter with bidirectional power flow capability is presented. It consists of a three-phase AC-DC converter, a high-frequency transformer and a DC-DC converter. Based on the space vector modulation method and the equivalent circuit of the proposed converter, a simple and efficient control strategy is suggested in this work. As shown in Figure 10, this topology allows bidirectional power flowing. It has been demonstrated up to 10 kW with an efficiency of 85 %.

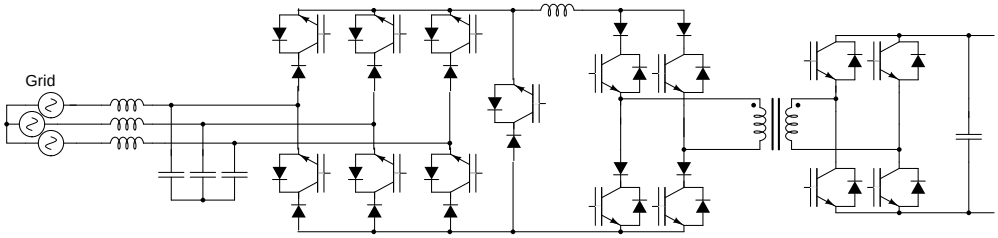


Fig. 10: Direct power flow in the AC-DC converter [13].

Single stage Converters

The single stage converters are as the name suggests a converter where the rectification is integrated in the creation the galvanic isolation. In this section several

concepts for realizing such a converter are presented.

A reduced number of switches is a desired requirement for a converter, as it increases the reliability and reduces cost and volume. In [14], a single-stage, high-frequency isolated, three-phase AC/DC converter is presented. It is composed by a forward/flyback converter as shown in Figure 11. The forward sub converter operates in continuous conduction mode (CCM) and the flyback sub-converter in discontinuous conduction mode (DCM). This is defined so that the forward sub-converter processes practically all of the power delivered to the load. The rectifier stage only uses three switches to perform the conversion. An appropriate design of the input filter is needed to achieve high power-factor. The concept is proven with a 2.5 kW converter with an efficiency of 80 %.

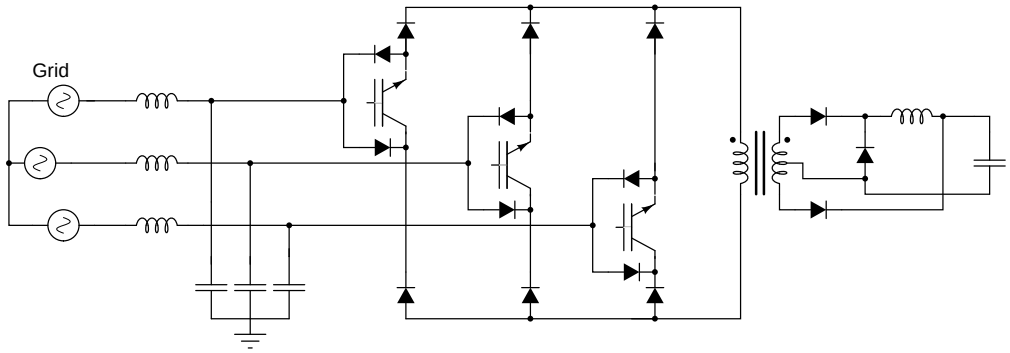


Fig. 11: High-frequency isolated three-phase AC-DC converter [14].

Three-phase AC-DC converters are usually formed by a rectifier and a DC-DC converter. The rectifier stage of the converter typically implies the use of six switches to perform the AC-DC conversion. In [15], a three-phase AC-DC rectifier with reduced switch count is presented. The input stage is a three-phase diode rectifier with a LC filter and the output stage is a zero-voltage, zero-current switching full-bridge converter (ZVZCS) as shown in Figure 12. It also implements power factor correction. However, this approach is usually power limited. The concept was demonstrated with a 2 kW converter. No efficiency was reported.

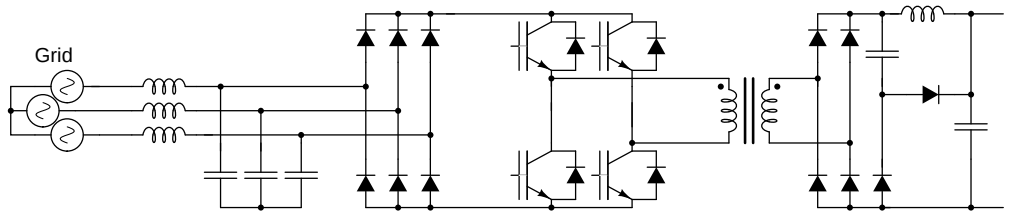


Fig. 12: Three- phase single-stage AC-DC ZVZCS full-bridge converter [15].

A three phase AC-DC single-stage converter is presented in [16]. It is composed of a bidirectional three-phase to one-phase cycloconverter and a bidirectional synchronous rectifier as shown in Figure 13. The cycloconverter increases the frequency in order to include a high-frequency galvanic isolation and reduce the weight and size of the converter. The converter consists of back to back swithces in order to create bidirectional switches. The proposed converter is capable at regenerating energy back to the grid and to control the power factor at the grid up to the unity. The converter is demonstrated up to 1.5 kW with an efficiency of 88.6 %.

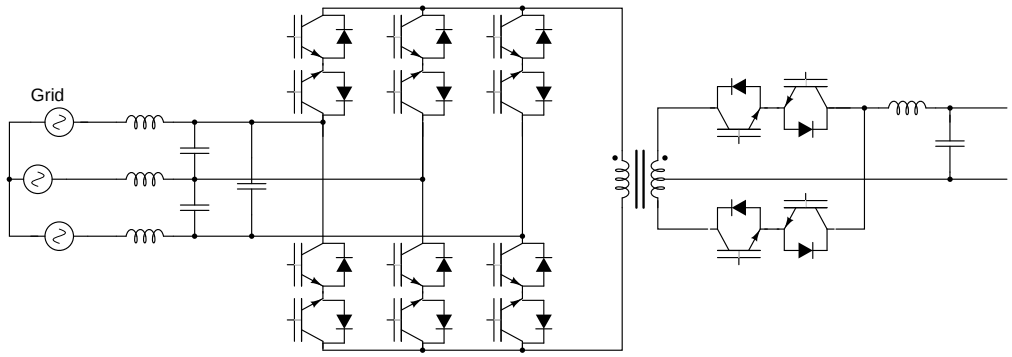


Fig. 13: Four quadrant AC-DC matrix converter with high-frequency isolation [16].

In [17], a three-phase single stage AC-DC converter is presented. It is a boost PWM converter with high-frequency isolation. The single stage topology shown in Figure 14 has the advantage of simple control structure and high power factor. It only uses five switches and the power factor is almost unity. It is demonstrated with a 2.5 kW converter, no efficiency is reported.

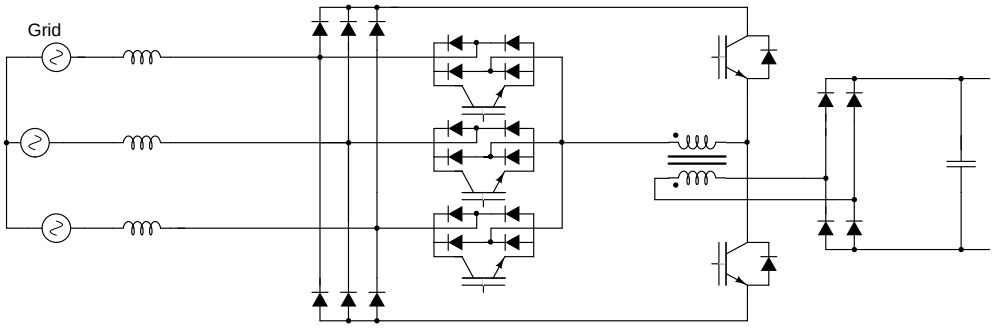


Fig. 14: Unidirectional three-phase single stage AC-DC converter [17].

3.2 Small Case study

In order to figure out demands for harmonic content IEC61000-3-2 (Electromagnetic compatibility (EMC) - Part 3-2: Limits - Limits for harmonic current emissions (equipment input current up to and including 16 A per phase)) was examined. The maximum harmonic content for equipment over 600 W is listed as absolute values for each harmonic number in amperes. This means that at lower power levels, a lower power factor is allowable. The maximum allowed THD can be calculated as:

$$\%THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \cdot 100 \tag{3}$$

In IEC61000-3-2 limits for each harmonic current is given. If taking these limits and calculating the maximum allowable THD (Total Harmonic Distortion) can be found as 70 % (power factor over 0.82), for a loss less system at 1000 W in a 230 V system. However the demands for each individual harmonic component should still be kept. These demands imply that a single phase system cannot be realized by using a simple single phase peak detection rectifier, at these power levels, but must have some kind of active or well filtered rectifier. The maximum allowable THD will be somewhat lower in the realized converter due to losses.

Again the converters can be divided into two different categories, single-stage converters and two-stage converters. The advantage of the single-stage converters is the more direct conversion and no large DC-link capacitor. However the two-stage approach is more applicable in higher power converters as it is easier to do soft-switching, and thereby reducing the switching losses, in these converters. The

next section will deal with various two-stage single phase topologies. Only single phase converters will be described.

Two-stage converters

The two-stage converter consists, as the name suggests, of two parts, a rectifier, and an isolated DC-DC converter. The job of the rectifier is to supply the DC-DC converter with a constant voltage. A block diagram of a two-stage converter is shown in Figure 5. In Figure 5 the converter is shown with a three-phase input. This converter could also be supplied from a single-phase input with a single-phase rectifier. This circumstance makes this approach more versatile than the single stage-converter which is more specific either three or single-phase.

The rectification can be done in many ways, but a popular way of implementing single phase input devices is to use an AC-DC boost converter to do the Power Factor correction [18]. This is shown in Figure 15.

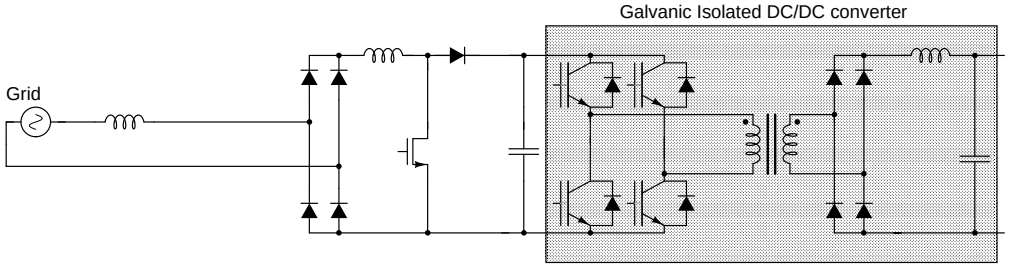


Fig. 15: Single phase boost rectifier and isolated DC/DC converter. [19].

The converter works by controlling the current through the inductor. The rectified current must be controlled as a rectified sinusoidal oscillation which is in phase with the grid voltage too achieve high power factor. This is a cheap and simple solution for achieving a unity power factor from a diode rectifier.

Besides the half-bridge, the full-bridge and the multiphase DC-DC converters mentioned for the large case converts there is a third possibility in this power range (1 kW), a two switch resonant converter. These converters only make sense up to around 1 kW, because of reduced efficiency at higher power levels. One example of these converters is the LLC resonant converter. This converter is shown in Figure 16.

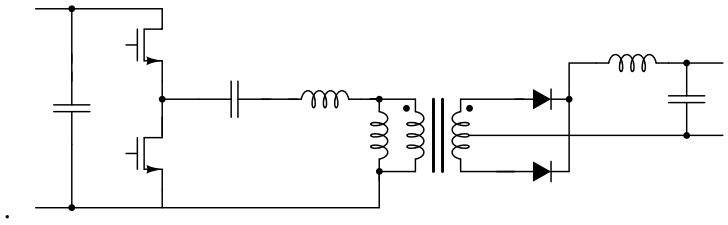


Fig. 16: LLC resonant converter [20].

The LLC converter has been realized as a 1 kW prototype with switching frequencies ranging from 870 kHz to 1 MHz [20].

Single-stage Converters

Another possibility for a more simple and cheap solution is to use single-stage converters. A single stage converter does the PFC and the transformation into high frequency in a single-stage, as opposed to a two-stage solution. There are many different topologies to do this single stage conversion. Generally they can be divided into three different approaches, current fed, voltage fed or resonant converter.

These different approaches have been described and to some degree compared by Gerry Moschopoulos in [21]. Starting with the simplest of the proposed converters is the current fed PWM full bridge converter. This is shown in Figure 17.

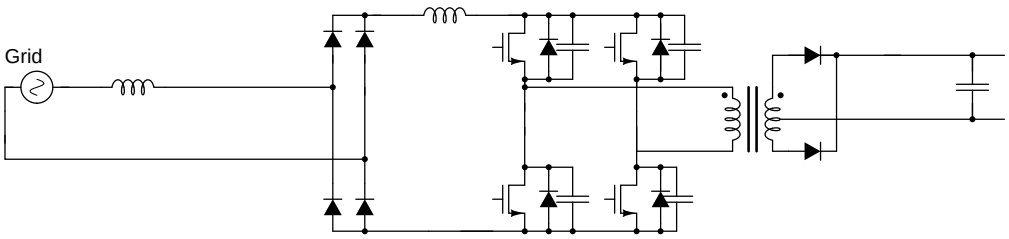


Fig. 17: Current fed PWM full bridge converter.

The operation of this converter can be seen as analogues to that of the boost rectifier. The current through the inductor is controlled by either shorting the inductor or transferring its energy to the load. The input current can be made discontinuous with a sinusoidal envelope or continues with a nearly perfect power factor. The converter can also be made applying zero voltage switching by adding an auxiliary circuit. One of the main disadvantages with this converter type is voltage overshoots and ringing on the DC-link caused by the leakage inductance

of the transformer. These over-voltages must be snubbed in some way, so that the semiconductors are not damaged by these voltages. This practically limits the maximum power to about 12 kW [21]. Also in this type on converter as with the boost rectifier there is a low frequency 100 Hz ripple in the output voltage due to the pulsating power nature of a single phase system. This either means that a very large output capacitance is necessary or that the output stage must have a large tolerance for ripple in the DC-voltage.

Another way to do the PWM full bridge converter is to make it a resonant converter. There has been done a lot of research in this area, as this way of switching reduces the switching losses, thus increasing efficiency and enabling higher power levels. The way this is done is by adding resonant components (inductor, capacitor) in series or parallel thus enabling zero voltage switching. This principle is shown in Figure 18.

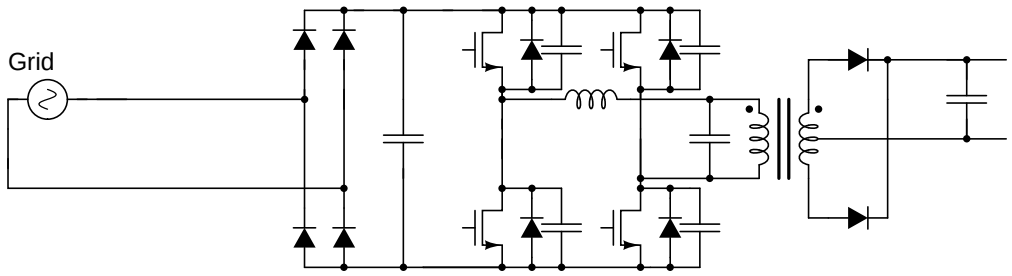


Fig. 18: Parallel resonance single stage converter [21].

It was shown in [22] that by adjusting the switching frequency along the input line cycle it is possible to achieve a unity power factor. An example of this converter type has been shown with efficiency up to 91 % for a 500 W, 230 Vrms input and 100 Vdc output [23]. It should be noted to Figure 18 that the input capacitance only is a small capacitance for filtering purposes.

A third possibility is to use a single stage converter with a large DC-link Capacitor. One of these converters is proposed in [24], and is shown in Figure 19.

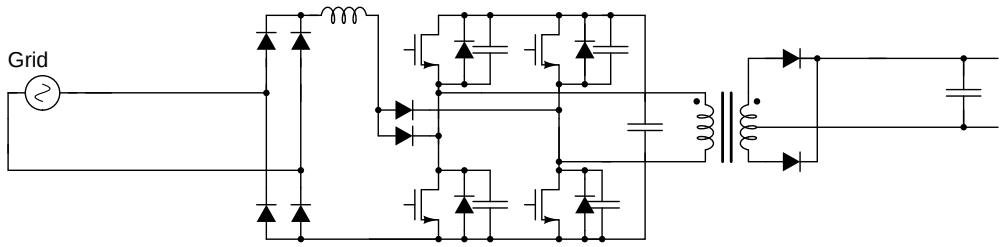


Fig. 19: Single-stage PWM full-bridge converter with large DC-link [24].

This converter shows an efficiency of around 80 % and a power factor over 0.8 for the whole power range, 100-500 W.

Others have since improved on this concept increasing the efficiency. One of the suggested topologies is shown in Figure 20.

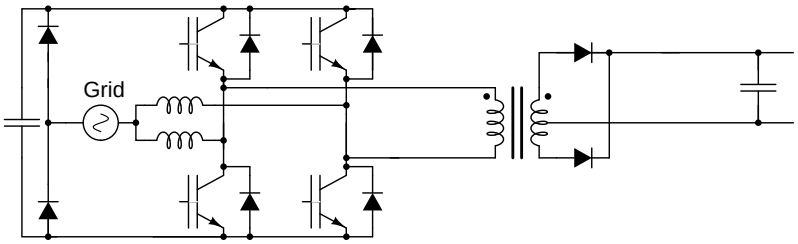


Fig. 20: 650W single-stage converter with large dc-link [25].

This converter has an efficiency of 94 % and operating at a 25 kHz transformer frequency [25]. The converter was realized as a 650 W prototype. Others have shown similar performance in a single stage converter with a DC-Link capacitor in a 1.5 kW prototype with a power factor between 0.89-0.91 [18].

3.3 Conclusion

A number of both single-stage and two-stage converters has been shown. A general summary of the topologies shown, plus some extras, are shown in Table 2 to 6. In general the efficiency of the single-stage three phase converters seems fairly low compared with 2-stage solutions. Therefore at higher power levels the two stage solutions seems more viable.

For single phase single stage power factor corrected converters the efficiency is up towards 94 % with a 25 kHz transformer. For a cheap single phase system a

single stage solution seems to hold advantages compared with a two-stage solution.

In the next part two different converter designs are discussed. They are designed in order to fulfill a set of demands derived from a particle accelerator magnet application.

Table 2: Comparison of the topologies discussed for the rectifier for the two stage solution

Three Phase Improved Power Factor Rectifiers								
Title	*Ref.*	*Topology*	*Eff.*	*T/D*	*Power*	*PF*	*THD*	*Pros/Cons*
Study and implementation of a single-stage three-phase AC-DC converter	[26]	Single-stage, unidirectional, three-phase, buck-boost AC-DC converter	74%	4/12	50-500 W	≈1	< 5 %	-Small prototype -Low efficiency
An improved high performance three phase AC-DC boost converter with input power factor correction	[27]	Three-phase, unidirectional, AC-DC converter	98 %	6/12	4 kW	≈1	< 5 %	-Many transistors + High efficiency
35 kW active rectifier with integrated power modules	[6]	Three-phase, unidirectional, AC-DC converter	97 %	3/18	35 kW	≈1		+Large prototype + High efficiency

Table 3: Comparison of the topologies discussed for three-phase single stage solution.

High-frequency Three Phase Single stage solution with high-frequency galvanic isolation								
Title	*Ref.*	*Topology*	*Eff.*	*T/D*	*Power*	*PF*	*THD*	*Pros/Cons*
A 12 kW three-phase low THD rectifier with high-frequency isolation and regulated DC output	[12]	Unidirectional, three-phase, three full-bridge AC-DC converter	90 %	12/32	12 kW	≈1	8.6 %	+Simple PF control +Modular -Many Components
A Single-Stage High-Frequency Iso-lated Three-Phase AC/DC Converter	[14] [28]	Unidirectional, three-phase, buck AC-DC converter	80 %	3/15	2.5 kW	≈1	<5 %	-Low efficiency +Few transistors
A Three-Phase Ac-Dc Rectifier with Reduced Switch Count	[15]	Unidirectional, three-phase, buck AC-DC converter		4/12	2 kW	≈1		+Simple -Sparse information
AC-DC-DC isolated converter with bidirectional power flow capability	[13]	Bidirectional, rectifier + DC-DC converter + Reverse blocking IGBTs	85 %	15/25	10 kW	≈1	<3 %	+Bidirectional -Complex -Efficiency

Table 4: Comparison of the topologies discussed for three-phase single stage solution contd.

High-frequency Three Phase Single stage solution with high-frequency galvanic isolation contd.								
Title	*Ref.*	*Topology*	*Eff.*	*T/D*	*Power*	*PF*	*THD*	*Pros/Cons*
Four-Quadrant AC-DC Matrix Converter with High-Frequency Isolation	[16]	Bidirectional matrix converter	88.6 %	16/16	1.5 kW	≈1		+Bidirectional -Complex -Efficiency
VIENNA rectifier II-a novel single-stage high-frequency isolated three-phase PWM rectifier system	[17]	Three-phase, Unidirectional, boost rectifier		5/20	2.5 kW	≈1	<	-Sparse Information +Few components
A Three-Phase Unity Power Factor Single-Stage AC-DC Converter Based on an Interleaved Flyback Topology	[29]	Flyback, unidirectional	>85%	3/19	8.4 kW	≈1	<2%	+Modular -Efficiency
A Three-phase Soft-switched Isolated AC/DC Converter without Auxiliary Circuit	[30]	Cyclo-converter, bidirectional switches bidirectional		16/16	40 kW			+Large Prototype -Complex

Table 5: Comparison of the topologies discussed of high frequency DC-DC converters.

High-frequency DC-DC converters with high-frequency galvanic isolation								
Title	*Ref.*	*Topology*	*Eff.*	*T/D*	*Power*	*PF*	*THD*	*Pros/Cons*
A novel three-phase DC/DC converter for high-power applications	[10]	Unidirectional, resonant, three-phase isolation DC-DC converter	98 %	6/6	5 kW	-	-	+Efficiency
Concept of 50kW DC/DC converter based on ZVS, Quasi-ZCS topology and integrated thermal and electromagnetic design	[8]	Bidirectional, H-bridge, resonant DC-DC converter	97 %	8/8	50 kW	-	-	+Efficiency
Design of a 5-kW, 1-U, 10-kW/dm3 Resonant DC/DC Converter for Telecom Applications	[31]	H-bridge with ZVS and ZCS, uni-directional	94.5 %	4/2	2 kW	-	-	+Compact -Efficiency
A High Output Power Density 400/400V Isolated DC/DC Converter with Hybrid Pair of SJ-MOSFET and SiC-SBD for Power Supply of Data Center	[9]	H-bridge with Hard switching, uni-directional	94.6 %	4/8	5 kW	-	-	+Compact -Efficiency
A Novel Three-Phase High-Power Soft-Switched DC/DC Converter for Low-Voltage Fuel Cell Applications	[11]	Multiphase DC-DC converter with ZVS and ZCS	>96%	12/6	3 kW	-	-	+Modular -Complex
1MHz-1kW LLC Resonant Converter with Integrated Magnetics	[20]	LLC converter		2/2	1 kW			+Few components -Power level

Table 6: Comparison of the topologies Discussed for single stage single phase isolated converters.

Single Stage Single Phase isolated Rectifiers								
Title	*Ref.*	*Topology*	*Eff.*	*T/D*	*Power*	*PF*	*THD*	*Pros/Cons*
A comparative study of AC-DC PWM Single-Stage Full-Bridge Converter	[18]	Buck, with auxiliary circuit (S-CONT-SS)	92 %	4/9	600 W	0.93	-	+-Low PF +Simple control
A comparative study of AC-DC PWM Single-Stage Full-Bridge Converter	[18]	Buck, (D-CONT-SS)	94 %	4/6	1.5 kW	-	-	+Efficiency +Large Prototype
Analysis and Design of a High-Efficiency Full-Bridge Single-Stage Converter With Reduced Auxiliary Components	[24]	Boost	94 %	4/4	650 W	-	15 %	+Efficiency -Few components
DCM/CCM ISOLATED PFC SINGLE-STAGE AC/DC CONVERTER	[32]	Boost	83 %	4/8	500 W	0.98		-Efficiency +Power Factor
A Single-Stage Zero-Voltage Zero-Current-Switched Full-Bridge DC Power Supply with Extended Load Power Range	[33]	Buck	90 %	4/8	250 W			-Small prototype -Low Switching frequency

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Part II

Design of converters

Converter designs

4 The design case

Together with Danfysik A/S a design case has been chosen. It has been chosen to design a particle accelerator magnet power supply with the specifications shown in Table 7. The purpose of the power supply is to drive a hybrid magnet (Green Magnet®) consisting of a magnet with both a permanent magnet contribution and conventional driven windings in order to stabilize and control the magnetic field, this is illustrated in Figure 21.

Table 7: Specification for the chosen design case

Parameter	Specification
Input voltage range (V_i)	208 - 400 V $\pm$10 % three phase
Input frequency (f_i)	50 - 60 Hz
Output voltage (V_o):	-50 - 50 V
Output current (I_o):	-100 - 100 A
Galvanic isolation	Yes
Inductive load range	0 - 1 H
Minimum Time Constant of Load	0 s
Maximum Time Constant of Load	1 s
Current Rise time (t_r):	1 s
Maximum physical size	3-unit rack

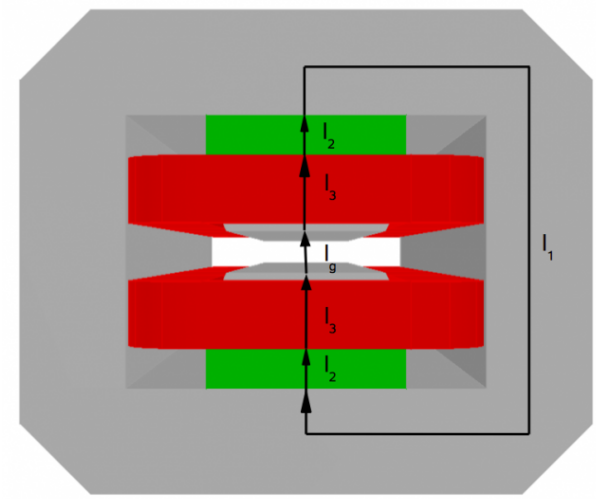


Fig. 21: Hybrid magnet type for evaluating the specifications, the green material is the permanent magnets and the red is the windings [1].

The specifications in Table 7 is for the complete power supply. As described this thesis will only consider the input converter. From Table 7 it can be seen that the input converter must supply the output converter so that it is able to deliver 5 kW with 50 V 100 A. The output converter the input converter must drive is an H-bridge. From the H-bridge design it is chosen therefore that the input converter must deliver a 60 V DC bus, in order to compensate for the voltage drop across the H-bridge. The specifications from Table 7 is translated into specifications for the input converter in Table 8. The output power from the input converter is increased for 5000 W to 5200 W in order to also supply the losses in the output converter.

Table 8: Specification for the input converter

Parameter	Specification
Input voltage range (V_i)	208 - 400 V $\pm$10 % three phase
Input frequency (f_i)	50 - 60 Hz
Output voltage (V_o):	60 V
Output current (I_o):	0 - 87 A
Output power	0 - 5200 W
Galvanic isolation	Yes
Current Rise time (t_r):	0.5 s
Maximum physical size	1/2 3-unit rack

In the next section the design of a converter fulfilling the demands is described. This is followed by a section describing a DC/DC converter with improved efficiency.

5 Silicon IGBT converter

In order to fulfill the specifications shown in Table 8 topologies for the input converter must be chosen. The maximum output power of the design case is 5.2 kW, therefore it is chosen to design a power supply with three phase input. In Section 3.3 it is concluded that a two-stage solution offers potentially higher efficiency. Therefore it is chosen to design a two-stage input converter.

The input converter provides a galvanic interface between the grid and the DC-bus. It is highlighted in the simplified diagram in Figure 22, while its internal structure is shown in Figure 23.

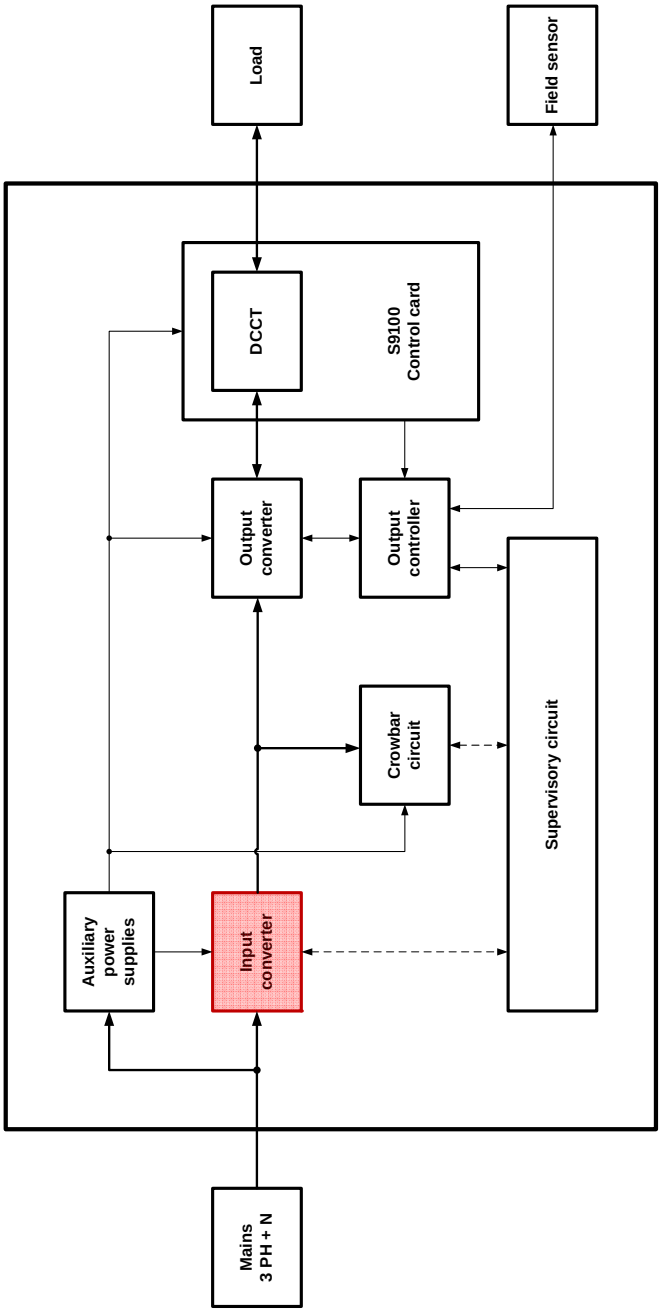


Fig. 22: Overall block diagram of complete power supply. The input converter is highlighted.

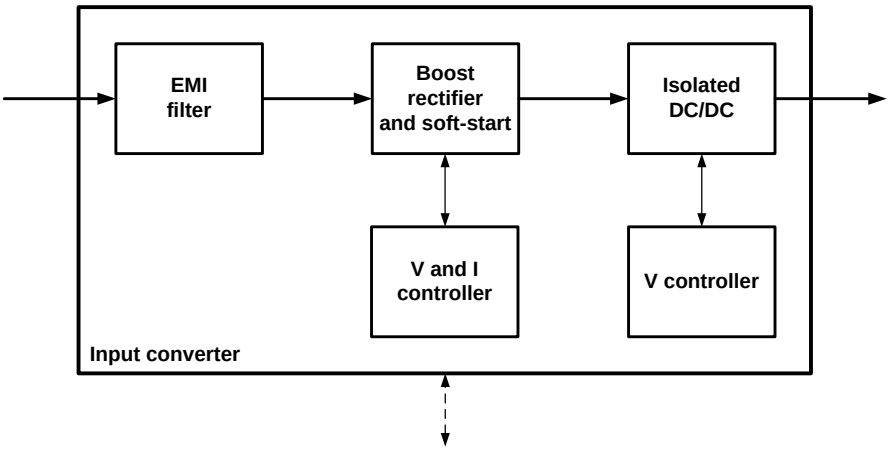


Fig. 23: Internal structure of the input converter.

The input converter consists of an EMI filter, a controlled boost rectifier and a controlled isolated DC/DC converter.

The EMI filter should ensure compliance with the EMC standards and ensure immunity towards conducted and transmitted noise. The EMI filter used in the current version is the EMI filter of a Danfysik S9100.

The boost rectifier allows a wide range of grid input voltage by stepping up the HV DC-bus voltage. The boost rectifier can draw current from the grid with a total harmonic distortion (THD) equal to 30 %. If a lower THD is required, three boost inductors on the grid side of the diode bridge could be used instead. Another option could be to connect the converter between two phases of a three phase grid and draw a sinusoidal current using the boost converter.

It has been chosen to base the input converter on a single Power Integrated Module (PIM). This solution has the advantages of making the PCB layout simpler, of simplifying the cooling and of keeping costs low. The internal structure of a PIM is shown in Figure 24.

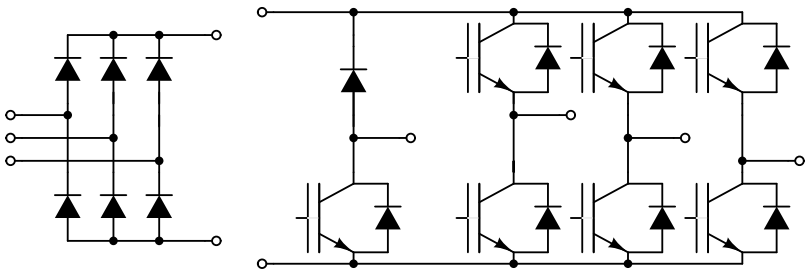


Fig. 24: The internal structure of Power Integrated Module

The main components of a PIM are a three phase diode rectifier, a brake consisting of an IGBT and a diode, and a three phase inverter consisting of 6 IGBTs. While PIMs normally are used to build small and compact three-phase inverters, in this case a PIM has been used instead for generating a constant DC-bus voltage.

Several different topologies using a PIM is shown in the article "“Innovative use of Power Integrated Modules for DC Power Supplies"', which is attached to the dissertation, see Paper A.

The chosen topology is shown in Figure 25. As can be seen from the figure, the PIM includes all the semiconductor components, excepting the secondary side rectification.

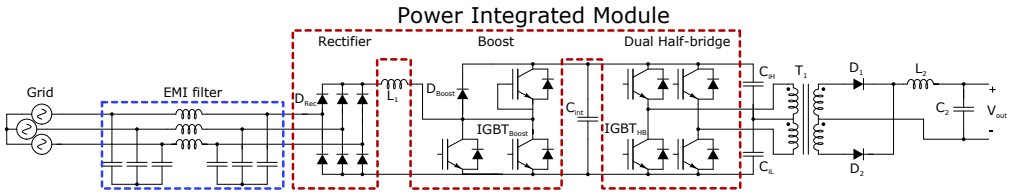
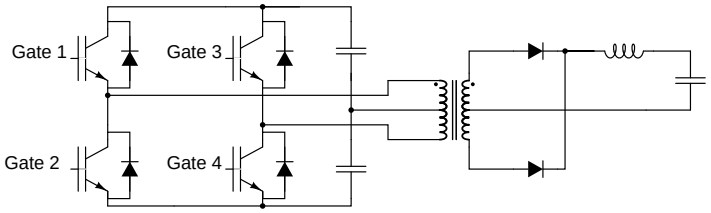


Fig. 25: Main circuit of the input converter, a three-phase boost rectifier with two parallel half-bridge converters.

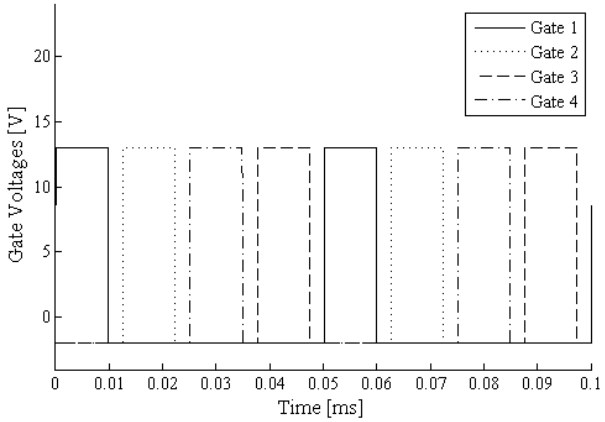
The three phase boost rectifier enables the reduction of L_1 to only 1 mH and allows a wide range of grid voltage. The three phase rectifier was also chosen based on the assumption that the customers would desire evenly power drawn from each phase.

For the galvanic isolating converter the solution using two half-bridges operating on one transformer was chosen mainly because of physical considerations on the transformer size, since it is possible to drive the transformer at a frequency

which is double than the one at which the IGBTs are switching. It was chosen to switch the IGBTs at 20 kHz leading to a switching frequency seen by the transformer equal to 40 kHz. When choosing a half-bridge the control is limited to voltage mode control. However, as the input converter is followed by a current controlled output converter it would still be possible to parallel power supplies for additional current capability. The switching scheme of the dual half-bridge converter is shown in Figure 26.



(a) Schematic



(b) Control signals

Fig. 26: Control signals for gates of the dual half-bridge.

5.1 Hardware description

In this section the hardware and the dimensioning of the components in the input converter will be described.

Dimensioning of PIM module

In order to size the PIM, the converter has been simulated to determine the current rating required by the PIM. The sizing is mainly done as a consequence of the maximum allowable power dissipation of the devices. As these PIMs are fairly small, the maximum power dissipation is also limited. The different available PIM in this power range is rather limited. Therefore the approach has been to find module that could fit the case and handle the power losses.

Therefore the PIM FP75R12KT4_B11 from Infineon has been chosen. This is a 75 A 1200 V module.

Selection of Driver

In order to drive the IGBTs of the PIM module, driver circuits must be designed and selected. The gate driver needs to supply both the high-side and low-side IGBTs. This means that the driver must be rated to drive an IGBT at 1200 V. The gate charge of the IGBT is Q_G = 0.57 μC. From this, the power that the driver should provide can be calculated

$$P_{GD} = Q_G \cdot (V_{G(on)} - V_{G(off)}) \cdot f_{sw} \ [W] \tag{4}$$

With $V_{G(on)}$= 15 V and $V_{G(off)}$ =-15 V, this gives a power of 0.34 W per switch, which means that a half-bridge driver must be able to deliver 0.68 W in total.

The average gate current can be approximated by

$$I_G = Q_G \cdot f_{sw} \ [A] \tag{5}$$

This can be calculated to 11.4 mA.

The peak current capability of the gate driver is also important. This can be calculated using the following equation:

$$I_{GPeak} = \frac{V_{G(on)} - V_{G(off)}}{R_G + R_{G(int)}} \ [A] \tag{6}$$

The internal resistance of the IGBTs is 10 Ω and the datasheet suggests an external gate resistor of 1.1 Ω. This leads to the choice of a gate driver that can supply 2.7 A peak, which is a fairly high current. In Figure 27, the switching losses versus external gate resistance are shown.

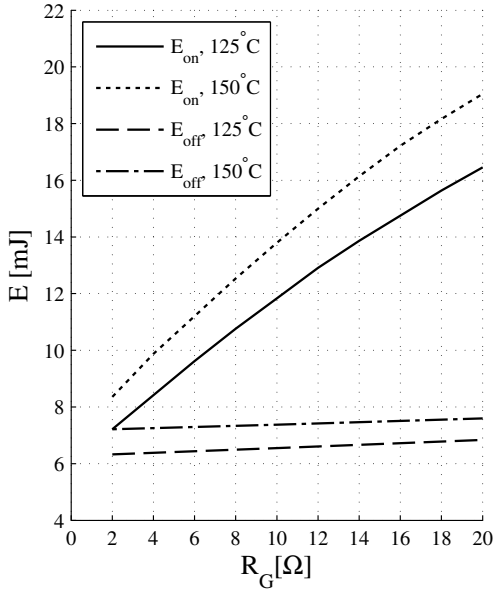


Fig. 27: Switching losses as a function of external gate resistance and junction temperature for the PIM module [2].

As it can be seen from Figure 27, only the turn on losses are dramatically increasing with the gate resistance. However, since the IGBTs in the two half bridges are turned on at zero current, the turn on losses are close to zero. The gate resistance can then be increased in order to reduce the peak current without increasing the switching losses. Therefore, a gate resistance of 10 Ω has been chosen for the half-bridges. This gives a current peak requirement for the driver equal to 1.5 A, for which a 2 A IR2213 half-bridge driver from international Rectifier has been chosen. The gate driver uses a boot strap configuration to drive the high-side switch, which can be used in this case because the duty cycle never goes above 25 %.

The IGBTs of the boost rectifier are never soft switched and therefore a gate driver that can deliver more current has been chosen. Due to its low cost (2 DKK per piece), the 10 A low side driver ZXGD3005E6TA has been chosen.

Sizing of DC-link capacitors and half-bridge capacitors

To size the DC-link capacitance, the allowed ripple in the dc-link must be considered. The ripple in the DC-link consists of two contributions: The ripple caused by the switching and the ripple caused by the not constant input current. This means

that there are two different frequencies in the ripple, 20 kHz from the boost rectifier, and 300/360 Hz from the rectification of the grid. The combined result of these two ripple contributions must be within the allowed specification.

Since the 300 Hz ripple can be reduced by using a voltage controller, the DC-link capacitor will be designed in order to minimize the 20 kHz ripple Δv. The DC-link ripple can be calculated by:

$$\Delta V = V_{out} \cdot R \cdot C \cdot d \cdot T_S \ [V] \tag{7}$$

where R is the load of the boost converter considering a constant load from the half-bridge converter, C is the capacitance of the DC-link capacitor C_{int}, d is the duty cycle at the highest current and T_s the switching period. The duty cycle increases when the input voltage decreases, thus the duty cycle is highest at 208 V input.

If 1 % ripple is accepted, the capacitance can be calculated to 40 μF. From simulation, the rms current is found equal to 8.6 A in steady state. The capacitor must also be able to withstand the 600 V plus a margin for over-voltages. Therefore a film capacitor has been chosen for the DC-link capacitor as well.

The chosen capacitors is a type B32778G0406 from EPCOS, with a maximum voltage rating of 1100 V and a capacity is 40 μF and with a current capability of 20 A rms at 20 kHz.

In order to size the half bridge DC-link capacitor C_{iH} and C_{iL}, the rms current, the ripple voltage and the frequency need to be defined. The highest rms value of the ripple current is 11 A with a fundamental frequency of 20 kHz.

The chosen capacitors are metalized film capacitors as they show high voltage capability together with a low equivalent series resistance (ESR), resulting in minimum volume at a given capacity. The chosen capacitors are type B32776G8306K from EPCOS, with a maximum voltage of 800 V, a capacity of 30 μF and an rms current capability of 14 A at 20 kHz.

Magnetic components

The first inductor, L_1, is as described a 1 mH inductor. It is made with 4 E65 cores in Super MMS-Sendust from Micrometals. It is wound with five 1 mm in diameter copper wires in parallel with 52 turns.

The double center tapped transformer, T_1 is designed with two parallel sets of E80 cores. The transformer is wound with a 4 to 1 turns ratio, 20 turns primary,

5 turns secondary. Both primary and secondary windings are wound with copper foil. The primary winding is interleaved with the secondary winding in order to reduce leakage inductance. The winding principle is illustrated in Figure 28.

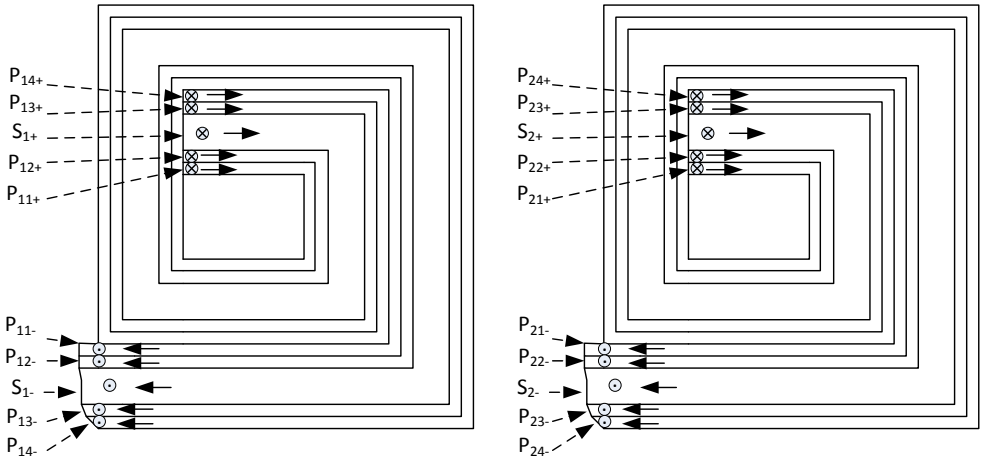


Fig. 28: Windin principle of the transformer. (left) Left winding of the transformer; (right) Right winding of the transformer.

The secondary inductor L_2 is a 13 μH inductor. It is also made with a set of E65 in Super MMS-Sendust from Micrometals. It is made with 8 turns in copper foil.

Secondary rectifier diodes

To rectify the voltage from the transformer Schottky diodes are chosen. Schottky diodes are chosen because of their almost zero reverse recovery. The diodes chosen are from MicroSemi type: APT100S20LCTG. 100 A, 200 V diodes.

5.2 Control for the Boost converter

The boost rectifier is controlled by a UC3843, using peak current control mode with an external voltage loop keeping a constant HV DC-bus voltage of 600 V. The diagram in Figure 29 shows the implemented control structure.

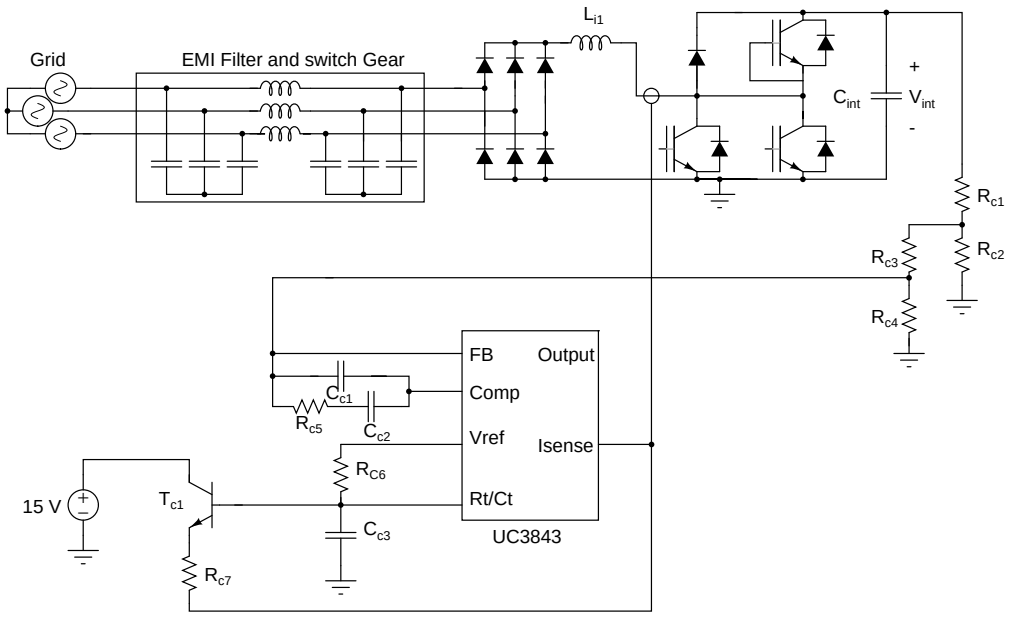


Fig. 29: Control structure of the boost rectifier.

Since the boost operating with 208 V as input voltage requires a duty cycle higher than 50 % to maintain 600 V at the output, the controller must be slope compensated. The slope compensation is done by T_{c1} and R_{c7} adding a small current to the sensed current and stabilizing the converter. The appropriate compensation was found to be a 10 kΩ resistor through experimentation.

The transfer function of the boost converter with peak current mode control in continues conduction mode can be described as [3], [4]:

$$H(s) = K\frac{\left[1+\frac{s}{\omega_z}\right]\left[1-\frac{s}{\omega_{zrhp}}\right]}{\left[1+\frac{s}{\omega_p}\right]\left[1+\frac{s}{\omega_{sw}}\right]^2} \tag{8}$$

$$\omega_z = \frac{1}{R_{esr}\cdot C_{int}} \tag{9}$$

$$\omega_{zrhp} = \frac{R_{load}\cdot(1-D)^2}{L_{i1}} \tag{10}$$

$$\omega_p = \frac{2}{R_{load}\cdot C_{int}} \tag{11}$$

$$K = \frac{V_{int}\cdot F_m}{(1-D)\cdot\left(1+2\frac{F_m\cdot V_{int}}{(1-D)^2\cdot R_{load}}\right)\cdot R_i} \tag{12}$$

$$F_m = \frac{f_{sw}}{S_e+S_n} \tag{13}$$

$$S_e = \frac{V_{pp}}{T_{sw}} \tag{14}$$

$$S_n = \frac{V_{in}}{L_{i1}}\cdot R_i \tag{15}$$

Where R_{esr} is the equivalent resistance of C_{int}, R_{load} is the equivalent load resistance, D is the duty cycle, R_i is the gain of the current measurement, f_{sw} is the switching frequency, V_{pp} is the ramp height of the PWM ramp and V_{in} is the input voltage.

Some of the challenges that should be considered when designing a controller are the fact that the gain K will change with changing input voltages, and that the placement of the right hand zero is influenced by the duty cycle operating point. However, the right hand zero is at such a high frequency (> 300 kHz) that it can be ignored. In Figure 30 the bode plot of the transfer function of the converter in CCM is shown.

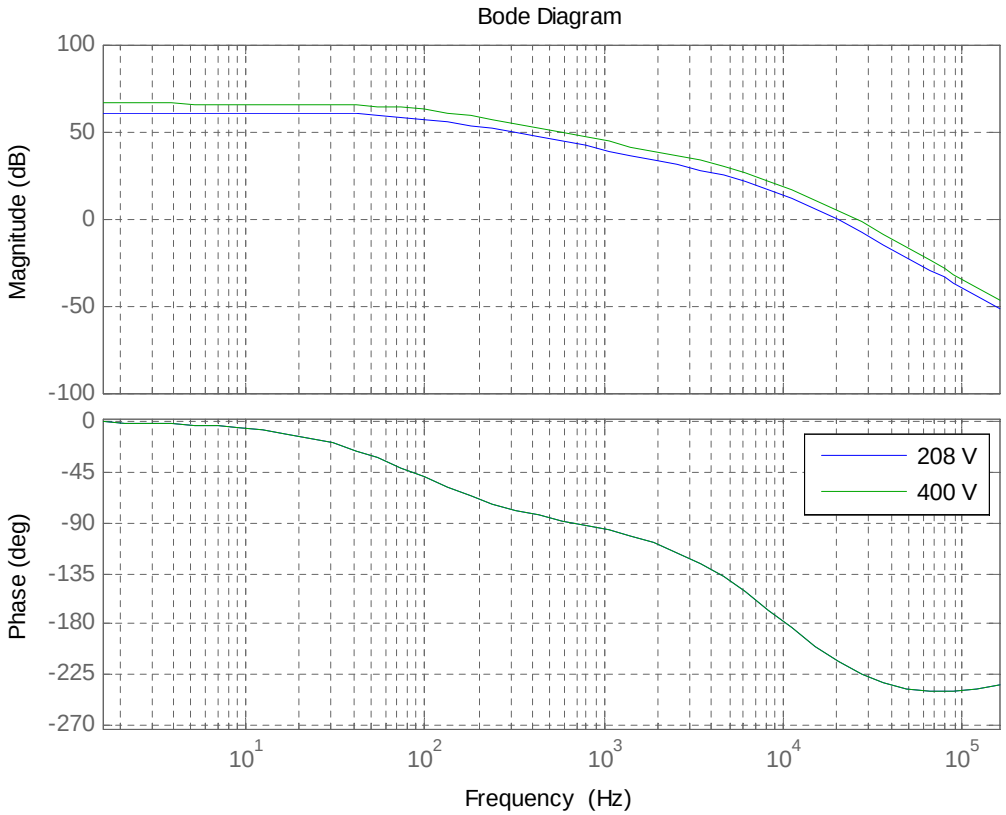


Fig. 30: Bode plot of transfer function in CCM at 208 V and 400 V input voltage

Since the converter needs to operate also at very light loads, the frequency response in discontinuous conduction mode is also of interest. The converter begins operating in discontinuous conduction mode at less than 1 kW with 208 V input and 662 W with 400 V input voltage.

The simplified transfer function of the boost converter with peak current mode

control in discontinuous conduction mode are expressed by [3]:

$$H(s) = \frac{G_{c0}}{1 + \frac{s}{\omega_p}} \tag{16}$$

$$G_{c0} = \frac{f_2 \cdot (R_{load} || r_2)}{R_i} \tag{17}$$

$$\omega_p = \frac{1}{(Rload || r_2) \cdot C} \tag{18}$$

$$f_2 = 2 \cdot \frac{I_2}{Ic} \tag{19}$$

$$r_2 = \frac{R_{load} \cdot (M-1)}{M} \tag{20}$$

$$M = \frac{P_{load}}{P_{load} - P} \tag{21}$$

$$P = \frac{\frac{1}{2} L_{i1} \cdot f_{sw}}{\left(1 + \frac{M_a}{M_1}\right)^2} \tag{22}$$

$$I_c = \frac{V_{in}}{L} T_{sw} \cdot D \tag{23}$$

$$D = \frac{\left(\frac{V_{int}}{V_{in}} - 1\right) \cdot 2 \cdot L \cdot \frac{P_{load}}{V_{int}}}{V_{in} \cdot T_{sw}} \tag{24}$$

$$I_2 = \frac{1}{2 \cdot T_{sw}} \cdot I_c \left(\cdot \frac{D \cdot T_{sw} \cdot V_{int}}{V_{int} - V_{in}} - D \cdot T_s \right) \tag{25}$$

Where R_{load} is the equivalent load resistance, D is the duty cycle, R_i is the gain of the current measurement, f_{sw} is the switching frequency and V_{in} is the input voltage.

In Figure 31 the transfer function H(s) is traced in a Bode plot, at the border between DCM and CCM.

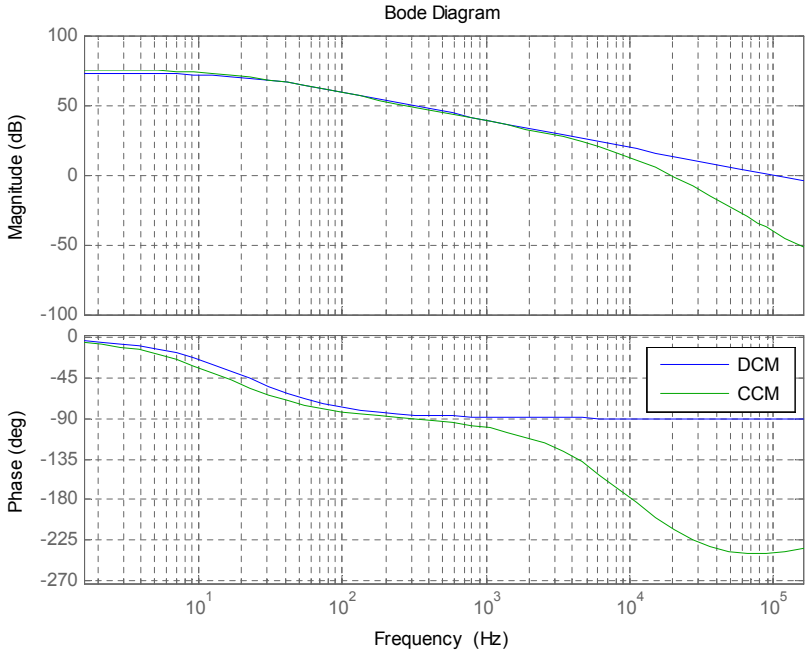


Fig. 31: Bode plot of the transfer function in the vicinity of CCM and DCM with 208 V input.

Since the converter in discontinuous conduction mode only exhibits a single pole, the design of the controller is easier and, therefore, the controller is focused on the CCM operation. The controller type chosen is a type-2 controller, whose transfer function can be described by:

$$G(s) = K\frac{\frac{s}{\omega_{zc}}+1}{s\cdot\left(\frac{s}{\omega_{pc}}+1\right)} \tag{26}$$

$$\omega_{zc} = \frac{1}{C_{c2}\cdot R_{c5}} \tag{27}$$

$$\omega_{pc} = \frac{1}{C_{c1}\cdot R_{c5}} \tag{28}$$

$$K = \frac{1}{R_{C3}\cdot\frac{R_{c2}+R_{c1}}{R_{c2}}\cdot C_{c2}} \tag{29}$$

If C_{c2}»C_{c1} and $R_{c3} >> R_{c2}$.

The controller parameters were found using Power 4-5-6, a program for designing switchmode power supply controllers, and then adjusted during the experimentation phase. The component values are summarized in Table 9.

Table 9: Values of control components of the boost converter.

Component	Value
R_{c1}	1000 kΩ
R_{c2}	100 kΩ
R_{c3}	1000 kΩ
R_{c4}	52.3 kΩ
R_{c5}	14.3 kΩ
C_{c1}	0.6 nF
C_{c2}	40 nF

This gives the loop responses shown in Figure 32 with 208 V input, Figure 33 full load at 400 V, Figure 34 light load (100 W) at 208 V and Figure 35 light load (100 W) 400 V. The system is stable at all operating points, and the lowest phase margin is 49 degrees, which has not been found to be a problem during testing.

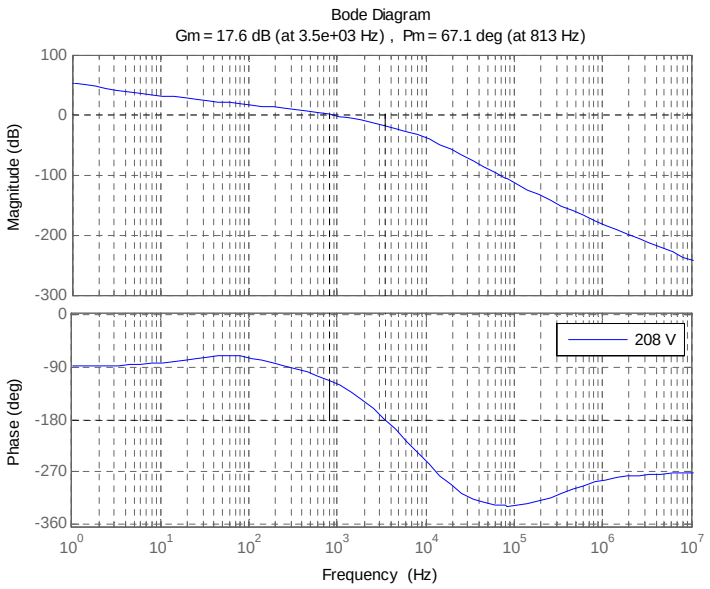


Fig. 32: Loop response with 208 V input at full load.

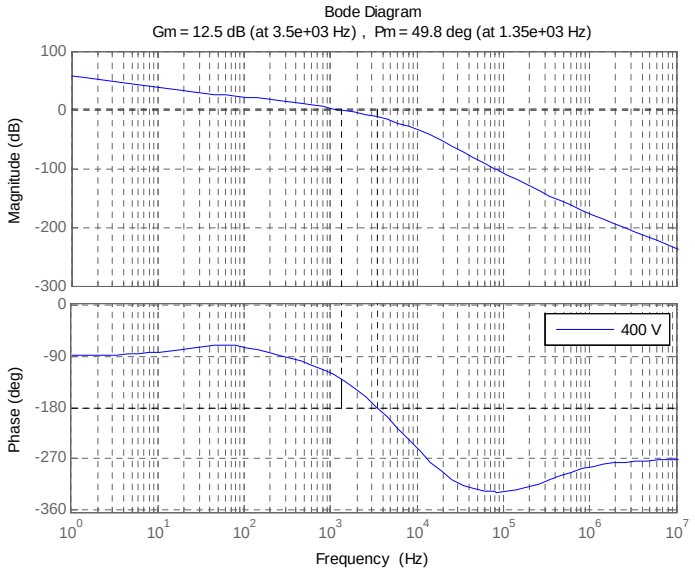


Fig. 33: Loop response with 400 V input at full load.

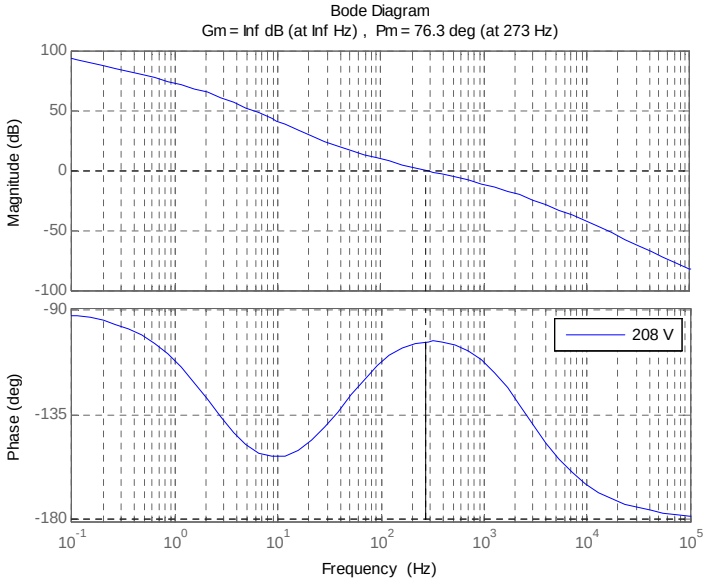


Fig. 34: Loop response with 208 V input at light load.

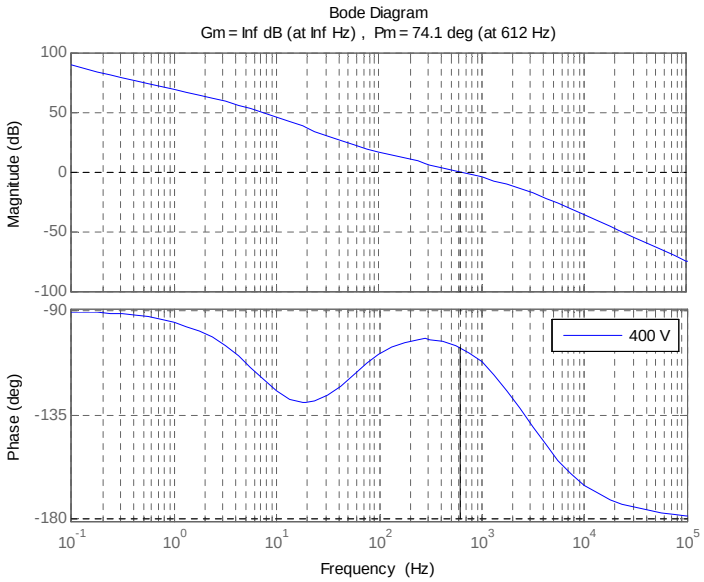
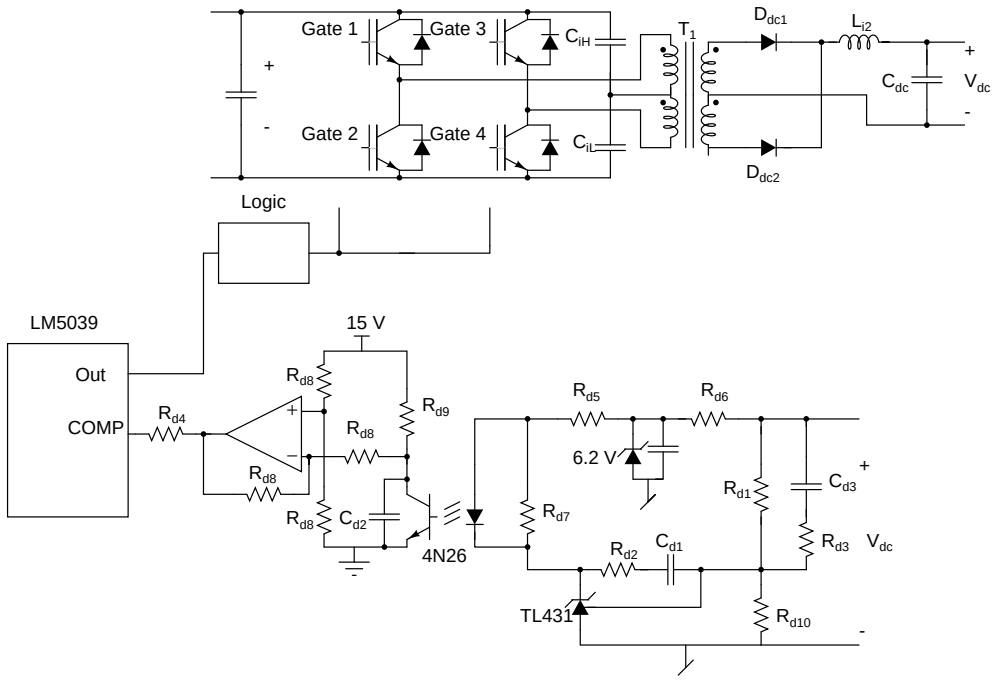


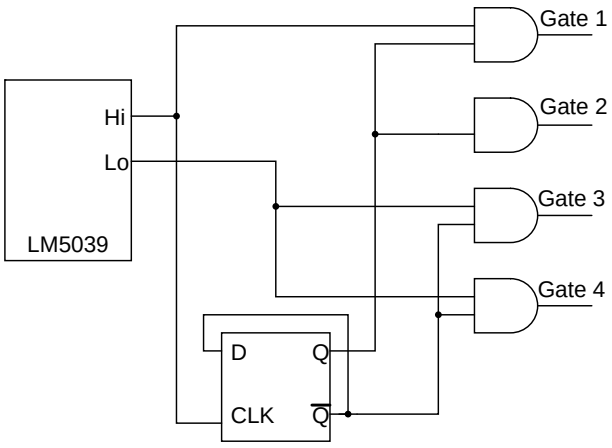
Fig. 35: Loop response with 400 V input at light load.

5.3 Control of the DC/DC converter

The control of the DC/DC converter is a done using voltage mode control in a type 3 controller [5]. The control is performed using the dedicated half-bridge controller LM5039. The control structure and the logic circuit generating the control signals is shown in Figure 36.



(a) Schematic



(b) Logic

Fig. 36: Control circuit for the DC/DC converter (a) the overall schematic (b) the logic circuit for dividing the control signals to the two half-bridges.

The gain, poles and the zeros in this controller can be determined by [6]:

$$P_1 = 0 \tag{30}$$

$$P_2 = \frac{1}{R_{\mathrm{d9}} \cdot C_{d2}} \tag{31}$$

$$P_3 = \frac{1}{R_{d3} C_{d3}} \tag{32}$$

$$Z_1 = \frac{1}{R_{d2} \cdot C_{d1}} \tag{33}$$

$$Z_2 = \frac{1}{C_{d3}\left(R_{d1} + R_{d3}\right)} \tag{34}$$

$$Gain = \frac{R_{\mathrm{d9}} \cdot R_{\mathrm{internal}}}{R_{\mathrm{d5}} \cdot R_{d4}} CTR \tag{35}$$

Where R_{internal} is the internal gain of the LM5039.

The controller parameters were found by simulation, and then adjusted during the experimentation phase. The component values summarized in Table 10 are found to work well.

Table 10: Values of control components of the boost converter.

Component	**Value**
R_{d1}	51 kΩ
R_{d2}	12 kΩ
R_{d3}	10 kΩ
R_{d4}	6 kΩ
R_{d5}	100 Ω
R_{d6}	6 kΩ
R_{d7}	1 kΩ
R_{d8}	100 kΩ
R_{d9}	750 Ω
R_{d10}	2.2 kΩ
C_{d1}	100 nF
C_{d2}	680 nF
C_{d3}	10 nF

A differential amplifier with a gain of one has been added after the optocoupler to increase the current through the optocoupler and to minimize the noise picked up by the optocoupler, since the controller circuit LM5039 sensitive to noise.

The LM5039 comes with a sof-start function which is utilized in order to ramp the output voltage of the converter.

5.4 Test results

The test results are divided into two parts. Test results from the Boost Rectifier and test results of the DC/DC converter. In Figure 37 a picture of the tested PCB is shown. The schematic can be found in Appendix A.

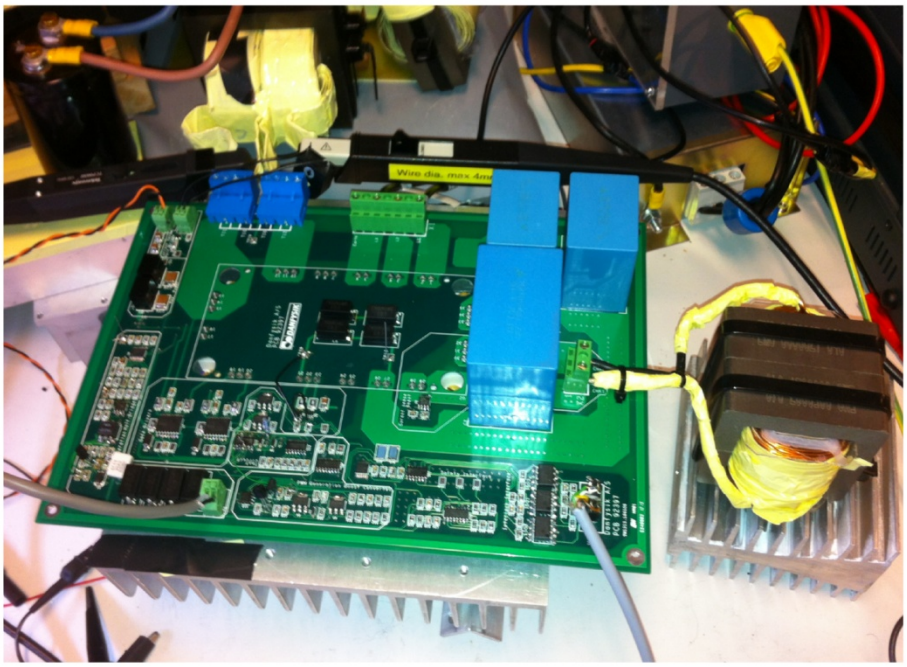


Fig. 37: The PCB used during the test.

Boost rectifier

The simulated and the measured results are shown in the figures below. The simulation is done using the spice simulator LTSpice. The phase currents are compared in Figure 38, while the DC-link voltages are compared in Figure 39. The results shown are with 208 V input and an output power of 5200W. The DC-link voltage reference is set to 570 V. As can be seen there is good correlation between the measurements and the simulated values.

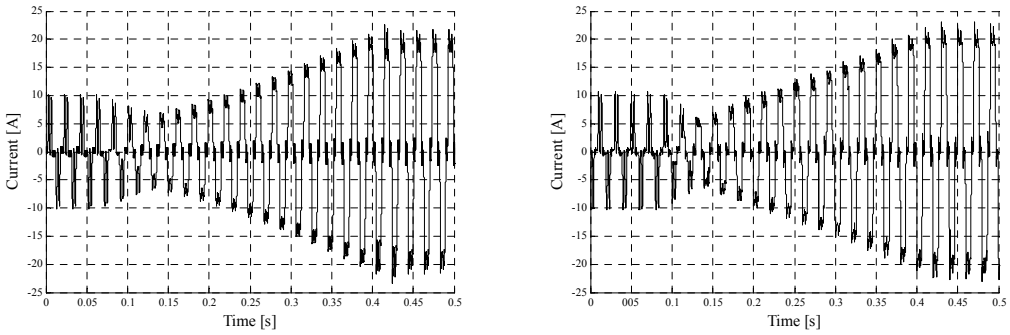


Fig. 38: (a) Simulations of the grid phase currents (b) Measurement of the grid phase currents. The waveforms are shown for a startup ramp, where the soft start is clearly seen.

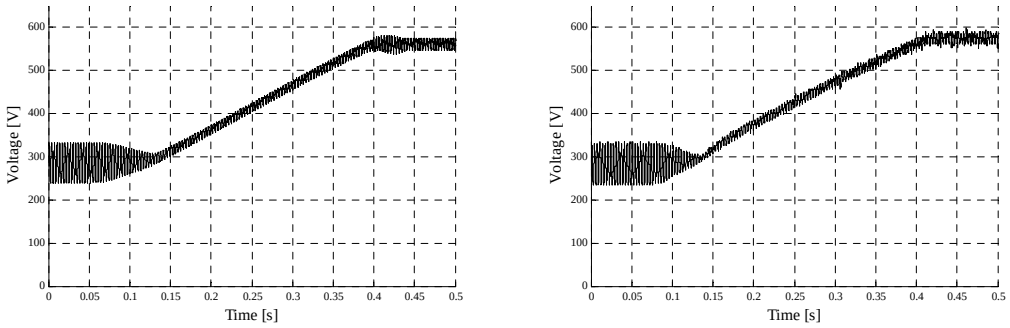


Fig. 39: (a) Simulations of the DC-Link Voltage (b) Measurement of DC- Link Voltage. The waveforms are shown for a startup ramp, where the soft start is clearly seen.

The efficiency has also been measured using a three phase power analyzer (Norma D6100) and the results are reported in Table 11.

Table 11: Values of control components of the boost converter.

208 V				**400 V**			
Pin [kW]	Pout [kW]	Power factor	Efficiency	Pin [kW]	Pout [kW]	Power factor	Efficiency
5.28	5.08	0.952	96.2	5.17	5.08	0.94	98.3
4.37	4.21	0.94	96.3	4.28	4.21	0.94	98.4
3.49	3.37	0.95	96.6	3.42	3.37	0.93	98.5
2.20	2.13	0.95	96.8	2.16	2.12	0.89	98.1
1.77	1.70	0.95	96.0	1.74	1.70	0.86	97.7
1.27	1.22	0.95	96.1	1.25	1.22	0.80	97.6
0.89	0.854	0.95	96.0	0.87	0.85	0.7	97.7
0.5	0.47	0.94	94.0	0.49	0.47	0.6	95.9

DC/DC converter

The efficiency of the DC/DC converter is shown in Figure 40, again measured with a power analyzer (Norma D6100). During testing, the DC/DC converter did not show the expected efficiency, which could be due to circulating currents resulting in increased switching and conduction losses, this is further analysed in Section 5.5. The problem can be seen in Figure 41. The efficiency measure is about 92 %.

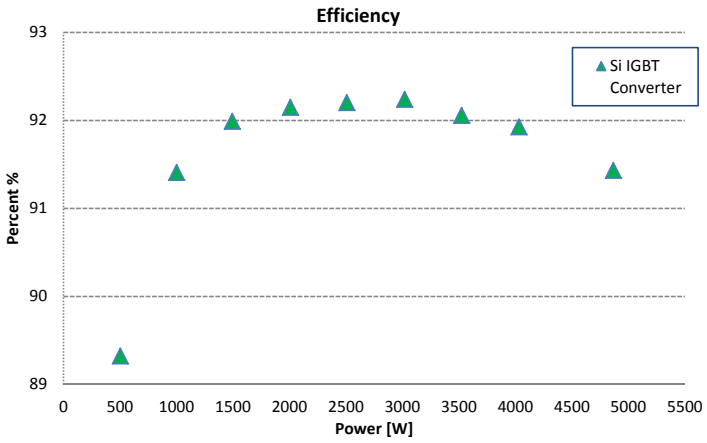


Fig. 40: Efficiency of the isolated DC/DC converter

5.5 Analysis of problems with DC/DC converter

As seen from the section before the efficiency and performance of the boost rectifier is high. However this is not the case for the DC/DC converter. A cause of this lack of performance from the DC/DC converter could be found in the current in the primary side transformer on the opposite winding of which there is actually being switched. The current is marked in Figure 41 and was found during the testing of the converter.

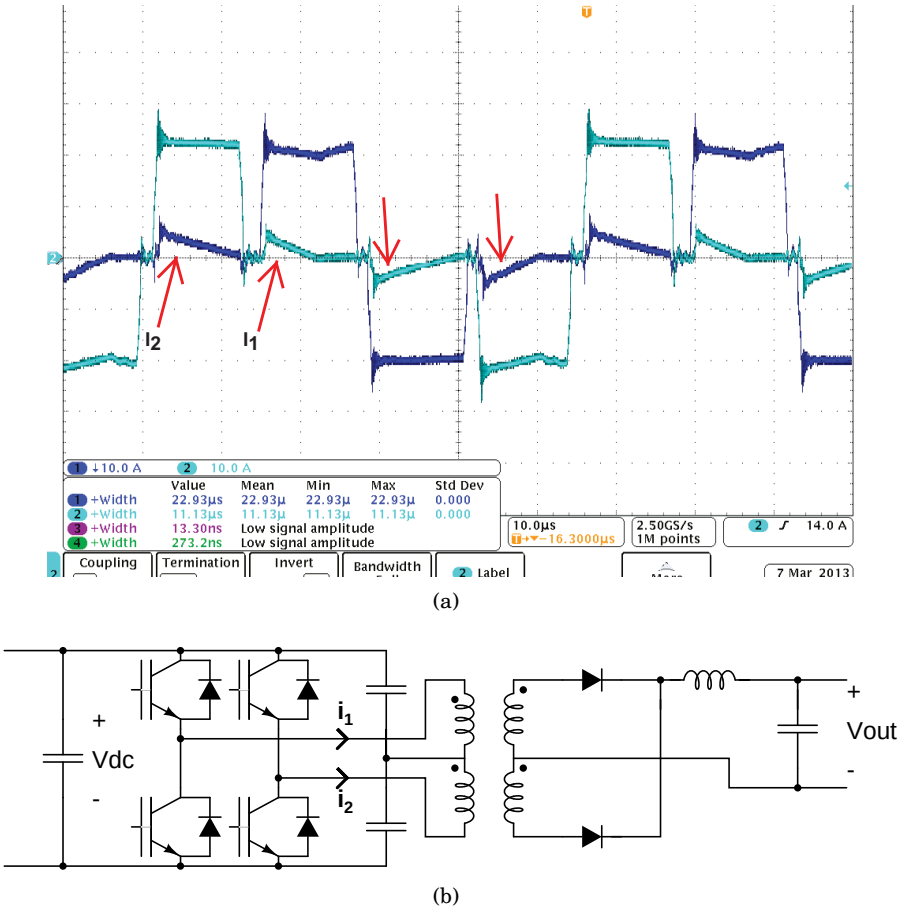


Fig. 41: Transformer currents in the primary side windings, marked current in opposite winding of which is being switched into. (a) Currents. (b) Circuit.

As can be seen the current is about 5 A and causes extra losses in the primary side diodes of the opposite winding, the windings of the transformer and the switching IGBT. So why is this current generated? In order to answer this an equivalent circuit of the case is drawn in Figure 42.

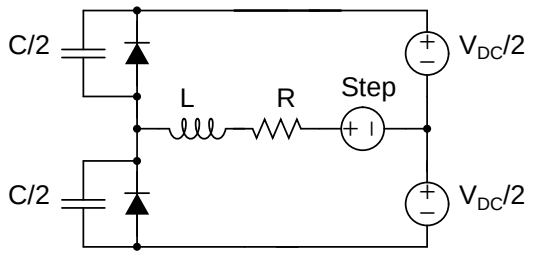


Fig. 42: Equivalent circuit describing the current in the opposite winding.

In the equivalent circuit the winding of the passive side of the transformer is equivalated by a step voltage source which is changing the voltage, as if it were done by the other primary winding. The IGBTs are replaced by only the freewheeling diodes and drain source capacitance as these are turned off during this time. The capacitors generating the midpoint voltage is equivalated by voltage sources, as during this short time period the voltage will not change significantly over these.

As is made clear from the equivalent circuit what is happening is a step voltage into an RLC circuit, which is drained by the freewheeling diodes of the IGBTs. The current in the inductor can be described by the following equation in the Laplace domain:

$$i(s) = v(s)\frac{1}{R + L \cdot s + \frac{1}{s \cdot C}} \tag{36}$$

$$i(s) = v(s)\frac{\frac{s}{L}}{s^2 + \frac{R}{L}s + \frac{1}{L \cdot C}} \tag{37}$$

The characteristic equation of the above differential equation can be described with equations below:

$$0 = s^2 + \frac{R}{L}s + \frac{1}{L \cdot C} \tag{38}$$

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}} \tag{39}$$

$$\alpha = \frac{R}{2 \cdot L} \tag{40}$$

$$0 = s^2 + 2\alpha \cdot s + \omega_0^2 \tag{41}$$

The roots of Equation 41 can be described with:

$$s_1 = -\alpha + \sqrt{\alpha^2 - \omega_0^2} \tag{42}$$

$$s_2 = -\alpha - \sqrt{\alpha^2 - \omega_0^2} \tag{43}$$

The current in the time domain can then be described by:

$$i(t) = A_1 e^{s_1 \cdot t} + A_2 e^{s_2 \cdot t} \tag{44}$$

Solving this equation requires to find the constants A_1 and A_2. This is done by solving with the two initial conditions $i(0) = 0$ and for a positive step $\frac{di(0)}{dt} = \frac{V_{dc}}{2 \cdot L}$. This yields that:

$$A_1 = -A_2 \tag{45}$$

$$A_1 = \frac{V_{dc}}{2 \cdot L \cdot (s_1 - s_2)} \tag{46}$$

After the initial increase in current the voltage across the capacitors will increase until the diode starts to conduct. Hereafter the current in the inductor will slowly decrease until zero current is reached. The current will decrease at a rate dictated by the voltage drop over the conducting diode and the resistance of the winding.

The leakage inductance of the transformer has been measured to be 1.4 μH in total using an LCR-meter. This gives 0.7μH in each primary winding. The resistance of one winding has been measured to be 5 mΩ In order for the waveforms to fit this corresponds to a capacitance between collector and emitter of the IGBT to be approximately 100 pF.

The resulting waveform with the given equations for a positive voltage step is shown in Figure 43. As can be seen there is a rapid increase in the current caused by the low leakage inductance. The current rapidly increases to approximately 5 A, at this points the voltage in the midpoint is increased so much that the upper diodes starts to conduct. From this point the inductor is discharged through the diode at a fairly low rate. From the datasheet it is seen that the voltage drop is around 0.4 V. In Figure 44 there is a zoom of the increase in the current.

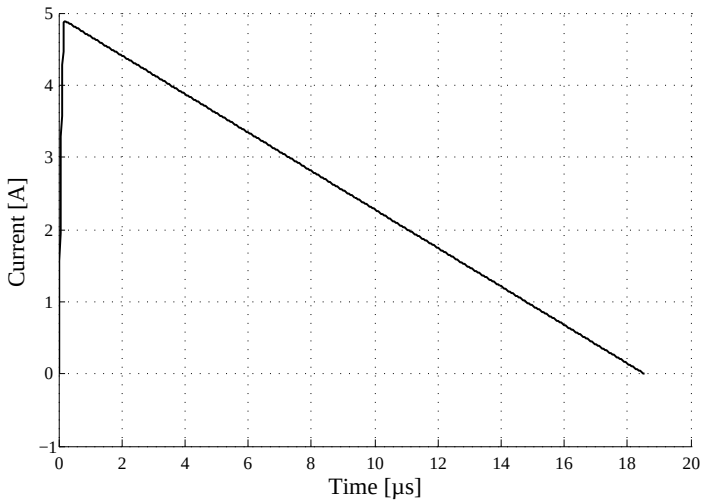


Fig. 43: Current waveform resulting from a step on the opposite winding.

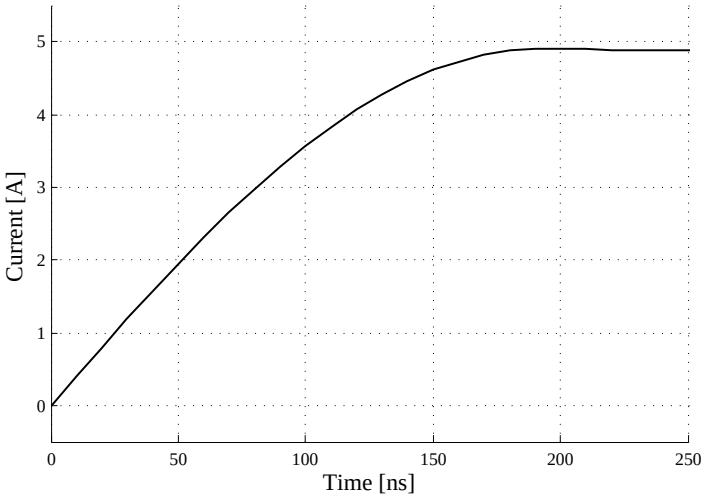


Fig. 44: Zoom of transient response in current during the step on the opposite winding.

Losses

As has been shown this current in the opposite winding of which is being switched is around 5 A, and almost present through the whole switching period. As has been

said this extra current not only affects the losses of the diode and the winding resistance. It also affects losses of the conducting transistor and the winding on the switching side. In Table 12 the losses caused by this current are summarized.

Table 12: Extra losses caused by the extra current

Diode	Winding 1	Winding 2	IGBT
2 W	72 mW		4 W

Dampening the LC circuit

In order to dampen the LC circuit and minimizing the current caused by the opposite winding switching and improving EMI performance different dampening schemes have been considered. As it is impractical to dampen across the leakage inductance, it has been chosen to dampen the LC circuit by adding a small inductance and dampening this with a resistor across [3]. This has been illustrated in Figure 45.

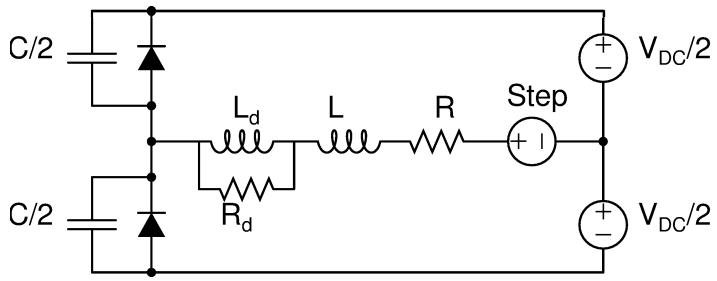


Fig. 45: Dampening of the LC circuit.

It is chosen to consider a 1 μH inductor as L_d. This value has been chosen as this is the range of leakage inductance and will be fairly cheap as it is available as an SMD component. In order to determine the size of the resistor R_d the transfer function is considered.

$$\frac{i_L(s)}{V_{step}(s)} = \frac{1}{L \cdot s + R_d || L_d + \frac{1}{C \cdot s}} \tag{47}$$

In order to determine the value of R_d multiple values have been calculated using Matlab's step function in order to determine the shortest settling time. The value

giving the shortest settling time has been determined to be 35 Ω giving a settling time of approximately 0.2 μs. This is illustrated in Figure 46.

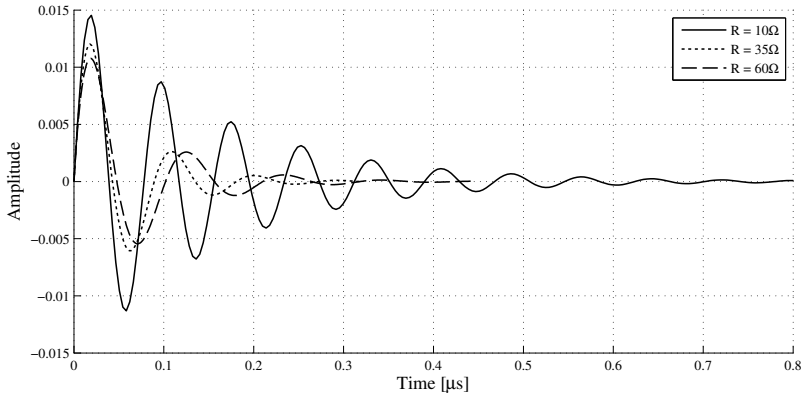
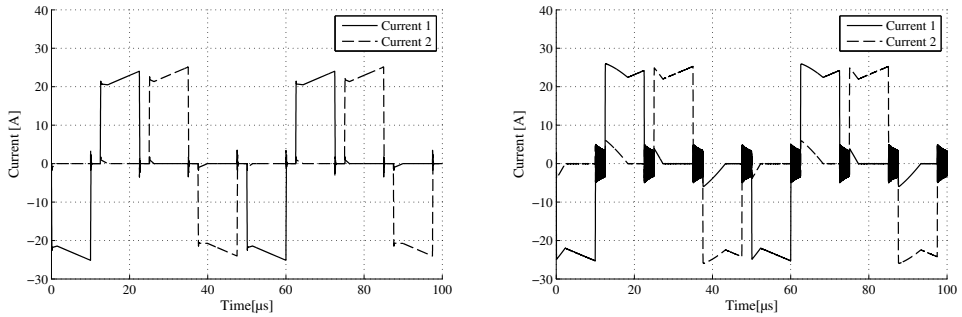


Fig. 46: Step response of dampening with different resistances.

In order to confirm that the dampening circuit has successfully dampened the oscillation the inductor current has been simulated in LTSpice, both with and without dampening. The results of these simulations are shown in Figure 47.



(a) With damping (b) Without damping

Fig. 47: Simulation of the transformer current with and without damping.

It is seen that the current pulse is reduced and the oscillations are almost removed.

5.6 Conclusion

The input converter has been designed and tested. It can deliver the 60 V for the output converter and the input voltage range has been tested from 208 to 400 V. The efficiency of the boost rectifier is high, above 98 % for 400 V input and above 96 % for the 208 V input. However the efficiency of the dual half-bridge DC/DC converter is low, around 92 %. A problem caused by reflected voltages on the primary side was observed and a snubber decreasing the current caused by the reflected voltage is presented.

The EMI performance still needs to be tested in order to determine whether the EMI filter is good enough, too small or can be reduced in size. The power factor obtained is around 0.94-0.95.

In the next chapter an isolated DC/DC converter with wide band gap devices is presented. This could help increase the efficiency of the converter, however compromising price and the idea of a one module converter.

6 SiC Converter

Wide bandgap material based semiconductors (Silicon Carbide – SiC or Gallium Nitride - GaN) are in these years going through a rapid development. These components promise much in efficiency and smaller dimension, but still have relatively high cost. However during the last years the prices has also been dropping and therefore SiC seems more and more like a reasonable competitor to Si based semiconductors [7]. In this section a galvanic isolated DC/DC converter based on wide bandgap semiconductors.

In all fields of power electronics there is a growth in demand for more efficient power electronics. In the past few years a lot of research has been done to improve or replace the existing silicon (Si) technology in power converter applications. Due to their material properties these devices have superior characteristics to equivalent Si devices [7]. This is resulting in higher operating temperature, higher operation frequency, and high thermal conductivity resulting in the possibility of higher power density. Many studies have been made in the virtues of SiC in power converters, in the pursuit of the higher efficiency or smaller dimension [8] [9] [10] [11] [12] [13] [14].

The design specifications of the efficiency optimized converter built with wide bandgap devices are listed in Table 13. It has been chosen to design the converter

as a phase-shifted full-bridge and with a current doubler in order to reduce switching losses of the switching semiconductors and conduction losses in the rectifier.

Table 13: Specifications for the SiC prototype DC/DC converter

Input voltage range	V_{int}	600-800 V
Output voltage	V_{dc}	60 V
Output power	P_o	5000 W
Switching frequency	f_{sw}	40 kHz
Target efficiency	η	98 %

The schematic of the Phase Shifted Full-Bridge converter with current is presented in Figure 48. The output voltage is controlled by the phase shift between the switches of the two legs in the inverter (right leg – leading, left leg - lagging), see Figure 49. To achieve Zero Voltage Switching (ZVS) the energy stored in the output filter inductors together with the device capacitances is utilized for the leading leg. To achieve ZVS in the lagging leg the energy stored in the transformer leakage and magnetizing inductance is exploited [15]. The dead-time between the switching of the upper and lower transistors has to be calculated differently for the leading and the lagging leg, due to the earlier mentioned different leakage energies [16]. To obtain high efficiency, keeping the simplicity of the topology and limit the leakage inductances, the full-bridge transistors are wide band gap devices. These transistors have low switching losses at high switching frequency and better heat management characteristics compared to Si semiconductor devices. The selected devices for this application were normally-off JFETs as their market price was much lower than the price of the SiC MOSFETs. On the other hand SiC JFETs require special gate drivers and bipolar gate supply. By paralleling two JFETs for each switch, 5 kW transferred power can be obtained [17].

The transformer and the filter inductors were designed for 40 kHz switching similarly to the IGBT converter. The two-winding transformer was designed with n=0.24 turns ratio to supply the controlled output voltage by the phase shift from the required input voltages. The output filter inductors were designed to conduct the half of the load current with a peak-to-average ripple of 20%. The SiC JFETs utilized are the SemiSouth SJEP120R100 JFETs, which are normally off 1200 V devices with an on-state resistance of 100 mΩ: The gate driver is also from SemiSouth SGDR2500P2, which is specifically designed to drive JFETs.

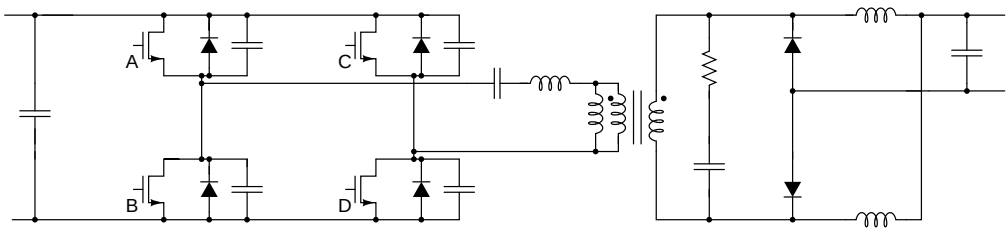


Fig. 48: Full bridge with paralleled JFETs and current doubler output diagram.

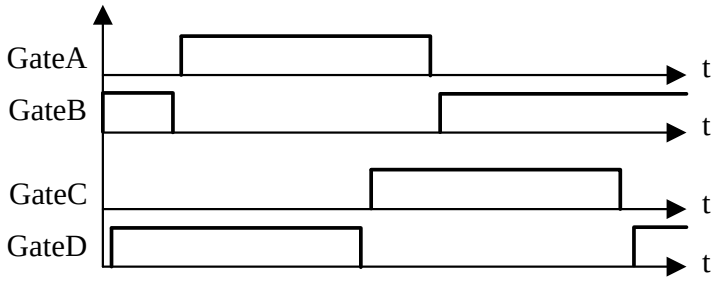


Fig. 49: Switching pattern for the SiC converter.

A photo of the tested converter is shown in Figure 50.

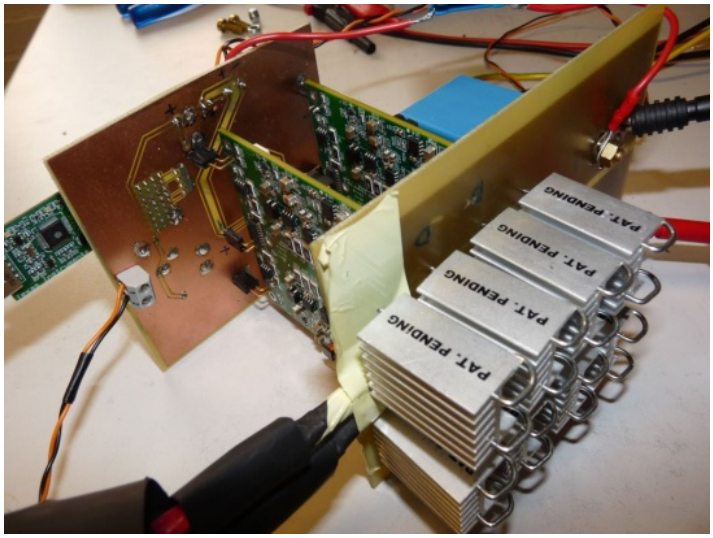


Fig. 50: Full bridge with paralleled JFETs and SGDR2500P2 gate-drivers.

6.1 Experimental results

The efficiency of the converter was measured with a Norma D6100 power analyzer and it has been plotted in Figure 51. The maximum efficiency of the SiC converter has been reached between 1 kW and 3 kW of the output power, and it is approximately 5 % higher than for the Si IGBT converter over a wide power range.

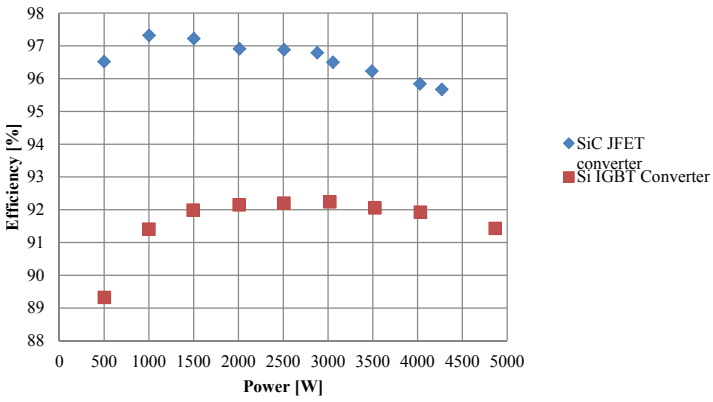


Fig. 51: Efficiency of Si IGBT converter and the SiC JFET converter

6.2 Cost comparison

In order to compare the costs of the two converters, initial and running costs need to be addressed. The initial cost is the price of the devices used in the two converters. An estimate of this has been summarized in Table 14, in which all the prices have been taken from the component distributor Farnell.

Table 14: Cost comparison between silicon and silicon carbide devices

	IGBT converter costs [€]	SiC converter costs [€]
Drivers	17.4	330
Semiconductors	69	200
Magnetics	47	67
Heat sink	122	46
Total	260	640

The cost of the SiC is more than the double of the IGBT converter, mainly because of the cost of the drivers and the cost of the semiconductors. The drivers for the SiC are more expensive because they need to support the special driving scheme required by the SiC JFETs. On the other side, the cooling requirement is much higher for the IGBT based converter than for the SiC based converter. However it should be said that the cost of the driver could be reduced by developing or adapting a conventional gate drive instead of utilizing a stock gate drive.

The average electricity price for industry in Europe in 2011 was 0.118 €/kWh [4]. From this price and the price difference of the two converters, the break even scenario for different output powers has been calculated and plotted in Figure 52.

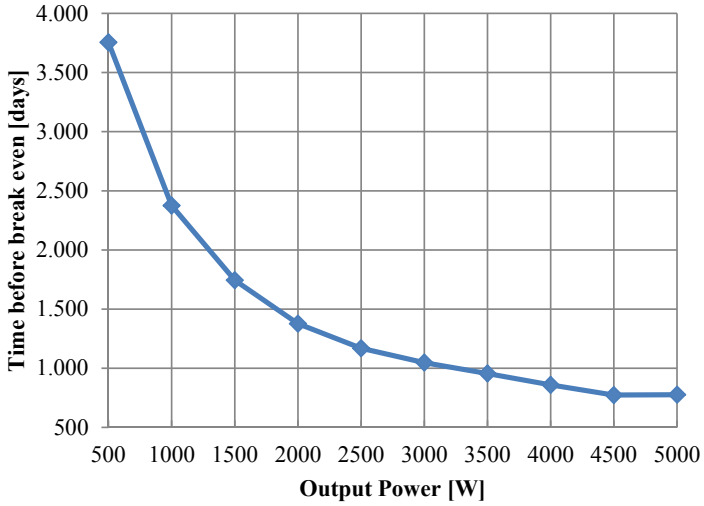


Fig. 52: Efficiency of Si IGBT converter and the SiC JFET converter

The time required to justify the use of a more expensive SiC based converter is a function of the time of operation of the converter. In the case of a 5 kW power supply running 24 hours/day at full power, the extra investment is paid back in 772 days, corresponding to 2.1 years. Based on these prices it seems unlikely any costumers would pay the extra price it the SMPS would cost to gain the higher efficiency.

In the next part the reliability of the converter with PIM module will be considered.

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Part III

Reliability considerations

Reliability

7 Reliability of power converters

One of the important aspects of a particle accelerator power supply is its reliabilit,y as these typically are in operation for several years many hours a day and there are typically many power supplies connected to a single particle accelerator. In a power supply there are many components, some of which are prone to failure. Statistical analysis of the components that most frequently gives rise to failures are found in [1] and [2]. According to [1], which is based on 200 products from 80 companies, the most fragile components are the PCB, followed by capacitors and semiconductors. In the second survey Yang et al. finds that the most fragile components are the semiconductors followed by capacitors and gate drives [2]. Both results are displayed in Figure 53.

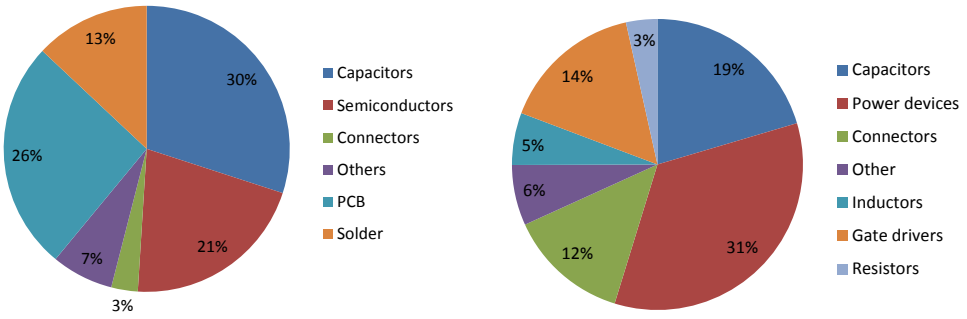


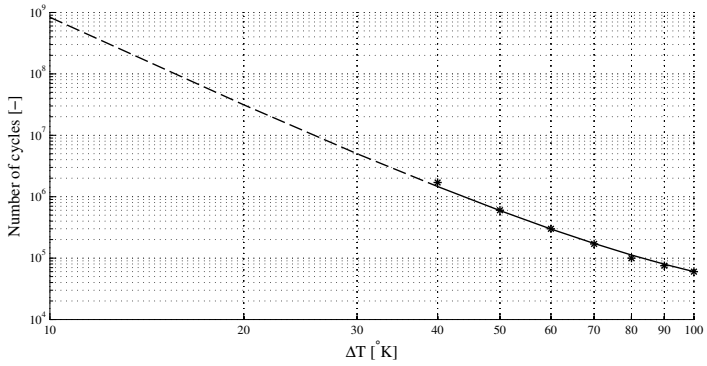
Fig. 53: Surveys on fragile components in power electronics (a) [1] (b) [2].

As can be seen from the statistics gathered the most fragile components seems to be the semiconductors followed by capacitors and gate drivers. In the proposed

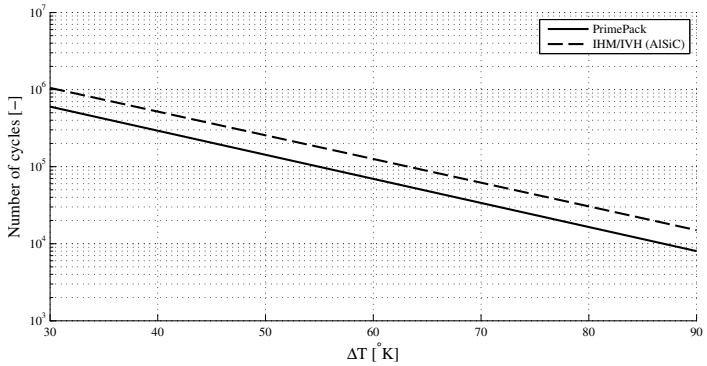
input converter based on a PIM mainly film capacitors has been utilized, the reliability of these are greatly improved compared with electrolytic capacitors. It is therefore considered improbable that these will be the failure prone components. In this thesis it has therefore been chosen to focus on the power module of the input converter.

One reason for believing that the power module could be the first component to fail during operation is that the power supply is specified to operate in ramp mode as seen in the specifications in Table 8. As can be seen from that table the shortest rise time from minimum to maximum current of the input converter is 0.5 s. If the converter is repeatedly ramped with this cycle it will reduce the lifetime of the module. Therefore it is interesting to examine how many ramps the module can be expected to last and ultimately what lifetime to expect.

When examining cycling there are two different types of cycling, thermal cycling and power cycling. The two types of cycling are defined as thermal cycling, being cycles lasting minutes, and power cycling, as short term cycling up to around 60 s. The effect on the lifetime is illustrated in Figure 54.



(a) Power cycling



(b) Thermal cycling

Fig. 54: Data from Infineon on their IGBT4 modules on (a) power cycling and a fit a LESIT Coffin-Manson model, $t_{on}+t_{off}=3$ s, and (b) thermal cycling capabilities of a Prime Pack module and a module with AlSiC baseplate, $t_{on}+t_{off}=5$ min. [3].

As can be seen from Figure 54 the slow thermal cycling yields a much lower amount of cycles than the module can withstand through power cycling. In order to understand how cycling affects the IGBT module it is necessary to look at how such a module is constructed. The cross sectional view of a typical IGBT module is shown in Figure 55.

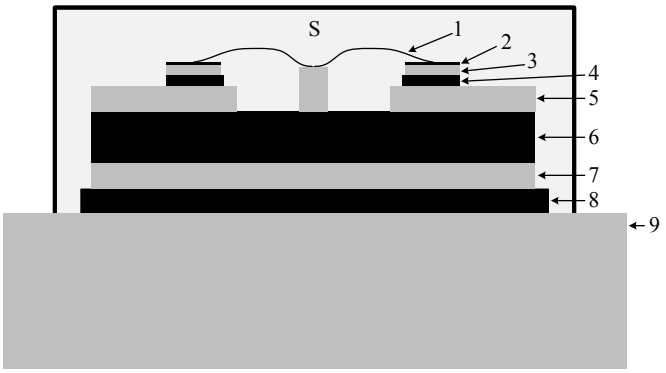


Fig. 55: Cross sectional view of a typical power module [4].

As can be seen from Figure 55 a typical IGBT modules consists of different materials. From the bottom up it is a mounting plate for cooling purposes. Onto the mounting plate there is soldered a DCB (direct copper bonding), which is a layer of ceramic with copper bonded onto its surface on both sides. On top of the DCB the silicon chips are soldered, these are then connected by aluminum bond wires to the terminals and other parts of the module. These materials are listed with typical thickness and Coefficient of Thermal Expansion (CTE) in Table 15.

Table 15: Materials in a typical IGBT module [4].

Parameter	Material	CTE ppm/^{o}C	Thickness μm
1: Bondwire	Al	22	400
2: Chip metal	Al	22	3
3: Chip	Si	3	300
4: Die attach	Solder paste	Compliant	50
5: DCB upper layer	Copper	17	300
6: DCB ceramic	Al2O3 or AlN	7 or 4	700
7: DCB lower layer	Copper	17	300
8: DCB attach	Solder paste	Compliant	100
9: Mounting plate	Copper or AlSiC	17 or 8	3000

From Table 15 it can be seen that the thermal coefficients of expansion are very different. Thereby during heat up or cool down the materials expand differently. This difference in expansion gives rise to stress in the interconnection. Especially the bond wires to the silicon chips and the solderings between DCB and mounting plate and between the DCB and the silicon chips are prone to failure.

Thermal cycling will typically cause failures in the solderings causing voids in the solder. This will lead to higher thermal resistance from the silicon chip to the heat sink, thereby also increasing the losses, and thus eventually cause failure in the module due to over temperature. Examples of heel cracking and solder voids is shown in Figure 56.

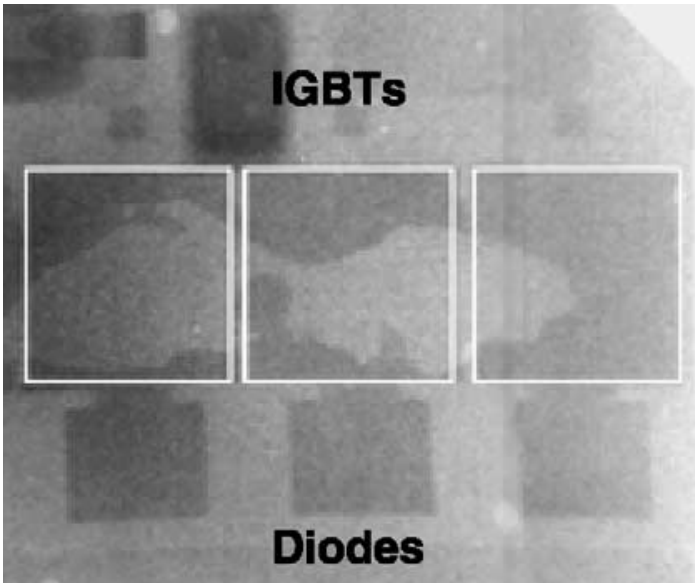
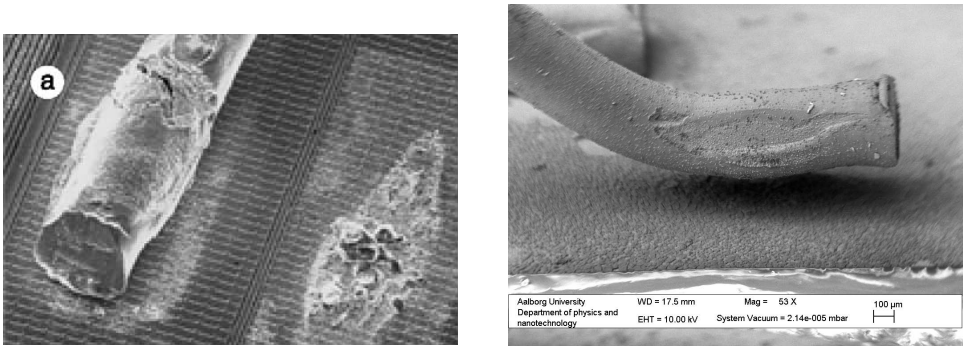


Fig. 56: X-ray microscopy of an IGBT module. Light spots below the IGBTs are present on the soldering layer indicating voids [4].

Power cycling will however typically cause failures with the bond wires, either as heel cracking or as bond wire lift off. An example of bond wire lift off is shown in Figure 57.



(a) (b)

Fig. 57: Examples of bond wire failure due to power cycling. Bond wire lift off, caused by fatigue in the interconnection between silicon chip and bond wire. [4]

As can be seen from Figure 54 thermal cycling or power cycling will give rise to a finite number of possible cycles before failure occurs in the module. In the next section models for approximating the number of cycles is presented. Models for the input converter module (PIM) is then set up and lifetime is calculated based on a given mission profile.

8 PIM lifetime modeling

In this section an expected number of cycles, considering the PIM used in the input converter, FP75R12KT4_B11, will be calculated. In order to be able to calculate the number of cycles before failure it is necessary to have three models:

1. Loss model
2. Thermal model
3. Life time model

The loss model should estimate the losses in the module. This is needed as input to the thermal model which will predict the temperature changes in the module. The temperature changes is then fed to the life time model which calculate the expected number of cycles for a given temperature profile.

In order for the loss model to calculate the losses a mission profile is needed. The total model structure is shown in Figure 58.

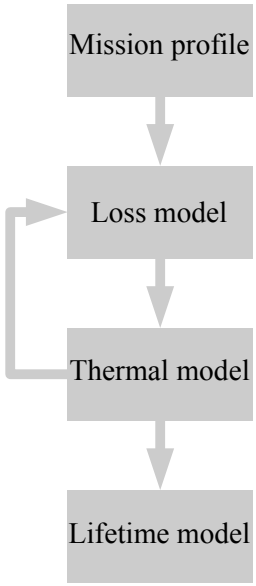


Fig. 58: Reliability simulation model block diagram.

From the thermal model there is a feedback to the loss model. This feedback is needed as many of the losses are depended on the junction temperature of the IGBTs and diodes. If the model should be even more correct there should also be a feedback from the lifetime model to both the thermal model and the loss model, as the thermal and electrical connections degrade when the module is cycled. This effect would accelerate the degradation further. However it is not within the scope of this thesis to create these models and it should be expected that these effects are included in the power cycling data given by the module manufacturer.

In the next section lifetime models in general will be described together with tests for determining lifetime of modules. This is followed by a loss model for the module used in the input converter. Thirdly the thermal model of the module and cooling system is described. Hereafter a mission profiles is presented. In the end the impact of different variables, such as input voltage, DC-Link voltage on switching frequency, on the lifetime of the module, is theoretically examined.

8.1 Life time model

In order to utilize the data from the thermal model a life time model for the module is necessary. Over the years many different lifetime models have been created.

The first research in IGBT life time models was published in the 1990's with the LESIT (Leistungselektronik Systemtechnik und Informationstechnologie) project. A project meant to increase the reliability of power electronics in railway applications. The project showed the strong correlation between the delta temperature change of the junction of the IGBTs and the lifetime. This they have modeled in a Coffin-Manson equation for plastic fatigue. Also included in their model is a Arrhenius equation [5], taking into account the medium temperature of the junction. The Arrhenius equation describes that the higher the temperature the faster the reaction rate. The proposed equation from the LESIT group is shown below [6]:

$$N_f = A \cdot (\Delta T_j)^{\alpha} \cdot \exp \frac{E_a}{\kappa_B \cdot T_m} \tag{48}$$

Where A= 302500 is a constant $K^{-\alpha}$, E_a = $9.89 \cdot 10^{-20}$ J, ΔT_J is the temperature swing, α= -5.039, $\kappa_B = 1.38066 \cdot 10^{23}$ $JK^{-}1$, T_M is the medium temperature in Kelvin and N_f is the expected number of cycles before failure.

The LESIT results was obtained through an extensive survey of modules with Al_2O_3 base plates. The results from the tests are summarized in Figure 59.

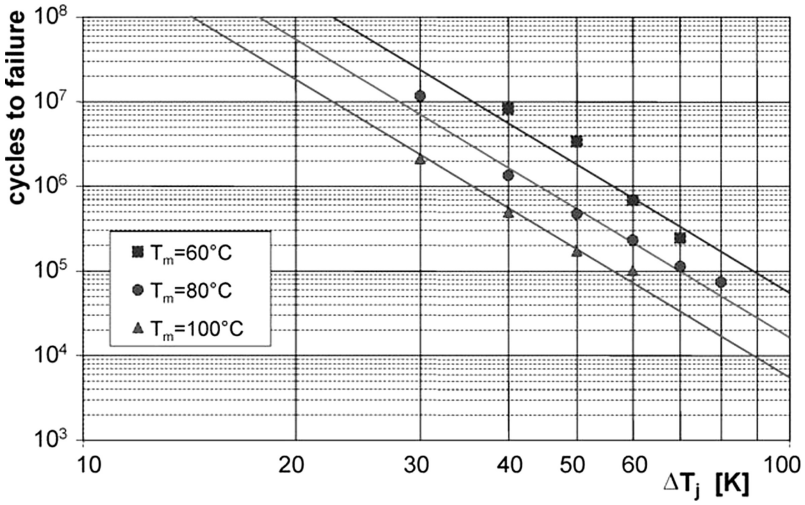


Fig. 59: The results from the LESIT project [6] ©1997 IEEE.

However even before the LESIT project research in the reliability of interconnecting materials was done [7]. Here also the frequency of the power cycling is

taken into account. The frequency of the cycle time has an effect on lifetime as the relaxation time constant of the solder is in the minute range, whereas the bond wire relaxation time constant is in the range of seconds [8].

This model however comes without parameters as this is generic for interconnections and not particularly minded on IGBT modules. The model is shown in Equation 49.

$$N_f = A \cdot f^B (\Delta T)^\alpha \cdot \exp \frac{E_a}{\kappa_N \cdot T_m} \tag{49}$$

Where f is the frequency of the cycle and B is a curve fitting component.

In 2008, Bayerer et. al. proposed another model. Here not only the temperature change, and medium temperature was included, but also the voltage rating, the current during the cycling and the diameter of the bond wire used in the module is included. This results in a model for IGBT4 modules which can be described by the following equation [9]:

$$N_f = A \cdot (\Delta T)^{B_1} \cdot \exp \frac{B_2}{T_m} \cdot t_{on}^{B_3} \cdot I^{B_4} \cdot V^{B_5} \cdot D^{B_6} \tag{50}$$

Where, all 6 B values are constants, t_{on} is the on time during power cycling, I is the current, V is the voltage rating, D is the diameter of the bond wire. The value of the constants can be found in the article [9].

The relationship with the factors given by Bayerer et. al. is found empirically, however it is possible, to give an explanation to the factors included in the model. The time dependence t_{on} can be caused by the transient thermal response of the module giving that a longer time period will give more time for the heat to propagate down through the entire module. The current is accelerating the end of life by heating up the remaining interface between the IGBT chip and bonding wires. The blocking voltage is related to the chip thickness, giving that a thinner chip will follow the expansion of wires, solders and substrates, thus the difference in thermal expansion is reduced for thin chips.

In 2013 Scheuermann et. al. proposed a fourth model. According to the authors new sintered modules, where the IGBT chip is sintered to the DCB, shows that the arc geometry of the bondwire is also important to the lifetime of the bonding interface. They believe that the previously this effect of the bondwire geometry was

masked by the fatigue of the solder. The model proposed by Scheuermann et. al is listed below [10]:

$$N_f = A \cdot (\Delta T)^{\alpha} \cdot ar^{\beta_1 \cdot \Delta T + \beta_0} \cdot (\frac{C + t_{on}^{\gamma}}{C+1}) \exp \frac{E_a}{\kappa_B + T_m} \cdot f_{Diode} \tag{51}$$

Where ar is the impact of the wire bond aspect ratio. The f_{Diode} is the a description of the chip thickness. Values for all the constants can be found in the article [10].

As can be seen there is a large number of different models for describing the lifetime of IGBT modules. To conclude on this a list of the factors influencing the lifetime of the IGBT modules is listed below in descending order from highest to smallest.

1. The ΔT, the change in junction temperature per cycle
2. T_m the absolute medium temperature of the junction
3. The t_{on}, the on time during the test.

Other factors such as the thickness of the die, the current through the device and bond wire geometry also seems to affect the lifetime of an IGBT module.

In the above a lot of different lifetime models for IGBT modules are described. However this is not the typical data you will get from the IGBT module manufacturers. Here you will typically get a curve describing their tested lifetime of a given IGBT type. An example of this is shown in Figure 54 (a). The dependents on cycle time to number of expected power cycles can according to Infineon be described by [11]:

$$\frac{N_{cyc}(t_{on})}{N_{cyc}(1.5)} = \left(\frac{t_{on}}{1.5}\right)^{-0.3} \text{ for } 0.1\ s < t_{on} < 60\ s \tag{52}$$

In order to understand how to extrapolate these types of models to an expected lifetime of a module it is necessary to know how the companies test the modules. In the next section different setups for testing the lifetime of IGBT modules is described.

Power cycling testing

In order to test the lifetime of IGBT modules different strategies and test setups can be used. The most common method is shown in Figure 60. This setup or one very similar is the typical test setup used by manufactures of IGBT modules.

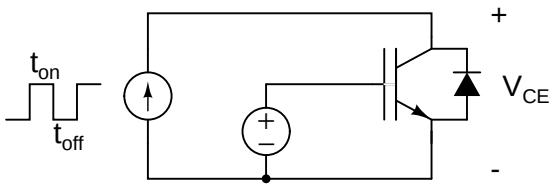


Fig. 60: Typical equivalent diagram of a power cycling test setup.

The current through the IGBT is controlled by the power source while the IGBT is constantly kept on. The conduction losses of the IGBT then generates the heat needed for the power cycling. Only conduction losses are here present and no switching losses contributes to the heating of the bondwire and modules. To achieve a significant temperature increase the use of this type of setup requires a longer on time to heat up or very high current.

Schuler et al. describes 4 different control schemes for testing the modules using the test setup in Figure 60 [12].

1. Constant on and off time
2. Constant Δ temperature of the base plate
3. Constant power dissipation
4. Constant Δ junction temperature

All of the control schemes, except the first, will to some degree compensate for the degradation of the module. However in normal operation of a power converter no compensation based on degradation is normally permitted. Therefore the manufacturers should give the lifetime curves for constant timing in the test. Tabel 16 shows the results from the tests performed by Schuler et. al.

Table 16: Lifetime of IGBT modules depended on control strategy [12].

Test strategy	Cycles before failure
1	32.073
2	47.485
3	69.423
4	97.000

From Table 16 the impact of the different control strategies is clearly seen. The difference between the constant ΔT and the constant timing is a factor of 3. Thus

the tested strategy of the manufacturer is very important when comparing the power cycling capability of IGBT modules.

Another possible method for power cycle testing IGBT is proposed in [13] [14] and [15] which is shown in Figure 61.

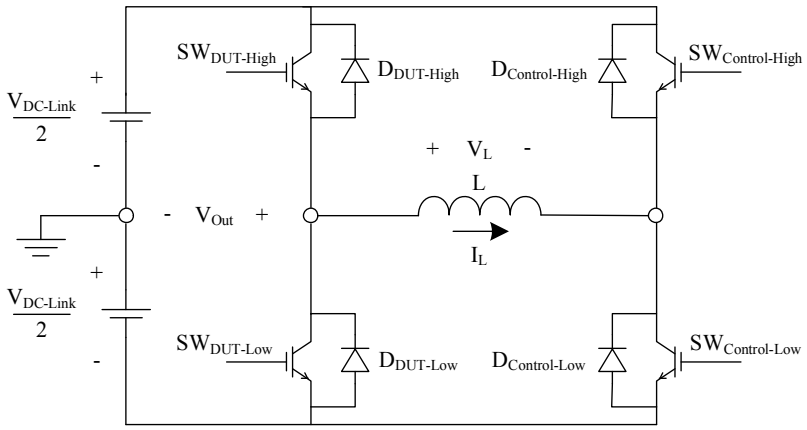


Fig. 61: Power cycling with an H-bridge allowing to test with a real life working point, with both switch and conduction losses. [13]

This setup allows the user to test the DUT device in a real life working point, both current, voltage, phase, etc., while only supplying the losses to the DC-link. This type of setup should give a more accurate picture of how the IGBT will perform in a real life application, though the test still needs to be accelerated in order to test the life time in a reasonable period.

In [16] it was shown that the above H-bridge test method gives result fairly close to the expected for 1700 V 1200 A IGBT4 modules from Infineon regarding the lifetime of the IGBT though longer lifetime of the diode than expected was observed. The test setup and results are explained further in Paper E and Paper F.

8.2 Loss model

In order to calculate the losses of the module, thermal depended loss models for IGBTs and diodes must be developed. These are developed using the data from the datasheet of the module.

The losses of an IGBT can be divided into two parts; conduction losses and switching losses. This will during one switching period cause losses as seen in Figure 62.

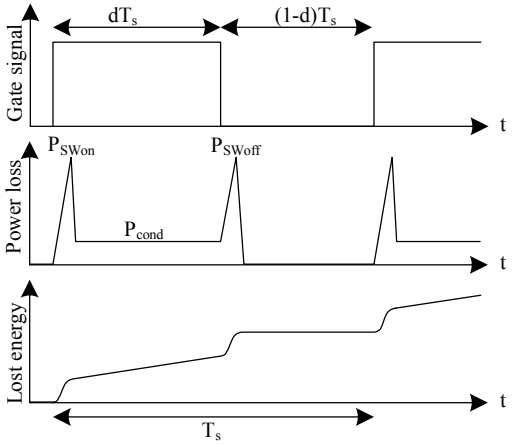


Fig. 62: Losses during one switching period.

The average power losses during one switching period can then be found in the following manner:

$$\langle p_{Loss} \rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} p_{Loss}(t) dt \quad \text{W} \tag{53}$$

In the next sections models for the conduction and switching losses, of the modules in the given application, will be determined based on datasheet values.

Conduction losses

In order to determine the conduction losses the equivalent model depicted in Figure 63 is used. A Schockley diode model is used in order to get a more accurate model at lower currents than a standard linear model which overestimates the losses at low currents.

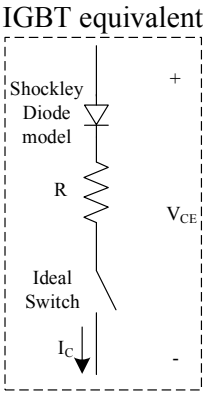


Fig. 63: Model for determining conduction losses in the IGBTs [17, p. 63-68].

The model consists of an ideal switch, a resistor and a Shockley diode model [17, p. 63-68]. However it is not possible to fit a pure Shockley diode model also a resistance is needed in order to get the right slope at higher currents. The equations for V_{CE} can then be written as:

$$V_{CE} = \underbrace{n \cdot V_T \cdot \ln\left(\frac{I_C}{I_S} + 1\right)}_{\text{Shockley Model}} + \underbrace{R \cdot I_C}_{\text{Resistance}} \quad \text{V} \tag{54}$$

Where n is a constant, V_T is the thermal voltage found as $V_T = \frac{kT_j}{q}$ V with Boltzmann's constant k=$1.38 \cdot 10^{-23}$ $\frac{\text{J}}{\text{K}}$ and the magnitude of elementary electron charge q=$1.60 \cdot 10^{-19}$ $\frac{\text{J}}{\text{V}}$ and I_S is the saturation current.

I_S is dependent of the temperature and the junction area. Also the resistance R is temperature dependent, so both R and I_S will be modeled as a function of the temperature.

The parameters are found using the function lsqcurvefit in Matlab, first finding the ideality factor n for each temperature, then rounding it to the nearest integer. Lsqcurvefit is a least square curve fitting script. Hereafter n is fixed, the resistance is then found for each temperature, 25, 125 and 150 °C still using lsqcurvefit. From these three the temperature coefficient α is estimated. In the end the saturation current I_s is found using lsqcurvefit for each temperature with the other parameters fixed. A temperature depended function for I_s is thereafter determined. The model is compared with the datasheet in Figure 64.

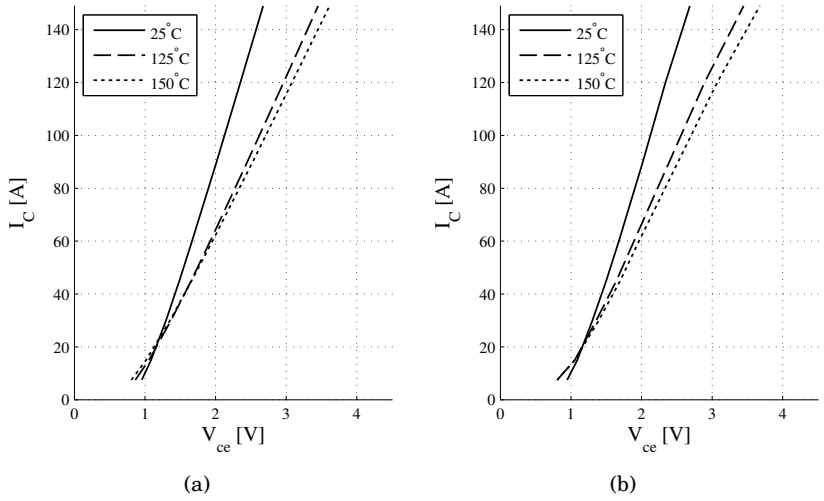


Fig. 64: V_{CE} as a function of the current (a) Simulated (b) Datasheet [18].

The parameters for the model is shown in the Table 17.

Table 17: Parameters for Schokley model for IGBT's

Parameter	Value
R	$(0.0061 \cdot (T_J - 273.15) + 1) \cdot 9.1$ mΩ
n	3
I_S	$3.3 \cdot 10^{-5} \cdot 2^{\frac{T_J - 273.15}{16.8}}$

Where: T_J is the junction temperature in Kelvin

The model is only valid within the given dataset, i.e. from 25-150 °C, as V_{CE} is not known at higher or lower temperatures.

Similarly models of the conduction losses of the IGBT diodes and the rectifier diodes are created. These are shown in Table 18 for the IGBT body diodes and Table 18 for the rectifier diodes.

Table 18: Parameters for Schokley model for IGBT diodes

Parameter	Value
R	$(0.0014 \cdot (T_J - 273.15) + 1) \cdot 5.6\ \mathrm{m\Omega}$
n	5
I_S	$2.2 \cdot 10^{-3} \cdot 2^{\frac{T_J - 273.15}{24.2}}$

The fit between the read datasheet values and the modeled value is shown in Figure 65.

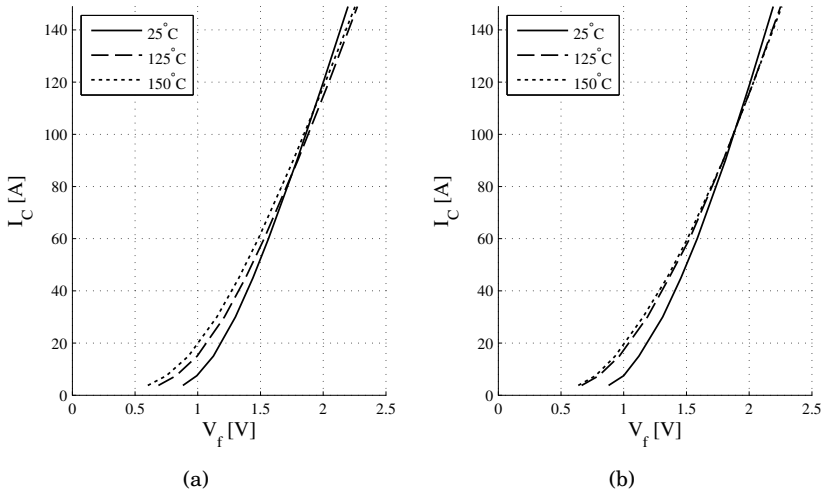


Fig. 65: V_f of the IGBT freewheeling diodes as a function of the current (a) Simulated (b) Datasheet [18].

For the rectifier diodes the forward voltage drop is only known at 25 °C and 150 °C. The fit between the read datasheet values and the modeled value is shown in Figure 66.

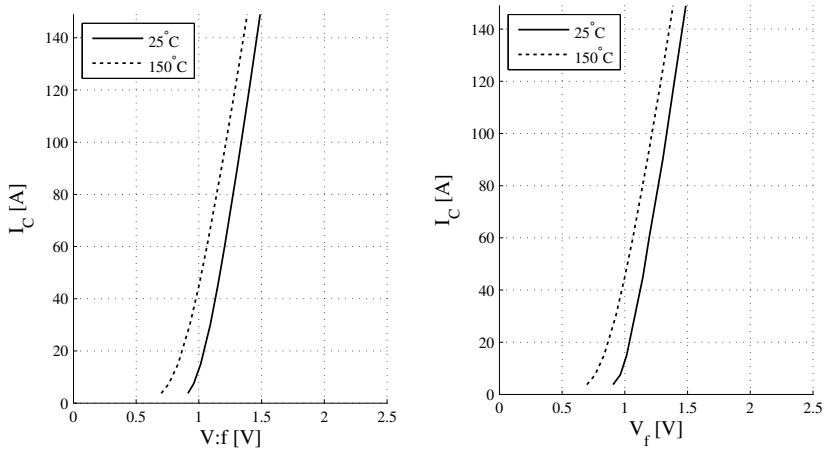


Fig. 66: V_{fr} of the rectifier diodes as a function of the current (a) Simulated (b) Datasheet [18].

The parameters for the rectifier diodes are shown in Table 19.

Table 19: Parameters for Schokley model for rectifier diodes

Parameter	Value
R	$(0.00064 \cdot (T_J - 273.15) + 1) \cdot 2.6\ \mathrm{m\Omega}$
n	5
I_S	$1.89 \cdot 10^{-8} \cdot 2^{\frac{T_J - 273.15}{10.71}}$

Models for the conduction voltage drops of the IGBTs, the freewheeling diodes and the rectifier diodes have been presented. In the next section models for the switching energies will be determined.

Switching losses

Similarly to the conduction losses switching losses is a function of current and temperature. However switching losses are also influenced by other parameters such as the switching voltages, switching frequencies and the gate resistors. Therefore it is necessary to look at the specific converter case in order to determine the switching losses.

The switching losses as a function of gate resistance can be seen in Figure 27. Here it seen that the turn on switching energy is very dependent of the gate resistance, however the turn off losses are almost independent. For the boost IGBTs a low gate resistance of 1.1 Ω as recommended in the datasheet was chosen in order to keep the turn on energy loss low. However for the half-bridges a gate resistance of 10 Ω was chosen, because the half-bridge IGBTs are turned on at zero current and therefore almost no energy is lost in turn on. As the turn off energy however does not increase with the gate resistance the effect of having a 10 Ω resistance is negligible.

The boost rectifier IGBT is switched on and off at full DC-link voltage of 600 V. Where the half-bridge is switched on at half DC-link voltage, 300 V. An linear relationship between switching voltage and switching energy is assumed. This leads to the following model for the switching losses of the IGBTs and diodes:

$$P_{sw} = f_{sw} \cdot \frac{V_{sw}}{V_{ds}} \left(E_{on}(T_j, I) + E_{off}(T_j, I) \right) \quad \text{W} \tag{55}$$

Where P_{sw} is the switching losses, f_{sw} is the switching frequency, V_{sw} is the switching voltage, V_{ds} is the switching voltage given in the datasheet, $E_{on}(T_j, I)$ is the turn on energy as a function junction temperature and current and $E_{off}(T_j, I)$ is the turn off energy as a function junction temperature and current.

Similarly a model model for the switching losses of the IGBT freewheeling diodes can be created:

$$P_{dsw} = f_{sw} \cdot \frac{V_{sw}}{V_{ds}} \left(E_{dio}(T_j, I) \right) \quad \text{W} \tag{56}$$

Where P_{dsw} is the diode switching losses and E_{dio} is the diode switching energy.

Polynomial fit of the on and off energies of the IGBT as a function of current was made. The result is shown i Figure 67

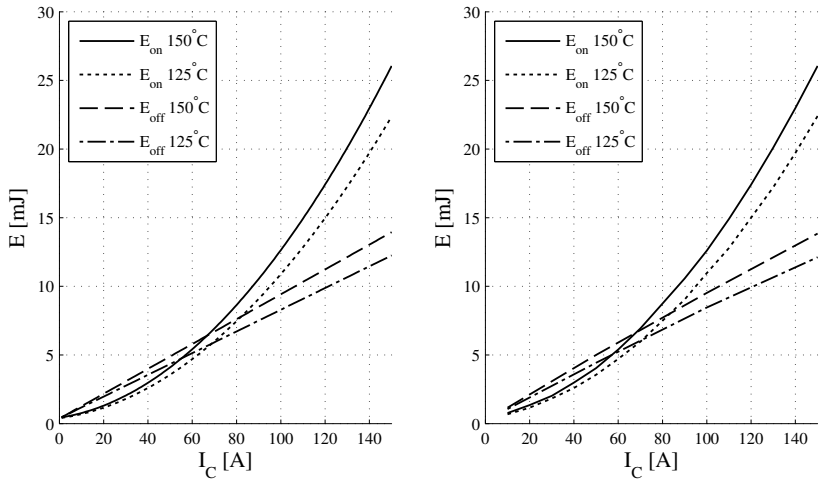


Fig. 67: Switching energy of the IGBT as a function of the current (a) Simulated (b) Datasheet [18].

A fit was made at 125 °C and 150 °C. The polynomials can be seen in Equations 57 to 60. A second order polynomial is fitted for the turn on energy and a first order for the turn off energy. A linear relationship between the switching energy and the temperature is assumed as the switching energy is only known at 125 °C and 150 °C, the principal is shown in Equations 61 and 62.

$$E_{on-125}(I) = 0.0008 \cdot I^2 + 0.0219 \cdot I + 0.39 \quad \text{mJ} \tag{57}$$

$$E_{on-150}(I) = 0.0010 \cdot I^2 + 0.0247 \cdot I + 0.43 \quad \text{mJ} \tag{58}$$

$$E_{off-125}(I) = 0.079 \cdot I + 0.39 \quad \text{mJ} \tag{59}$$

$$E_{off-150}(I) = 0.091 \cdot I + 0.36 \quad \text{mJ} \tag{60}$$

$$E_{on}(T_j, I) = E_{on-125}(I) + \frac{E_{on-150}(I) - E_{on-125}(I)}{25} \cdot (T_j - 125) \quad \text{mJ} \tag{61}$$

$$E_{off}(T_j, I) = E_{off-125}(I) + \frac{E_{off-150}(I) - E_{off-125}(I)}{25} \cdot (T_j - 125) \quad \text{mJ} \tag{62}$$

Similar a third order polynomial was fitted for the switching losses in the diodes. The fit is shown in Figure 68 and the model is shown in Equations 63 to 65.

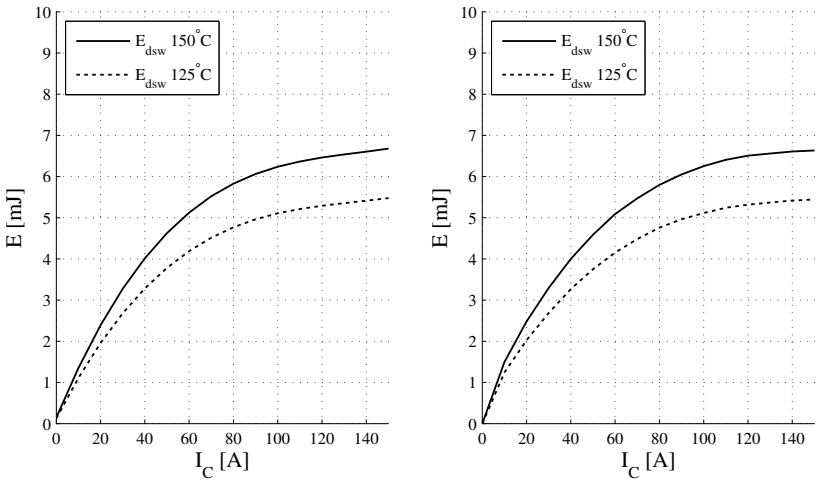


Fig. 68: Switching energy of the IGBT freewheeling diodes as a function of the current (a) Simulated (b) Datasheet [18].

$$E_{dsw-125}(I) = 1.8 \cdot 10^{-6} \cdot I^3 - 0.00074 \cdot I^2 + 0.105 \cdot I + 0.125 \quad \text{mJ} \tag{63}$$

$$E_{dsw-150}(I) = 2.3 \cdot 10^{-6} \cdot I^3 - 0.00091 \cdot I^2 + 0.129 \cdot I + 0.145 \quad \text{mJ} \tag{64}$$

$$E_{dsw}(T_j, I) = E_{dsw-125}(I) + \frac{E_{dsw-150}(I) - E_{dsw-125}(I)}{25} \cdot (T_j - 125) \quad \text{mJ} \tag{65}$$

Circuit model

In order to calculate the losses as described in the previous sections a model for the currents and voltages in the converter is needed. This is divided in to three parts. One for the rectifier, one for the boost converter and on for the DC/DC converter. In the next sections each loss part

Rectifier

In order to calculate the losses in the rectifier diodes only the current is needed. This is assumed because the frequency of the commutation between the diodes is low. The voltage from the rectifier is modeled in Matlab Simulink. The current is

calculated based on the rectified input voltage, see Equation 66

$$i_{rec}(t) = \frac{P_{in}(t)}{v_{rec}(t)} \quad \text{A} \tag{66}$$

Where $i_{rec}(t)$ is the current through the diodes in the rectifier, $v_{rec}(t)$ is the rectified input voltage and $P_{in}(t)$ is the input power to the converter given by the .

The power in the rectifier diodes can then be calculated. This is shown in Equation 67. As can be seen the current multiplied with the forward voltage is divided with three. This is done in order to take into account that each diode is only conducting a third of the time.

$$p_{rec}(t) = \frac{i_{rec}(t) \cdot V_{fr}(i, T_j)}{3} \quad \text{W} \tag{67}$$

Where $p_{rec}(t)$ is the instantaneous power dissipated in one rectifier diode and $V_{fr}(i, T_j)$ is the forward voltage drop of the diode as a function of current and junction temperature.

Boost converter

The losses in the boost converter is calculated by first determining the average current in the boost inductor over a switching period and the duty cycle over a switching period. All the losses are calculated based on the inverter IGBT characteristics as the parameters for the break IGBT and diode is not well known. This could give some inaccuracy and the current could be share unequally in the two parallel IGBTs and diodes. For these calculations this is disregarded but should be studied further if the model should be improved.

The duty cycle is calculated in under CCM conditions in the manner shown in Equation 68.

$$< d_b >_{Ts} = 1 - \frac{v_{rec}(t)}{V_{DC-Link}} \tag{68}$$

Where $< d_b >_{Ts}$ is the duty cycle of the boost rectifier and $V_{DC-Link}$ is the DC-link voltage seen as a constant voltage.

The average current in the inductor is calculated as shown in Equation 66. The conduction losses of the IGBTs are then calculated as described in Equation 69. As can be seen the current is divided with two, taking into account the two parallel IGBTs in the boost rectifier.

$$p_{bci}(t) = \frac{i_{rec}(t) \cdot < d >_{Ts} \cdot V_{CE}(\frac{i_{rec}(t)}{2}, T_j)}{2} \quad W \tag{69}$$

Where $p_{bci}(t)$ is the instantaneous conduction loss of the boost rectifier IGBT and $V_{CE}(\frac{i_{rec}(t)}{2}, T_j$ is the collector emitter voltage drop of the IGBT as a function of the current and junction temperature.

The switching losses of the IGBT is then calculated as shown in Equation 70

$$p_{bswi}(t) = \left(E_{oni}(\frac{i_{rec}(t)}{2}, T_j) + E_{offi}(\frac{i_{rec}(t)}{2}, T_j) \right) \cdot f_{sw} \cdot \frac{V_{DC-Link}}{600} \quad W \tag{70}$$

Where p_{bswi} is the switching losses in the boost rectifier IGBTs, f_sw is the switching frequency and $E_{oni}(\frac{i_{rec}(t)}{2}, T_j)$ and $E_{offi}(\frac{i_{rec}(t)}{2}, T_j)$ is respectably the turn on and turn off energy of the IGBT as a function of the current and the junction temperature.

The conduction losses of the diodes are calculated using Equation 71

$$p_{bcd}(t) = \frac{i_{rec}(t) \cdot (1 - < d >_{Ts}) \cdot V_f(\frac{i_{rec}(t)}{2}, T_j)}{2} \quad W \tag{71}$$

Where $p_{bcd}(t)$ is the conduction losses of the diodes and $V_f(\frac{i_{rec}(t)}{2}, T_j)$ is the forward voltage drop of the diode.

The switching losses of the diodes are calculated as described in Equation 72

$$p_{bswd}(t) = E_{dsw}(\frac{i_{rec}(t)}{2}, T_j) f_{sw} \cdot \frac{V_{DC-Link}}{600} \quad W \tag{72}$$

Where p_{bswd} is the switching losses of the boost rectifier diodes and $E_{dsw}(\frac{i_{rec}(t)}{2}, T_j)$ is the switching energy dissipated in the diode as a function of the current and the junction temperature.

DC/DC converter

The losses in the dual half-bridge DC/DC converter is calculated in a similar fashion. First the duty cycle is determined. Hereafter the average current over a switching period is determined. From these two conduction and switching losses are calculated.

The duty cycle of the dual half-bridge DC/DC converter is calculated assuming a perfect coupling and turns ratio of 1:4. This is shown in Equation 73

$$D_h = \frac{V_{out} \cdot 4}{V_{DC-Link} \cdot 2} \tag{73}$$

Where D_h is the duty cycle of the each IGBT in the dual half-bridge converter and V_{out} is the output voltage of the converter, specified to 60 V.

The average switching current in the IGBT is determined as described in Equation 74

$$< I_{ch} >_{Ts}(t) = \frac{P_{in} \cdot 2}{V_{DC-link} \cdot D_h} \quad \text{A} \tag{74}$$

Where $< I_{ch} >_{Ts}(t)$ is the average swithcing current during a period.

The conduction losses are calculated as shown in Equation 75.

$$p_{hci}(t) = \frac{< I_{ch} >_{Ts}(t) \cdot D_h \cdot V_{CE}(\frac{i_{rec}(t)}{2}, T_j)}{2} \quad W \tag{75}$$

Where $p_{hci}(t)$ is the conduction losses of a single IGBT in the dual half-bridge converter.

The switching losses of the IGBTs only consists of turn off losses as the IGBTs are turned on at zero current, see Equation 76

$$p_{hswi}(t) = \left(E_{offi}(< I_{ch} >_{Ts}(t), T_j)\right) \cdot f_{sw} \cdot \frac{V_{DC-Link}}{2 \cdot 600} \quad W \tag{76}$$

Where $p_{hswi}(t)$ is the switching losses of the half-bridge IGBTs.

8.3 Thermal model

In this section the thermal model for the module and cooling system is described. The model is based on the values of the transient thermal impedance given in

the datasheet. The model is set up as a Foster model as this is the model the parameters in the datasheet are given for. The Foster model is chosen even though a Cauer model is more physical correct. Series coupling of Foster networks is not usually recommended, however as the thermal time constant of the heatsink is large (air cooled heatsink) the error is much smaller than if it had been a water cooled system with small thermal time constants [19]. For the interface between the heatsink and case the values from the datasheet of the module is used. The principle drawing of the thermal system is shown in Figure 69. For simplicity no thermal coupling between the dies inside the module is assumed, and full coupling is assumed within the heatsink.

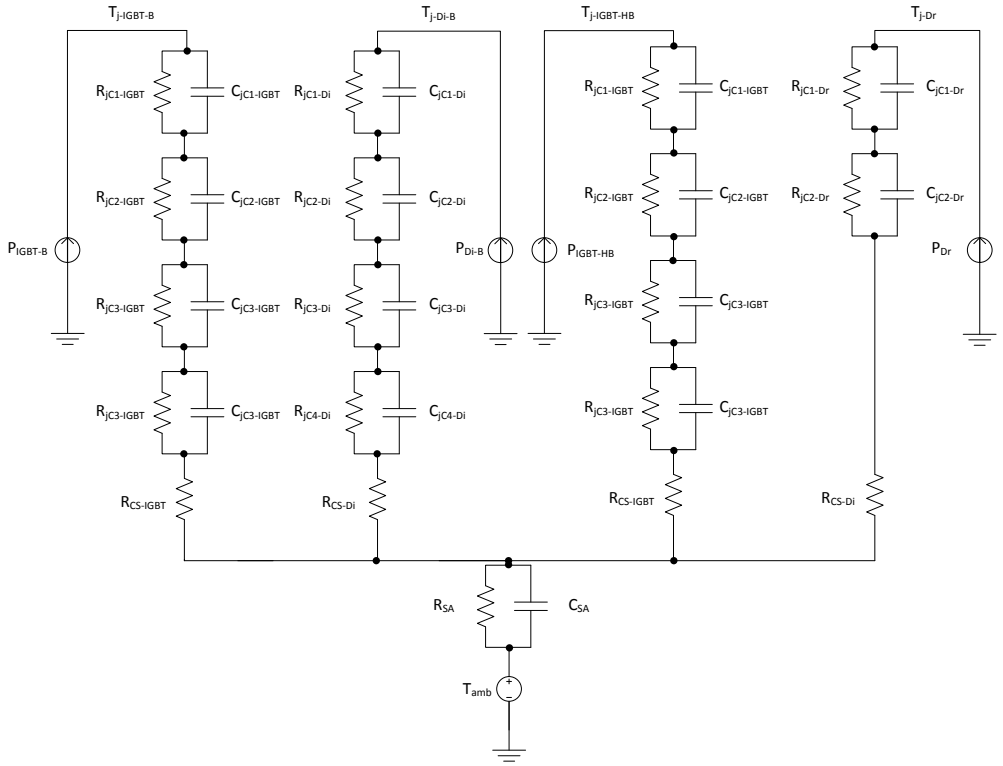


Fig. 69: Thermal model of the power module and the heatsink.

The parameters used for the thermal model is displayed in Table 20.

Table 20: Parameters for the thermal model

Parameter	Value	Parameter	Value
$R_{jC1-IGBT}$	0.0234 K/W	$R_{jC2-IGBT}$	0.1287 K/W
$R_{jC3-IGBT}$	0.1248 K/W	$R_{jC4-IGBT}$	0.1131 K/W
$C_{jC1-IGBT}$	0.4274 J/K	$C_{jC2-IGBT}$	0.1554 J/K
$C_{jC3-IGBT}$	0.4006 J/K	$C_{jC4-IGBT}$	0.8842 J/K
R_{jC1-Di}	0.0372 K/W	R_{jC2-Di}	0.2046 K/W
R_{jC3-Di}	0.1984 K/W	R_{jC4-Di}	0.1798 K/W
C_{jC1-Di}	0.2688 J/K	C_{jC2-Di}	0.0978 J/K
C_{jC3-Di}	0.2520 J/K	C_{jC4-Di}	0.5562 J/K
R_{jC1-Dr}	0.65 K/W	R_{jC2-Dr}	0.215 K/W
C_{jC1-Dr}	0	C_{jC2-Dr}	0
$R_{CS-IGBT}$	0.13 K/W	R_{CS-Di}	0.205 K/W
R_{SA}	0.2 K/W	C_{SA}	100 J/K

8.4 Mission profile

In order to determine a mission profile the specifications are consulted, the specification can be seen in Section 8. It can be seen that the steepest rise time is 0.5 s from zero load to maximum load. It has been decided to have a period of 0.2 s at maximum load and at minimum load between each transition. This mission profile is illustrated in Figure 70.

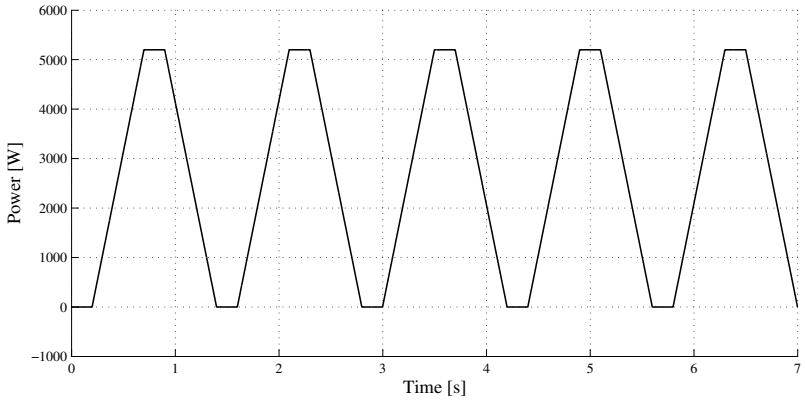


Fig. 70: Mission profile proposed for the reliability calculations.

8.5 Simulation results

In this section the results of the model is shown varying different parameters one at a time. This is done in order to determine the influence of these parameters on losses and ultimately lifetime of the module. To determine the lifetime the Coffin-Manson equation shown in Equation 48 is used. The parameters used in the model was found and verified in an earlier project [14]. The parameters is: A= 3315000 $K^{-\alpha}$, E_a = $9.89 \cdot 10^{-20}$ J, α= -5.039, $\kappa_B = 1.38066 \cdot 10^{23}$ $JK^{-}1$. As can be seen the constant A has been greatly increased compared with the LESIT results, this is done to take into account the improvement of the module since the LESIT results.

The thermal behavior of each semiconductor element is shown in Figure 71. The parameters for the simulations is 208 V line to line input voltage, an ambient temperature of 40 °C, the DC-link voltage of 600 V and a 20 kHz switching frequency.

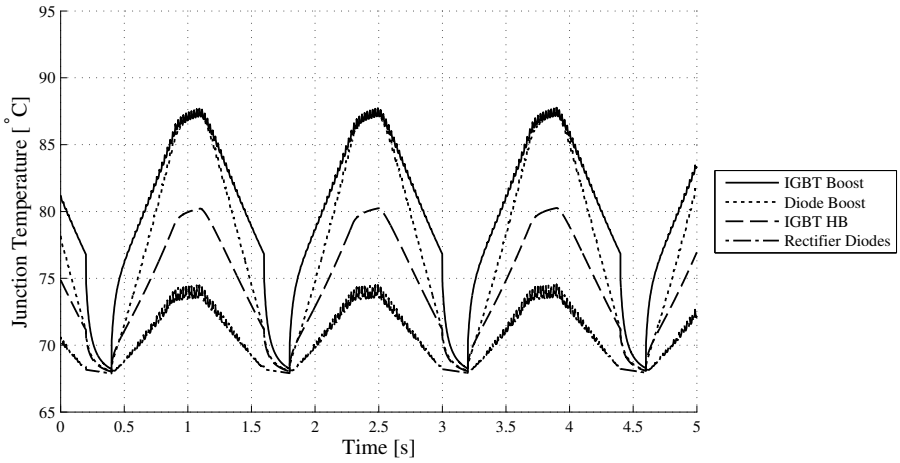


Fig. 71: Thermal behavior of the semiconductors in the PIM with the following parameters fixed: 208 V line to line, ambient temperature 40 °C, DC-link=600 V and 20 kHz switching frequency.

In Figure 72 the lifetime of the different components in the module is shown as a function of the switching frequency. It is clearly seen that the lifetime is decreasing, as a consequence of the higher switching losses.

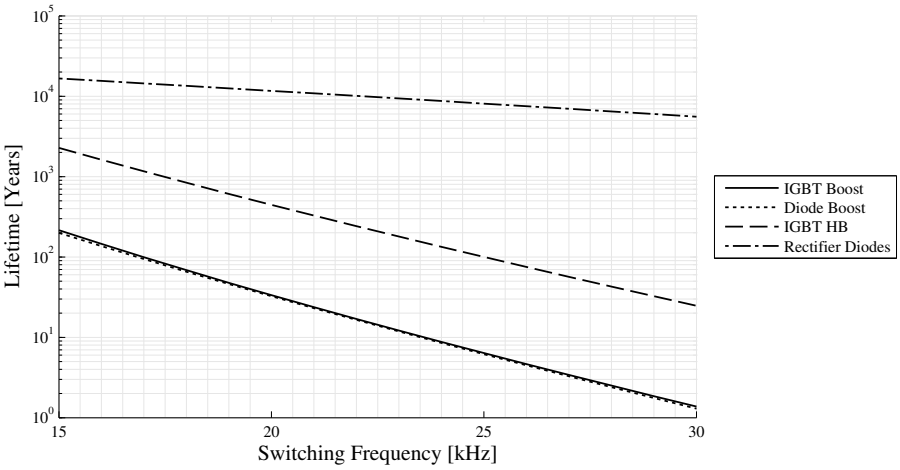


Fig. 72: Lifetime as a function of switching frequency with the following parameters fixed: 208 V line to line, ambient temperature 40 °C, DC-link=600 V.

Figure 73 the lifetime as a function of a each component is shown as a function

of DC-link voltage. It is clearly seen that the dual half bridge IGBTs are almost not affected by the increase in DC-link voltage however the boost converter components, IGBTs and diodes show a significant decrease in lifetime at higher DC-link voltage. This is because the switching losses in the boost converter is proportional to the DC-link voltage but the conduction losses does not decrease as the output power and thus the current in the inductor is still the same.

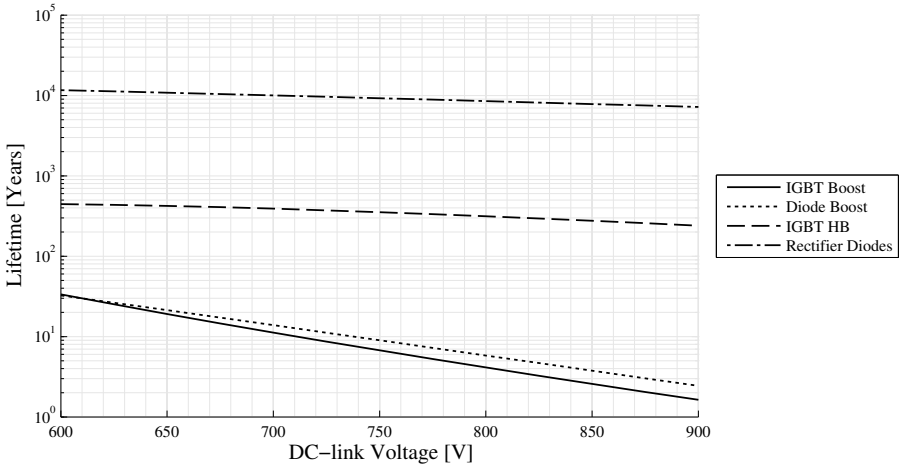


Fig. 73: Lifetime as a function of DC-link voltage with the following parameters fixed: 208 V line to line, ambient temperature 40 °C, switching frequency 20 kHz.

Figure 74 shows the lifetime of the components of the module as a function of ambient temperature. Here it is very clear that the lifetime is greatly decreasing with the ambient temperature. This is because the medium temperature of the components are increased.

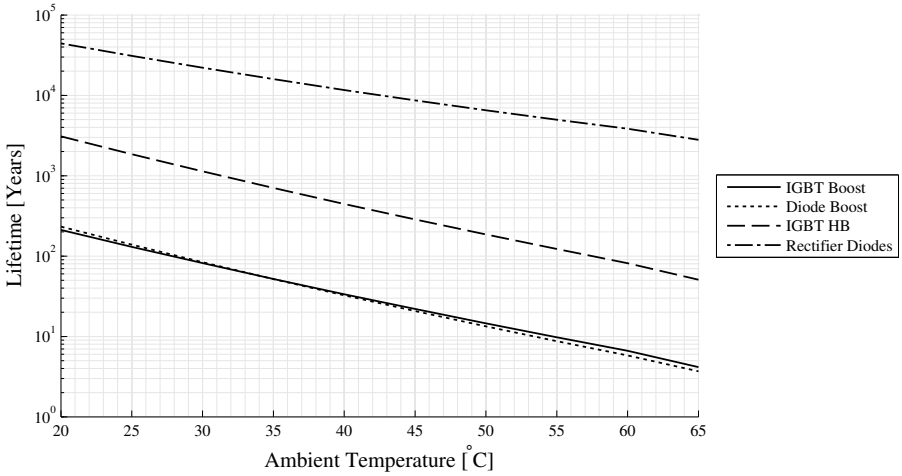


Fig. 74: Lifetime as a function of ambient temperature with the following parameters fixed: 208 V line to line, DC-link=600 V, switching frequency 20 kHz.

In Figure 75 the lifetime is shown as a function of the line to line input voltage. Again the IGBT's in the dual half-bridge DC/DC converter is more or less unaffected. However it is seen that the losses of the boost converter and rectifier diodes are decreasing due to lower current in the DC choke.

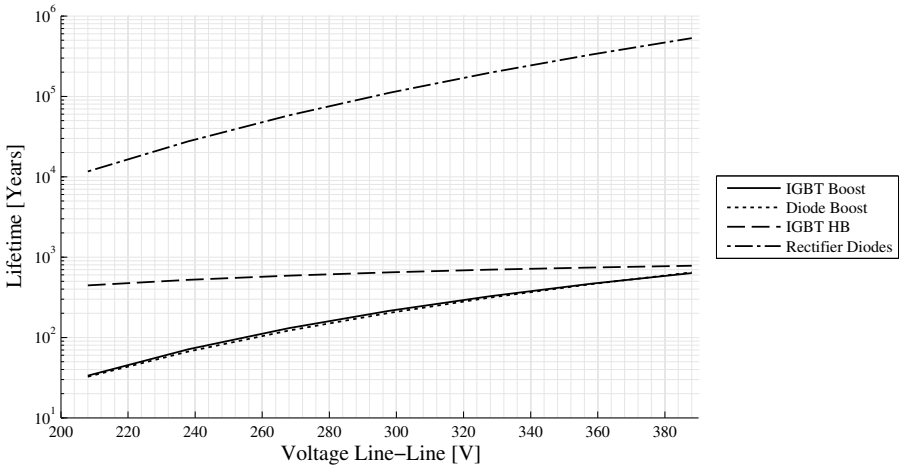


Fig. 75: Lifetime as a function of line to line input voltage with the following parameters fixed: Ambient temperature 40 °C , DC-link=600 V, switching frequency 20 kHz.

What is also clear from Figure 71 and Figure 72 is that the boost devices see the highest stress and thus have the shortest expected lifetime. This is because of the large boost needed for the wide input range. However it can also be seen that the half-bridge IGBTs are not very stressed with an expected lifetime a factor of 10 longer than that of the boost components, so it might be possible to move some of the losses from the boost devices to the half-bridge devices and thereby increase the overall lifetime expectancy and thus the reliability of the SMPS. The large dependency of the input voltage is shown in Figure 75. It can be seen that with a smaller boost from the boost converter the lifetime of the boost devices increase significantly, while the lifetime of the half-bridge IGBTs almost has the same expected lifetime for all input voltages.

A way to decrease the stress of the devices in the boost converter is to lower the DC-link voltage demand. This could be achieved by decreasing the turn's ratio of the transformer from for instance 4:1 to 3:1. This will make it possible to run the converter at lower DC-link voltages at the lower input voltages. However an adaptable DC-link voltage will then be needed in order to cope with the demand for also 400 V input if any margin to boost in should be left.

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Part IV

Conclusion and future work

Conclusions and Future work

9 Conclusion

From this thesis it can be concluded that magnet power supplies plays a large role in today's particle accelerators. The demands for these magnet power supplies are very high in terms of current accuracy and stability both in the long and short term. The power supplies require galvanic isolation. In this thesis and overview of different topologies interfacing with the grid and giving the galvanic isolation for such a power supply has been shown and discussed. Both single-stage and two-stage topologies are shown. It is concluded that for the three phase converter in the higher power range (above 2 kW) the reported efficiency of the single stage converters is lower than what can be obtained in a two stage solution.

For the single-stage one phase converter the reported efficiencies are high, and thus these seems to be viable for the lower power magnet power supplies. The single stage solution could be preferable because of lower component count or smaller passive components.

A 5 kW two-stage galvanic isolated input converter was constructed. This was done using a single power module on the primary site of the transformer, consisting of a boost rectifier and a dual half-bridge isolated DC/DC converter. It was shown that it is possible to create a power supply using a single module and that this approach could lead to improved layout and smaller converter size.

The boost rectifier exhibited high efficiency and it was shown that it is feasible to create a the power supply with universal input voltage. This enables the power supply to be utilized in an international market.

The isolated DC/DC converter was constructed using a dual half-bridge topology. The efficiency of DC/DC was not as high as desired and there were problems with reflected voltage from primary winding to primary winding. A method of mitigating the current spikes caused by the reflected voltages was shown.

A high efficiency isolated DC/DC converter was also developed using SiC JFETs as switching elements. The efficiency was compared with the converter based on Silicon IGBTs and a 5 % increase in efficiency was demonstrated. A cost comparison between the two converters was also performed. This comparison showed that the payback time at full load is around 772 days based on 2011 industrial electricity prices.

The reliability of power converters is a relevant research topic which receives a lot of attention in these years. It is found that one of the components most prone to failure are the semiconductors/power modules. Typical reasons for failures in power modules are found. From this it is concluded that power cycling and thermal cycling are some of main reasons for wear down in power modules, especially with varying load.

Different lifetime models to describe the wear down of the power modules are shown. Based on these lifetime models, a loss model and a thermal model is created for the single power module converter. A lifetime model and a mission profile is chosen. Combining these four models together with an environmental description makes it possible to calculate an expected lifetime of the power module. It is then shown that by varying parameters such as switching frequency, DC-Link voltage, ambient temperature and input voltage from the grid the expected lifetime of the module is influenced.

From the lifetime models a method for improving the expected power cycle capability of the power module in the single power module converter is described.

10 Scientific contributions from the Author's point of view

1. State of the art examination of isolated grid connected single stage and two stage converters.
   Several topologies describing the state of the art of isolated single stage converters have been shown. Also several two stage converter topologies has been examined.
2. An innovative use of power integrated module to create an isolated DC/DC

converter.
The design and demonstration of a single power integrated module has been shown. This enables the design of more compact converter with better PCB layout.

3. Design of SiC galvanic isolated DC/DC converter and comparison with a Si based converter.
An isolated DC/DC converter based on SiC JFETs has been demonstrated. It has been shown that there is a large increase in efficiency, however at the moment the cost difference between and SiC and Si based converter is large.

4. Lifetime models for power modules.
Several lifetime models for power modules are collected and the history of these models is described.

5. A method of improving the reliability of a power supply.
A method of predicting the lifetime for the converter based on the PIM has been shown. This method enables the user to improve the lifetime of the power module in the converter.

11 Future research work

In this section topics for future research work is proposed.

- Experimental validation of thermal models.
The lifetime model designed depends heavily on the thermal model and the loss model. In order to validate the thermal model experimental work to determine the junction temperature is needed. This could be achieved either through an online V_{CE} measurement, which is heavily depended on junction temperature, or with an open module and thermal imaging. The latter is difficult due to the lack of gel in the open module.

- Experimental validation of lifetime models.
The chosen lifetime model is based on data from the module manufacturer. In order to validate the module one of the two methods proposed in Section 8.1 could be used.

- Development of cheaper gate drive for SiC JFETs
If a converter should be developed based on SiC JFETs that is market ready a new and cheaper gate drive needs to be developed as the stock gatedrive price is very high. Another options could be to use SiC MOSFETs which need less complicated gate drives.