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Harmonics Mitigation of Dead Time Effects in PWM Converters Using a Repetitive Controller

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Abstract—In order to prevent the power switching devices (e.g., the Insulated-Gate-Bipolar-Transistor, IGBT) from shoot-through in voltage source converter during a switching period, a dead time is added either in the hardware drivers of the IGBTs or implemented in the software Pulse-Width Modulation (PWM) scheme. Both methods will lead to a degradation of the injected current power quality. Thus, the harmonics induced by the dead time have to be compensated in order to achieve a satisfactory current as required by the standards. In this paper, a repetitive controller has been introduced to eliminate the dead-time effect in grid-connected PWM converters. The repetitive controller has been plugged into a proportional resonant based fundamental controller. Compared with the traditional dead-time compensation solutions, the repetitive controller can effectively compensate the dead-time harmonics as well as other low-order distortions, and also it is a simple method without hardware modifications. Experimental results are demonstrating the advantages of the proposed dead-time effect mitigation method compared to the resonant based harmonic compensator.

I. INTRODUCTION

Power electronic converters have brought an increasing power quality challenge to the grid-connected renewable energy systems like PhotoVoltaic (PV) and wind turbine systems [1], [2], due to a) the intermittent nature of renewable energies [3] and b) Pulse-Width Modulation (PWM) control of the power converters [3], [4]. In order to alleviate the harmonic injections from the grid-connected PWM converters, many advanced current controllers have been developed, like the Proportional Resonant (PR) controller [5]–[8]. With those controllers, the current quality can be improved to some extend in terms of a lower Total Harmonic Distortion (THD). Using higher-order passive filters (e.g., *LCL* filter) [9] is an alternative, contributing to a further enhancement of the power quality, yet leading to more power losses, increased complexity, and higher cost [10]. Increasing the switching frequency will result in a possibility to use smaller output filters and thus lower the cost, but the non-linearity like the dead time effects will be magnified and thus the current quality will be poorer [11].

Nevertheless, in practice, the dead time has to be implemented in the PWM drivers to prevent the inverter from shoot-through during a switching interval [12]–[21]. However, it also introduces potentially harmonic problems in the PWM

converters [13]–[15]. For example, it can contribute to a decrease of the fundamental component of the converter output, and also it will generate low order harmonics in the output PWM voltage of the converter [16]. Both issues can lead to distortions of the injected current [4] as well as additional losses, and this situation may become even worse with an increase of the switching frequency as mentioned above [18]. In addition, harmonics in the injected current can be magnified in the case that the grid voltage is distorted, since the current control is normally achieved in a closed-loop system without feed-forward. Thus, the dead time has to be compensated in such applications and harmonic compensators incorporated in the current controller are also preferred.

Most dead time compensation methods are based on an average value theory [12], [15], [16], [18]. In those techniques, the lost voltage because of the dead time is averaged over an entire period, and the resultant value is correspondingly added to the inverter voltage reference to compensate for the dead time effect. However, those methods rely on the detection of the current polarity, leading to an increase of the overall complexity and also a decrease of noise immunity at zero-crossing points of the current. Moreover, such methods can not correctly estimate the lost voltage around zero current points as discussed in [18]. Thus, other dead time compensation solutions have been reported in the literature [16], [18], [22]–[24]. For instance, in [16], a compensation method using the controller integrator output has been introduced, and in [18], an adaptive dead time compensator has been developed, which calculates the feed-forward compensation duty cycle. In addition, since the dead time mainly introduces low order harmonics [16], it is possible to mitigate these harmonics simply by using multiple ReSonant Controllers (RSCs). This technique can effectively compensate the low order harmonics, but may also trigger the system resonance when higher order harmonics (e.g. 11th- and/or 13th-order harmonics) are compensated in order to fully mitigate the dead time effect. In contrast, a Repetitive Controller (RC) based on the internal model principle [25] can suppress all the harmonics (including the harmonics induced by the dead time) without the concern of resonance if it is designed properly, which thus might be a promising solution for the harmonic compensation.
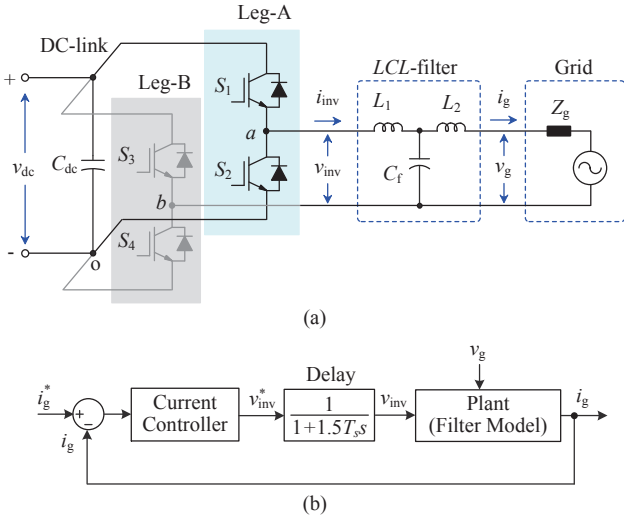
Fig. 1. A single-phase grid-connected PWM inverter system with an *LCL* filter: (a) schematics of the hardware and (b) the closed-loop current control system, where T_s is the sampling period.

Fig. 2. Output voltages of Leg-A shown in Fig. 1 considering the dead time effect in one switching period.

Therefore, this paper presents harmonics mitigation method for the dead time effects based on an RC in § III after a brief introduction of the control of single-phase grid-connected inverters. The RC based solution for the dead time compensation does not require additional hardware modifications as well as complicated mathematical derivations. When it is implemented in a digital controller, the RC is plugged in parallel with a PR fundamental-frequency controller as the harmonic compensator. In order to verify the effectiveness of the RC based dead time harmonic mitigation, experiments have been performed on a 2-kW single-phase grid-connected inverter system, and the testing results are provided in § IV. In addition, comparisons between the RC based mitigation method and the RSC based dead time compensation solution in the case of grid voltage background distortions are also carried out before the conclusion.

II. CONTROL OF SINGLE-PHASE INVERTERS

Fig. 1(a) shows a single-phase grid-connected PWM inverter system with an *LCL* filter, which is a typical configuration for single-phase residential PV systems of lower power ratings (e.g., 1 kWp $\sim$ 3 kWp). For such a grid-connected PWM converter, it is commonly required to operate at unity power factor or to maintain a minimum power factor of 0.85 [3], [4], [26], [27]. Consequently, in respect to the control of the grid-connected PWM converters, it consists of two-cascaded loops – the outer voltage/power control loop for a reference current generation and the inner current control loop taking the responsibility to shape the injected grid current (i.e., the power quality issue). In the following, only the current controller is considered, as it is shown in Fig. 1(b).

Moreover, the grid current i_g has to be synchronized with the grid voltage v_g by means of a Phase Locked Loop (PLL) system [26]. In terms of controlling the AC grid current, the
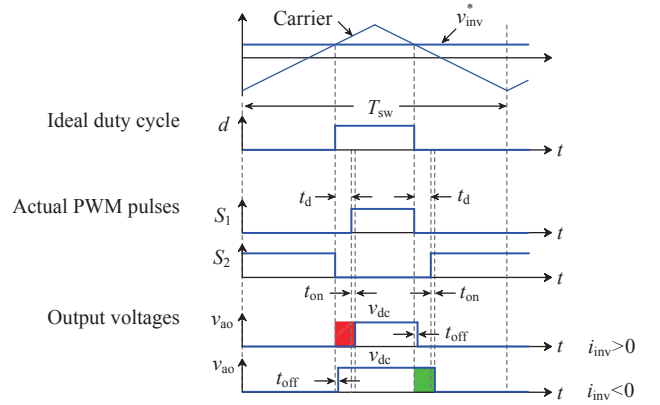
PLL system also enables the use of a Proportional Integrator (PI) controller in the dq−synchronous rotating reference frame [5], [7], [26]. However, it requires at least two reference frame transformations (i.e., $dq \rightarrow \alpha\beta$ and/or $\alpha\beta \rightarrow dq$), which leads to an increase of complexity and controller design difficulties. An alternative is to implement the current control in the $\alpha\beta$−stationary reference frame, where a PR controller or a deadbeat controller is able to achieve a lower tracking error [5], [8], [26]. It is clear that the grid current i_g is the main control variable in order to ensure an appropriate power injection with a satisfactory power quality, whilst it is also the "victim" of the dead-time. Therefore, harmonic compensators can be implemented in parallel with the fundamental current controller to mitigate the distortions induced by the dead-time and also the background distortions, which will be illustrated in details in the following.

III. REPETITIVE CONTROL BASED DEAD-TIME HARMONICS COMPENSATION

A. Dead Time Effect on Current Distortions

The effect of the dead time t_d on the inverter output voltages (i.e., v_{ao}, v_{bo}, and $v_{inv} = v_{ao} - v_{bo}$) is demonstrated in Fig. 2, where it also shows the power switching device (IGBT) turn-on (t_{on}) and turn-off (t_{off}) delay time. It can be observed in Fig. 2 that the inverter output PWM voltage v_{ao} is dependent on the polarity of the phase current (e.g., i_{inv}) in each switching interval (T_{sw}). Specifically, when the phase current is positive ($i_{inv} > 0$), the inverter output voltage v_{ao} is reduced (red zone in Fig. 2), and when the phase current is negative ($i_{inv} < 0$), the inverter output voltage v_{ao} is increased (green zone in Fig. 2), in contrast with the ideal case where no dead time is inserted.

According to Fig. 2, in one switching period, the distorted voltage Δv (i.e., the red and green zones) can be averaged as,

$$\Delta v = \begin{cases} \frac{-t_d - t_{on} + t_{off}}{T_{sw}} v_{dc}, & i_{inv} > 0 \\ \frac{t_d + t_{on} - t_{off}}{T_{sw}} v_{dc}, & i_{inv} < 0 \end{cases} \tag{1}$$

and assuming $t_{on} = t_{off}$ yields,

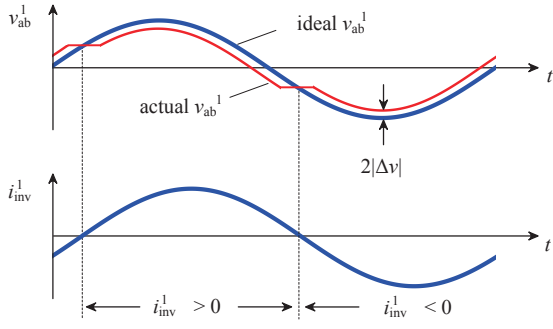$$|\Delta v| \approx \frac{t_d}{T_{sw}} v_{dc} \tag{2}$$

Fig. 3. Dead time effect on the fundamental-frequency inverter output voltage v_{ab}^1 in the case of a pure sinusoidal output current i_{inv}^1 [11].
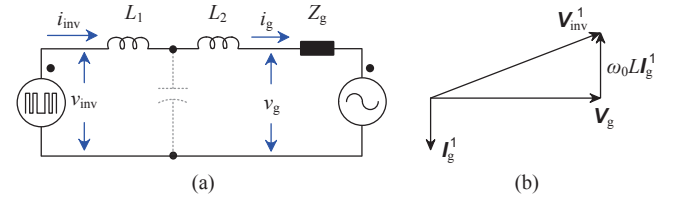

Fig. 4. Simplified single-phase inverter system: (a) *LCL* filter model and (b) fundamental-frequency phasor diagram in the unity power factor operation, where $L = L_1 + L_2$.

where T_{sw} is the switching period and v_{dc} is the instantaneous DC-link voltage. It can be seen in Eq. (2) that both a decrease of the dead time and an increase of the switching period (i.e., decreasing the switching frequency) will contribute to less voltage distortions. However, a PWM converter with a lower switching frequency requires a large filter to mitigate the high-frequency harmonics, and with a smaller dead time, the converter legs may have a risk of short-circuiting.

Similar analysis can be applied to Leg-B in order to obtain the dead time effect on the inverter output voltage v_{inv}. When considering the leakage currents [2], a bipolar modulation scheme is adopted, in which two pairs of power devices (S_1-S_4 and S_2-S_3) of Leg-A and Leg-B are switched synchronously in a diagonal way, and consequently $v_{bo} = -v_{ao}$. Therefore, the inverter output voltage $v_{inv} = v_{ab}$ can be obtained as,

$$v_{inv} = v_{ao} - v_{bo} \approx \begin{cases} v_{ab}^1 - 2|\Delta v|, & i_{inv} > 0 \\ v_{ab}^1 + 2|\Delta v|, & i_{inv} < 0 \end{cases} \quad (3)$$
$$\approx v_{ab}^1 - 2 \cdot \text{sgn}(i_{inv}) \cdot |\Delta v|$$

in which v_{ab}^1 is the ideal inverter output voltage without the dead time t_d.

It can be observed in Eq. (3) that, due to the dead time voltage distortion Δv, the inverter output PWM voltage v_{inv} will be degraded, as shown in Fig. 3. Consequently, the distortions of the inverter output PWM voltage v_{inv} will propagate to the inverter output current i_{inv}, and thus the injected grid current i_g in the case of a closed-loop control [4]. This can be further illustrated with a simplified system model shown in Fig. 4. In accordance to Fig. 4(a), the inverter output voltage v_{inv} can be given as,

$$v_{inv} = v_g + L\frac{di_{inv}}{dt} = v_g + L\frac{di_g}{dt} \quad (4)$$

and thus the grid current i_g can be expressed as,

$$i_g = \frac{1}{L}\int(v_{inv} - v_g)dt$$
$$= \underbrace{\frac{1}{L}\int(v_{inv}^1 - v_g)dt}_{i_g^1: \text{ fundamental}} + \underbrace{\frac{1}{L}\int v_{inv}^h dt}_{i_g^h: \text{ harmonics}} \quad (5)$$

with $L = L_1 + L_2$ being the *LCL* filter total inductance, v_{inv}^1 and v_{inv}^h being the fundamental and the harmonics of the inverter output voltage, respectively, where the grid voltage v_g is almost harmonic-free. Then, the fundamental-frequency phasor diagram in the case of the unity power factor operation can be obtained as shown in Fig. 4(b), where ω_0 is the grid fundamental angular frequency.

It can be seen from Eqs. (3) and (5) that the harmonics of the inverter output voltage v_{inv} will affect the injected grid current i_g. Assuming $v_{ab}^1 = v_{inv}^1$, it yields,

$$i_g^h = \frac{1}{L}\int\{-2 \cdot \text{sgn}(i_{inv}) \cdot |\Delta v|\}dt \quad (6)$$

which implies that the grid current distortions induced by the dead time depend on the duration of this "blanking" period and the polarity of the inverter output current as explained in the following.

1) *Dead Time Duration Effect*

It is clear that a large dead time will contribute to more voltage gains or losses according to Fig. 2, Fig. 3, and Eq. (3), thus leading to more distortions, since a couple of pulses are "covered" by the dead time (i.e., missing PWM pulses). As a consequence, the inverter will be operated in a square-wave modulated mode, where one pair of the power switching devices will always be in OFF- or ON-state during such a short period. It will in return increase the magnitude of the fundamental inverter output voltage v_{inv}^1 [11], and therefore the magnitude of the fundamental grid current i_g^1 will also increase according to Fig. 4(b). As a result, the injected grid current will be deteriorated, as it is shown in Fig. 5. In order to avoid this degradation, the maximum dead time can be approximated as,

$$t_d^m \approx \frac{1}{2f_{sw}}\left(1 - \frac{V_{gm} + \omega_0 L I_{gm}}{V_{dc}}\right) \quad (7)$$

in which V_{gm}, I_{gm} are the grid voltage amplitude and the grid current amplitude, respectively, V_{dc} is the DC-link voltage, $f_{sw} = 1/T_{sw}$ is the switching frequency, and ω_0, L have been defined previously.

However, it is difficult to mitigate these distortions in a closed-loop current controller even with harmonic compensators due to its high non-linearity. Instead, according to Eq. (7), an increase of the DC-link voltage V_{dc} will reduce such harmonics, since a larger magnitude of the fundamental inverter output voltage is possible to tolerate the dead time effect in this case.
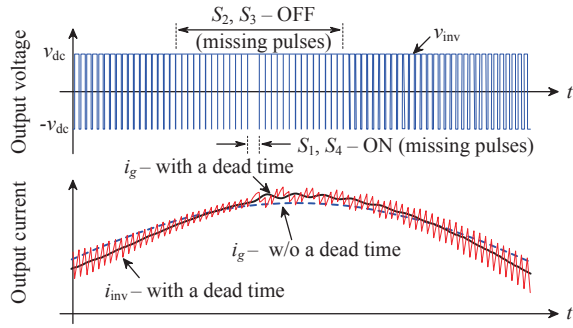
Fig. 5. Effect of a large dead time on the closed-loop controlled grid current with a fixed DC-link voltage ($V_{dc} = 400$ V).
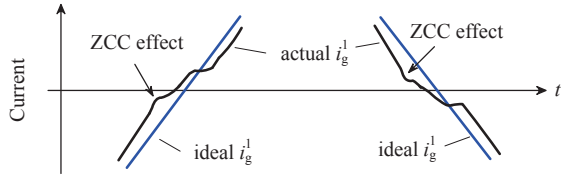

Fig. 6. Effect of zero-crossing points (ZCC: zero-current-clamping) on the fundamental injected grid current.

2) *Polarity Effect (Zero-Crossing)*

Eq. (3), Eq. (6), and Fig. 3, demonstrate that the degradation of the inverter output voltage and thus the distortions of the grid current are dependent on the inverter output current polarity. In general, when the inverter output voltage and the inverter output current have the same polarity, the inverter voltage magnitude will be reduced; otherwise, the dead time will give a magnitude increase of the inverter output voltage, as illustrated in Fig. 3. This implies that the transition from voltage gains to losses or vice versa occurs when either the polarity of the inverter output current or the polarity of the inverter output voltage changes. It happens especially in grid-connected applications in order to achieve the unity power factor operation, as shown in Fig. 4(b).

Moreover, as it is shown in Fig. 5, the output inverter current contains high switching frequency ripples, and thus multiple polarity changes will occur around current zero-crossing points. This will also affect the inverter output current [18], [22]. In the case of a grid-connected PWM inverter operating at unity power factor as shown in Fig. 4, the inverter output current (and thus the grid current) should be lagging behind the inverter output voltage. As a consequence, before the inverter output current polarity changes from negative to positive (or vice versa), there will be a polarity inverse for the inverter output voltage, which will contribute to Zero-Current-Clamping (ZCC). Therefore, the injected grid current will approach to zero in both cases, as it is exemplified in Fig. 6. A detailed analysis of the ZCC impact on the current distortions is also directed in [18], [22] and [28].
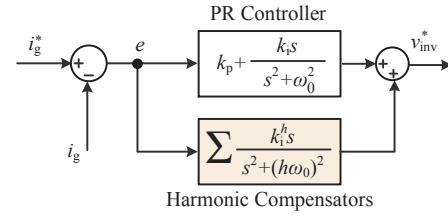

Fig. 7. Current controller for a single-phase system with multiple resonant controllers (RSCs) based dead time harmonic compensator.

The above analysis reveals that the dead time effect is of high non-linearity, which thus results in much difficulty to compensate the distortions. However, the harmonics induced by the dead time can still be expanded into Fourier series, whose frequencies are integer-times of the fundamental grid frequency (even- and odd-order harmonics), mainly consisting of low-order harmonics [11], [16]. It thus enables the use of harmonic compensators to achieve a satisfactory THD of the injected grid current.

B. Resonant Control based Harmonic Compensation

In order to ensure a good power quality, parallel RSCs can be used as the harmonic compensators [4], [7]. For simplicity, a PR controller has been used as the fundamental current controller. In that case, the entire current control system with a RSC based harmonic compensator is shown in Fig. 7, and thus the open-loop transfer function can be obtained as,

$$G_{op}(s) = \frac{v_{inv}^*(s)}{e(s)} = \underbrace{k_p + \frac{k_i s}{s^2 + \omega_0^2}}_{G_{PR}(s)} + \underbrace{\sum_h \frac{k_i^h s}{s^2 + (h\omega_0)^2}}_{G_{RSC}(s)} \quad (8)$$

where k_p and k_i are the control gains for the PR controller $G_{PR}(s)$, k_i^h is the control gain for an individual RSC harmonic compensator $G_{RSC}(s)$ with h being the harmonic order, and ω_0 is defined previously.

As the harmonics induced by the dead time are mainly low-order harmonics, the RSC based harmonic compensation can effectively compensate those harmonics according to Eq. (8). It is also demonstrated by the Bode diagram shown in Fig. 8, which illustrates that the RSC gain will approach to infinity at its resonant frequency. Hence, paralleling multiple RSCs is an attractive alternative to compensate any harmonic of interest with much simplicity and also flexibility of parameter tuning. However, it may trigger the system resonance (e.g., the filter resonance) when the harmonics (e.g., the 11th harmonic) induced by the dead time are compensated, and thereby challenging the overall system stability. In addition, multiple parallel connections also increase the computational burden [8] when implemented in a digital signal processor.

C. Repetitive Control based Harmonic Compensation

Due to its limitation of triggering resonances, the RSC harmonic compensator is normally used to compensate selected low-order odd harmonics (e.g., the 3rd-, the 5th-, and the 7th-order harmonics), since these are the main contributors to the
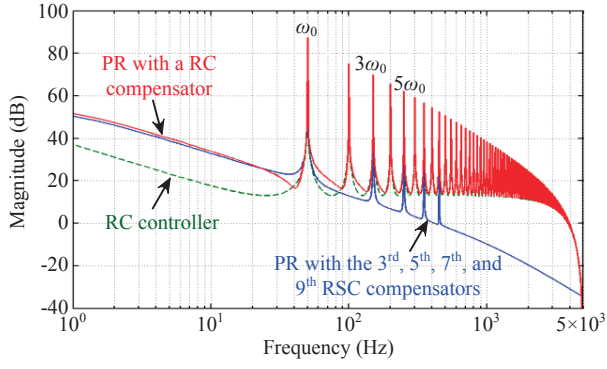
Fig. 8. Magnitude response of the open-loop current controllers: PR - proportional resonant, RSC - resonant controller, and RC - repetitive controller, where the sampling frequency f_s = 10 kHz.

Fig. 9. Current controller for a single-phase system with a repetitive control (RC) based dead time harmonic compensator.

current distortions. However, the dead time mainly induces low-order distortions [11], [16] that may be up to a higher order and also may contain even-order harmonics. Therefore, a good THD of the injected current is far reached only by compensating these low-order odd harmonics based on the RSC compensators.

Alternatively, according to the internal model principle [8], [25], zero-error tracking of any periodic signal (e.g., the expanded dead time harmonics) in steady-state can be achieved, as long as a generator of the reference is included in a stable closed-loop control. The RC controller is a typical representative of the internal model principle based controller. Thus, this inspires the use of the RC as a harmonic compensator to mitigate the dead time distortions [4], [22]. However, it should be noted that, although the RC can suppress all harmonics below the Nyquist frequency theoretically, its response is slow and the stability might be challenged as discussed in [18] and [22], where the RC harmonic compensator is implemented in the angle domain. By doing so, the complexity is increased. However, in this paper, the RC controller is reconstructed by introducing an appropriate phase-lead compensation and a low pass filter, so that the controller can operate with an ensured stability, while with an enhanced performance in contrast to the RSC based harmonic compensator.

Considering the dynamic response, the PR controller is adopted as the current controller to ensure a fast tracking of the fundamental grid current, and the RC is thus taken as a plug-in parallel harmonic compensator, as it is shown in Fig. 9. According to Fig. 9, the entire current controller with an RC harmonic compensator $G_{RC}(s)$ can be expressed as,

$$G_{op}(s) = \frac{v_{inv}^*(s)}{e(s)} = G_{PR}(s) + \underbrace{k_{rc}\frac{e^{-T_0 s}Q(s)G_f(s)}{1 - e^{-T_0 s}Q(s)}}_{G_{RC}(s)} \quad (9)$$

in which k_{rc} is the control parameter of the RC harmonic compensator $G_{RC}(s)$, $\omega_0 = 2\pi/T_0$ is the grid fundamental frequency with T_0 being the grid fundamental period. Notably, as aforementioned, a low pass filter $Q(s)$ is included in the RC compensator to eliminate the high frequency harmonics
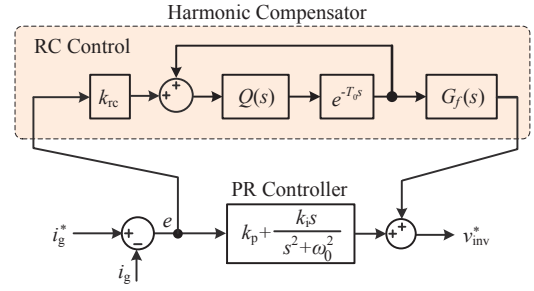
so that the controller stability can be attained. However, the tracking accuracy might be degraded by the low pass filter. Thus, normally, it is chosen in the z-domain as [8]:

$$Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1} \quad (10)$$

where $2\alpha_1 + \alpha_0 = 1$, $\alpha_1 > 0$, and $\alpha_0 > 0$. In addition, a phase-lead compensator $G_f(s)$ is also incorporated in the RC controller considering the closed-loop system stability. In the z-domain, it can be expressed as,

$$G_f(z) = z^m \quad (11)$$

with m being the phase-lead number, which is determined by experiments in practical applications. With the above design considerations, the controller of Eq. (9) can be implemented in a cost-effective digital signal processor without many computational efforts [8], where a more detailed parameter tuning of the RC controller can also be found.

Actually, the RC in Eq. (9) can also be expanded as,

$$G_{RC}(s) = k_{rc}\left[-\frac{1}{2} + \frac{1}{T_0 s} + \frac{1}{T_0}\left(\sum_h^\infty \frac{s}{s^2 + (h\omega_0)^2}\right)\right] \quad (12)$$

in which $h = 1, 2, 3, ...$ is the harmonic order (including the fundamental component). In practical applications, $h \leq N$, where $N = \lfloor f_s T_0/2 \rfloor$ with f_s being the sampling frequency. It is indicated by Eq. (12) that the RC controller can compensate the harmonics up to the Nyquist frequency $f_s/2$, since it contains N individual RSCs in parallel. Each RSC can approach an infinite gain at the corresponding resonant frequency $h\omega_0$, as it is shown in Fig. 8. It is also confirmed in Fig. 8 and Eq. (12) that the PR current controller with the RC harmonic compensator can suppress all the harmonics, including the dead time harmonics, which will be demonstrated by the following experimental tests. However, as it can be observed in Eq. (12), it is difficult to optimize its dynamic performance since it has an identical control gain k_{rc}/T_0 when compared to the multiple RSC harmonic compensator with separate gains (i.e., k_i^h) to tune. Nevertheless, efforts have been devoted to develop optimal selective harmonic controllers [8] based on the internal model principle. Such optimized harmonic controllers can also be applied to the harmonic mitigation of the dead time effect, which however is out of the scope of this paper.
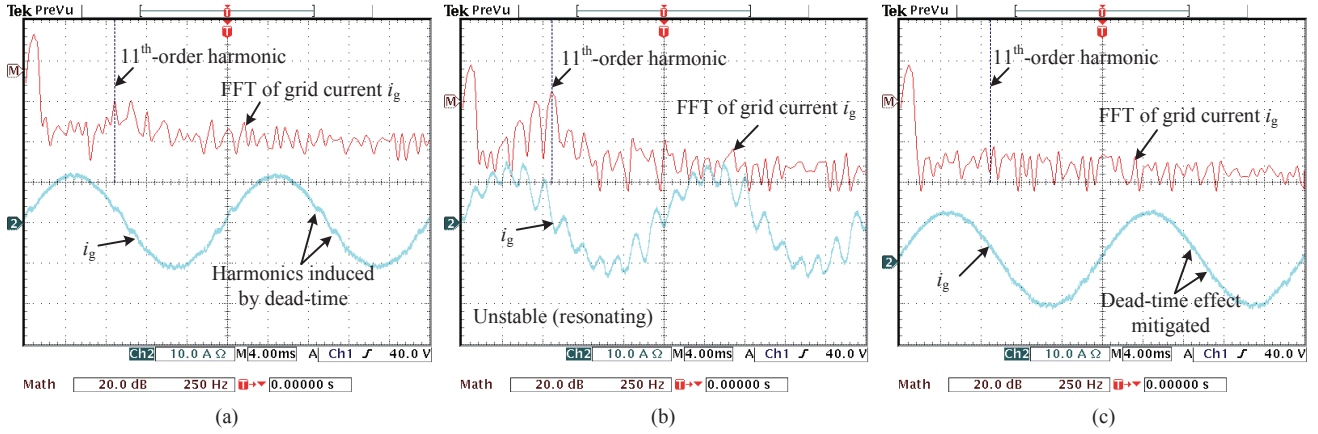
Fig. 10. Experimental results of a 2-kW single-phase grid-connected PWM inverter system at unity power factor operation (f_{sw} = 10 kHz, t_d = 3.25 μs, V_{dc} = 400 V) with the RSC or RC harmonic compensator, CH 2 - grid current i_g [10 A/div, 4 ms/div] and CH M - FFT of the grid current i_g [20 dB/div, 250 Hz/div]: (a) with the 3rd-, 5th-, 7th-, and 9th-order RSCs, (b) when the 11th-order RSC is adopted, and (c) with the RC compensator.

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TABLE I
SYSTEM PARAMETERS OF THE SINGLE-PHASE SYSTEM FOR THE TEST.

Parameter	Symbol	Value
Rated power	P_n	2 kW
DC-link voltage	V_{dc}	400 V
Grid voltage in RMS	V_g	230 V
Grid frequency	ω_0	$2\pi \times 50$ rad/s
DC-link capacitor	C_{dc}	1100 μF
	L_1	3.6 mH
LCL filter	C_f	2.35 μF
	L_2	4 mH
Sampling frequency	f_s	10 kHz

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TABLE II
CONTROLLER PARAMETERS FOR THE EXPERIMENTAL TESTS.

Controller	Parameter
PR controller	$k_p = 10$, $k_p = 1200$
RSC controller	$k_i^3 = k_i^5 = k_i^7 = 800$, $k_i^9 = 500$, $k_i^{11} = 200$
RC Controller	$k_{rc} = 0.8$
Low pass filter $Q(z)$	$\alpha_0 = 0.5$, $\alpha_1 = 0.25$
Phase-lead number	$m = 3$

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IV. EXPERIMENTAL VERIFICATIONS

Referring to Fig. 1, experiments have been performed on a single-phase inverter to verify the effectiveness of the RC based dead time harmonic mitigation. A Delta DC power supply is adopted as the DC-link. A commercial inverter with a fixed dead time of t_d = 3.25 μs (hardware dead time) and a constant switching frequency of f_{sw} = 10 kHz is connected to a programmable grid simulator (California Instrument MX-30) through an LCL filter and an isolation transformer. Control systems are implemented in a dSPACE DS 1103 system, which can produce programmable PWM signals with different dead time durations (software dead time). The other parameters of the system are given in Table I. The controllers are designed in accordance to the above discussions, and the parameters are listed in Table II.

The single-phase PWM inverter only with the hardware dead time was firstly tested under a "clean" grid (i.e., very low background distortion). Fig. 10 shows the experimental results of the system operating at the unity power factor with RSC or RC as the harmonic compensator to mitigate the harmonics due to the dead time effect. As it is shown in Fig. 10, both the RSCs and the RC can effectively mitigate the low order harmonics. However, as it can be seen from the Fast Fourier

Transform (FFT) results of the grid current i_g in Fig. 10(a), the dead time also induces higher odd-order harmonics, e.g., 11th- and 13th-order harmonics. In order to compensate those harmonics using the RSC harmonic compensators and thus to further improve the current quality, the 11th-order RSC has been added in parallel with other RSC controllers. However, the system resonance is triggered, and then the system goes into instability, as it is shown in Fig. 10(b). In contrast, the use of RC can be beneficial to the dead time harmonic mitigation without resonant issues, as illustrated in Fig. 10(c). However, the harmonics are not fully eliminated, which means that the control parameters have to be further tuned and optimized, as discussed in § III.

Additionally, the PR controller with the RC harmonic compensator is also tested under various grid voltage distortions (background distortion) with different dead time durations. The THDs of the injected current i_g are compared to those of the same system, where the RSC harmonic compensators are adopted in parallel with the PR fundamental current controller. Figs. 11 and 12 firstly demonstrate the steady-state performance of the PR controlled system with different harmonic compensators under a distorted grid and a large dead time, respectively. As it can be seen in Fig. 11(a), although the RSC based compensator can suppress the harmonics to some extend, the dead time effect remains in the injected grid current, requiring a higher-order RSC to mitigate the problem.
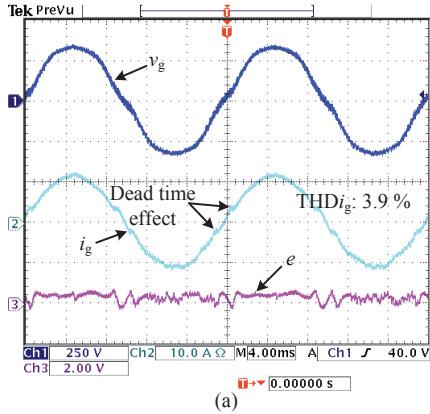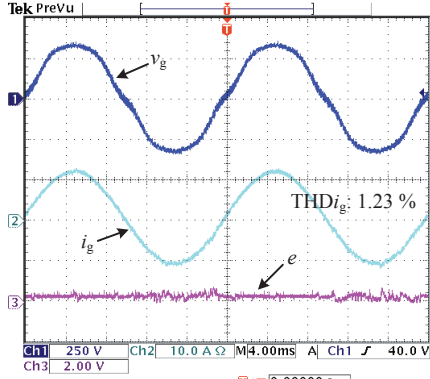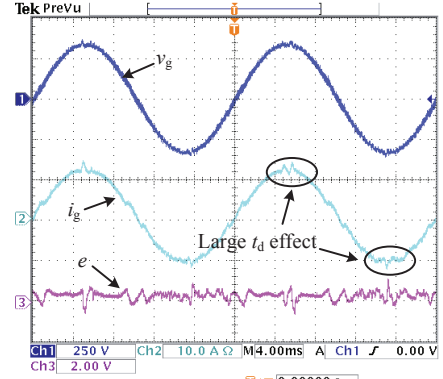
Fig. 11. Steady-state performance of the system under a distorted grid with (a) the 3rd-, 5th-, 7th-, and 9th-order RSCs and (b) the RC based harmonic compensator (grid voltage THD 4.6%, dead time duration t_d = 3.25 μs, grid voltage v_g [250 V/div], grid current i_g [2 A/div], current tracking error $e = i_g^* - i_g$ [4 A/div], time [4 ms/div]).

Fig. 12. Steady-state performance of the system under a large dead time with (a) the 3rd-, 5th-, 7th-, and 9th-order RSCs and (b) the RC based harmonic compensator (grid voltage THD 0.86%, dead time duration t_d = 5.25 μs, grid voltage v_g [250 V/div], grid current i_g [2 A/div], current tracking error $e = i_g^* - i_g$ [4 A/div], time [4 ms/div]).
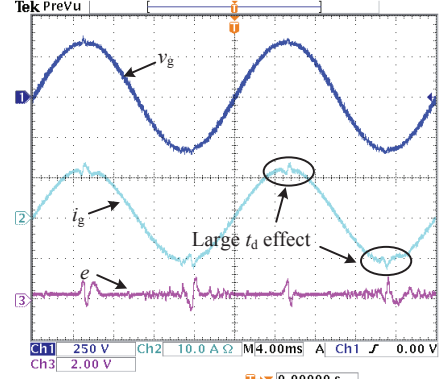
However, this may lead to resonances as demonstrated in Fig. 10. In contrast, the PR current controller with the RC harmonic compensator can effectively eliminate the harmonics either from the grid voltage background distortions or the dead time effect, and thus contributing to an almost "clean" grid current, as it is shown in Fig. 11(b).

However, when the dead time is increased to 5.25 μs, the effect from dead time on the current distortion appears again, as it is shown in Fig. 12. According to Eq. (7) and the parameters in Table I, the maximum dead time can be approximated to $t_d^m \approx 5.7$ μs. In the consideration of a weak grid (i.e., the leakage inductance of the isolation transformer in the experiments), the maximum dead time will be smaller than 5.7 μs. As a consequence, a large dead time of 5.25 μs will exceed the limitation, resulting in more distortions in the grid current. As it is shown in Fig. 12, such harmonics are difficult to compensate even using the RC controller due to the high non-linearity. These results are in agreement with the discussion in § III, where it has mentioned that increasing the DC-link voltage is a possibility to remove these distortions.

More comparisons are presented in Fig. 13 under various voltage distortions. It can be observed that the PR current controller with the RC harmonic compensator can achieve

an overall lower current THD, regardless of the grid voltage distortions with a shorter or longer dead time. In contrast, although the PR control with RSC harmonic compensators can also achieve an overall THD lower than 5 %, the individual harmonic may exceed the limitations that are defined in standards, e.g., the *IEEE Std. 1547* [27]. These harmonics become of interest in order to meet the requirements. However, with RSC harmonic compensators, resonances may be triggered as it has been demonstrated in Fig. 10. Nonetheless, the experimental results have verified the effectiveness of the RC based harmonic controller to compensate the harmonics, even including the distortions induced by the dead time.

V. CONCLUSION

In this paper, the harmonics induced by the dead time in PWM converters have been compensated using a repetitive controller, where an analysis of the dead time effect on the grid current quality has been conducted. In contrast to the conventional solutions, the repetitive based method requires no hardware modifications and it is easy to implement in a cost-effective digital controller. Experimental verifications have been performed on a single-phase grid-connected inverter with the repetitive based harmonic compensator. It is also
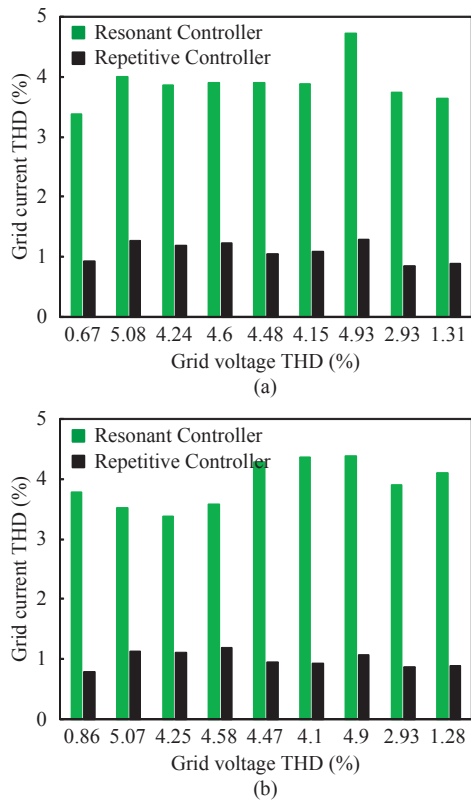
Fig. 13. Total harmonic distortion (THD) of the injected current under different grid voltage THDs using resonant (blue) and repetitive (black) controllers as the harmonic compensator considering different dead time t_d: (a) $t_d = 3.25$ μs and (b) $t_d = 5.25$ μs.

compared with the parallel resonant harmonic controllers to compensate the dead time harmonics, which may introduce instability due to resonances. Test results have verified that, regardless of the background voltage distortions, the repetitive controller based harmonic mitigation can effectively improve the current power quality (i.e., mitigate the dead time effect) without stability problems if designed properly, compared to the resonant controller.

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