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A Simplified Control Architecture for Three-Phase Inverters in Modular UPS Application with Shunt Active Power Filter Embedded

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***Abstract*— In this paper, a simplified control architecture, including individual layer control and recover layer control, is proposed for a modular online uninterruptible power supply (UPS) system is presented. The parallel control algorithm of for the DC/AC modules are mainly concentrates on the active power sharing performance due to the existence of the shunt active power filter (APF). APF will deal with the reactive power brought by the nonlinear load to guarantee that all DC/AC modules are faced with a resistive type load. On the other hand, since there is no regulation on the UPS output voltage frequency or phase angle, the recovery layer control is only concerned with the amplitude of the UPS output voltage, which means that the working load of the communication network is reduced by half. Consequently, the reliability of the system is improved. Experimental results are presented in this paper in order to validate the proposed system architecture and control.**

***Keywords*— Modular UPS system, Simplified control architecure, shunt active power filter.**

I. INTRODUCTION

Nowadays, the active development of modern technologies has brought more and more challenge to the utility [1]. Issues, related with the power quality of the utility, are receiving more and more attention from both researchers and engineers. UPS system, which is a good power quality regulator, is developing fast since it is capable of supporting many critical load, such as medical equipment, database and so on, in case of the utility blackout.

Normally, the UPS system is able to be categorized into three types, namely offline, online and line-interactive according to the IEC-62040-3 [2]. Online UPS system, which is also known as double conversion UPS, is proliferating fast due to its outstanding capability of cancelling the distortion of the utility [3]-[5]. However, a conventional online UPS system is lack of flexibility and expandability. Thus this leads to the development of modular online UPS system [6].

In Fig. 1, a typical modular online UPS system is shown. Normally, it is consisted of an AC/DC, a battery pack, an isolating transformer and numbers of DC/AC modules that are working together as the inverter stage at the same time. Such kind of system structure allows the system to be expanded easily and maintained without interrupting the system working condition. As a result, parallel technologies for DC/ACs are becoming a dominant issue that will affect the system performance.

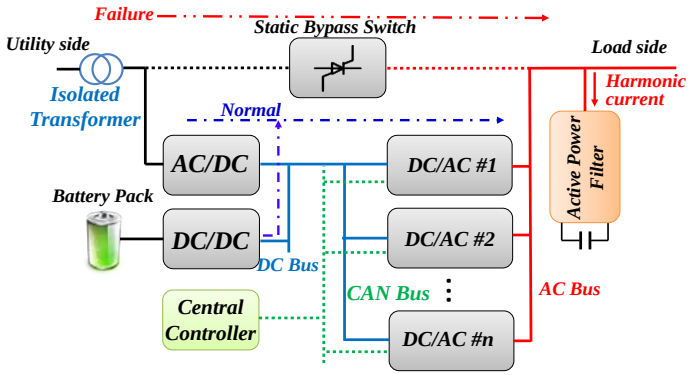


Fig. 1. Proposed Modular Online UPS Structure.

A number of parallel control algorithms were proposed, namely central control [7], master-slave [8], [9] and average load sharing [10], [11]. However, they depend on interactive lines between different modules. These critical interaction lines will reduce the reliability of the system and increase the cost of the system. Thus parallel technology based on "*droop control*" comes to the fore [12], [13]. Interactive lines are avoided but it needs to regulate to the output voltage amplitude, frequency or phase angle of the system, which results in deviations between voltage reference and actual output voltage. This is an undesired condition for an online UPS system. So voltage recover control is required [14]. Since the mature DSP technology gives a small communication delay for CAN bus [15], compensating values for voltage reference that are calculated by voltage recover control loop is transferred through a CAN communication network. Normally, six values, including three phase voltage amplitude and three phase angle, are broadcast through the CAN bus. Nevertheless, CAN bus still has some possibility of failure. And it is still critical to reduce the communication burden of CAN bus.

APF, as one of the most commercialized harmonic dealers, is developing actively during the past decades [16]. Normally, there are two categories, namely voltage type and current type [17]. The voltage type is mainly dealing with the voltage and it will compensate the voltage distortion. However, it usually requires an isolating transformer and this will increase the system cost [16]. Current types, also known as shunt active power filter is mainly concentrating on eliminating current

harmonics flowing from the source. It can be connected to the front end of the load directly.

In this paper, a shunt active power filter is connected to the output of the UPS system, as shown in Fig. 1. Thus all DC/AC modules will see resistive load no matter which kind of load the system has since the shunt APF eliminates the harmonics brought by the load. As a result, DC/AC modules provide only active power. Hereby, a virtual resistor is inserted into the control loop, which aims at sharing active power equally among all the modules. No reactive power issues are required to be taken into consideration, which means that there is no regulation on voltage frequency or phase angle. In the recovery layer control, only compensation for the voltage amplitude drop caused by virtual resistor is considered. So three phase compensating values for voltage amplitude references are sent in the CAN bus network, which means that the working load of the CAN bus network is reduced to half.

This paper is organized as follows. Section II depicts the basic control architecture of the proposed modular UPS system while Section III presents the critical parameters analysis. Simulation results are presented in Section IV. And Section V shows the experimental results, which validate the proposed control architecture. Finally, a conclusion is presented in Section VI.

II. Proposed Control Architecture for Online Modular UPS System

As shown in Fig. 1, the proposed modular UPS system mainly are divided into two parts, namely conventional UPS part and APF part. So in this Section, the control will be explained in two parts separately.

A. Conventional UPS Part Control Scheme

In convention UPS part, the control is carried out in two layers - individual layer and recover layer.

Individual layer control, as shown in Fig. 2, mainly concentrates on voltage regulation of each DC/AC module, which is considered in $\alpha\beta$ frame,

$$G_v(s) = k_{pv} + \frac{k_{rv}s}{s^2 + \omega_o^2} \tag{1}$$

$$G_c(s) = k_{pc} + \frac{k_{rc}s}{s^2 + \omega_o^2} \tag{2}$$

being k_{pv}, k_{rv}, ω_o, h, k_{pc}, and k_{rc} as voltage proportional term, fundamental frequency voltage resonant term, fundamental frequency, harmonic order, current proportional term and fundamental frequency current resonant term respectively. Although PR controller has the ability to compensate the output voltage in linear load condition, it is not required here since the harmonics are mainly eliminated by the shunt type APF.

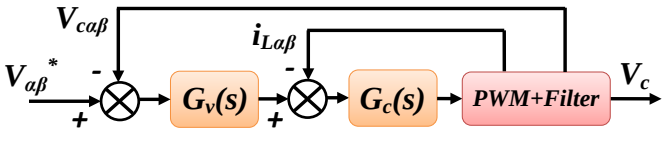


Fig. 2. Inner loop for each DC/AC module in $\alpha\beta$ frame.

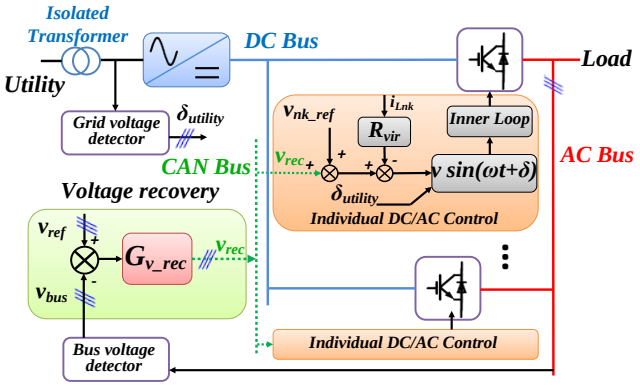


Fig. 3. Overall control diagram for the UPS part.

In order to achieve equal active power sharing among DC/AC modules, a virtual resistor loop is inserted into the control loop, as shown in Fig. 3. It is known that the output voltage amplitude will be decreased proportionally to the virtual resistor value if it is set to be a fixed value,

$$V_{nk} = V_{nkref} - R_{vir} i_{nLk} \tag{3}$$

Here n is the number of DC/AC module (1, 2, 3…N), k is the phase order (a, b, c), V_{nkref} is the nominal voltage reference and R_{vir} is the virtual resistor.

Each phase voltage references are calculated and modified respectively, referring to (4), (5) and (6), making preparations for unbalance load compensation,

$$v_a = (V_{aref} - R_{vir} i_{La}) \cdot \sin(\omega t + \delta_{utility\_a}) \tag{4}$$

$$v_b = (V_{bref} - R_{vir} i_{Lb}) \cdot \sin(\omega t + \delta_{utility\_b}) \tag{5}$$

$$v_c = (V_{cref} - R_{vir} i_{Lc}) \cdot \sin(\omega t + \delta_{utility\_c}) \tag{6}$$

Consequently, without a recover loop, the output voltage always has deviations with the given reference. In order to keep the output voltage synchronized with the given reference, a voltage recover controller is used. Hereby, the central control monitors the AC bus voltage amplitude (RMS) value, through a typical PI controller,

$$v_{k\_rec} = \left(V_{utility\_k} - V_{bus\_k}\right) \cdot G_{v\_rec}(s) \tag{7}$$

$$G_{v\_rec}(s) = k_{pv\_rec} + \frac{k_{iv\_rec}}{s} \tag{8}$$

a voltage compensating reference can be calculated, which is transferred to all the DC/AC modules through CAN bus network as shown in Fig. 3. Hereby, k_{pv_rec} and k_{iv_rec} are the proportional term and integral term for voltage recovery.

B. APF Part Control Scheme

APF, as one of the most commercialized harmonic

eliminator, used various kinds of control architecture [18]-[21]. Normally, a double *DQ*-frame controller is used including positive-sequence and negative-sequence. *DQ* frame harmonic detection methods need to know the exact harmonic orders to extract harmonic current reference for APF. Usually, nonlinear load, such as uncontrolled rectifiers, will bring mainly 5th, 7th and 11th harmonics. In the control architectures, only these three orders are controlled. But actually the harmonic content

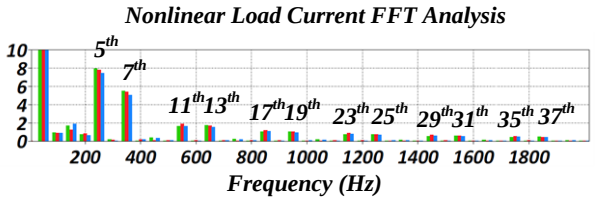


Fig. 4. Harmonic component analysis of typical uncontrolled rectifier.

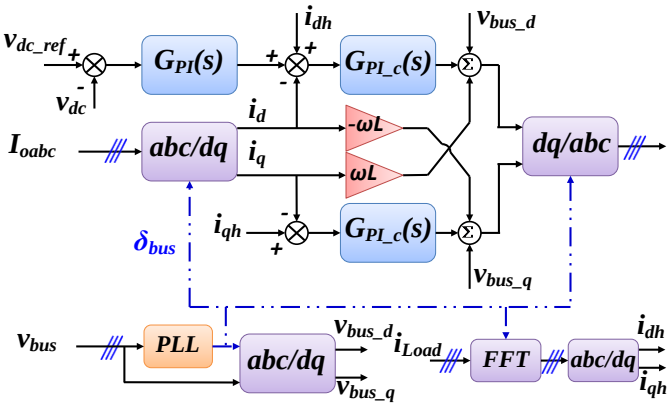


Fig. 5. Control diagram for APF.

consist many other harmonic component, as shown in Fig. 4. If the more harmonics are required to be eliminated, harmonic extraction part will laid more working load on the control part.

In this paper, Fast Fourier Transformation (FFT) is used to extract the harmonic component in the load current without considering the exact harmonic order. Thus the detailed control structure of APF is derived as shown in Fig. 5. A double loop scheme, including voltage loop-aiming at controlling DC capacitor voltage and current loop-compensate harmonic current, is chosen,

$$G_{PI}(s) = k_{pdc} + \frac{k_{idc}}{s} \tag{9}$$

$$G_{PI\_c}(s) = k_{p\_c} + \frac{k_{i\_c}}{s} \tag{10}$$

being k_{pdc}, k_{idc}, k_{p_c}, and k_{i_c} as DC voltage proportional term, DC voltage integral term, current proportional term and current integral term respectively.

III. Stabilty Analysis

Since the system is constructed mainly in two part. The critical parameters impact on system stability will be analyzed in conventional UPS system and APF respectively.

A. Conventional UPS System

Based on Fig. 2, the voltage and current inner loop is considered in $\alpha\beta$ frame. In order to obtain a detailed mathematical model for the control, a delay block due to PWM and sampling is given,

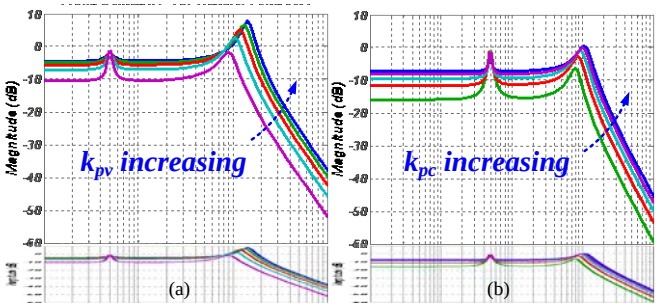


Fig. 6. Bode diagram of inner loop. (a) Bode diagram with variable k_{pv}. (b) Bode diagram with variable k_{pc}.

$$G_d(s) = \frac{1}{1.5T_s s + 1} \tag{11}$$

where T_s is the PWM period. So by combining (1), (2) and (12), transfer function from reference voltage to output capacitor voltage is derived,

$$G(s) = \frac{d}{as^2 + bs + c} \tag{12}$$

with $a = LR_{Load}C$, $b = L + G_{current}G_dR_{Load}C$, $c = R_{Load} + G_{current}G_d + G_{voltage}G_{current}G_dR_{Load}$,

where L, C and R_{Load} are filter inductance, filter capacitance and load respectively. Consequently, *bode* diagram of the system is presented in Fig. 6. It can be observed that 0 dB is achieved on the fundamental frequency (50Hz). With the proportional term k_{pv} increasing, the gain in low frequency range is increased. A similar performance is observed in the current loop, as shown in Fig. 6(b).

Since output voltage amplitude of the UPS system is decreased proportionally to the inductor current while considering a fixed virtual resistor value. According to the IEC 62040-3, voltage variation should be limited to minimum 10% due to different load condition. So according to the full load working condition, the virtual resistor value can be chosen as,

$$\left| \frac{i_L Z_{vir}}{V_{\max}} \right| \le 0.1 \tag{13}$$

being i_L, V_{max} as the inductor current under full load condition and nominal output voltage amplitude respectively.

Furthermore, voltage recover control is presented with G_{delay} being the delay function caused by communication network in Fig. 7. Since the AC bus voltage is directly used to achieve the voltage recover control, the diagram shown in Fig. 3 is able to be simplified as shown in Fig. 7 by considering that the inner loop of each DC/AC module is well tuned and operated (v_{bus} is equal to v). The transfer function for voltage recover is obtained by considering G_{dealy} as the time delay of CAN bus,

$$v = \frac{G_{v\_rec}G_{delay}v_{ref} + v_{nk\_ref} - Z_{vir}i_{Lnk}}{1 + G_{v\_rec}G_{delay}} \quad (14)$$

Considering the dynamic performance of the system, the closed loop function is expressed as follows by giving G_{delay}

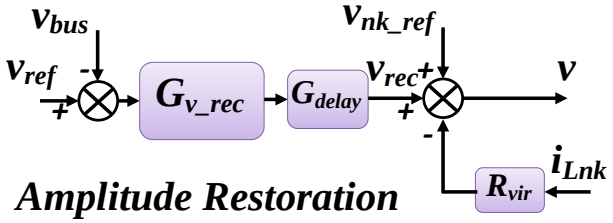


Fig. 7. Control loop for voltage recovery.

the same type as G_d but with a different T_s,

$$G_{rec}(s) = -\frac{1.5Z_{vir}T_s s^2 + s}{1.5T_s s^2 + (1 + k_{pv\_rec})s + k_{iv\_rec}} \quad (15)$$

Fig. 8 shows the *pz* map of voltage restoration control block. While k_{pv_rec} is moving from 0 to 2, one dominating pole moves obviously towards origin point while the second one tends to move inconspicuously towards unstable area but still in the stable region, as shown in Fig. 8(a). Also, it can be observed that k_{iv_rec} has indistinctive effect on the dominating poles' movements. Both two dominating poles almost stay in the same position with changing k_{iv_rec}. So mainly, k_{pv_rec} determines system dominating poles' position, which indicates crucial impacts on system performance.

B. Analysis for APF

Since control diagram architecture for APF is similar to a conventional three phase grid-connected converter, a similar analysis method is adopted.

Fig. 9 shows the current loop for APF in *DQ* frame by considering

$$G_f(s) = \frac{1}{Ls} \quad (16)$$

As a result, the transfer function for current loop is derived,

$$G_{capf} = \frac{k_{p\_c}s + k_i}{1.5T_s Cs^3 + Cs^2 + k_{p\_c}s + k_{i\_c}} \quad (17)$$

In Fig. 10, *pole-zero* map for current loop is presented. With k_{p_c} moving from 0 to 100, dominating poles of current loop is moving towards the left inside the stable region.

On the other hand, the DC capacitor voltage control loop is shown in Fig. 11. Hereby, the current is treated as an ideal loop, which is $1/(3sT_s)$. The transfer function for DC voltage control loop is derived,

$$G_{dc}(s) = \frac{\sqrt{3}(k_{pdc}s + k_{idc})}{6CT_s s^3 + 2Cs^2 + \sqrt{3}k_{pdc}s + \sqrt{3}k_{idc}} \quad (18)$$

When proportional term k_{pdc} is changing from 0 to 2, two dominating poles are moving from unstable region into stable area while the other dominating poles are moving in the right direction inside the stable region as shown in Fig. 12.

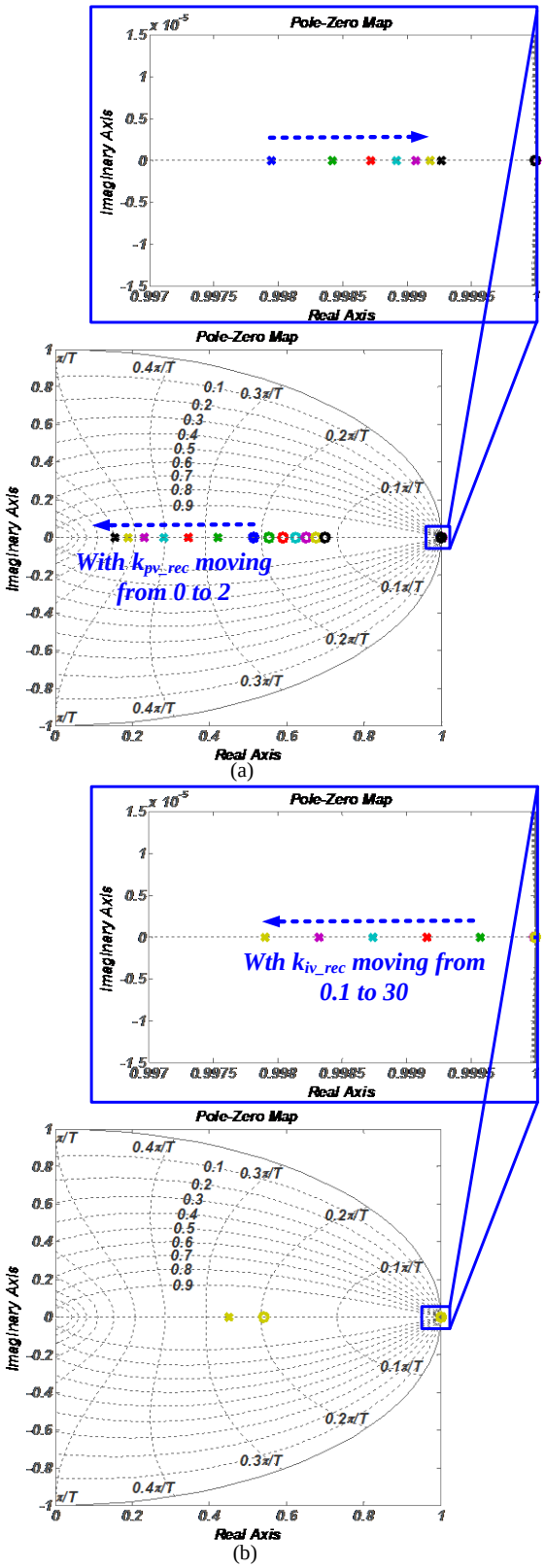


Fig. 8. *PZ* map of voltage amplitude restoration. (a) *pz* map with variable k_{pv_rec}. (b) *pz* map with variable k_{iv_rec}.

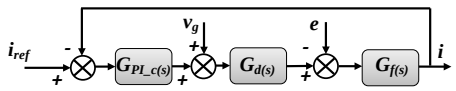


Fig. 9. Current control loop in DQ frame for APF.

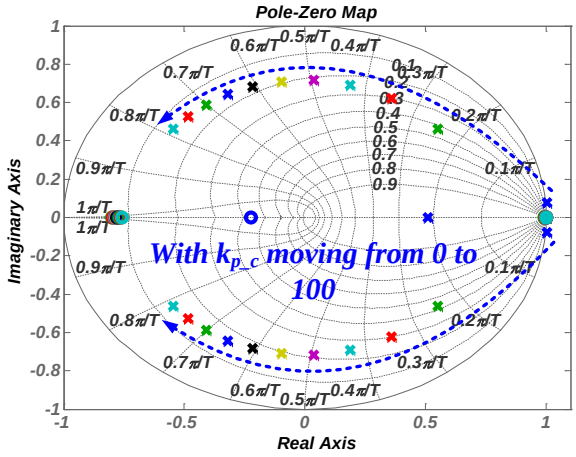


Fig. 10. *PZ* map for current loop.

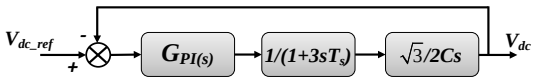


Fig. 11. Control loop for DC voltage in DQ frame of APF.

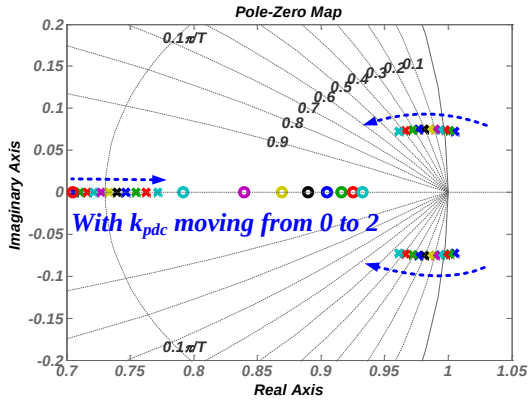


Fig. 12. *PZ* map for DC voltage control loop of APF.

IV. Simualtiong Results

A three-DC/AC-module online UPS system with APF embedded, as shown in Fig. 1, was established in the PLECS. Fig. 13 presents the simulation results under non-ideal utility condition. In the simulation, the UPS system entered Failure mode at t_g, and moved back to Normal mode at t_i. In the process of mode transition, AC bus voltage is tightly controlled with small oscillation as shown in Fig. 13(a) and (b).

Also the total load current flowing out of the UPS system was kept sinusoidal at both modes. From Table I, it can be observed that total load current THD is controlled around 3% in Failure mode and around 1.5% in Normal mode. And in normal mode, AC bus voltage THD is kept under 1% since APF had dealt with nearly all the harmonics caused by nonlinear load. Detailed THD performance is presented in Table I. With the virtual impedance loop, active power was well shared among three DC/AC converter modules during the whole mode transition, as shown in Fig. 4(c). The Fourier analysis at t_f, t_h and t_j are presented in Fig. 4(d), (e) and (f). It can be seen that 5th, 7th, 11th, 13th and other harmonics brought by nonlinear load and the utility are well suppressed by the APF. And APF lets this kind of hybrid load present resistive features. Consequently, the AC bus voltage shape in normal condition is well controlled by DC/AC converter modules parallel operation.

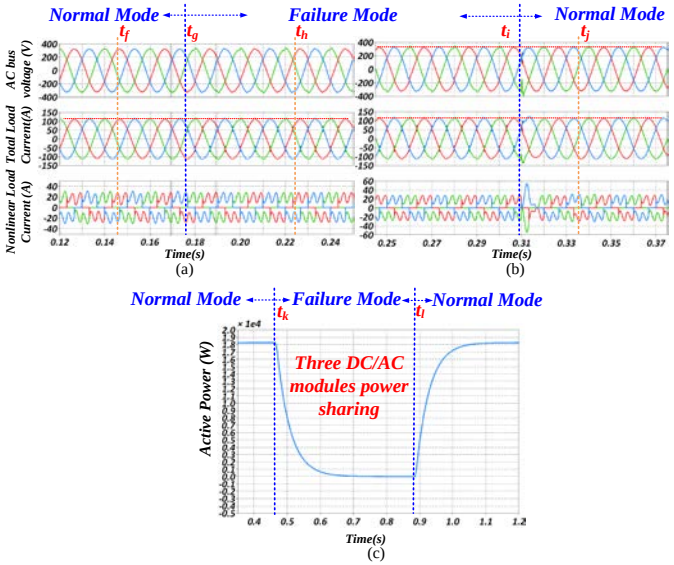


Fig. 13. Simulation results of mode transition under non-ideal utility. (a) Normal mode to Failure mode. (b) Failure mode to Normal mode. (c) Active power sharing performance.

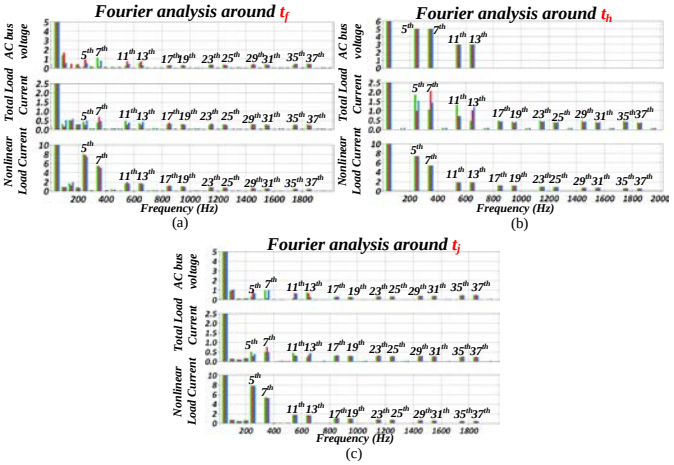


Fig. 14. FFT Analysis in different condition. (a) t_f. (b) t_h. (c) t_j.

TABLE I. System THD under different condition under non-ideal utility

	AC bus voltage (%)			*Total load current (%)*			*Nonlinear load current (%)*		
Phase	***a***	***b***	***c***	***a***	***b***	***c***	***a***	***b***	***c***
Normal Mode	0.74 25	0.87 93	0.71 17	1.47 90	1.54 51	1.54 11	49.11 09	55.35 80	46.81 17
Failure Mode	2.53 37	2.53 37	2.53 37	3.06 47	2.96 01	2.98 43	48.83 29	48.82 58	48.81 35
Normal Mode	0.78 74	0.78 62	0.81 51	1.46 74	1.47 88	1.41 79	49.76 56	51.85 58	48.14 05

V. Experimental Results

A modular online UPS system shown in Fig. 1 was built the intelligent MicroGrids laboratory (Fig. 15) [22]. with four *Danfoss* converters, shown in Fig. 15. Two were working as DC/AC, one is AC/DC and the left one is the APF. The control items was established in the Matlab/Simulink and complied into the dSPACE 1006 to achieve the control of the whole system. Critical parameters are listed in the TABLE II. The performance of the proposed system structure is validated through experimental results.

TABLE II. Parameters of Experimental Setup

Symbol	Parameter	Values
	Converters	
f_{sw}	Switch frequency of AC/DC and DC/AC module	10kHz
f_{sw_apf}	Switch frequency of APF module	10kHz
L	Filter inductance of DC/AC module	1.8mH
C	Capacitor of DC/AC module	27uF
L_{apf}	Filter inductance of APF module	1.8mH
C_{apf}	DC capacitor of APF	0.55mF
	Inverters Control Parameters	
k_{pv}	Proportional voltage term	0.55
k_{rv}	Resonant voltage term	70
k_{pc}	Proportional current term	1.2
k_{rc}	Resonant current term	150
V_{ref}	Reference voltage	230V (RMS)
	APF Control Parameters	
k_{pv_apf}	Proportional voltage term	0.1
k_{iv_apf}	Integral voltage term	756
k_{pi_apf}	Proportional current term	65
k_{ii_apf}	Integral current term	2360
V_{ref_apf}	Capacitor voltage reference for APF	700V
	Secondary Control	
k_{pv_rec}	Proportional voltage term	3.2
k_{iv_rec}	Integral voltage term	30.5
$k_{p\delta\_rec}$	Proportional phase term	0.2
$k_{i\delta\_rec}$	Integral phase term	9

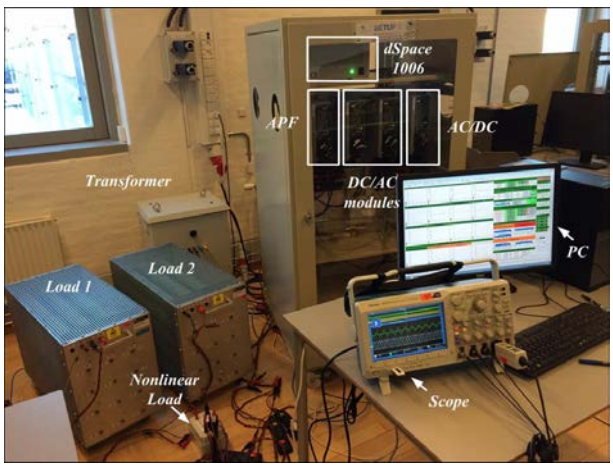


Fig. 15. Experimental setup.

A. The Performance of the Proposed APF

Fig. 16 shows the comparison of output voltage performance of the two DC/AC modules. It can be observed

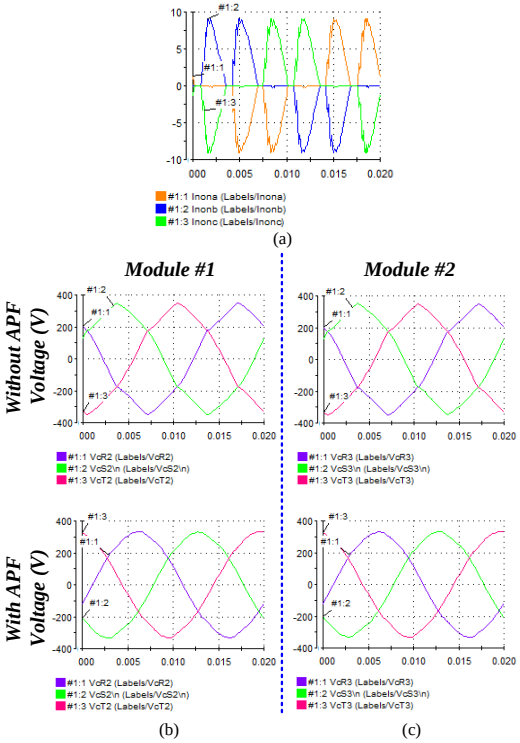


Fig. 16. Comparison of output voltage performance of each module under nonlinear load condition. (a) load current. (b) output voltage of Module #1. (c) output voltage of Module #2.

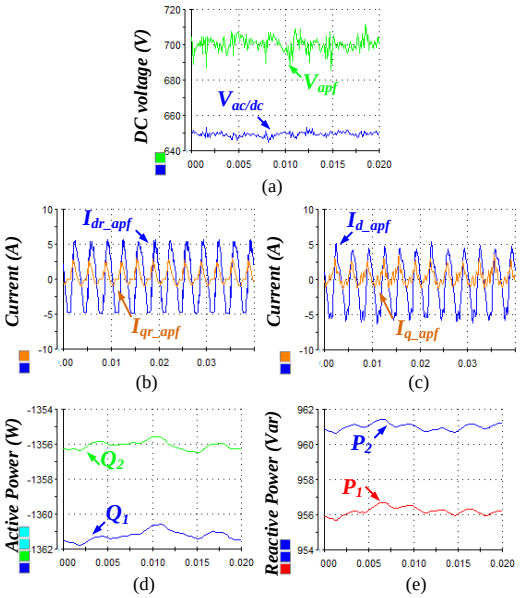


Fig. 17. Performance of APF. (a) Capacitor voltage of APF. (b) Harmonic current reference of APF in DQ frame. (c). Actual output current of APF in DQ frame. (d).Reactive power of the two DC/AC modules. (e). Active power of the two DC/AC modules.

that although the load current peak almost reaches 10A (Fig. 12(a)), both modules output voltage are kept sinusoidal due to the existence of APF. On the other hand, the DC capacitor

voltage of the APF is controlled tightly around 700V as shown in Fig. 17(a). Since the APF control is proposed in *DQ* frame, the current controller of APF is presented in Fig. 17(b) and (c). It can be seen that the output current of the APF tracks the harmonic current reference with small errors.

Furthermore, another function of the APF is to deal with all the reactive power in the system. In Fig. 17(d), it can be found that both modules reactive power is around 1360Var. Since the inductor current is used to calculate the reactive power of each module, so the reactive power brought by filter capacitance of *LC* filter is also included. Theoretically, each module reactive power should be $3*230^2*2*\pi*50*27e^{-6}$, which is 1346Var. Hereby, due to the steady state errors of the APF, not all the reactive power is eliminated. Quite a small amount, around 15Var, of it flows through each module. On the other hand, the virtual resistor loop guarantees that the active power is equally shared among the two modules, which is shown in Fig. 17(e). There is a 4W error between the two DC/AC modules.

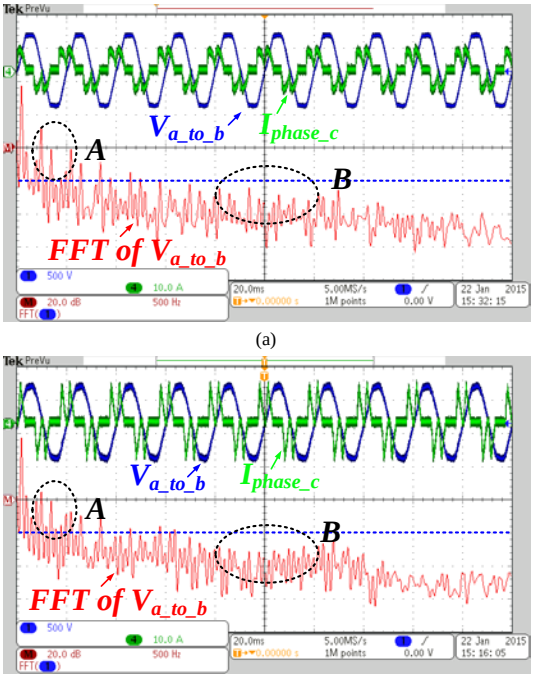
B. Total UPS System Test

Since these DC/AC modules, AC/DC and APF are working together to make up a modular UPS system finally, the total system is tested in several different scenarios.

Fig. 18 presents the output line to line voltage of the proposed modular UPS system when the APF is connected or disconnected. Here the line to line voltage (*phase a* to *phase b*) and *phase c* load current were monitored through the scope. And the FFT analysis results of the voltage were also obtained. According to the dashed blue line in Fig. 18 (Part A and Part B), it can be observed that when the APF is connected to the system, the harmonic content of the load is compensated and the output voltage of the system is kept sinusoidal without any compensation control in each DC/AC module.

Moreover, since there is no phase recovery control in the proposed modular UPS system, the phase error between UPS output voltage and the utility voltage was observed, as presented in Fig. 19. Fig. 19(a) shows the hybrid load condition, which means that the load is composed of a three phase resistor and a three phase rectifier. It can be seen that there is a small phase error between the UPS output voltage and the utility voltage. Furthermore, the pure nonlinear load condition is also tested as shown in Fig. 19(b). With APF connected or disconnected, the phase error between the UPS system and the utility is kept quite small.

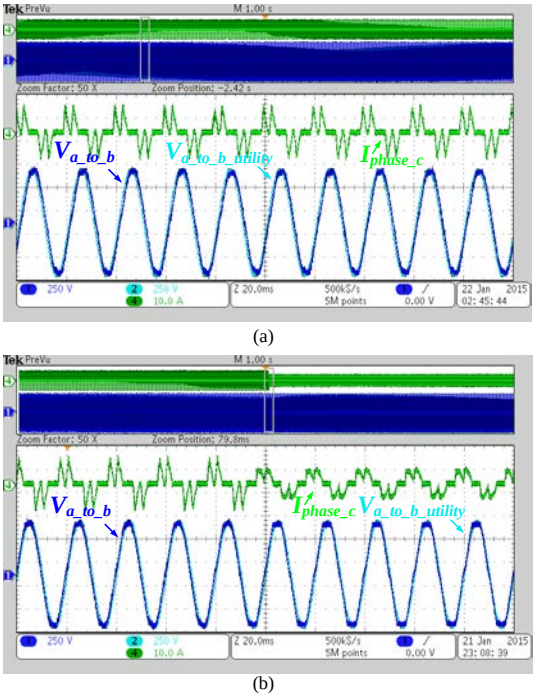
On the other hand, the load step test is also carried out in order to test the voltage amplitude recover control performance. In Fig. 20(a), a load step was performed at t_a while the load is turned off at t_b. During the whole process, the active power is equally shared between the two modules. What's more, the reactive power of the each module is almost kept the same value with some mall overshoot or dip due to the load step (Fig .20(b)). In Fig. 20(c), RMS value of the UPS output voltage is recorded. There is a voltage overshoot or dip during the transient process, which is around 15V. Compared with nominal value (230V), it is around 6.5% of the nominal value and it meets the standard IEC 62040-3. Additionally, the UPS output voltage and current details are presented in Fig. 21. It can be found that the real-time voltage oscillation is quite small.



(a)

(b)

Fig. 18. UPS line to line voltage and phase *c* current under nonlinear load condition. (a) Without APF. (b) With APF.



(a)

(b)

Fig. 19. UPS line to line voltage, utility line to line voltage and phase c current under nonlinear load condition. (a) Hybrid load. (b) Nonlinear load.

VI. Conclusion

In this paper, a simplified control architecture is proposed

by embedding an APF into the modular online UPS system. Due to the APF, reactive power is almost eliminated to make sure that all DC/AC modules are dealing with active power. And equal active power sharing among modules is achieved due to virtual impedance loop. And AC bus voltage is well controlled and it meets the standard IEC 64020-3. Furthermore, communication burden for CAN bus network is reduced to half since only three phase voltage amplitude are required to recover, which means that a higher reliability. Experimental results are shown in order to validate the proposed control architecture.

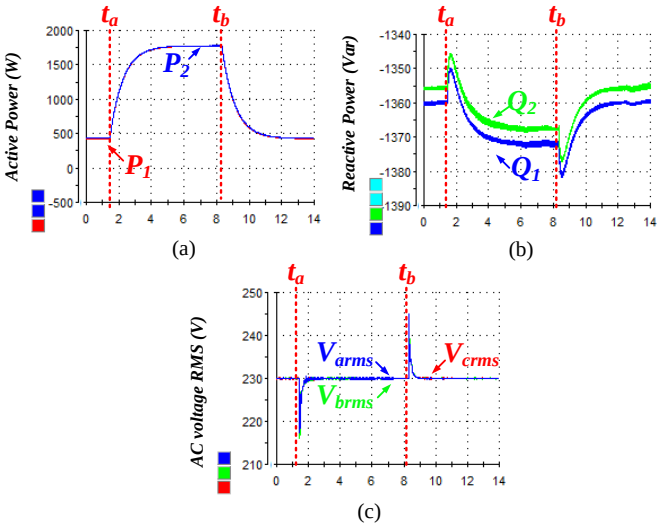


Fig. 20. Hybrid load step test. (a) Active power of each module. (b) Reactive power of each module. (c) Output voltage of the total UPS (RMS).

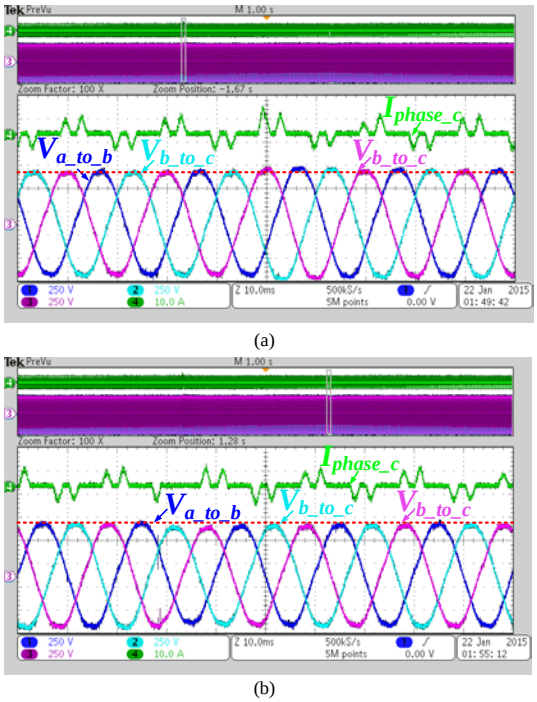


Fig. 21. Transient details of the system (a) Voltage and current details at t_a. (b) Voltage and current details at t_b.

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