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Line Filter Design of Parallel Interleaved VSCs for High Power Wind Energy Conversion Systems

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Abstract—The Voltage Source Converters (VSCs) are often connected in parallel in a Wind Energy Conversion System (WECS) to match the high power rating of the modern wind turbines. The effect of the interleaved carriers on the harmonic performance of the parallel connected VSCs is analyzed in this paper. In order to achieve low switching losses, the $60°$ clamp Discontinuous PulseWidth Modulation (DPWM1) is used to modulate the VSCs. A step-by-step design procedure of the line filter, which ensures the desired harmonic performance under all operating conditions, is presented. The analytical harmonic solution for the two parallel interleaved VSCs is derived in order to obtain the worst case voltage magnitude of the individual harmonic components. The required value of the filter admittance for the specific harmonic component is obtained by using the worst case voltage magnitude and the allowable harmonic injection limit. In order to achieve the desired filter performance with optimal values of the filter parameters, the use of a LC trap branch with the conventional LCL filter is proposed. The expressions for the resonant frequencies of the proposed line filter are derived and used in the design to selectively choose the values of the line filter components. The analysis and design methodology are also verified experimentally.

Index Terms—Voltage source converters (VSC), parallel, interleaving, filter design, trap filter, discontinuous pulse-width modulation (DPWM), wind power

I. INTRODUCTION

The power electronics converters play a vital role in integrating a wind turbine into the power system [1]. The full scale power converter is often used in modern Wind Energy Conversion System (WECS) due to its ability to provide the reactive power compensation and a smooth grid connection for the entire speed range, and it is generally realized using three-phase two-level pulsewidth modulated Voltage Source Converter (VSC) [2]. The general trend is to use the wind turbines with high output power (megawatt scale) [3] and the switching frequency of the semiconductor devices employed in these systems is often limited [4]. Therefore, large filters are required in order to meet the stringent power quality requirements imposed by the utility [5]. These filters occupy significant amount of space in the overall system [6]. Moreover, considerable losses occur in the filter components and the overall conversion efficiency is compromised if large filter components are used [4]. They also result in increased cost of the overall converter system [7]. Therefore, the filter size should be made as small as possible to achieve efficient, compact and cost-effective WECS system.

Due to the limited power handling capability of the existing semiconductor devices, the two level VSCs are often connected in parallel [8]–[11] to match the high power rating

of the wind turbine. The parallel connected VSCs can be operated with interleaved carriers to reduce the value of the filter components [12]–[18]. However, the carrier interleaving results in common-mode voltage difference across the parallel VSCs. If the conventional three limb three-phase differential mode inductor is used without any additional circulating current filter, high common-mode circulating current flows as there is no high permeability magnetic path available for the common-mode flux in the three limb three-phase differential mode inductor [19]. Another approach is to use the single phase inductor, which acts as both the circulating current filter and the line filter and permits the use of the interleaved carriers without having any additional circulating current filter. However, the use of the single phase inductor does not bring any advantages in terms of size reduction of the filter components [20] and a dedicated filter to suppress the circulating current is often required.

The use of the parallel interleaved VSCs for the active power filter application is presented in [13], [14], where a common-mode inductor is employed to suppress the circulating current and the reduction in the size of the passive components is demonstrated. A use of Coupled Inductor (CI) for suppressing the circulating current is presented in [21] and substantial size reduction of the filter components can be achieved by using the CI over the single phase line inductor solution [20]. However, the control complexity increases as the precise control over the fundamental frequency circulating current is required in order to avoid the saturation of the CI [22].

Some of the harmonic components that are present in the switched output voltage of the individual VSCs can be canceled by using the interleaved carriers. Miller *et al.* [12] studied the line current harmonic cancellation effect of N parallel interleaved VSCs. The effects of the PulseWidth Modulation (PWM) scheme, the interleaving angle, and the modulation indices on the line current quality are analyzed in [15]. The optimal interleaving angle to improve the line current quality is discussed in [16]. Mao *et al.* [17] presented a hybrid PWM scheme, involving multiple switching sequences and different interleaving angles to improve the line current quality.

The interleaved carriers in the parallel VSCs can reduce the filtering requirement by phase shifting some of the harmonic components and thus fully or partially cancel their contribution in the line current. Further reduction in the values of the filter components can be achieved by using a high-order filter [23]. The LCL filter is an attractive option [24]–[26], and it is commonly used in the WECS [2]. For the LCL filter, the
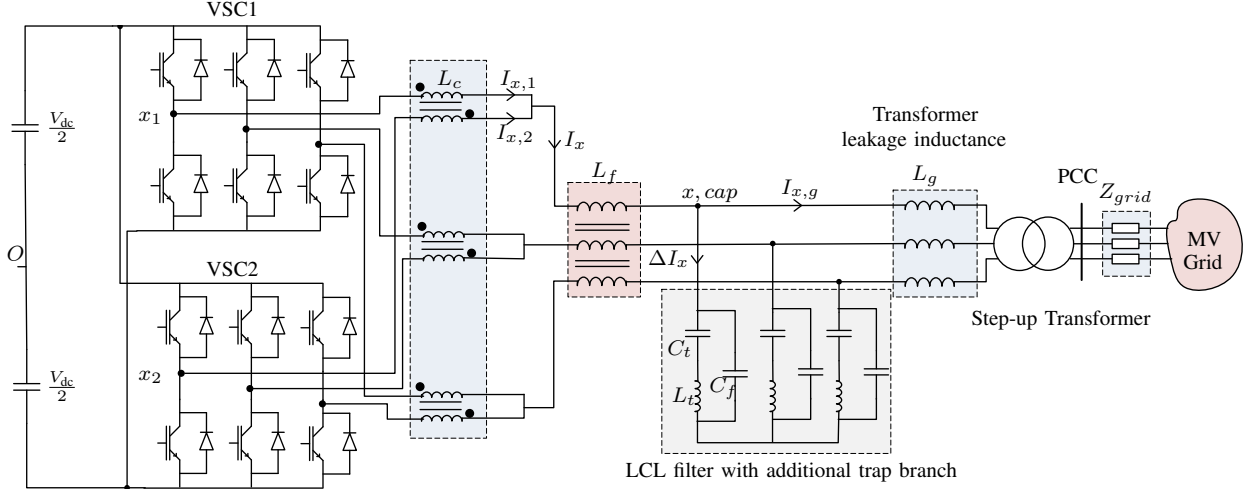
Fig. 1. The grid side converter of the WECS, comprised of two parallel VSCs with interleaved carriers, connected to the medium voltage network by using a step-up transformer. $x = \{A, B, C\}$

admittance transfer function is given as

$$Y_{LCL}(s) = \left.\frac{I_g(s)}{V_{PWM}(s)}\right|_{V_g=0} = \frac{1}{L_f L_g C_f} \frac{1}{s(s^2 + \omega_{r,LCL}^2)} \tag{1}$$

where L_f is the converter side inductor, L_g is the grid side inductor, C_f is the filter capacitor, I_g is the grid current, V_g is the grid voltage, and V_{PWM} is the switched voltage of the VSC. The resonant frequency of the LCL filter is given as

$$\omega_{r,LCL} = \sqrt{\frac{L_f + L_g}{L_f L_g C_f}} \tag{2}$$

Due to the presence of the complex conjugate poles, the roll-off of the high frequency components (higher than the $\omega_{r,LCL}$) is -60 dB/decade. Therefore, the LCL filter offers good attenuation to the high frequency harmonic components, and it can effectively reduce the differential mode electromagnetic interference (above 150 kHz) [24]. The switched voltages at the VSC terminals have harmonic components concentrated around the multiple of the carrier frequency. Due to the limited switching capability of the semiconductor devices used in the high power applications, a fairly high value of the filter components are required for the LCL filter to attenuate the major harmonic components (first carrier frequency and its sideband harmonics).

The value of the filter components can be reduced by using a LC trap branch, which is tuned to attenuate the major carrier harmonics and its sideband harmonics. This can be realized by inserting an inductor in series with the capacitor of the LCL filter [27]. The use of the LC trap branch to attenuate the sideband harmonic components around the carrier frequency is proposed in [27], [28]. The multiple LC trap branches are used, to attenuate the carrier harmonic and its sideband harmonic components around the carrier frequency and its multiple, in [29], [30]. The admittance transfer function of the line filter with the LC trap branch, commonly known as

trap filter, is given as

$$Y_{trap}(s) = \left(\frac{1}{(L_f + L_g) + \frac{L_f L_g}{L_t}}\right)\frac{s^2 + \omega_t^2}{s(s^2 + \omega_{r,trap}^2)} \tag{3}$$

The resonant frequencies are given as

$$\omega_t = \frac{1}{\sqrt{L_t C_f}}$$

$$\omega_{r,trap} = \frac{1}{\sqrt{\left(\frac{L_f L_g}{L_f + L_g} + L_t\right)C_f}} \tag{4}$$

where L_t is the inductor inserted in series with the capacitor C_f of the LCL filter. From (4), it is evident that the $\omega_{r,trap}$ is less than the ω_t. Due to the introduction of the complex conjugate zeros, the roll-off of the high frequency components (higher than the ω_t) is -20 dB/decade. This leads to a poor attenuation of the high frequency harmonic components. On the contrary, the LCL filter offers good attenuation to the high frequency harmonic components. Therefore, the LC trap branch along with the LCL filter can be used to achieve the desired filtering performance (both at the low and the high frequency components) with small values of the filter components. The use of such a filter for single VSC is presented in [31]. However, the high frequency attenuation is compromised due to insertion of the damping resistor in series with the capacitive branch.

The VSCs are often connected in parallel in the WECS and the use of interleaved carriers to fully or partially cancel the effect of some of the harmonic frequency components is proposed in this paper. The design procedure of the LCL filter with additional LC trap branch of two parallel interleaved VSCs is presented. The paper is organized as follows: the operation of the parallel interleaved VSCs is briefly described in Section II. The analysis of the proposed high-order line filter is discussed in Section III and the filter design constraints along with the step-by-step design procedure are presented in Section IV. The simulation and the experimental results are finally presented in Section V to verify the analysis.

II. PARALLEL INTERLEAVED VOLTAGE SOURCE CONVERTERS

The carrier signals, of the parallel connected VSCs in WECS (shown in the Fig. 1), are interleaved to reduce the value of the filter components. The effect of the interleaved carriers on the operation of the parallel VSCs is analyzed in this section.

The interleaved operation of the parallel VSCs:

1) Improves the line current quality.
2) Reduces the switch current ripple of each VSC, provided the circulating current is suppressed effectively.

Therefore, the value of the filter components can be reduced. However, additional inductive filter is required to suppress the circulating current. A CI is used as a circulating current filter [15], [20]–[22], [32]–[34] due to its effectiveness in suppressing the circulating current. Multiple parallel interleaved VSCs with magnetic coupling between the parallel interleaved legs of the corresponding phase can be realized using the following configurations [21]:

1) Whiffletree configuration.
2) Cyclic cascade configuration.
3) Using a magnetic structure with multiple parallel magnetic limbs.

In addition to suppress the circulating current, the CI also performs the function of averaging the switched output voltage of the parallel interleaved legs [21]. The values of the line filter components depend on the magnitude of the individual harmonic component in the average output voltage, which is the same in all of the above mentioned CI configurations. Therefore, the line filter design can be carried out independently, without considering the circulating current filter arrangement.

In this paper, the WECS with two parallel interleaved VSCs is considered. However, the line filter design approach, presented in this paper, can be used for any number of parallel interleaved VSCs. The use of the LC trap branch with the conventional LCL filter is proposed. The converter side inductor L_f, the grid side inductor L_g, and the capacitor C_f forms the LCL filter. The series connection of the L_t and C_t forms the LC trap branch. The WECS is connected to a medium voltage network by using a step-up transformer. The leakage inductance of a step-up transformer often ranges from 0.04-0.06 pu [35], and it is considered as a part of the grid side inductance L_g.

The interleaving angle of $180°$ is used as it results in optimal harmonic performance at high modulation indices [16]. The closed form analytical solution to determine the individual voltage harmonic components of the pulsewidth modulated voltage is derived. Moreover, the relationship between the maximum value of the switch current ripple and the converter side inductor is also obtained in this section.

A. Modulation Scheme

The $60°$ clamp discontinuous PWM (DPWM1) [36] scheme clamps the output terminals of the VSCs to the positive and the negative terminals of the dc-link for a $60°$ interval each in a
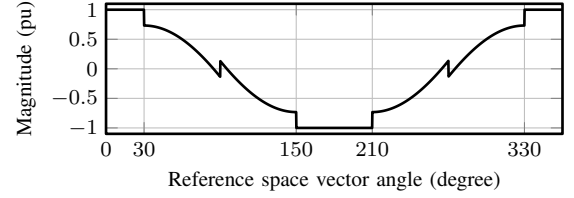

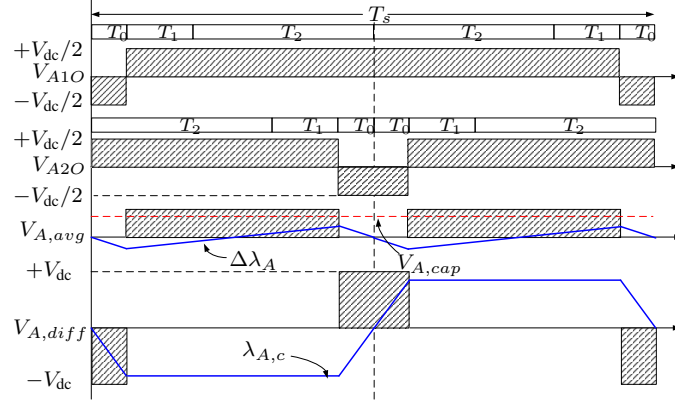Fig. 2. Modulation waveform of $60°$ clamp PWM (DPWM1) scheme with modulation index $M = 1$.

Fig. 3. The effect of the interleaved carriers. The pole voltages of phase A of the individual VSCs and their average $V_{A,avg}$ and difference $V_{A,diff}$ are depicted. The modulation index is M=1, the interleaving angle is $180°$ and the reference space vector angle is $\psi = 45°$.

fundamental cycle, as shown in Fig. 2. The clamping intervals of $60°$ are arranged around the positive and negative peak of the fundamental reference voltage. For the applications, where the displacement power factor is close to unity, the switching is avoided when the current through the devices is near its peak [37]. In addition to the active power, the WECS is also required to provide reactive power within a power factor range of 0.95 leading to 0.95 lagging. In this case, the use of the DPWM1 would result in the switching losses reduction up to 45% compared to that of the continuous space vector modulation [38].

B. Voltage Harmonic Distortion

As a result of the interleaved carriers, the pole voltages (measured with respect to the dc-link midpoint O in Fig. 1) of the VSC2 are phase shifted by the interleaving angle with respect to that of the VSC1. The pole voltages of phase A of two interleaved VSCs are shown in Fig. 3. The resultant switched voltage is an average of the individual pole voltages. The difference between the average of the pole voltages and the grid voltage ($V_{A,avg} - V_{A,g}$) appears across the line filter, whereas the difference in the pole voltages ($V_{A10} - V_{A20}$) is the potential across the circulating current filter L_c. The equivalent circuit of the hth harmonic component with two parallel interleaved VSCs is shown in Fig. 4. The harmonic components in the grid current depend on the magnitude of the individual harmonic components in the average pole voltage and the line filter admittance. Therefore, the magnitude of the individual harmonics components of the average pole voltage

$$f(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n}\cos(n[\omega_0 t + \theta_0]) + B_{0n}\sin(n[\omega_0 t + \theta_0])]$$

$$+ \sum_{m=1}^{\infty} [A_{m0}\cos(m[\omega_c t + \theta_c]) + B_{m0}\sin(m[\omega_c t + \theta_c])] \tag{5}$$

$$+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} [A_{mn}\cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0]) + B_{mn}\sin(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0])]$$

$$A_{mn}1 = \frac{4V_{\text{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{3}J_n(q\frac{\pi}{2}\sqrt{3}M)\cos(\frac{n\pi}{6})\sin[(m+n)\frac{\pi}{2}]\cos(\frac{q\pi}{2}) \\ +\frac{1}{2n}\sin(\frac{n\pi}{6})\Big(\sin[(q+m)\frac{\pi}{2}] - \cos(n\pi)\sin[(q-m)\frac{\pi}{2}]\Big)|n\neq 0 \\ +\frac{1}{n}\sin(\frac{n\pi}{6})\cos(\frac{n\pi}{3})J_0(q\frac{\pi}{2}\sqrt{3}M)\Big(\sin[(q+m)\frac{\pi}{2}]\cos(n\pi) - \sin[(q-m)\frac{\pi}{2}]\Big)|n\neq 0 \\ +\sum_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n+k)\frac{\pi}{6}]\cos[(2n+k)\frac{\pi}{6}] \\ \Big(\cos[(n+k)\pi]\sin[(k+q+m)\frac{\pi}{2}] + \sin[(k-q+m)\frac{\pi}{2}]\Big) \\ +\sum_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n-k)\frac{\pi}{6}]\cos[(2n-k)\frac{\pi}{6}] \\ \Big(\cos[(n-k)\pi]\sin[(k+q+m)\frac{\pi}{2}] + \sin[(k-q+m)\frac{\pi}{2}]\Big) \end{pmatrix} \tag{6}$$

$$A_{mn},avg = \frac{4V_{\text{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{3}J_n(q\frac{\pi}{2}\sqrt{3}M)\cos(\frac{n\pi}{6})\cos(\frac{m\pi}{2})\sin(\frac{n\pi}{2})\cos(\frac{q\pi}{2}) \\ +\frac{1}{2n}\sin(\frac{n\pi}{6})\sin(\frac{q\pi}{2})\cos(\frac{m\pi}{2})[1 - \cos(n\pi)][1 - 2\cos(\frac{n\pi}{3})J_0(q\frac{\pi}{2}\sqrt{3}M)]|n\neq 0 \\ +\sum_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n+k)\frac{\pi}{6}]\cos(\frac{m\pi}{2})\cos[(2n+k)\frac{\pi}{6}] \\ \Big(\cos[(n+k)\pi]\sin[(k+q)\frac{\pi}{2}] + \sin[(k-q)\frac{\pi}{2}]\Big) \\ +\sum_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n-k)\frac{\pi}{6}]\cos(\frac{m\pi}{2})\cos[(2n-k)\frac{\pi}{6}] \\ \Big(\cos[(n-k)\pi]\sin[(k+q)\frac{\pi}{2}] + \sin[(k-q)\frac{\pi}{2}]\Big) \end{pmatrix} \tag{7}$$

where V_{dc} is the dc-link voltage, M is the modulation index, and $q = m + n(\omega_0/\omega_c)$.
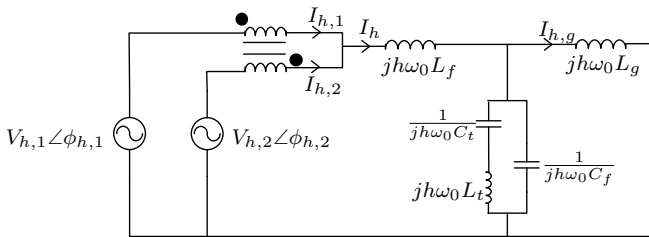

Fig. 4. The equivalent circuit of the hth harmonic with two parallel interleaved VSCs ($h \neq 1$).

is derived hereafter.

As a result of the modulation, the pole voltages have undesirable harmonic components in addition to the desired fundamental component. This harmonic components can be represented as the summation series of sinusoids [36], characterized by the carrier index variable m and the baseband index variable n as shown in (5). The hth harmonic component is defined in terms of m and n, and it is given as

$$h = m(\frac{\omega_c}{\omega_0}) + n \tag{8}$$

where ω_0 is the fundamental frequency and ω_c is the carrier frequency.

The harmonic coefficients A_{mn} and B_{mn} in (5) are evaluated for each $60°$ sextant using the double Fourier integral. The closed form theoretical harmonic solution for the first VSC for asymmetrical regular sampled DPWM1 is evaluated and given in (6). The coefficients in (6) contains $J_y(z)$, which represents the Bessel functions of the first kind of the order y and argument z. The carrier signal for the second VSC is phase shifted by an interleaving angle of $180°$. The theoretical harmonic solution for the second VSC is also evaluated. The magnitude of the individual harmonic components is the same in both of the VSCs. However, some of the harmonic components in the pole voltage of VSC2 are in phase opposition to that of the VSC1. As a result, these harmonic components do not appear in the harmonic spectra of the average pole voltage.

The theoretical closed form harmonic solution of the average pole voltage is given by (7) and the harmonic spectrum for the modulation index $M = 0.95$ is also depicted in Fig. 5(b). The double summation term in (5) is the ensemble of all possible frequencies, formed by taking the sum and the
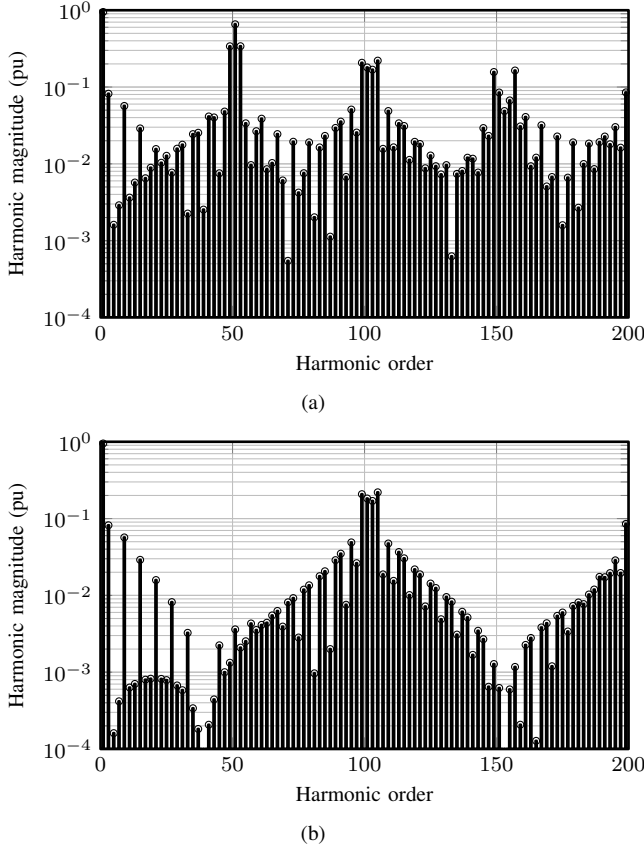
Fig. 5. Theoretical harmonic spectrum with the modulation index $m = 0.95$ and pulse ratio $\omega_c/\omega_0 = 51$. (a) Harmonic spectrum of the pole voltage of the individual VSC, (b) Harmonic spectrum of the average pole voltage of the interleaved VSCs with an interleaving angle of $180°$.

difference between the carrier harmonics, the fundamental waveform and its associated baseband harmonics [36]. Careful examination of (7) reveals that the $\cos\left(\frac{m\pi}{2}\right)$ term appears as a multiplication factor in each summation term. As a result, the harmonic coefficients in (7) are zero for all the odd multiple of the carrier index variable m. Therefore, the side band harmonics around the odd multiple of the carrier harmonic frequencies are reduced. This is evident from Fig. 5(b), where the pulse ratio is $\omega_c/\omega_0 = 51$. The magnitude of the harmonic components around the $51th$ harmonic and its odd multiple is reduced considerably compared to that of the individual VSC, as shown in Fig. 5. Also the magnitude of all even harmonic components is negligible. This happens due to the presence of the $\sin\left(\frac{n\pi}{2}\right)$ as a multiplication term in the nth order Bessel function, as given in (7).

C. Switch Current Ripple

The switch current ripple influences the design of both the passive and the active components. Therefore, the maximum value of the peak-to-peak switch current ripple for interleaved VSCs is derived in this subsection. Due to the phase symmetry, only the current through the semiconductor devices of phase A is analyzed.

Even when the carriers are not interleaved, small circulating current flows due to the hardware and control asymmetries.

Due to the interleaved carriers, this current further increases. Therefore, the switch currents $I_{x,1}$ and $I_{x,2}$ have the following two distinct components:

1) The component contributing to the resultant line current
2) The circulating current

and the switch current can be given as

$$I_{x,1} = I_{x1} + I_{x,c}$$
$$I_{x,2} = I_{x2} - I_{x,c} \tag{9}$$

where, x = phase $[A, B, C]$. I_{x1} and I_{x2} are the components of the switch currents contributing to the resultant line current and $I_{x,c}$ is the circulating current. By neglecting the effect of the hardware and the control asymmetries, the line current is assumed to be shared equally between the VSCs ($I_{x1} = I_{x2}$). From (9), the circulating current can be given as

$$I_{x,c} = \frac{I_{x,1} - I_{x,2}}{2} \tag{10}$$

and the dynamic behavior of the circulating current can be described as

$$\frac{dI_{x,c}}{dt} = \frac{V_{x1O} - V_{x2O}}{L_c} \tag{11}$$

where L_c is the inductance offered to the circulating current. A CI is used as a circulating current filter due to its effectiveness in suppressing the circulating current. The CI is constructed without introducing any intentional air gap in the magnetic flux path. As a result, it offers high inductance to the circulating current and thus the contribution of the circulating current towards the switch current can be neglected. This assumption is also verified by the experimental studies given in section V.

The resultant current I_x is assumed to be shared equally between the VSCs and by neglecting the contribution of the circulating current, the switch current is given as

$$I_{x,1} = I_{x,2} \cong \frac{I_x}{2}$$
$$\cong \frac{I_{x,f}}{2} + \frac{\Delta I_x}{2} \tag{12}$$

where $I_{x,f}$ is the fundamental frequency component of the line current and the ΔI_x is the ripple current.

D. Ripple Component of the Resultant Line Current ΔI_x

The switch current ripple is half of the ripple component of the resultant line current ΔI_x and the relationship between the ΔI_x and L_f is derived in this sub-section. In the interest of brevity, following assumptions are made:

1) The grid voltage is assumed to be free from the harmonic distortions.
2) The fundamental component of the switch current is assumed to be in phase with the fundamental component of the reference voltage.

The reference space voltage vector is synthesized using the discrete voltage vectors such that the volt-second balance is maintained. The difference between the applied voltage vector and the reference space vector is known as the error voltage vector, and it is illustrated in Fig. 6. The harmonic flux vector is a time integral of this error voltage vector, and it
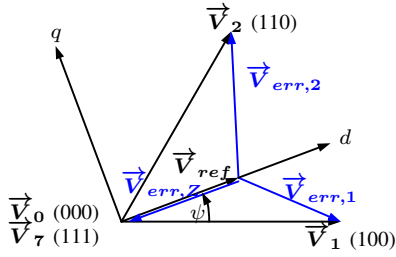
Fig. 6. The active and the zero vectors to synthesize a given reference vector and corresponding error voltage vectors.
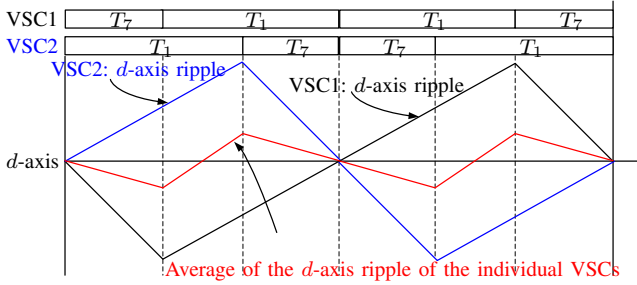

Fig. 7. d-axis component of the harmonic flux ripple over a carrier cycle of two parallel VSCs and their average. The interleaving angle is $180°$ and reference space vector angle $\psi = 0°$.

Fig. 8. The single phase equivalent circuit of the LCL filter with additional LC trap branch.

Fig. 9. The variation of the magnitude of the admittance transfer function of the line filter with frequency.

is directly proportional to the ripple current [39]–[41]. For the parallel interleaved VSCs, the flux linkage in the converter-side inductor L_f is the average of the harmonic flux vectors of the individual VSCs.

The harmonic flux vector can be decomposed into d-axis and q-axis components. For the unity power factor operation, the switch current ripple for phase A becomes maximum for the reference space vector angle $\psi = 0°$. At this instant, the ripple current of phase A can be obtained by only evaluating the d-axis component of the harmonic flux vector, and it is given as

$$\overrightarrow{Vd_{err,1}}T_1 = \tfrac{2}{3}V_{dc}[\cos\psi - \tfrac{3}{4}M]T_1 \tag{13a}$$

$$\overrightarrow{Vd_{err,2}}T_2 = \tfrac{2}{3}V_{dc}[\cos(60° - \psi) - \tfrac{3}{4}M]T_2 \tag{13b}$$

$$\overrightarrow{Vd_{err,z}}T_z = -\tfrac{1}{2}V_{dc}MT_z \tag{13c}$$

where T_1, T_2 and T_z are the dwell time of voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_0}/\overrightarrow{V_7}$, respectively. The d-axis component of the harmonic flux ripple for individual VSCs and their average flux ripple for $\psi = 0°$ are depicted in Fig. 7.

The peak-to-peak value of the resultant d-axis harmonic flux for $\psi = 0°$ is given as

$$\lambda_{d(pp)} = \frac{V_{dc}(1 - \tfrac{3}{4}M)(\tfrac{3}{2}M - 1)}{3f_c} \tag{14}$$

This is equal to the peak-to-peak value of the flux linkage in the L_f and the peak-to-peak current ripple in the I_x is given as

$$\Delta I_{x(pp)} = \frac{V_{dc}(1 - \tfrac{3}{4}M)(\tfrac{3}{2}M - 1)}{3f_cL_f} \tag{15}$$

Considering an equal current sharing between the VSCs, the peak-to-peak value of the switch current ripple is half of the $\Delta I_{x(pp)}$. From (15), it is evident that the switch current ripple
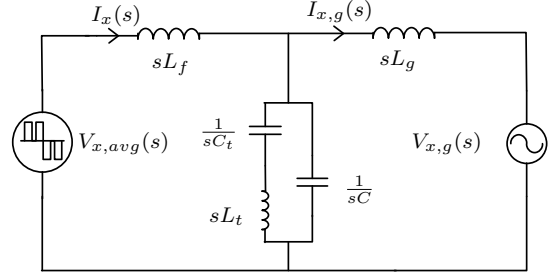
is the function of a dc-link voltage V_{dc}, the modulation index M, and the switching frequency f_c. For the given V_{dc} and f_c, the peak-to-peak value of the switch current ripple is maximum for the modulation index of $M = 1$, and it is given as

$$\Delta I_{x1(pp,max)} = \frac{V_{dc}}{48f_cL_f} \tag{16}$$

Once the desired maximum value of the switch current is chosen, the minimum value of the converter side inductance $L_{f,min}$ can be obtained using (16).

III. LINE FILTER

The line filter arrangement for the parallel interleaved VSCs is shown in Fig. 1 and its single phase equivalent circuit is also depicted in Fig. 8. The converter side inductor L_f, the grid side inductor L_g, and the capacitor C_f forms the LCL filter. The series connection of the L_t and C_t forms the LC trap branch. The L_f and L_g are designed to carry the rated current and the Equivalent Series Resistance (ESR) of these inductors are normally small [42] compared to the L_t and its effect in the low frequency region (upto 9 kHz) can be neglected for the filter design. The admittance transfer function of the filter (only considering the ESR of the LC trap branch) is given by (17). The resonant frequencies of the complex conjugate poles are given by (18). The complex conjugate zeros are also introduced due to the presence of the LC trap branch, and it

$$\left.\frac{I_{x,g}(s)}{V_{x,avg}(s)}\right|_{V_g=0} = \left(\frac{1}{L_f L_g C}\right) \frac{s^2 + \frac{\omega_t}{Q_t}s + \omega_t^2}{s(s^2 + \frac{\omega_{r1}}{Q_{r1}}s + \omega_{r1}^2)(s^2 + \frac{\omega_{r2}}{Q_{r2}}s + \omega_{r2}^2)} \tag{17}$$

$$\omega_{r1} = \frac{1}{\sqrt{2}}\sqrt{\left(\frac{1}{LC} + \frac{1}{L_t C_{eq}}\right) - \sqrt{\frac{1}{LC^2}\left[\frac{1}{L} + \frac{2(C_t - C)}{L_t C_t}\right] + \frac{1}{L_t^2 C_{eq}^2}}}$$

$$\omega_{r2} = \frac{1}{\sqrt{2}}\sqrt{\left(\frac{1}{LC} + \frac{1}{L_t C_{eq}}\right) + \sqrt{\frac{1}{LC^2}\left[\frac{1}{L} + \frac{2(C_t - C)}{L_t C_t}\right] + \frac{1}{L_t^2 C_{eq}^2}}}$$

$$\text{(18)}$$

$$\text{where } L = \frac{L_f L_g}{L_f + L_g}, \text{ and } C_{eq} = \frac{C C_t}{C + C_t} \tag{19}$$

is given as

$$\omega_t = \frac{1}{\sqrt{L_t C_t}} \tag{20}$$

The quality factors are given as

$$Q_t = \frac{1}{R_t}\sqrt{\frac{L_t}{C_t}}$$

$$Q_{r1} = \frac{1}{R_t C_t}\frac{1}{\omega_{r1}}\frac{(\omega_{r2}^2 - \omega_{r1}^2)}{(\omega_{r2}^2 - \omega_t^2)} \tag{21}$$

$$Q_{r2} = \frac{1}{R_t C_t}\frac{1}{\omega_{r2}}\frac{(\omega_{r2}^2 - \omega_{r1}^2)}{(\omega_t^2 - \omega_{r1}^2)}$$

where R_t is the ESR of the LC trap branch.

The variation of the magnitude of the admittance transfer function of the line filter with respect to the frequency is depicted in Fig. 9. The magnitude of the simplified admittance transfer function closely matches with magnitude of the actual filter transfer function (considering the ESR of all the filter components) in the low frequency region, as shown in Fig. 9. The effect of the additional LC trap branch is evident in the vicinity of the frequency of $2f_c$, as shown in Fig. 9. The magnitude of the admittance transfer function of the trap filter proposed in [27], [28] is also plotted in Fig. 9 for comparison. Due to the presence of the capacitive branch C, the line filter offers a good attenuation to the high frequency components. Therefore, it can effectively reduce the differential mode electromagnetic interference (above 150 kHz). However, the additional pole pairs with a resonant frequency ω_{r2} are present in the proposed filter, as shown in Fig. 9. The value of the resonant frequency ω_{r1} of the proposed filter is slightly less than that of the trap filter $\omega_{r,trap}$ and it is important to incorporate necessary damping to avoid amplification of the harmonic components, present in close proximity of ω_{r1}. The parallel R_d/C_d branch is used to provide necessary damping at ω_{r1}. However, the introduction of the damping branch slightly reduces the attenuation offered to the high frequency harmonic components, as shown in Fig. 9.

IV. Filter Design

The filter is designed for a 2.2 MVA WECS system shown in Fig. 1. The WECS is connected to a medium voltage network using a step-up transformer. The leakage inductance

TABLE I
BASE VALUES FOR PER-UNIT SYSTEM

Parameters	Base Values (analysis)	Base Values (experiments)
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Voltage	690 V	400 V
Current	1840 A	15.87 A
Frequency	50 Hz	50 Hz
Inductance	688 μH	46 mH
Capacitance	14709 μF	218 μF

of a step-up transformer often ranges from 0.04-0.06 pu [35], and it is considered as a part of the grid side inductance L_g. The analysis and the design methodology are also verified by performing experiments on a small scale (11 kVA) laboratory setup. The base values for both of the systems are given in Table I. The filter design constraints and the step-by-step design procedure are given in this section.

A. Design Constraints

1) Harmonic Current Injection Limits: The harmonic current injection limit for a generator connected to the medium-voltage network, specified by the German Association of Energy and Water Industries (BDEW) [5], [26], [43], is considered in this paper. The permissible harmonic current injection is determined by the apparent power of the WECS and the Short-Circuit Ratio (SCR) at the Point of the Common Coupling (PCC). The maximum current injection limit of the individual harmonic components up to 9 kHz is specified in the standard and the limits for the WECS connected to the 10 KV medium-voltage network are given in Table II. Special limits are set for the odd-ordered integer harmonics below the 25th harmonic, as given in Table II. The SCR is taken to be 20 and the allowable injection limits of individual harmonic components on the low voltage side (690 V) for the 2.2 MVA WECS are calculated. The calculated current injection limits for the individual harmonic components are shown in Fig. 10.

2) Maximum Switch Current Ripple: The controllability of the system is affected if the switch current has a high ripple content [6]. Therefore, the maximum value of the peak-to-peak switch current ripple is restricted to 0.45 pu in this design.

TABLE II
BDEW HARMONIC CURRENT INJECTION LIMITS FOR THE WECS
CONNECTED TO THE 10 KV MEDIUM VOLTAGE NETWORK

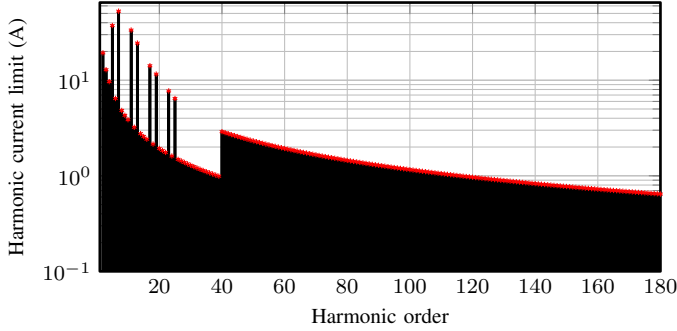| Harmonic Order h	Current Injection Limit (A/MVA/SCR)
5	0.058
7	0.082
11	0.052
13	0.038
17	0.022
19	0.018
23	0.012
25	0.01
Even-ordered $h < 40$	0.06 / h
$40 < h < 180$	0.18 / h

Fig. 10. BDEW [5] harmonic current injection limits for 2.2 MVA WECS on the low voltage side of the transformer with SCR=20.

3) Reactive Power Consumption: The current flowing through the semiconductor devices, the converter side filter inductor L_f and the circulating current filter L_c can be minimized by limiting the current drawn by the shunt branches of the line filter. Moreover, when VSCs are modulated using DPWM1, the switching losses increase with the increase in the phase difference between the reference voltage and the fundamental component of the switch current. Therefore, the switching losses can also be minimized by making the reactive power consumption of the line filter as small as possible. The grid voltage may vary over a range of 1 ± 0.1 pu and the reactive power consumption of the shunt branches of the line filter is restricted to 0.05 pu for the maximum grid voltage of 1.1 pu.

B. Filter Design Procedure

The value of the line filter components are mainly determined based on:
1) The individual voltage harmonic components that appear across the line filter.
2) The maximum value of the switch current ripple.

The magnitude of the individual harmonic frequency components that appears across the line filter is determined by the difference of the magnitude of the corresponding harmonic frequency component in the average of the phase voltages of the parallel interleaved legs and the magnitude of the same harmonic frequency component in the grid voltage. The average of the phase voltages of the parallel interleaved legs is independent of the arrangement of the CI. Therefore, the
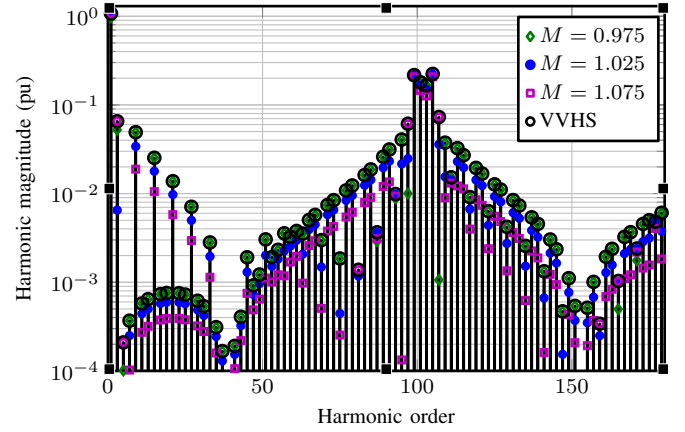

Fig. 11. The magnitude of the individual voltage harmonic component of the average pole voltage.

design of the line filter can be carried out independently. The interleaved operation of the parallel VSCs partially or completely eliminates some of the voltage harmonic components in the average of the phase voltages of the interleaved legs. Therefore, the reduction in the value of the line filter components can also be achieved. A step-by-step design procedure for the proposed line filter is illustrated in this subsection.

1) Virtual Voltage Harmonics: The magnitude of the individual harmonic components in the injected grid current is the multiplication of the magnitude of the respective harmonic component in the averaged pole voltage and the admittance offered by the filter at that harmonic frequency. The theoretical harmonic solution of the $V_{x,avg}$ can be obtained using (7). From (7), it is evident that the harmonic coefficients are the function of the dc-link voltage V_{dc} and the modulation index M. Therefore, for a given value of the dc-link voltage, the magnitude of the individual harmonic components varies with the modulation index M. The magnitudes of the individual voltage harmonic component of $V_{x,avg}$ for the different modulation indices are shown in Fig. 11. In order to satisfy the harmonic current injection limit over the entire operating range, the worst case magnitude of the individual harmonic components of $V_{x,avg}$ is required. The spectrum comprises the maximum values of the individual voltage harmonic components over the entire operating range and it is defined as a Virtual Voltage Harmonic Spectrum (VVHS) [26].

VVHS for the considered modulation range and the maximum value of the dc-link voltage is calculated and it is depicted in Fig. 11. The magnitude of most of the harmonic components (except those harmonic components, which are present around the even multiple of the carrier harmonic) increases as the modulation index approaches the lower limit. On the other hand, the harmonic components around the even multiple of carrier frequency harmonic increases with increase in the modulation index, as shown in Fig. 11.

2) Required Filter Admittance: The worst case filter admittance requirement is obtained from the harmonic current injection limit and the VVHS of the phase voltage. The required admittance for the h*th* harmonic component is given

as

$$Y_h^* = \frac{I_{h,BDEW}^*}{V_{h,VVHS}} \quad (22)$$

where $I_{h,BDEW}^*$ is the BDEW current injection limit of the hth harmonic component and $V_{h,VVHS}$ is the voltage magnitude of the corresponding harmonic component in VVHS of the phase voltage. The VVHS of the average pole voltages comprises a common mode component in all phase, which gets canceled out in the line-to-line output voltage. The VVHS of the phase voltages is obtained by removing this common mode component from the VVHS of average pole voltages.

3) Selection of the LC Trap Branch Parameters: As a result of the interleaved carriers with an interleaving angle of $180°$, the magnitude of the harmonic components around the odd multiple of the carrier frequency is reduced considerably. Therefore, the major voltage harmonic components appear around the 2nd carrier frequency harmonic ($2f_c$), as shown in Fig. 11. The line filter should offer small admittance to these harmonic components, which can be achieved by tuning the LC trap branch, such that the resonant frequency ω_t is equal to $2f_c$.

The resonant frequency of the LC trap branch is given by (20). The attenuation offered by the filter to the base band harmonics of the 2nd carrier frequency harmonic depends on the quality factor of the LC trap branch, given by (21). The magnitude of the voltage harmonic components in vicinity of the 2nd carrier frequency harmonic increases with increase in the modulation index, as shown in Fig. 11. Therefore, the required value of the quality factor of the LC trap branch strongly depends on the maximum operating value of the modulation index M.

The capacitors are available in standard values and the selection of the values of the L_t and C_t to realize the required value of the quality factor is driven by the availability of the capacitor. The value of C_t is chosen to be 0.02 pu in this design. The value of L_t is taken to be 0.0048 pu in order to have the resonant frequency of the trap branch at twice the switching frequency. The quality factor of the trap branch is 25, which is sufficient to achieve the required attenuation around the 2nd carrier frequency harmonics.

4) Selection of L_f, L_g and C: As a result of an interleaved carrier, the voltage magnitude of the odd multiple of the carrier harmonics and its side bands is reduced considerably, as shown in Fig. 11. The proposed line filter introduces a resonance at ω_{r1} and ω_{r2}. The damping requirement can be reduced by choosing the filter parameters such that the resonances occur at the frequencies where the magnitude of the voltage harmonics are small.

The values of ω_{r1} and ω_{r2} are chosen to be 2.05 kHz and 7.65 kHz, respectively. Once the values of ω_t, ω_{r1}, and ω_{r2} are decided, the Q_{r1} and Q_{r2} are obtained using (21). From these values, the C_{eq} is calculated, which is given as

$$C_{eq} = \left(\frac{1}{L_t}\right)\frac{1}{\omega_{r1}^2 + \omega_{r2}^2 + \frac{\omega_{r1}\omega_{r2}}{Q_{r1}Q_{r2}} - \frac{\omega_{r1}^2\omega_{r2}^2}{\omega_t^2}} \quad (23)$$
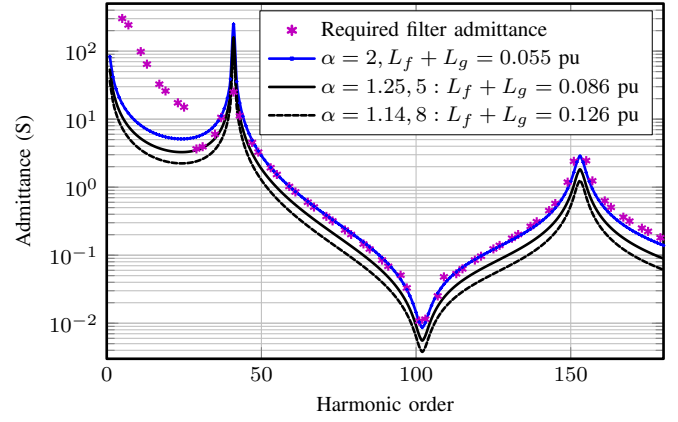

Fig. 12. Filter admittance plot for different values of α.

For the given values of the ω_t, ω_{r1}, and ω_{r2}, the product of L and C is given as

$$LC = \frac{\omega_t^2}{\omega_{r1}^2\omega_{r2}^2} \quad (24)$$

As the value of C_t is already fixed, the value of C can be obtained using (19) and (23). The desired value of the L can be achieved by selecting the proper values of L_f and L_g. Many possible combinations of L_f and L_g exist. Let,

$$L_g = \alpha L \quad (25)$$

where α is a constant, and it is greater than one. Using (19) and (25), L_f can be given as

$$L_f = \left(\frac{\alpha}{\alpha - 1}\right)L \quad (26)$$

For the given range of grid voltage variation, the maximum value of the dc-link voltage, which is required to ensure the VSC operation in a linear modulation range, is decided by the value of the inductance ($L_f + L_g$). Therefore, $L_f + L_g$ should be made as small as possible. The minimum value of $L_f + L_g$ can be obtained by selecting $\alpha = 2$, where the values of L_f and L_g are equal. However, from a cost point of view, this combination may not be optimal. For $\alpha > 2$, the value of L_g is more than the value of L_f. The reverse is true for $1 \leqslant \alpha \leqslant 2$. The value of $\alpha = 2$ is taken as the starting point. In case a harmonic injection limit is violated, the design is discarded and a new value of the α will be selected. The maximum value of the α is limited by the switch current ripple, and it is given as

$$\alpha_{max} = \frac{1}{1 - \frac{48Lf_c\Delta I_{x1(pp,max)}}{V_{dc}}} \quad (27)$$

In case a harmonic injection limit is violated even with α_{max}, the design is discarded and new design will be evaluated by changing the parameters of the LC trap branch. The filter admittance plot for different values of α is shown in Fig. 12.

As mentioned earlier, appropriate damping is required to avoid amplification of the harmonic components around ω_{r1} and ω_{r2}. Therefore, a C_d/R_d branch has been added. The capacitive branch is split into two separate branches and a
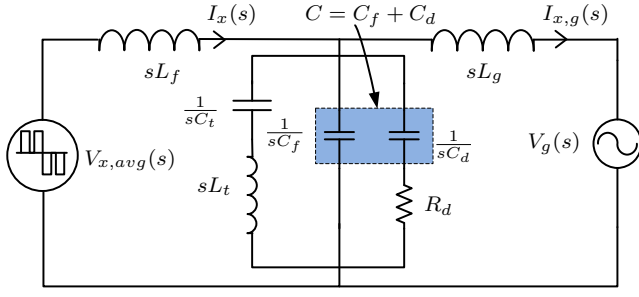
Fig. 13. The single phase equivalent circuit of the LCL filter with additional LC trap and a C_d/R_d damping branch.
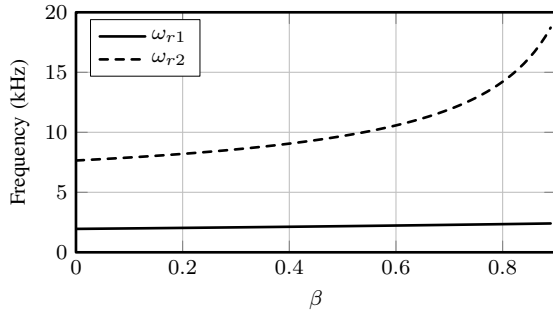

Fig. 15. Admittance plot of the designed filter. The effect of the grid inductance variation is also depicted.

Fig. 14. Worst case variation in the resonant frequencies as a function of β.

Fig. 16. Single phase equivalent circuit of the LCL filter with parallel R_d/C_d damping branch.

resistor is inserted in one of the branches, as shown in Fig. 13. Let,

$$C_d = \beta C$$
$$C_f + C_d = C \qquad (28)$$

The introduction of the C_d/R_d damping branch changes the resonant frequencies ω_{r1} and ω_{r2}. The worst case change in the resonant frequency can be obtained by setting $R_d = \infty$ [44]. The worst case variation in the resonant frequencies as a function of β is shown in Fig. 14. The ω_{r1} varies in a small range, whereas the variation in ω_{r2} is more and increases sharply as β approaches one. For a given value of R_d, the losses in the damping branch and admittance offered to the high frequency components also increase as β approaches one. In order to restrict the variation in the resonant frequencies in a narrow range and to reduce the inventory [25], β is taken to be 0.5.

The C_d/R_d damping branch introduces an additional zero ($z = -1/C_dR_d$) and a pole ($p = z/\gamma$ and $\gamma < 1$) in the admittance transfer function of the line filter. The value of γ can be obtained by solving the denominator polynomial, as given in the Appendix. Considering the complexity involved in solving the quintic function, only the information of the additional zero is used to obtain the minimum value of the damping resistor $R_{d,min}$. Once $R_{d,min}$ is obtained, the required value of the damping resistor R_d is determined by using the frequency response characteristic of the filter admittance transfer function given in the Appendix. The improved resonance damping can be achieved by selecting R_d and C_d such that the $|z| < \omega_{r1}$ [44]. Using this relation, the minimum value of the required
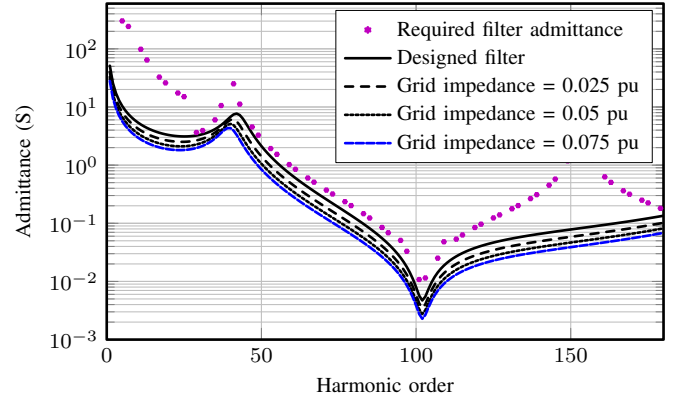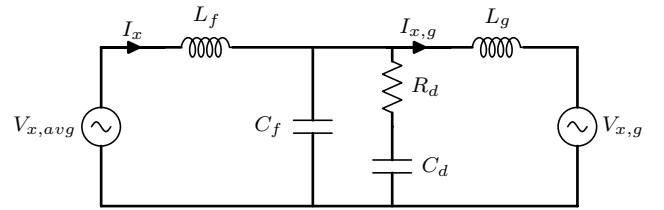
damping resistor $R_{d,min}$ can be obtained, and it is given as

$$R_{d,min} = \frac{1}{\omega_{r1}C_d} \qquad (29)$$

The line filter is designed by following the above mentioned procedure. The final filter parameters are given in Table IV and the its admittance plot is also depicted in Fig. 15. The effect of the line impedance (L_{grid}) variation on the filter performance is also shown. The value of ω_{r1} reduces slightly with the increase in the grid impedance, whereas the ω_t remains unaltered.

5) Comparison with the LCL Filter: Reduction in the value of the filter components is achieved using the proposed high order filter. This has been verified by comparing the values of the filter components of the proposed filter with that of the LCL filter.

The single phase equivalent circuit of the LCL filter with the parallel R_d/C_d damping branch is shown in Fig. 16. L_f is the converter side inductor, L_g is the grid side inductor, and C_f is the filter capacitor. The parameters of the damping branch are chosen as per the procedure specified in [6]. The admittance transfer function of the LCL filter is given by (1). The value of the filter components of the LCL filter is chosen such that the filter admittance is less than the required value of the filter admittance for the harmonic frequency components upto 9 kHz (as per the BDEW limits). The admittance plot of the LCL filter along with the required filter admittance is shown in Fig. 17.

The values of the filter components of the designed LCL filter are given in Table III, along with the filter parameters of the proposed filter. The total shunt capacitance ($C_f + C_d + C_t$)

TABLE III
FILTER PARAMETERS OF THE PROPOSED FILTER AND THE LCL FILTER

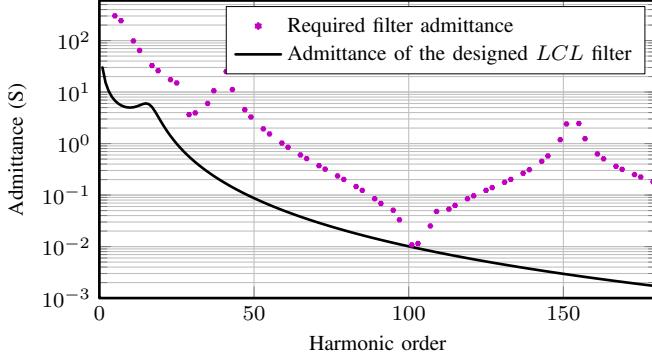| Parameters	Proposed filter	LCL filter
$L_f + L_g$	61.92 μH (0.09 pu)	106.75 μH (0.155 pu)
Capacitor	$(C_f + C_d + C_t)$ 566 μF (0.0386 pu)	$(C_f + C_d)$ 2400 μF (0.16 pu)
Trap inductor L_t	3.3 μH (0.0048 pu)	-

Fig. 17. Admittance plot of the designed LCL filter, with $L_f = 0.065$ pu (44.75 μH), $L_g = 0.09$ pu (62 μH), $C_f = 0.08$ pu (1200 μF), $C_d = 0.08$ pu (1200 μF).
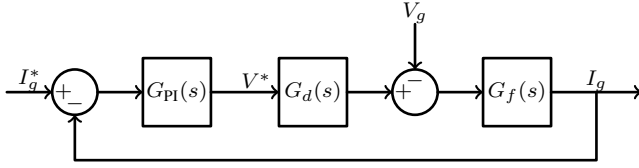

Fig. 18. Grid current controller structure.

in the proposed filter is 0.0386 pu, against the 0.16 pu in the LCL filter. The reduction in the value of the shunt capacitor improves the efficiency, as shunt capacitors draws reactive current and increases resistive losses. In addition, it also increases switching losses when the VSCs are modulated using the DPWM1 scheme. The use of the proposed line filter result in 42 % reduction in the values of the series inductors ($L_f + L_g$). This reduces the volume of the inductive components, as inductors L_f and L_g are designed to carry the rated value of the current and occupy significant amount of space. The proposed line filter requires an additional trap inductor $L_t = 0.0048$ pu. However, the value of L_t is very small. In addition, L_t is placed in the shunt branch and carries small current. Therefore, the volume of this additional inductor is small compared to the reduction achieved in L_f and L_g.

C. Controller Design

The grid current is controlled using the Proportional-Integral (PI) controller, as shown Fig. 18. The control variables are transformed to a synchronously rotating frame, which rotates at the fundamental frequency of the grid voltage. The transfer function of the PI controller is given by

$$G_{\text{PI}}(s) = K_p + \frac{K_i}{s} \qquad (30)$$

TABLE IV
PARAMETERS FOR SIMULATION AND EXPERIMENTAL STUDY

| Parameters	Simulation study	Experiment
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Switching frequency	2.55 kHz	2.55 kHz
AC voltage (line-to-line)	690 V	400 V
DC-link voltage	1080 V	650 V
L_f	13.76 μH (0.02 pu)	0.87 mH (0.019 pu)
L_g (+ Transformer leakage)	48.16 μH (0.07 pu)	3.1 mH (0.0675 pu)
Trap capacitor C_t	294 μF (0.02 pu)	4.4 μF (0.02 pu)
Trap inductor L_t	3.3 μH (0.0048 pu)	220 μH (0.0048 pu)
Capacitor $C_f = C_d$	136 μF (0.0093 pu)	2 μF (0.0093 pu)
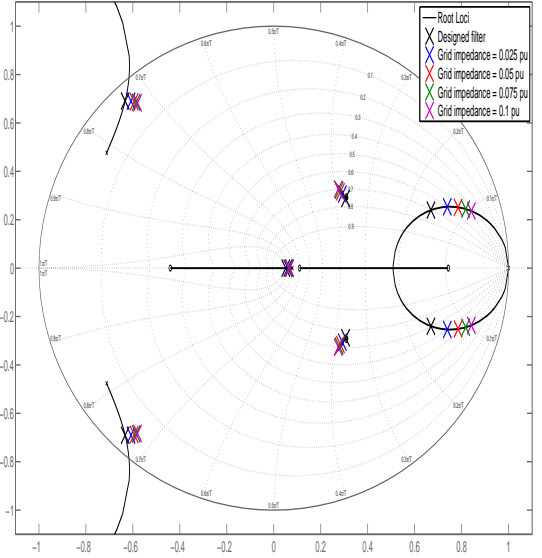
Fig. 19. Root loci of the closed loop system with the designed controller. The closed loop poles are marked using 'x'.

where K_i is the integral gain and the K_p is the proportional gain of the PI controller. The control and PWM delay is represented by the $G_d(s)$. The transfer function of the filter $G_f(s)$ is given in the Appendix. The parameters of the designed filter are given in Table IV. The continuous transfer functions are discretized and the controller parameters are calculated in the discrete time domain using the root locus theory. The controller is designed to have a damping factor of 0.707. The parameters of the PI controller to meet the given damping factor requirement are $K_p = 0.168$ and $K_i = 1310$. Fig. 19 shows the root locus in the z-plane of the closed-loop
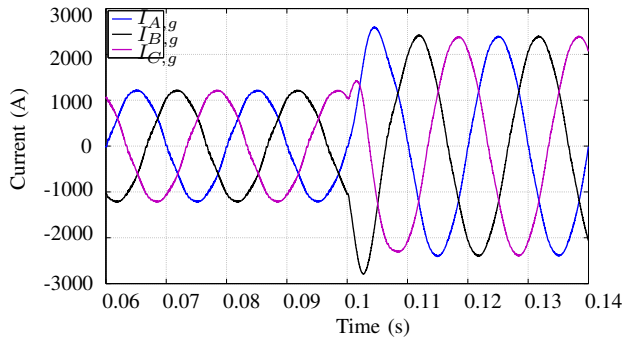
Fig. 20. Step response of the controller. The d-axis current reference is changed from 0.5 pu to 1 pu at $t = 0.1$ s.

system with the designed controller parameters.

The pole map of the closed-loop system for varying values of the grid side inductance L_g is also shown in Fig. 19, where L_g is the summation of the leakage inductance of the step-up transformer and the line inductance L_{grid} (inductance of the electrical network between the PCC and the source). The value of the L_g is varied from 0.07 pu to 0.17 pu. With the increase in the value of the L_g, the damping factor decreases from 0.707 to 0.5. However, the system remains stable with the designed PI controller, as evident from Fig. 19.

V. SIMULATION AND EXPERIMENTAL RESULTS

The simulation study and the experimental verification is carried out to verify the analysis and the design methodology and the results are presented in this section.

A. Simulation Study

The simulations have been carried out using the PLECS simulation tool. The parameters used for the simulation study are given in Table IV. The controller behavior to the step change in the reference signal is shown in Fig. 20. The d-axis current reference is changed from 0.5 pu to 1 pu. The grid current tracks the reference and transient performance is also found to be satisfactory. Fig. 21, shows the simulated waveforms of the system, operating under rated conditions with the unity power factor operation. The harmonic spectrum of the simulated grid current is obtained by using fast Fourier transform (FFT) and plotted along with the BDEW harmonic current injection limit in Fig. 22. The major harmonic components around the 2nd carrier harmonic frequency are effectively suppressed. All harmonic components are within the specified harmonic current injection limits.

B. Experimental Results

To verify the analysis and the design methodology, a line filter for a small scale (11 kVA) laboratory prototype with two interleaved VSCs was designed. The parameters of the line filter used in this setup are listed in Table IV. In order to avoid the effect of the background harmonics present in the grid voltage, an AC power source MX-35 from the California Instruments is used as a harmonic free grid emulator. The grid impedance is taken to be $Z_{grid} = 0.04$ pu. The control
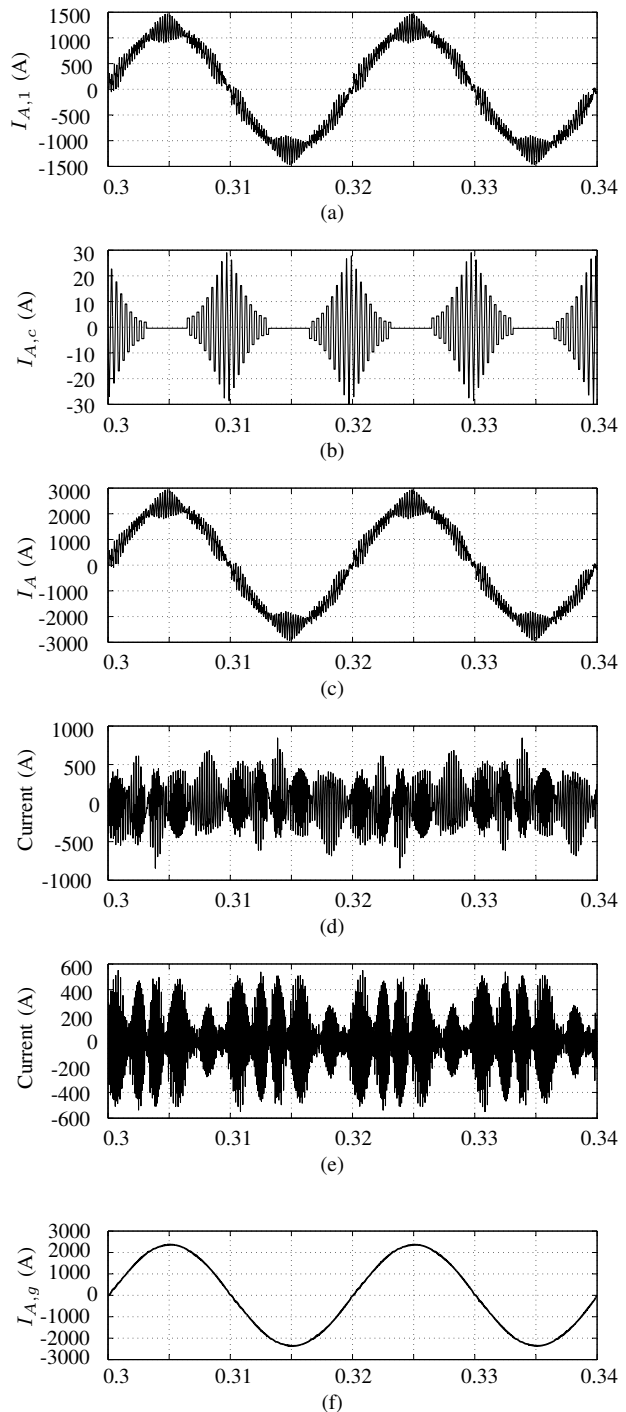

Fig. 21. Simulated currents of phase A with asymmetrical regular sampled DPWM1 with an interleaving angle of $180°$. (a) VSC1: Phase A current, (b) Circulating current, (c) Resultant current, (d) Current in LC trap branch, (e) Current through the C_f, (f) Grid current.

is implemented using TMS320F28346 floating-point digital signal processor.

A 0.6 mH, three phase inductor is used as a converter side inductor. The circulating current filter L_C has a leakage inductance of 0.27 mH. Therefore, the total converter side inductance $L_f = 0.87$ mH (0.019 pu). A three phase, 10 kVA, 1:1 transformer is used. The leakage inductance of this

TABLE V
MAGNITUDE OF THE CHARACTERISTIC HARMONICS WITH THE TRANSFORMER AND WITH EQUIVALENT INDUCTOR

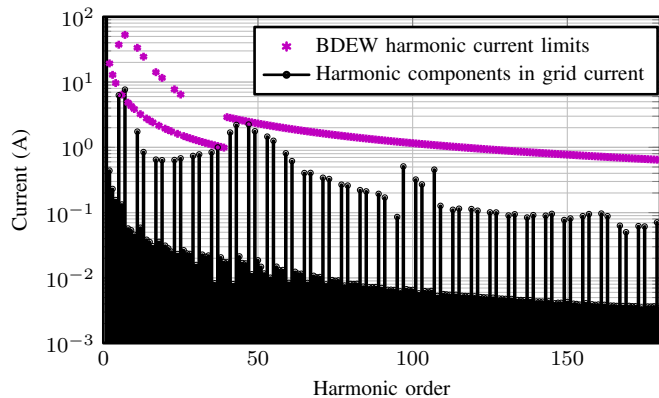| Harmonic	5th	7th	11th	13th	17th	19th	23rd	25th
With transformer	294 mA	310 mA	67 mA	43 mA	20 mA	26 mA	18 mA	19 mA
With eq. inductor	112 mA	77 mA	12 mA	32 mA	20 mA	17 mA	12 mA	18 mA

Fig. 22. Performance verification of the line filter. The harmonic spectrum of the simulated grid current is depicted.

(a)

(b)

Fig. 23. The experimental results. (a) Ch1: VSC1 phase A current ($I_{A,1}$), Ch2: VSC2 phase A current ($I_{A,2}$), Ch3: Circulating current ($I_{A,c}$), Ch4: Resultant current (I_A), (b) Ch1: Current through the LC trap branch, Ch2: Current through the C_f branch, Ch3: Grid current ($I_{A,g}$), Ch4: Grid voltage at PCC.

transformer is measured to be 3.1 mH (0.0675 pu), which is nearly equal to the required value of the 0.07 pu. Therefore, L_g is comprised of the leakage inductance of the transformer only and an additional inductor is avoided.

The experiment was performed at rated conditions with unity power factor operation. Fig. 23, shows the experimental waveforms. The circulating current is effectively suppressed by using CI, as shown in Fig. 23(a). As a result, the effect of the circulating current in the individual VSC currents can be conveniently neglected. Therefore $I_{A,1} \approx I_{A,2}$ and the sum of these two currents (I_A) is also shown in Fig. 23(a). The maximum value of the switch current ripple is 0.4 pu against the design constraint of 0.45 pu.

The current through the LC trap branch and the capacitive branch C_f is shown in Fig. 23(b). The LC trap branch provides low impedance path to the 2nd carrier frequency harmonic and its side bands. Whereas, the capacitive branch C_f sinks the high frequency harmonic components. The injected current and voltage at the PCC are also shown in Fig. 23(b). The measured grid current had a THD of 3.1 % and the magnitude of the individual harmonic component is plotted in Fig. 24. The magnitude of all the harmonic frequency components of the grid current is lower than the specified BDEW harmonic current injection limits. The major harmonics components around the 2nd carrier harmonic are suppressed effectively and the magnitude of these components are also within the prescribed current injection limits. The relative amplitude of the harmonic components in the low frequency range is more in the measured grid current than on the simulated grid current. The even order harmonics are mainly present due to the asymmetrical three limb structure of the inductor L_f and the transformer (L_g). The transformer also draws nonlinear magnetizing current and increases the magnitude of the odd
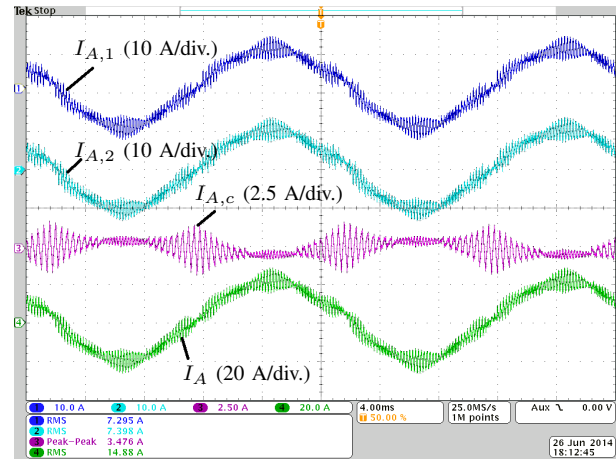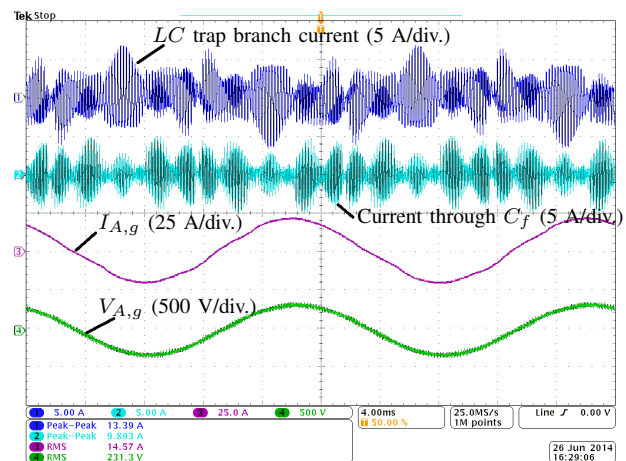
order harmonics as well. To validate the filter performance, the experiment was also performed by replacing the transformer with a 3.1 mH, three limb inductor. The grid impedance is also set to zero. The grid current waveform is shown in Fig. 25 and the measured grid current had a THD of 1.38 %. The magnitude of the low order odd harmonic components present in the grid current is given in Table V and it is compared with the magnitude of the corresponding harmonic components of a grid current with a transformer. The magnitude of the low order harmonic components is significantly smaller with the equivalent inductor than that with the transformer. Therefore, it is concluded that the magnetizing current of the transformer significantly contributes towards the low order odd harmonic
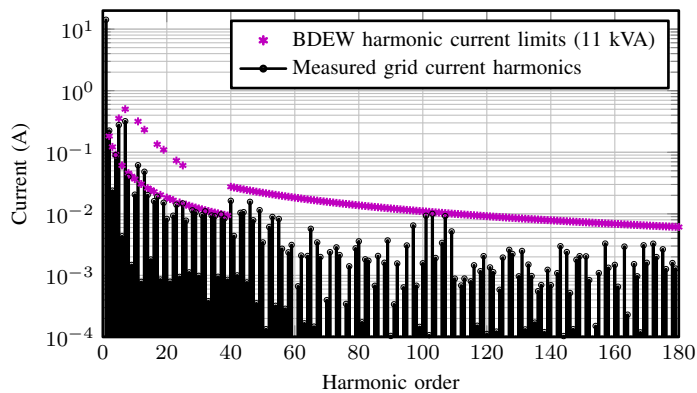
Fig. 24. Performance verification of the line filter of the laboratory prototype.
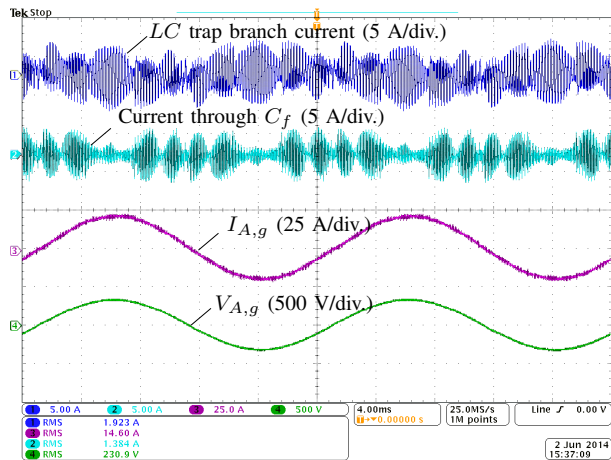

Fig. 25. The experimental results obtained by replacing transformer with equivalent three phase inductor. Ch1: Current through the LC trap branch, Ch2: Current through the C_f branch, Ch3: Grid current ($I_{A,g}$), Ch4: Grid voltage.

components of the grid current.

VI. CONCLUSION

A step-by-step design procedure of the line filter for the high power WECS is presented in this paper. In-depth analysis of the effect of the interleaved carriers on the harmonic performance of the parallel connected VSCs has been made. The closed form analytical harmonic solution for the two parallel interleaved VSCs, modulated by asymmetrical regular sampled DPWM1 scheme, is derived and the reduction in the magnitude of some of the harmonic components is demonstrated. The effect of the interleaved carriers on the switch current ripple is also analyzed. The set of the worst case individual voltage harmonic components in the entire operating range (VVHS) is derived, and it is used to obtain the required value of the filter admittance for each harmonic components. The additional LC trap branch with the conventional LCL filter is used. The characteristics of the proposed line filter is analyzed and the design procedure to select the filter parameters, such that the filter admittance closely matches with the required admittance at all concerned harmonic frequencies is presented. Although the design example presented in the paper considers DPWM1 as the modulation scheme, the proposed filter design

approach can be equally applicable to other PWM schemes as well. The performance of the filter has been tested. The magnitude of the individual harmonic components in the grid current is within the harmonic current injection limits, specified by the BDEW standards.

VII. APPENDIX

Considering the single phase equivalent circuit of the proposed filter, as shown in Fig. 13, the admittance transfer of the filter is given as

$$\frac{I_{x,g}(s)}{V_{x,avg}(s)}\bigg|_{V_g=0} = G\frac{s^3 + A_2s^2 + A_1s + A_0}{s(s^5 + B_4s^4 + B_3s^3 + B_2s^2 + B_1s + B_0)}$$

where

$$G = \left(\frac{1}{L_fL_gC_f}\right)$$

$$A_0 = \frac{1}{L_fC_tC_dR_d}, A_1 = \frac{1}{L_tC_t} + \frac{R_t}{L_tC_dR_d}$$

$$A_2 = \frac{R_t}{L_t} + \frac{1}{C_dR_d}$$

$$B_0 = \frac{L_f+L_g}{L_fL_gL_tC_tC_fC_dR_d}, B_1 = \frac{L_f+L_g}{L_fL_gL_tC_f}\left(\frac{1}{C_t}+\frac{R_t}{C_dR_d}\right),$$

$$B_2 = \frac{L_f+L_g}{L_fL_gC_f}\left(\frac{R_t}{L_t}+\frac{1}{C_dR_d}\right)+\frac{C_f+C_d+C_t}{L_tC_fC_tC_dR_d}$$

$$B_3 = \frac{L_f+L_g}{L_fL_gC_f}+\frac{C_f+C_t}{L_tC_fC_t}+\frac{R_t(C_f+C_d)}{L_fC_fC_dR_d}$$

$$B_4 = \frac{R_t}{L_t}+\frac{C_f+C_d}{C_fC_dR_d}$$

(31)

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