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Hierarchical Coordinated Control of Distributed Generators and Active Power Filters to Enhance Power Quality of Microgrids

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***Abstract*—This paper addresses the coordinated control of distributed generators (DGs) inverters and active power filters (APFs) to compensate voltage harmonics in microgrids. For this, a hierarchical control system is proposed to mitigate voltage harmonic distortion. The hierarchical control structure includes two control levels: primary control and secondary control. Primary control consists of power controllers, selective virtual impedance loops and proportional-resonant (PR) voltage/current controllers. Secondary control manages the compensation of voltage harmonic distortion of sensitive load bus (SLB). Compensation of SLB harmonics by control of DGs may cause excessive voltage harmonics at the terminal of one or more of DGs interface inverters and/or overloading of the inverters. After occurrence of each of these cases, active power filter (APF) participates in harmonic compensation and consequently the compensation efforts of DGs decrease to avoid excessive harmonics or loading of DGs' inverters. Effectiveness of the proposed control scheme is demonstrated through simulation studies.**

***Index Terms*—Active power filter, hierarchical control, microgrid, power quality, selective virtual impedance, voltage harmonic distortion.**

I. Introduction

MICROGRIDS are a collection of distributed generators (DGs), loads and energy storage resources that can act either connected to the main utility grid (grid-connected) or isolated from that (islanded). Usually DGs connect to electric network by power-electronic converters. The output stage of the converter is an inverter. Recently, some control strategies based on interface inverter control have been proposed to compensate power quality problems in microgrid [1-9]. In the scope of present paper, the works related to voltage harmonic compensation in microgrids are reviewed as follows.

In [7] sinusoidal waveform for DG output voltage is obtained by decoupling fundamental and harmonic components of PWM current and providing controllable resistive behavior for them. This strategy (resistance emulation) is also applied in [8], moreover, a droop characteristic is used to control this resistance value according to harmonic reactive power of each unit. Applying a single phase DG as an active power filter (APF) to compensate voltage harmonics by injecting harmonic current is discussed in [9]. The methods suggested in [7]-[9] consider DGs output voltage compensation whereas compensation at the point of common coupling (PCC) or sensitive load bus (SLB) is more important. The works of [5],[6] and [10] address this point.

In [10] an interface inverter control based on voltage control method (VCM) is proposed to compensate PCC voltage through providing proper terminal voltage by a single phase DG. In [5] a voltage harmonic compensation method for PCC based on interface inverter control is proposed that is executable in both islanded and grid-connected microgrids. In this method, harmonic distortion power (HDP) characteristic is used to share power between DGs properly. A selective voltage harmonic compensation based on the rate of voltage harmonic distortion of SLB is proposed in [6]. In this method, compensation effort of each DG is proportional to its rated power.

Despite significant quality improvement of SLB voltage using the approach of [6], output voltages of one or more of DGs may become distorted, moreover, the rated power of interface inverters are not considered in this method. Distortion in output voltage of DGs reduces power quality in proximity of DGs and causes harmful effects on the performance and life of the equipment in those areas. Furthermore, ignoring the rated power of interface inverters may causes technical problems. To cope with these problems, the present paper addresses voltage harmonic compensation of microgrids considering the voltage quality at SLB as well as DGs terminal by proposing a method for control coordination between interface inverters and APFs.

II. Proposed Hierarchical Control Scheme

A hierarchical control structure is proposed which includes two control levels, namely primary and secondary. Primary control consists of droop controller and virtual impedance loop to share fundamental powers and harmonic current among DGs, respectively. In addition, it contains voltage and current controllers. Centralized secondary controller causes reduction in SLB voltage harmonics by sending proper control signals to each DG and makes APF cooperate with DGs for compensation whenever is necessary. Fig. 1 shows the hierarchical control system where "1" and "h" stand for fundamental and h^{th} harmonic component, respectively. It is possible that secondary controller is located far from DGs and SLB; thus, SLB data are sent to this level by low bandwidth communication (LBC) [6]. Compensation references (e.g. C_{dq}^{h}) are generated in secondary control and sent to primary level. In

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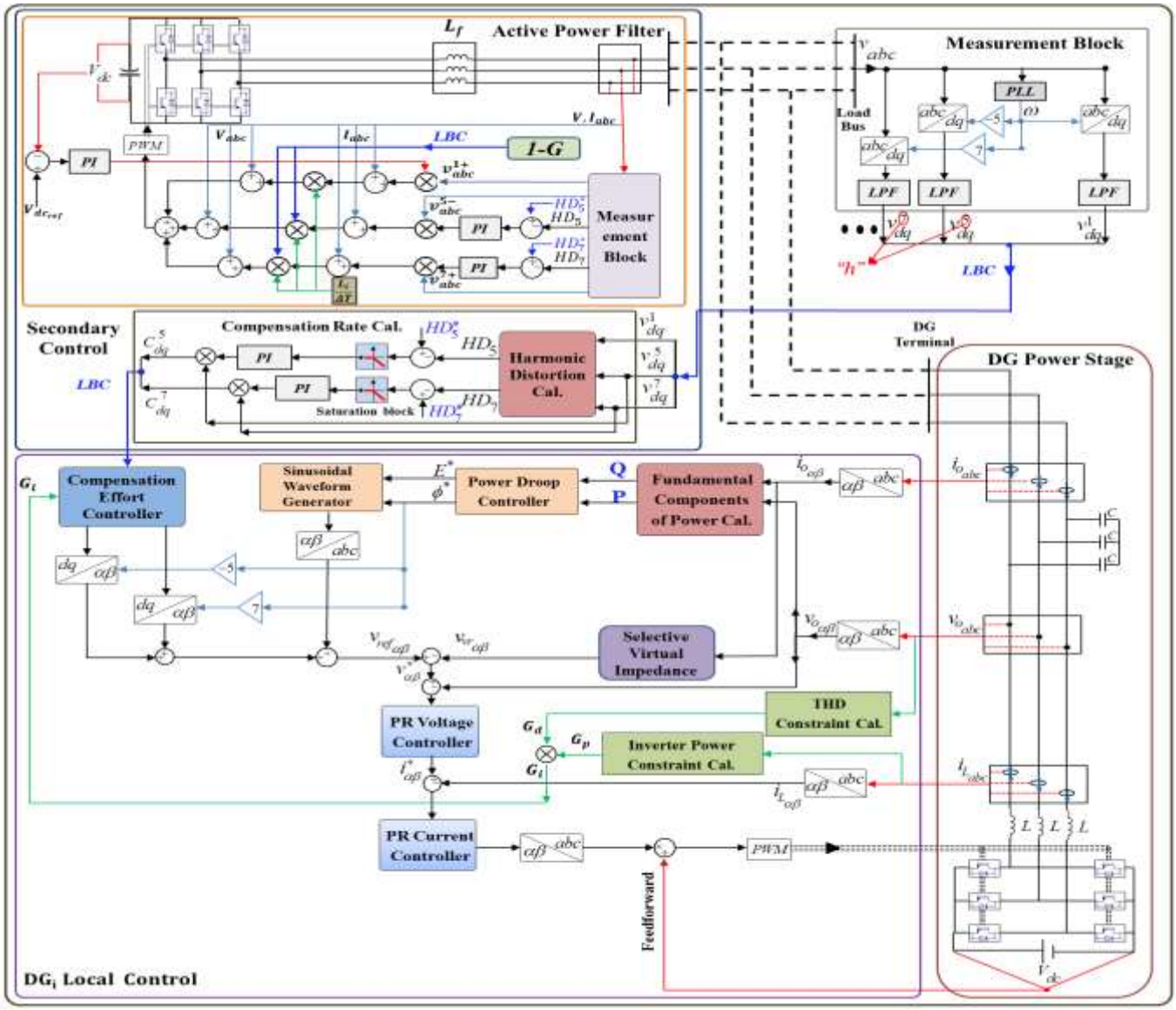


Fig. 1. Block diagram of proposed hierarchical control scheme.

addition, the data concerning the APF stage of secondary control (G) generated in primary control is transferred to this stage by LBC.

A. Primary (Local) Control

Local control contains voltage and current controllers, power droop controller and selective virtual impedance controller. The principle of local control is as follows.

A.1 Selective Virtual Impedance

Fig. 2 illustrates selective virtual impedance [6]. It is worth noting that MSOGI-FLL extraction method [13] is used to extract fundamental and harmonic components of output current.

A.2 Power Droop Controller

To apply power droop controller, it is needed to extract fundamental component of active/reactive power [1], [11]. This controller regulates output active and reactive power in regard to variation of output frequency and voltage by generating suitable reference values for them. More details can be found in [11], [12], and [14].

A.3 Compensation Effort Controller

Fig. 3 shows block diagram of compensation effort controller. As can be seen, at first the needed harmonics are extracted, then h[th] current harmonic distortion is estimated as [6]:

$$HD_I^h = \frac{I_{rms_{o\alpha}}^h}{I_{rms_{o\alpha}}^{1+}} \quad (1)$$

The value obtained for HD_I^h is subtracted from maximum current harmonic distortion of relative component ($HD_{I,max}^h$) to provide a droop scheme [6]. Also, coefficients generated in secondary control (G_j,C_{dq}^h) and DG's rated power coefficient (G_s) are applied to generate final value for compensation effort controller ($C_{dq,j}^h$)(see Figs. 1 and 3).

The way of determining G_j and C_{dq}^h will be explained in following sections, but G_s can be obtained as:

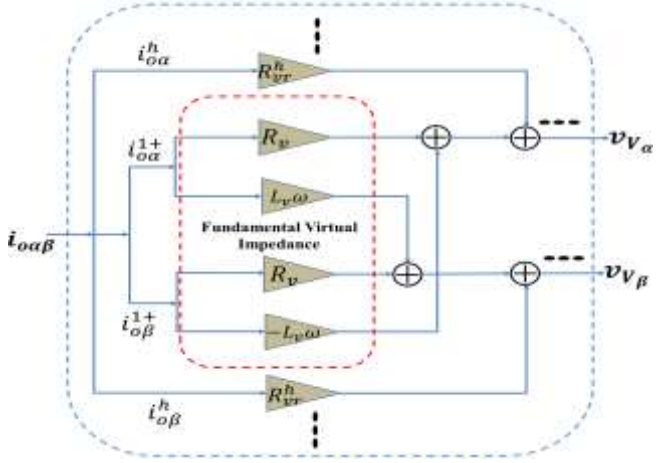


Fig. 2. Block diagram of selective virtual impedance.

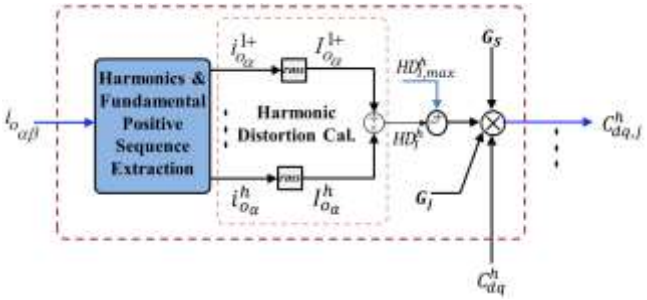


Fig. 3. Block diagram of compensation effort controller for DG_j.

$$G_S = \frac{S_{0,j}}{\sum_{i=1}^{n} S_{0,j}} \tag{2}$$

where $S_{0,j}$ is nominal power of j^{th} DG and *n* is the number of DGs.

A.4 Voltage and Current Controllers

Voltage and current controllers provide proper signals for pulse with modulation (PWM) block to generate output voltage of inverters. Proportional-resonant (PR) controllers are used for this purpose. The way of designing these controllers is explained in [1] and [14].

B. Secondary (Central) Control

Secondary control is designed for improving power quality of SLB. Therefore essential data of SLB, gained by "Measurement Block", are sent to this level by LBC (Fig. 1) To tune required compensation rate of SLB and reduce voltage harmonic distortion to its reference value (HD_h^*), it is necessary to calculate voltage harmonic distortion (HD_h) of SLB. The difference value between HD_h and HD_h^* is sent to a proportional-integrator (PI) controller. The output of PI controller is multiplied by relative harmonic voltage of SLB (v_{dq}^h) to generate compensation reference (C_{dq}^h) which is sent to local controller (Fig. 1). More details can be found in [6].

III. Coordinated Control of Interface Inverters and Active Power Filter

Improving power quality of SLB by proper control of interface inverters is achieved at the price of losing power quality in DGs' buses [6]. In order to solve this problem, it is proposed in this paper to add another control loop for involving APF in harmonic compensation. For the sake of simplicity, the proposed approach is explained with considering an APF, but it can be easily expanded to several APFs.

A. Active Power Filter Control

The structure and control scheme of APF applied in the present paper is based on [15]. The APF structure can be seen in Fig. 1. APF compensates the harmonics by providing proper conductance in a selective way. Following equation illustrates the performance of APF:

$$i_{abc}^* = \sum_h G_h^* \cdot \tilde{E}_{abc_h} \tag{3}$$

where *h* is the order of harmonic and G_h^* is tuned gain that acts as a conductance. G_h^* is multiplied by relative harmonic voltage ($\tilde{E}_{abc_h}$) to compensate corresponding voltage harmonic at the bus of APF installation. The gain is determined automatically based on voltage harmonic distortion. In the case that voltage harmonic distortion is more than its reference value, a PI controller is acting to determine G_h^*. Finally, according to the reference current (i_{abc}^*) and voltage/current measured at the place of APF, current regulator specifies voltage reference (v_{abc}^*) of APF based on following function:

$$v_{abc}^* = E_{abc} - \frac{L_i}{\Delta T}(i_{abc}^* - i_{abc}) \tag{4}$$

where L_i is APF's inductor and ΔT is sampling period [15].

B. Coordination Process

Coordination process between APF and interface inverters is based on total voltage harmonic distortion (THD) of DGs buses and interface inverters nominal power constraint. Since compensation of SLB by interface inverters may cause exceeding THD maximum allowed value in the output voltage of DGs or violating inverters maximum power, APF can help interface inverters by compensating SLB partially. *G* in Fig. 1 represents decrease of compensation efforts of interface inverters without exceeding the constraints explained in detail in the next subsection. Fig. 4 shows the coordination process. In this figure, the coefficients corresponding THD and inverter power constraints are shown by G_{di} and G_{pi} in local control of i^{th} DG, respectively. These two values are multiplied to determine a G_i which affects the compensation effort of i^{th} DG. Each G_i calculated in local control of each DG is sent to APF stage of secondary control by LBC.

Then, these values are summed up and divided by *n* (number of DGs) to generate a number between zero and one (*G*) which determines the ability of all inverters for compensating SLB. Therefore, in case of complete compensation of SLB harmonics by DGs, *G* will be equal to one. In other words, *G* determines the duty of all inverters in compensation considering both constraints and *1-G* is the compensation amount that should carry out by APF.

It is obvious that in the case of having more than one APF, this compensation effort should be shared among APFs according to the rated power of them. Compensation rate of APF is applied through multiplying by G_h^*.

C. Constraints

Fig. 5 shows the calculation process of THD constraint coefficient.To apply THD constraint, at first THD of output DG voltage is measured and then compared with its maximum allowable value, if the measured value exceeds the maximum value, an integrator controller tries to reduce THD of output voltage by reducing DG compensation effort through decreasing G_d. Moreover, a limiter is used to limit G_d between minimum and maximum values of compensation rate.

Interface inverter nominal power constraint is determined based on inverter output current. To apply this constraint, an strategy similar to THD constraint is used. Amplitude of inverter output current is calculated by the following equation:

$$I_{dq} = \sqrt{[(I_d^1)^2 + (I_q^1)^2] + [(I_d^{OS})^2 + (I_q^{OS})^2]} \qquad (5)$$

IV. Simulation Results

Fig. 6 shows the test system considered for simulation. The islanded microgrid consists of two DGs, an APF that is connected to SLB also a linear load and a nonlinear load (modeled by a diode rectifier) that are connected to SLB. Simulation is performed by *MATLAB/Simulink*. Nominal voltage and frequency of microgrid are 230 V (rms value of phase voltage) and 50 Hz, respectively. Switching frequency of DGs and APF inverters is 10 KHz. Inductor and capacitor values of APF are $L = 35\,mH$ and $C = 4000\,\mu F$, respectively. Also, sampling period in equation (4) is $\Delta T = 1.25 \times 10^{-4}$. It is worth noting that the maximum allowable value for voltage THD is 5% according to *IEEE519 Standard*[5]. Voltage compensation is done for SLB voltage 5^{th} and 7^{th} harmonics (main harmonic orders) with the reference value of 1%. The test system parameters are listed in Table I. Table II shows the coordinated control data. Note that the rated power of DG_1 inverter is considered to be twice of that of DG_2 (and this fact is reflected in maximum current values). Other parameters of primary and secondary control can be found in [6].

To examine the proposed control scheme, simulation process is divided to four steps:

- First Step ($0 < t < 2s$)
  Virtual impedance loops in fundamental component is active.
- Second Step ($2 < t < 4s$)
  Selective virtual impedance is added to the previous step, so primary control is completely active.
- Third Step ($4 < t < 7s$)
  A part of secondary control initiates and voltage compensation of SLB by interface inverters happens.

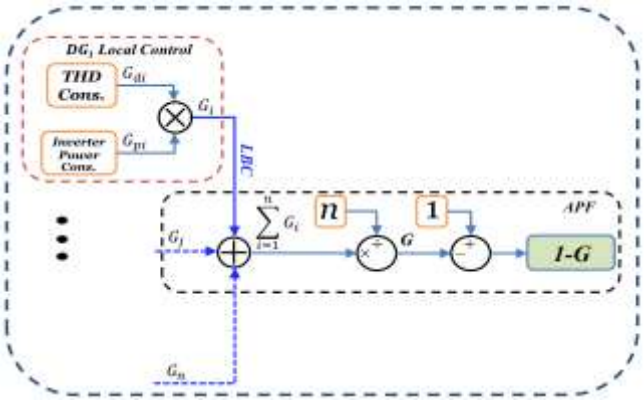


Fig. 4. Block diagram of coordination process.

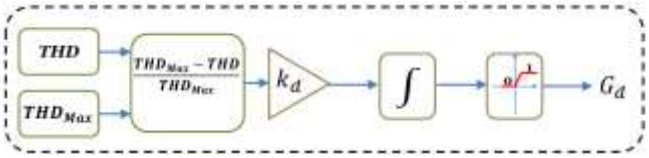


Fig. 5. Block diagram of THD constraint

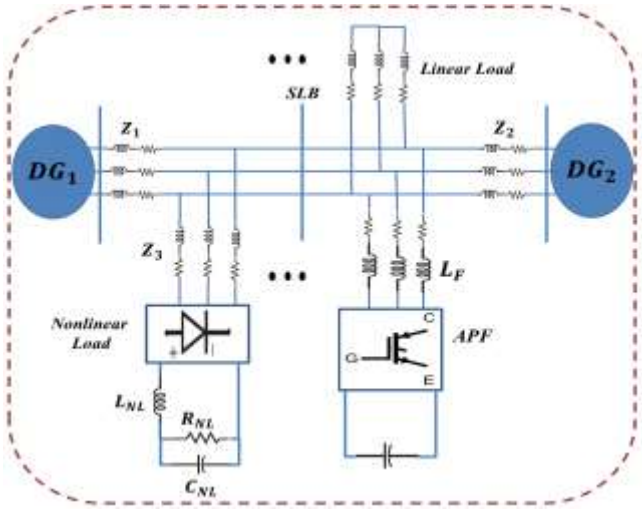


Fig. 6. Test system

- Fourth Step ($7 < t < 10s$)
  APF is added to secondary control and cooperation between interface inverters and APF to compensate the voltage of SLB occurs.

Note that droop controllers and voltage/current controllers are active during all four steps.

Table III shows output voltage of DG_1 and DG_2 and the voltage of SLB in all four steps. According to the table output voltage of DGs are completely sinusoidal in the first step, it demonstrates that droop controllers, virtual impedance and voltage/current controllers are tuned accurately. However, voltage of SLB is distorted due to line impedances. Since selective virtual impedance loop is added to the primary control in the second step, harmonic current sharing occurs at price of increase in voltage distortion of DGs buses and SLB. In the third step, secondary control initiates and it can be seen that voltage of SLB is improved significantly but output voltage of $DG_1$is distorted severely. However, in step four that coordinated

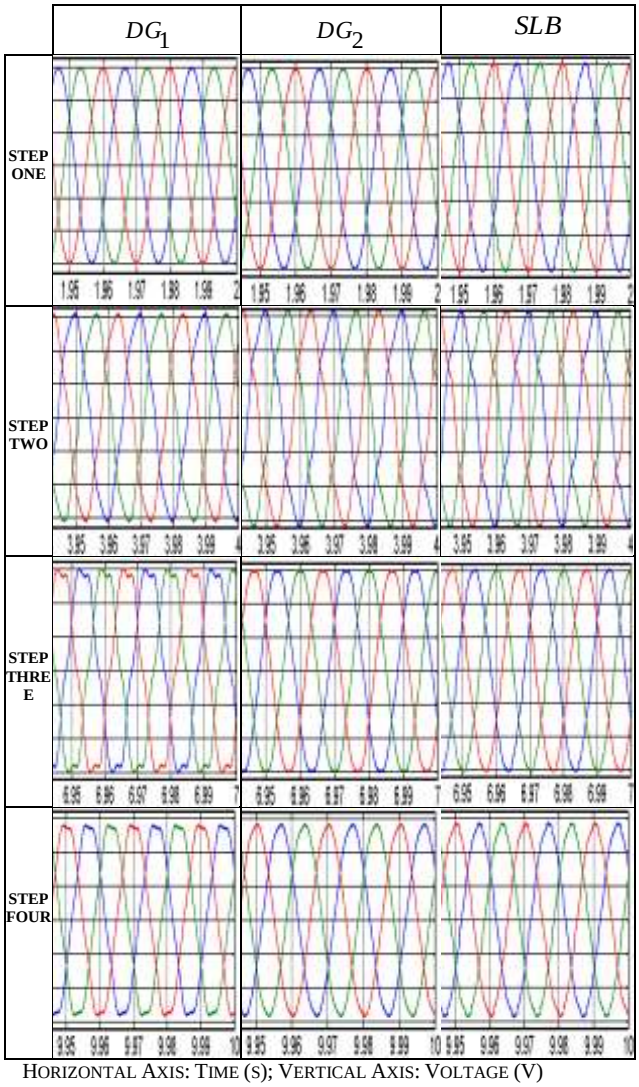
TABLE I
TEST SYSTEM PARAMETERS

Distribution Lines			Nonlinear Load			Linear Load
Z_1 (Ω-mH)	Z_2 (Ω-mH)	Z_3 (Ω-mH)	C_{NL} (μF)	R_{NL} (Ω)	L_{NL} (mH)	Z_L (Ω-mH)
0.2-3.6	0.1-1.8	0.2-3.2	235	30	0.084	50-20

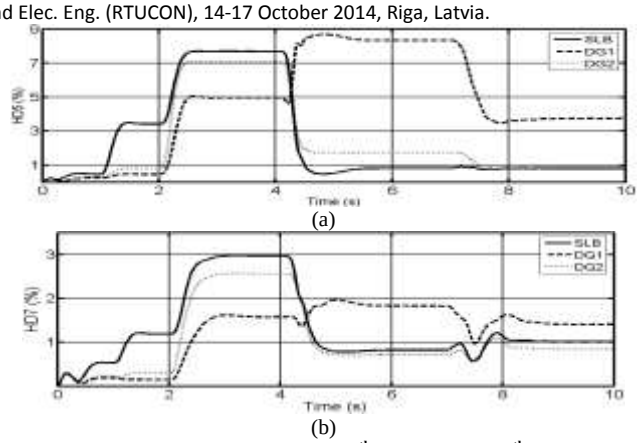
TABLE II
COORDINATED CONTROL AND APF PAEAMETERS

APF Capacitor PI Controller			
K_p		K_i	
0.5		0.05	
APF Harmonic PI Controller			
5th Harmonic		7th Harmonic	
K_p	K_i	K_p	K_i
18	250	8	100
Constraints (Integrator Controller)			
Interface Inverters Constraint		THD Constraint	
K_p		K_d	
15		1.5	
Maximum Inverters Current in dq Framework (A)			
DG_1		DG_2	
18		9	

TABLE III
VOLTAGE WAVEFORM AT DIFFERENT SIMULATION STEPS.



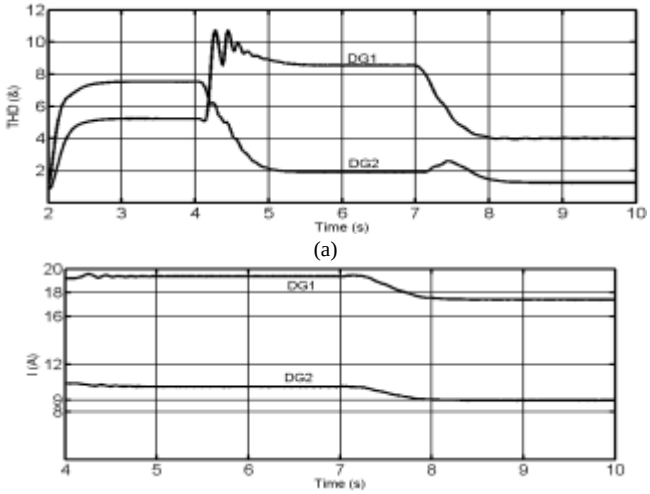
HORIZONTAL AXIS: TIME (S); VERTICAL AXIS: VOLTAGE (V)



(a)

(b)

Fig. 7. Voltage harmonic distortion. (a) **5th** Harmonic, (b) **7th** Harmonic.



(a)

(b)

Fig. 8. Constraints. (a) THD constraint of output DGs voltage. (b) Inverters nominal power constraint.

control initiates and APF undertakes a part of compensation, output voltage of DG_1 is improved.

Fig. 7 illustrates the percentage of 5^{th} and 7^{th} voltage harmonic distortion of DGs buses and SLB. According to the figure, in the first step voltage harmonic distortions of DGs are very small but this parameter is high in SLB due to voltage drop occurred on line impedances. The percentage of voltage harmonic distortion of all buses increases in the second step because selective virtual impedance causes voltage harmonics increase to share harmonic current. In the third step, it is shown that voltage harmonic distortion of DG_1 increases significantly whereas this parameter decreases in DG_2. However, voltage harmonic distortion of SLB is decreased to the reference value in this step. In step four that APF helps DGs to compensate SLB harmonics, voltage harmonic distortion of DG_1 is mitigated significantly while voltage harmonic distortion of SLB is unchanged; it shows the good performance of APF in undertaking a part of compensation instead of inverters.

The curves related to constraints are depicted in Fig. 8 and show that violation from THD constraint of output DGs voltage occurs only for DG_1 and violation from inverters nominal power takes place for both inverters in the third step. However, all violations are eliminated in step four by participating APF in compensation. Fig. 9 shows the

compensation rate of each DG considering both constraints. Based on Fig. 9(b), compensation rate for DG_2 is decreased just for the violation occurred in inverter power constraint (violation in THD constraint is not occurred in DG_2 output voltage, Fig. 8(b)). Fig. 10 shows compensation rate of both DGs and APF. It can be seen that compensation rate in step three is 100% for both DGs but it is reduced to nearly 55% in step four by undertaking 45% of compensation by APF.

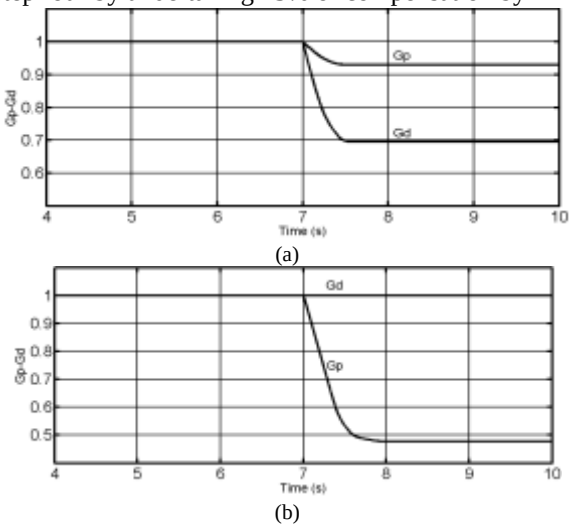


Fig. 9. Compensation rate by DGs in regard to constraints. (a) DG_1. (b) DG_2.

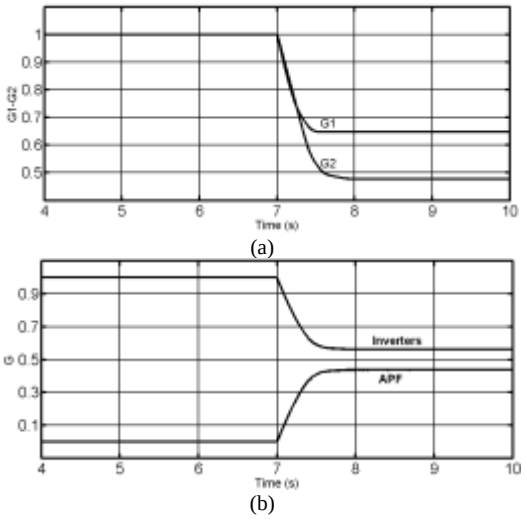


Fig. 10. Compensation rate of DGs and APF. (a) DGs. (b) DGs and APF.

V. CONCLUSION

Proposed hierarchical control scheme to enhance power quality in main buses of islanded microgrid contains two levels. Primary control includes droop controller and selective virtual impedance. Voltage compensation of SLB in secondary control is performed by DGs interface inverters. During compensation by the inverters, if THD of DGs buses exceeds its maximum value and/or interface inverters have to tolerate overload, APF cooperates in compensation in coordination with interface inverters. Therefore, acceptable power quality for SLB and DGs buses of microgrid is provided simultaneously by using the proposed hierarchical control system.

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