A Temperature-Dependent Thermal Model of IGBT Modules Suitable for Circuit-Level Simulations

Wu, Rui; Wang, Huai; Ma, Ke; Ghimire, Pramod; Iannuzzo, Francesco; Blaabjerg, Frede

Published in:
Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE)

DOI (link to publication from Publisher):
10.1109/ECCE.2014.6953793

Publication date:
2014

Document Version
Early version, also known as pre-print

A Temperature-dependent Thermal Model of IGBT Modules Suitable for Circuit-level Simulations

Rui Wu, *Student Member*, Huai Wang, *Member*, *IEEE*, Ke Ma, *Member*, *IEEE*, Pramod Ghimire, *Student Member*, Francesco Iannuzzo, *Senior Member*, and Frede Blaabjerg, *Fellow*, *IEEE*
Centre of Reliable Power Electronics (CORPE), Department of Energy Technology
Aalborg University, Pontoppidanstraede 101, 9220
Aalborg, Denmark
rwu@et.aau.dk, hwa@et.aau.dk, kema@et.aau.dk, pgh@et.aau.dk, fia@et.aau.dk, fbl@et.aau.dk.

***Abstract*— A basic challenge in the IGBT transient simulation study is to obtain realistic junction temperature, which demands not only accurate electrical simulation but also precise thermal impedance. This paper proposed a novel thermal impedance model considering of local temperature effects through Finite Element Method (FEM) simulation. The proposed method is applied to a case study of 1700 V/1000 A IGBT module. Furthermore, a testing setup the studied IGBT open module and an ultra-fast infrared (IR) camera has been constructed to validate the proposed model.**

I. INTRODUCTION

When design modern power electronic systems, it is critical to improve whole system performance meanwhile fulfilling the robustness and reliability requirements [1]. One of the critical robustness requirements for IGBT converters design is how to monitor power semiconductor's junction temperature precisely and then control it at adequate level. This is because junction temperature is a key parameter for predicting and preventing IGBT's failure. For instance, a critical high junction temperature is usually connected with the phenomena of current constriction, thermal runaway, which are responsible for failures of IGBT modules during heavy loads and short-circuits. High junction temperature is also connected to various initial failure-triggering factors for final destruction (e.g. dynamic voltage breakdown, gate driver failure) [2].

In long-term real-time operation, it is prevail to use saturation voltage $V_{ce,sat}$ to estimate virtual junction temperature. However, it is still a challenge to measure transient junction temperature during short-circuits or overloads, which may cause IGBT overstress failure [3]. Meanwhile, simulation techniques have provided immense possibilities in researching and optimized designing of thermal management and junction temperature control in power electronic systems [4]. A precise thermal impedance model is essentially required to accurately estimate the junction temperature of IGBT modules to prevent potential failures with high confidence levels in circuit design.

The Cauer and Foster thermal impedance models have been widely used in power electronic circuit simulations. The former model is correlated to the physical property and packaging structure of IGBT modules and the latter is an equivalent one fitted from measured or simulated results [5]. These models are simple, time efficient, and can be easily integrated in various circuit simulators (e.g. PLECS, Spice, Saber) [6]-[8]. However, there is still a deficiency for current Cauer and Foster models. The present models are applying temperature-invariant parameters, which are not realistic due to most material's physical properties are temperature dependent. This shortage becomes more fatal especially in case of wide temperature range (from room temperature to hundreds of degree) in IGBT transient operations (μs or ms - level), typical situation during short-circuits and overloads.

It has been proved that temperature influences strongly to the physical parameters of the semiconductor components in prior-art research. The correlation of thermal resistance and ambient temperature has been studied in [9]-[12] for the semiconductor devices. However, the studies on thermal resistance of low power devices (e.g. LED [9], transistors [10]) may not be applicable to high power IGBTs due to the dramatic difference in material and geometry. IGBT thermal resistance dependence on power loss is studied and proved by experiments in [11], whereas it is difficult to apply the results in circuit simulations due to a lack of quantitative conclusion. A case study of dynamic thermal behavior is implemented with IGBT modules with sintered nano-silver, which evidences that the Finite-Element Method (FEM) is suitable for accurate transient thermal impedance study [12].

On the foundation of the above study, this paper proposes a novel thermal model for IGBT junction temperature simulation. It is based on FEM thermal simulations with the consideration of temperature-dependent physical parameters. Then an updated Cauer thermal model with varying thermal parameters is obtained, which can be applied to IGBT circuit-level simulations.

Furthermore, to verify the proposed thermal impedance model, a test setup with the 1700 V/1000 A IGBT open module has been constructed, and a +/- 1% accuracy temperature map corroborating model predictions has been obtained by an advanced infrared (IR) camera.

This paper is organized as follows: Section II describes the detailed principles of thermal impedance analysis, including traditional thermal modeling methods, FEM analysis theory, as well as temperature effects. Section III illustrates the procedures of the proposed approach and how to apply it in circuit-level simulations. Section IV applies the proposal method to study the transient thermal impedance under different ambient temperature with a 1700 V IGBT module case study, which demonstrates the validity of the method. Section V evidences experimental validation of the model proposed in Section IV with an advanced infrared camera. Section VI offers concluding remarks.

II. PRINCIPLES OF THERMAL IMPEDANCE THEORY

A. Thermal Impedance Theory

The basic principle of the thermal impedance network is to initially transform the thermal parameters into the corresponding electrical parameters, as shown in Table I. Afterwards the corresponding equivalent network can be solved by applying advanced electrical network simulation tools (e.g. PSpice, Saber, PLECS). Finally, the results are transformed back into the thermal parameters. Similarly to the electrical time constant, the product of resistance and capacity $\tau=R\cdot C$, the corresponding thermal time constant is defined as $\tau_{th}=R_{th}\cdot C_{th}$.

Thermal resistance between two positions is defined, similarly to Ohm's law, as the temperature difference divided by the heat flow:

$$R_{th}=\frac{\Delta T}{P} \tag{1}$$

1) Cauer Model.

Cauer thermal impedance model is correlated to the physical property. Its equivalent circuit for modeling heat conduction properties is as shown in Fig. 1.

Cauer thermal model is based on object's geometry and properties. As with the electrical parameters, the thermal resistance and capacitance are related to the thermal conductivity and pressure specific heat capacity,

TABLE I. CORRESPONDENCE BETWEEN ELECTRICAL AND THERMAL PARAMETERS

Electrical Parameters	Thermal Parameters
Voltage, U (V)	Temperature difference, ΔT (K)
Current, I (A)	Heat flow, P (W)
Resistance, R (V/A)	Thermal resistance, R_{th} (K/W)
Capacitance, C (As/V)	Thermal capacitance, C_{th} (Ws/K)

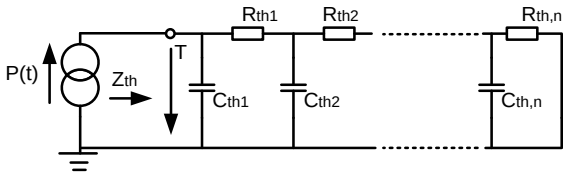

Fig. 1. Cauer thermal model.

respectively. Thermal resistance R_{th} and thermal capacitance C_{th} can be calculated respectively, through:

$$R_{th}=\frac{1}{k}\cdot\frac{d}{A} \tag{2}$$

$$C_{th}=c_p\cdot\rho\cdot d\cdot A \tag{3}$$

Where d is the material thickness, A is the cross-sectional area, k is the thermal conductivity, ρ is the density, and c_p is the pressure specific heat capacity.

For IGBT module, the individual RC elements can be assigned to the individual layers, for example chip, chip solder, substrate, substrate solder and baseplate. Therefore, each layer's temperature can be gained by Cauer model.

2) Foster Model.

Another thermal model is Foster model, which describes the thermal behavior as "black box".

The individual RC elements represent the terms of a partial fractional division of the thermal transfer function of the system, whereby the order of the individual terms is arbitrary. The partial fractional representation directly shows the uniqueness of this network which is given by the fact that it has a mathematically simple, closed-form specifiable step response:

$$Z_{th}=\sum_{m=1}^{n}R_m\left(1-e^{-\frac{t}{R_mC_m}}\right) \tag{4}$$

In this way, it can determine the values of the equivalent elements based on calculation of temperature curves for simple power dissipation profiles. It is the reason of the wide application and popularity of this equivalent network. There is no relationship between the physical nodes and the internal structure of this network.

The Foster model can be extracted according to IEC standard 60747-9 6.3.13 [13]. Thus, it is commonly used by the manufacturers, and can be found in datasheets.

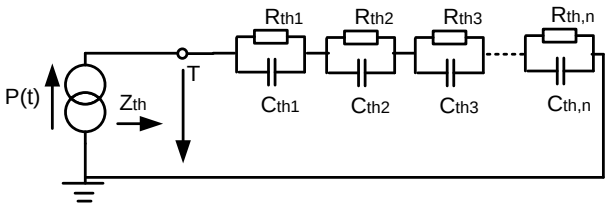

Fig. 2. Structure of Foster thermal model.

3) FEM Model.

The other common thermal analysis model is FEM model. The geometric data of the package is entered into the FEM model to calculate the thermal impedance. In this way, the time-consuming measurements in the upper two models can be avoided.

The basic principle is to apply FEM to solve the diffusion-convection-reaction problem. Defined by Fourier's law, the heat flux in a given direction is from the thermal conductivity and the temperature gradient [14]:

$$q_i'' = k_i \nabla_i T(\vec{r}, t) \tag{5}$$

In Eq. (5), q_i'' is the absorption/production coefficient, k_i is thermal conductivity, T is temperature, $\vec{r}$ is the location, t is time.

By regarding the situation as a flow problem and utilizing conservation of energy the diffusion-convection-reaction equation can be derived:

$$\rho c_p \frac{\partial T}{\partial t} = \nabla \cdot \left[\vec{k} \nabla T(\vec{r}, t) \right] + H \tag{6}$$

where ρ is the density, c_p is the heat capacity at constant pressure.

The first term of Eq. (6) is the transient properties of the temperature. The first term on the right is the steady state heat conduction. The final term is the change in stored internal energy. Solving Eq. (6) is ideal for a finite element approach which can be based on the ANSYS/Icepak [15] or COMSOL [16].

With solving the Eq. (6), the temperatures of the individual components (chip, solder, and baseplate) can be obtained. What's more, the temperatures can be viewed individually or in combination.

FEM simulation provides accurate temperature estimation, while at the expense of increased simulation time. This is very critical to circuit level simulation. Therefore, it could be a promising approach to extract a simplified Cauer model for circuit-level simulation based on FEM simulations.

B. Temperature Effects on Thermal Parameters

At present, temperature effects on thermal parameters are not considered in thermal models usually. However, basically all material's properties are temperature related.

Although variation of the density in power devices relevant working temperature range (from 25 ℃ to about 200 ℃) is limited, thermal parameters are dramatically dependent on temperature.

The common used materials for IGBT modules are Silicon (Si), Aluminium (Al) and Copper (Cu). The thermal conductivity, heat capacity and density information of these typical materials used in the power module at 25 ℃ is listed in Table II.

TABLE II. IGBT MODULE MATERIAL PROPERTIES AT 25 ℃ [14].

Material	Aluminum	Silicon	Solder	Copper
Thermal Conductivity (W/m-K)	237	148	57	401
Heat Capacity (J/Kg-K)	897	705	220	385
Density (kg/m^3)	2700	2329	7500	8960

TABLE III. MATERIALS THERMAL PROPERTIES AT DIFFERENT TEMPERATURE [14].

Temperature		25 ℃	75 ℃	125 ℃	225 ℃	325 ℃
Si	Thermal Conductivity (W/m-K)	148	119	98.9	76.2	61.9
	Heat Capacity (J/Kg-K)	705	757.7	788.3	830.7	859.9
Al	Thermal Conductivity (W/m-K)	237	240	240	236	231
	Heat Capacity (J/Kg-K)	897	930.6	955.5	994.8	1034
Cu	Thermal Conductivity (W/m-K)	401	396	393	386	379
	Heat Capacity (J/Kg-K)	385	392.6	398.6	407.7	416.7

Table III reports the detailed information for thermal conductivity and specific heat of the materials (Si, Al, Cu) [14], [17]-[18]. The temperature effects on the thermal parameters of Si, Al, and Cu are plotted in Fig. 3. From Table III and Fig. 3, it can be seen that the thermal conductivity of silicon decreases strongly with an increasing temperature; the exact opposite is the case with the pressure specific heat capacity. According to the handbook, the silicon thermal conductivity around 250 ℃ is only half of the value around 25 ℃ [17]. Based on this, it is clear that the power module thermal behavior depends directly on the local temperature [18].

This point is very critical for overloads and short-circuits analysis, where the chip temperature rises dramatically (several hundreds of ℃), even if for limited time duration (in the range of several milliseconds). Therefore, this nonlinear temperature behavior should also been included in the FEM model to improve the simulation accuracy.

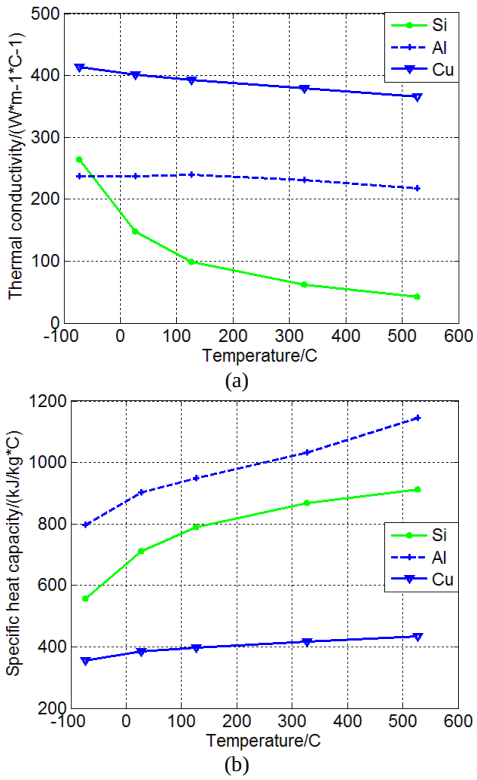

Fig. 3. Temperature effects on material's thermal properties (a). Thermal conductivity, (b). Specific heat capacity of Si, Al, Cu.

III. Proposed Novel Thermal Impedance Model

Based on the analysis in Section II, an updated Cauer model based on FEM model with temperature effects is promising for the circuit-level thermal simulations. With temperature-dependent thermal parameters, it can obtain a more accurate junction temperature.

At first, a detailed model should be constructed in FEM software, which should include the geometry and material information. The information in Table II and III, is also included, as illustrated in last section.

Second step is to perform transient thermal impedance simulations at different ambient temperature and power loss levels. After that, lumped thermal impedance network would be extracted from the FEM results. Finally, the obtained thermal impedance values will be integrated into the updated Cauer model.

In the updated Cauer thermal network, Z_{th}(chip) is related to local temperature (e.g. power loss $P_{loss}(t)$ and ambient temperature T_a), as shown in Fig. 4. The function parameters are obtained by aforementioned FEM simulations. The detailed procedures are illustrated in the case study in section IV.

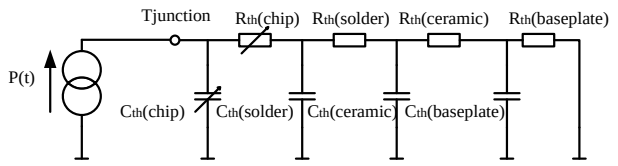

Fig. 4. The proposal updated Cauer thermal model with temperature-dependent thermal parameters.

IV. A Study Case of the Proposed Model

A. Information of the Studied IGBT Module

In order to well illustrate the proposal thermal model, a case study of a 1700 V/1000 A commercial IGBT module is given below.

The main specifications of the IGBT module are shown in Table IV. The maximum operation temperature is 150 ℃.

The module's internal structure is as follows: the chips are soldered on a standard DCB layer, which consists of a ceramic layer (Al_2O_3) and two Cu layers. DCB is further soldered to a Cu baseplate, and the detailed cross section is as shown in Fig. 5.

The internal structure of the power module is shown in Fig. 6. There are six identical sections connected in parallel inside the IGBT module. Each section has two IGBT chips and two freewheeling diode chips, which are configured as a half-bridge. Ten Al bond-wires connect each IGBT chip emitter and the freewheeling diode chip anode.

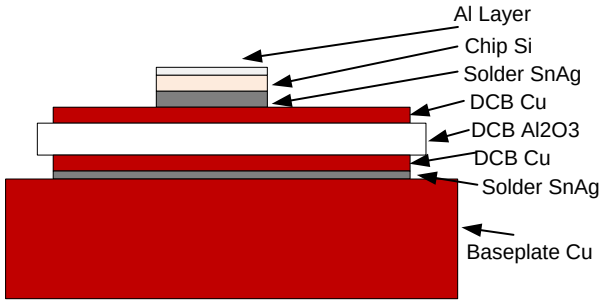

Fig. 5. Schematic cross-section of the multilayer in a typical IGBT power module.

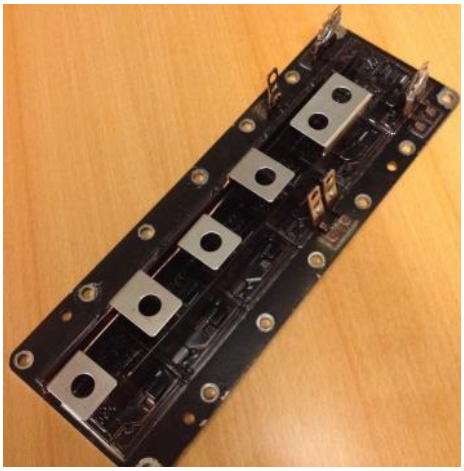

Fig. 6. Geometry of the 1700 V/1000 A IGBT power module with six sections in parallel.

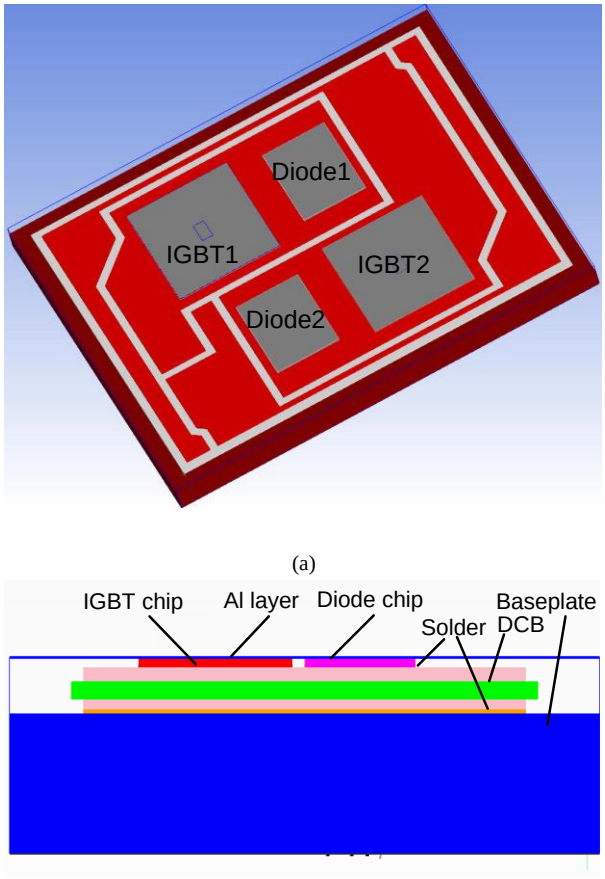

Fig. 7. IGBT model in Icepak (a). Geometry of one section of IGBT power module in Icepak, (b) details of the cross section on the vertical plane.

B. *IGBT Model in Icepak*

FEM thermal analysis is conducting in the ANSYS/Icepak, the detailed model is illustrated as follows:

TABLE IV. MAIN SPECIFICATIONS OF THE IGBT MODULE UNDER SIMULATIONS.

Specifications	Value
Collector-emitter voltage V_{CES}	1700 V
Continuous DC collector current I_{Cnom}	1000 A
Total power dissipation	6.25 kW
Temperature under switching conditions	-40 ℃ ~ 150 ℃
OperationTemperatureT_{vjop}	150 ℃
Rated short-circuit current I_{SC}	4 kA
Gate-emitter maximum voltage V_{GES}	+/- 20V
Internal gate resistance	4 Ω
Number of parallel sections	6

1) IGBT Module Model.

On the basis of information from manufacturer and the cross-section, one IGBT section model is constructed in Icepak. The model geometry in Icepak is shown in Fig. 7 (a). It contains two IGBT chips and two freewheeling diode chips.

The cut plane information of the Icepak model is shown in Fig. 7 (b). It contains Al top layer, IGBT trench gate layer, IGBT body layer, solder, DCB and baseplate. Power source is located in the IGBT body layer. 543,000 nodes are defined in Icepak model. The thermal conductivity and heat capacity information of the materials are as shown in Table III and Fig. 3.

2) IGBT Chip Model.

It is prevail to use trench-gate structure in modern IGBT devices. Because trench-gate structure can reduce on-state voltage drop comparing with a planar-gate IGBT under the same blocking voltage capability, especially for devices with high switching speed [19].

The gate region is formed after the diffusion of the P-base and N+ emitter regions. The gate oxide is formed on the surface of the trench followed by the deposition of poly-silicon as the gate electrode. The poly-silicon is planarized to recess the gate electrode slightly below the silicon surface. On the top of emitter, there is a very thin Al metallization layer (several μm).

In order to model the trench-gate structure, three layers are modeled in Icepak, as shown in Fig. 8. From top to bottom, there are Al metallization layer, gate layer and body layer. Individual thermal parameters are defined for the layers independently. The power source which generates power loss is located near the top of the body layer.

During the thermal simulation, heat is generated inside the IGBT body layer and then spreading both the up and down directions. Meanwhile, temperatures of each layer is monitored and extracted.

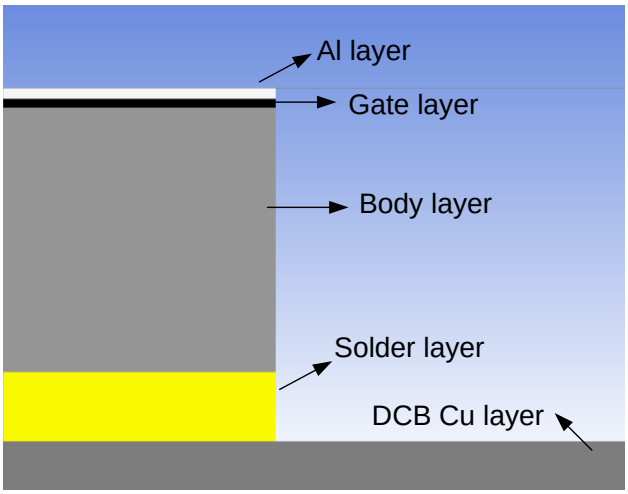

Fig. 8. IGBT chip model in Icepak.

TABLE V. IGBT THERMAL IMPEDANCE OBTAINED BY SIMULATIONS UNDER DIFFERENT AMBIANT TEMPERATURES.

Ta	25 ℃	50 ℃	75 ℃	125 ℃	150 ℃
$R_{th(chip)}$ (K/W)	9×10^{-3}	10×10^{-3}	11×10^{-3}	13×10^{-3}	14×10^{-3}
$C_{th(chip)}$ (J/K)	0.122	0.133	0.143	0.164	0.177
$R_{th(DCB)}$ (K/W)	0.085	0.085	0.085	0.086	0.087
$C_{th(DCB)}$ (J/K)	0.433	0.437	0.447	0.457	0.46
$R_{th(baseplate)}$ (K/W)	0.032	0.032	0.032	0.032	0.032
$C_{th(baseplate)}$ (J/K)	2.81	2.81	2.81	2.85	2.88

C. Simulation Results

In order to simulate the thermal impedance, the IGBT power module is heated with a constant power until all temperatures are stable. Then the power is removed, and temperatures of each layer in Fig. 7 are monitored and recorded. Thermal impedance is calculated based on the temperatures.

In order to study the temperature effects, FEM thermal simulations are implemented at different ambient temperatures (T_a) at given power loss (P_{loss}). Simulation is conducted under ambient temperatures: room temperature (T_a = 25 ℃), normal working condition (T_a = 50 ℃ and 75 ℃), severe condition (T_a = 125 ℃) and most critical condition (T_a = 150 ℃) respectively. The applied power loss is 20 W. The calculated thermal impedances are shown in Tab. V.

With the ambient temperature increasing, both the thermal resistance and thermal capacitance increase. It is noted that the thermal resistance and thermal capacitance of DCB and baseplate layers do not vary much with temperature. This phenomenon is more obvious for the silicon chip layer. The chip thermal resistance $R_{th(chip)}$ under T_a = 150 ℃ is 50% higher than that under T_a = 25 ℃. These parameters can be integrated in the model shown in Fig. 9. The extracted Cauer model can be used for circuit-level thermal simulations.

V. EXPERIMATAL VERIFICATION OF TEMPERATURE EFFECTS WITH INFRARED CAMERA

In order to validate the proposed thermal model of temperature effects, an experimental setup with infrared camera is built in the lab.

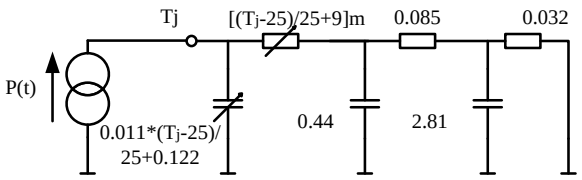

Fig. 9. The extracted Cauer thermal model with temperature-dependent thermal parameters.

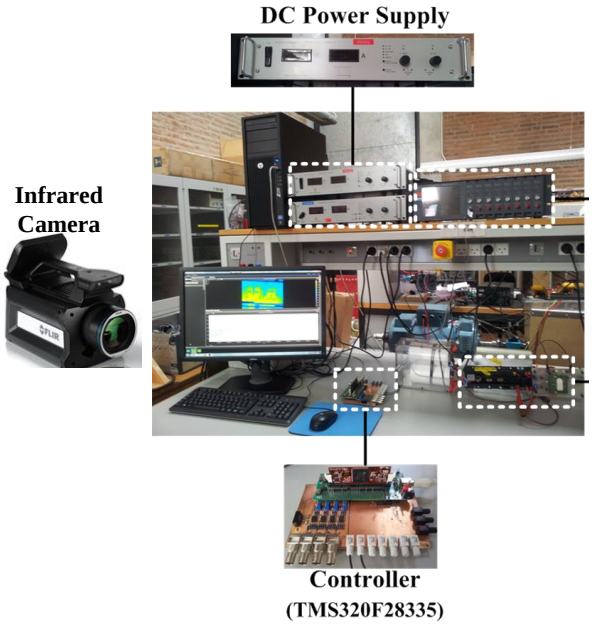

Fig. 10. Test setup for the transient thermal impedance with the advanced infrared camera.

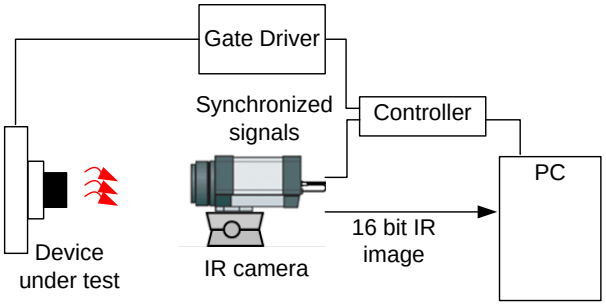

Fig. 11. The method of integrating and synchronizing the infrared camera.

A. Experimental Setup

A test setup is constructed to validate the thermal model. A heat plate is arranged underneath the open module to control the ambient temperature. The device under test is the considered 1700 V/1000 A IGBT open module (as shown in Fig. 6). An infrared camera is used to monitoring the temperatures. The setup implementation is illustrated in Fig. 10.

In order to obtain accurate and fast temperature acquisitions of the IGBT module, a high-definition 1.3 million pixels infrared camera is adopted, with an achievable integration time at μs-level [20]. In real-time mode, it has an adjustable frame rate of up to 106 Hz at full frame size and

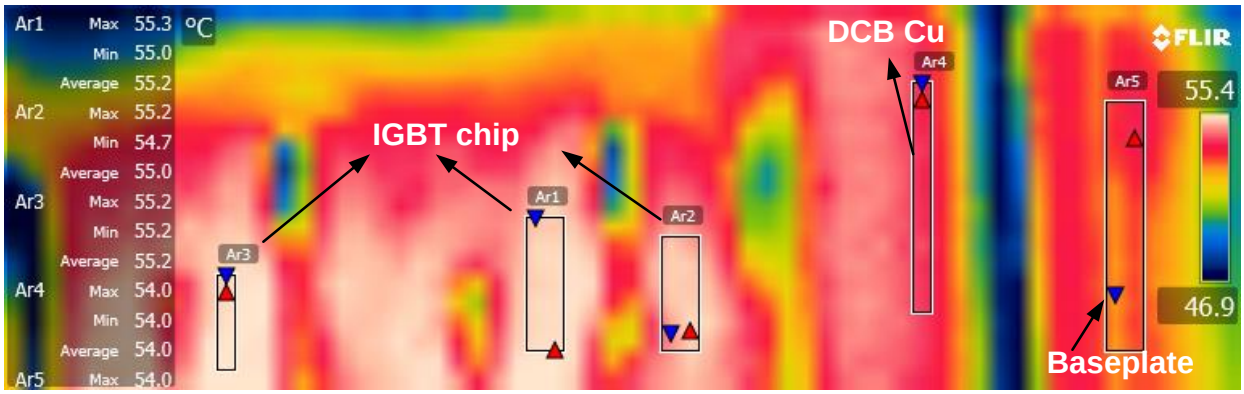

Fig. 12. Temperature image obtained by infrared camera.

more than 3 kHz at 48x4 pixels. It can measure temperatures up to +3000 ℃, with a high accuracy of +/- 1 ℃ or +/- 1%. The camera can be controlled by computer with a user-friendly interface. What's more, it is equipped with a Wi-Fi interface which enables remote control, and the lenses are changeable. The infrared camera is connected to a personal computer (PC), so that the infrared images and data can be recorded. The way of infrared camera integrated to the testing setup is illustrated in Fig. 11.

Because the metals on the IGBT module surfaces have very low emissivity (0.19-0.55), it is difficult to directly obtain accurate thermal acquisitions [17]; even if a calibration procedure could be adopted [21]. Because black-painting the module surface can gain uniform emissivity, it is commonly used for infrared camera detections. With the black-painted open module, one of the module temperature images during the T_a = 50 ℃ testing is shown in Fig. 12. Three areas of IGBT chip surface (Ar1 - Ar3), one area of DCB Cu layer surface (Ar4) and one area of baseplate top (Ar5) temperatures are monitored, as illustrated in Fig. 12.

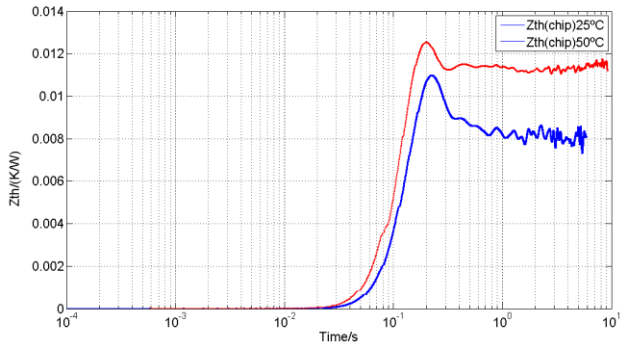

Fig. 13. Measured transient thermal impedance under different ambient temperatures.

B. *Experimental Validation Results*

The experimental operations can be divided into two states: preparation state and measurement state.

In preparation state, the ambient temperature is controlled by the heat plate underneath the power module. The module is operating at normal condition by the controller. Meanwhile, the infrared camera is monitoring the temperature. At the end of preparation stat, temperatures of the power module and heat plate should be stable.

In measurement state, the IGBT module is turned-off by the controller, and the temperatures of the module are decreasing. And temperatures of IGBT chip surface, DCB Cu layer surface and baseplate surface should be monitored and recorded in real time, as illustrated in Fig. 12. Thermal impedance of each layer is calculated based on the temperatures.

The tests are conducted under 25 ℃ and 50 ℃ respectively, and thermal impedance curves are shown in Fig. 13. It can be noted that thermal impedance of 50 ℃ is higher than for 25 ℃ ambient temperature. The testing results are coincidence with simulation results in Table V.

VI. Conclusion

A novel thermal impedance model with considering temperature effects has been proposed in this paper. Thermal impedance is increasing with temperature. It is observed by FEM simulations with a case study of 1700 V/1000 A IGBT module. Furthermore, a test setup has been constructed with open IGBT modules and an ultra-fast infrared camera. Experimental results confirm the proposed model's predictions.

Acknowledgment

This work is conducted under the Center of Reliable Power Electronics (CORPE) project framework at Aalborg University, Denmark.

REFERENCES

[1] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics - challenges, design tools and opportunities," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17-26, Jun. 2013.

[2] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters - An overview," *Proc. of the Annual Conference of the IEEE Industrial Electronics Society (IECON)*, pp.505-511, 2013.

[3] P. Ghimire, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, P.B. Thøgersen, "A review on real time physical measurement techniques and their attempt to predict wear-out status of IGBT", *Proc. of the 15th European Conference on Power Electronics and Applications (EPE2013)*, pp. 1-10, 2013.

[4] H. Ohashi and I. Omura, "Role of simulation technology for the progress in power devices and their applications," *IEEE Trans. on Electron Devices*, vol.60, no.2, pp.528-534, Feb. 2013.

[5] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. de. Doncker. "Semiconductor power devices- physics, characteristics, reliability". Springer, Berlin, 2011, ISBN: 3642111246, pp.353-358.

[6] N. Hingora, X. Liu, et al, "Power-CAD: a novel methodology for design, analysis and optimization of power electronic module layouts," *Proc. of Energy Conversion Congress and Exposition (ECCE)*, pp.2692-2699, Sept. 2010.

[7] P. Solomala, A. Castellazzi, M. Mermet-Guyennet, and M. Johnson, "New technology and tool for enhanced packaging of semiconductor power devices," *Proc. of IEEE International Symposium on Industrial Electronics(ISIE)*, pp.2020-2025, July 2009.

[8] A. Nejadpak, A. Nejadpak, and O.A. Mohammed, "A physics-based, dynamic electro-thermal model of silicon carbide power IGBT devices," *Proc. of Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp.201-206, March 2013.

[9] L. Jayasinghe, Y. Gu, N. Narendran. "Characterization of thermal resistance coefficient of high-power LEDs" *Proc. of Sixth International Conference on Solid State Lighting*, pp. 1-10, 2006.

[10] J.-C.-J. Paasschens, S. Harmsma, R. Van der Toorn. "Dependence of thermal resistance on ambient and actual temperature", *Proc. of the 2004 Meeting Bipolar/BiCMOS Circuits and Technology*, pp.96-99, 2004.

[11] M. Chen, A. Hu, B. Wang and Y. Tang, "Test of IGBT junction-case steady state thermal resistance and experimental analysis," *Proc. of International Conference on Intelligent System Design and Engineering Application*, vol.2, pp.557-560, 2010.

[12] G. Chen, D. Han, Y.-H. Mei, X. Cao, T. Wang, X. Chen, and G.-Q. Lu, "Transient thermal performance of IGBT power modules attached by low-temperature sintered nanosilver," *IEEE Trans. on Device and Materials Reliability*, vol.12, no.1, pp.124-132, March 2012.

[13] Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs), IEC Standard 60747-9.

[14] F. Incropera, D. Dewitt, T. Bergman, and A. Lavine, Fundamentals of Heat and Mass Transfer, 5th ed., John Wiley & Sons, 2007, ISBN: 0471386502, pp. 675-677.

[15] Introduction to ANSYS Icepak,
http://www.ansys.com/Support/Training%20Center/Courses/Introduction%20to%20ANSYS%20Icepak.

[16] IntroductionToCOMSOLMultiphysics,
http://www.comsol.com/shared/downloads/IntroductionToCOMSOLMultiphysics.pdf.

[17] Engineering Fundamentals website: www.eFunda.com

[18] S. Filippis, H. Köck, M. Nelhiebel, V. Kosel, S. Decker, M. Glavanovics, and A. Irace, "Modelling of highly anisotropic microstructures for electro-thermal simulations of power semiconductor devices", *Microelectronics Reliability*, vol. 52, pp. 2374-2379, 2012.

[19] B. Jayant Baliga, Fundamentals of Power Semiconductor devices, Springer Verlag, 2011, ISBN: 978-0-387-47313-0, pp. 966-988.

[20] FLIR "Advanced thermal imaging cameras for R&D and Science applications",
http://www.flirmedia.com/MMC/THG/Brochures/T820168/T820168_EN.pdf.

[21] A. Irace, "Infrared thermography application to functional and failure analysis of electron devices and circuits," *Microelectronics Reliability*, vol.52, pp. 2019-2023, 2012.