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Accelerated Successive Approximation Technique for Analog to Digital Converter Design

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ACCELERATED SUCCESSIVE APPROXIMATION TECHNIQUE FOR ANALOG TO DIGITAL CONVERTER DESIGN

by

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Submitted in Partial Fulfillment of the Requirements for the

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Approved by:

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Dr. Jun Qin

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TITLE: ACCELERATED SUCCESSIVE APPROXIMATION TECHNIQUE FOR ANALOG TO DIGITAL CONVERTER DESIGN

MAJOR PROFESSOR: Dr. Haibo Wang

This thesis work presents a novel technique to reduce the number of conversion cycles for Successive Approximation register (SAR) Analog to Digital Converters (ADC), thereby potentially improving the conversion speed as well as reducing its power consumption. Conventional SAR ADCs employ the binary search algorithm and they update only one bound, either the upper or lower bound, of the search space during one conversion cycle. The proposed method, referred to as the Accelerated-SAR or A-SAR, is capable of updating both the lower and upper bounds in a single conversion cycle. Even in cases that it can update only one bound, it does more aggressively. The proposed technique is implemented in a 10-bit SAR ADC circuit with 0.5V power supply and rail-to-rail input range. To cope with the ultra-low voltage design challenge, Time-to-Digital conversion techniques are used in the implementation. Important design issues are also discussed for the charge scaling array and Voltage Controlled Delay Lines (VCDL), which are important building blocks in the ADC implementation.

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CHAPTER 1

INTRODUCTION

The evolution of the semiconductor industry in terms of both revenue and global market has been phenomenal over the past few decades. The next forthcoming years will be pivotal and very interesting for an inquisitive researcher to see the happenings and inventions in the industry. Low power VLSI design has been on the rise due to emerging applications, including portable devices, wireless sensors, etc. There are diverse types of VLSI circuits for carrying out various functionalities. This thesis investigates circuit design techniques for Analog to Digital converter (ADC), an important VLSI circuit that is used in various applications.

1.1 MOTIVATION

Signals in the real world are typically analog signals. But the computation power of electronic systems is mainly provided in digital format. Analog to Digital converters bridge the analog signals and the computation power provided by computer and digital signal processing circuits. Among various ADC implementation techniques, Successive Approximation Register Analog to Digital Converter (SAR ADC) topology is particularly attractive for low-power medium resolution and medium speed ADC implementation. Recently, many low voltage low-power SAR ADC circuits have been reported in literature. However, SAR ADC conversion speed is typically degraded with the reduction of supply voltage, making them too slow for many applications. Such observation

motivated this research which investigates circuit techniques that can enhance SAR ADC speed and meanwhile reduce circuit power consumption.

1.2 OBJECTIVES

The objective of the research is to investigate circuit techniques for low-voltage low power SAR ADC design. With the scaling down power supply voltage, the headroom for signal swing is reduced. To cope with this challenge, time-to-digital conversion techniques have been used in some recently reported low-voltage SAR ADCs. By this approach, voltage signal is translated into time domain information by Voltage Controlled Delay Lines (VCDL). This provides large headroom for signal swing (delay). This work will examine important design issues for VCDL used in SAR ADC. The use of Voltage to Time conversion technique may adversely affect the ADC conversion speed. An N-bit SAR ADC typically requires N conversion cycles and 1 sampling cycle to digitize the analog input. If the number of conversion cycles for an ADC input can be reduced, it not only potentially improves the ADC overall conversion speed, but also significantly reduces the overall circuit power consumption.

1.3 MAJOR CONTRIBUTION OF THE RESEARCH

This thesis work presents a novel technique for SAR ADC design which reduces the number of conversion cycles, thereby accelerating the speed and reducing power consumption. The method is named as Accelerated Successive Approximation Register Technique, or simply A-SAR. Conventional SAR ADCs employ binary search algorithm to find the voltage level that is closest to the ADC input. During one conversion cycle,

the binary search algorithm reduces the search space by half and it updates only one bound, either the lower bound (LB) or the upper bound (UB) of the search space. The accelerated-SAR or A-SAR method is capable of updating both the LB and UB of the search space in a single conversion cycle thereby reducing the overall required number of clock cycles. Even in cases that it can update only one bound, it updates the bound more aggressively (more than half). Compared to other techniques [1] that reduce SAR ADC conversion cycles and power consumption, the proposed technique does not require ADC inputs to have the characteristic of short bursts followed by long periods of stationary values. Thus, the proposed technique is applicable to a wide range of applications. The proposed technique is implemented and evaluated in a 10-bit SAR ADC circuit, which uses time-to-digital conversion techniques. This is mainly to achieve low voltage operation. Important design issues on the implementation of the charge-scaling capacitor array and Voltage Controlled Delay Line are also discussed in the thesis.

1.4 ORGANIZATION OF THE THESIS

The rest of the thesis is organized as follows. Chapter 2 surveys the related work reported in recent literature. The topics being surveyed include SAR ADC, Time-to-Digital converter and Voltage Controlled Delay Lines. The proposed A-SAR technique is described in Chapter 3. Circuit implementation and evaluation of a 10-bit ADC with using the proposed technique are presented in Chapter 4. Conclusions and future work are discussed in Chapter 5.

CHAPTER 2

LITERATURE SURVEY

A survey of the recent development on SAR ADCs is presented in this chapter. This reveals the intensified interests as well as the current trend in the design of low-voltage low-power SAR ADC circuits. In addition, the design techniques of Voltage Controlled Delay Lines (VCDL) and Time-to-Digital Converter (TDC) are summarized in the chapter, since such circuits are used in the SAR ADC circuits developed in this work.

2.1 RECENT DEVELOPMENT OF SAR ADC

Recently, there are strong research interests in the design of low-voltage low-power SAR ADC. Table 2.1 lists the SAR ADC circuits reported in major journals and conferences from 2010 to 2014. It lists the parameters such as resolution, sampling rate, figure of merit and power supply of the SAR ADCs. To highlight the design trend and technology advancement, key ADC design parameters including sampling rate, resolution, power supply and Figure of Merit (FoM) are plotted in Figures 2.1, 2.2, 2.3 and 2.4. In literature, Figure of Merit (FOM) is often used to compare the performance of ADC energy efficiency. It is calculated as:

$$FOM = \frac{Power\ consumed}{Sampling\ frequency\ f_S * 2^{ENOB}} \quad (1)$$

Table 2.1 List of recent developments in SAR ADC

Year	Authors	Resolution	Sampling Rate (MS/s)	Power Supply	Figure of Merit
2010	Young-Kyun et al [2]	9	80	1 V	78
2010	Chun-Cheng Liu et al [3]	10	50	1.2 V	29
2010	Yan Zhu et al [4]	10	100	1.2 V	77
2011	Jia Hao Cheong et al [5]	8	0.08	1 V	19.5
2011	Masanori Furuta et al [6]	10	40	1.1 V	65
2011	Sang-Hyun Cho et al [7]	10	40	1.2 V	50
2011	Wenbo Liu et al [8]	12	45	1.2 V	51.3
2011	Yongsheng et al [9]	12	0.05	1.8 V	1.74
2011	John A. McNeill et al [10]	16	1	1 V	20
2012	Tao Jiang et al [11]	6	1250	1.2 V	148
2012	Akira Shikata et al [12]	8	1.1	0.5 V	6.3
2012	I. Kianpour et al [13]	8	0.0178	0.7 V	2.2
2012	Hegong Wei et al [14]	8	400	1.2 V	42
2012	Guan-Ying et al [15]	10	0.2	0.6 V	8.03
2012	Dai Zhang et al [16]	10	0.001	1 V	94.5
2012	Jon Guerber et al [17]	10	0.008	1.2 V	16.9
2012	Ruoyu Xu et al [18]	10	0.768	1.8 V	74
2012	Martin et al [19]	11	0.08	1.02 V	36.8
2013	Vikram et al [20]	8	1	1 V	42.3
2013	Lukas Kull et al [21]	8	1200	1 V	34
2013	Weibo Hu et al [22]	8	0.002	1.1 V	79.9
2013	Ryota Sekimoto et al [23]	9	0.0001	0.5 V	5.2
2013	Ying-Zu Lin et al [24]	9	200	1.3 V	27.2
2013	Marcus Yip et al [25]	10	2	1 V	22.4
2013	Si-Seng Wong et al [26]	10	170	1 V	30.8
2013	Ji-Yong Um et al [27]	11	0.01	0.5 V	74.8
2013	Pieter Harpe et al [28]	12	0.04	0.6 V	2.2
2013	Seung-Yeob et al [29]	12	3	2.3 V	368
2013	Ron Kapusta et al [30]	14	80	1.2 V	23.7
2014	Hung-Yen Tai et al [31]	6	1000	1.2 V	180
2014	Indrajit Das et al [32]	8	0.04	1.8 V	13
2014	Younghoon Kim et al [33]	9	0.1	0.6 V	65
2014	Howard Tang et al [34]	10	0.001	0.9 V	10.94
2014	Yan Zhu et al [35]	10	100	1.2 V	55

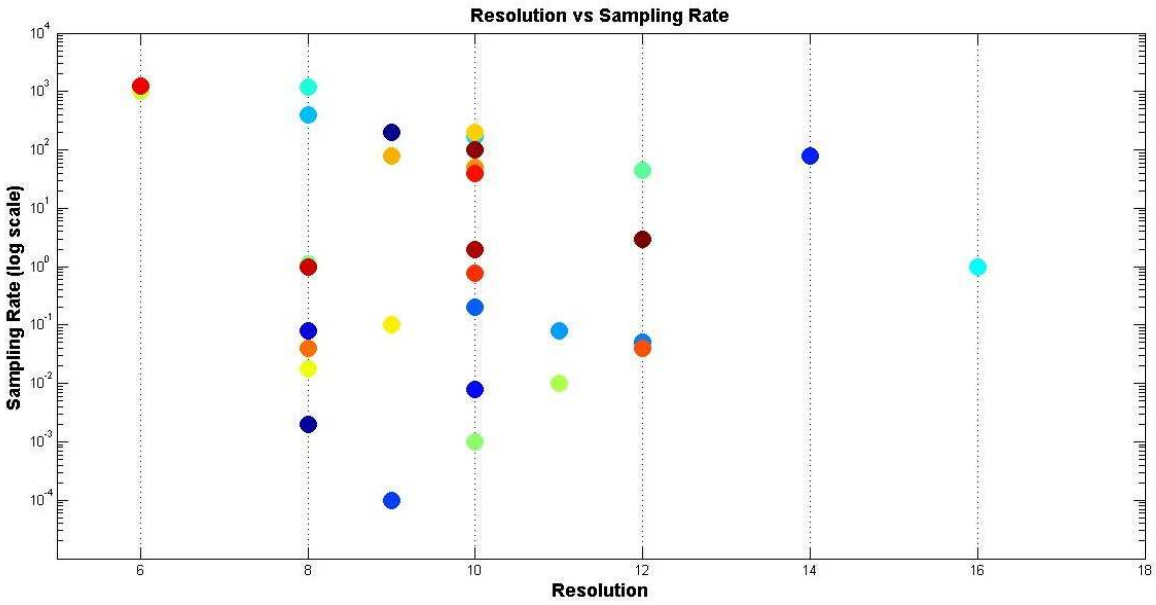

Figure 2.1 Resolution vs Sampling Rate

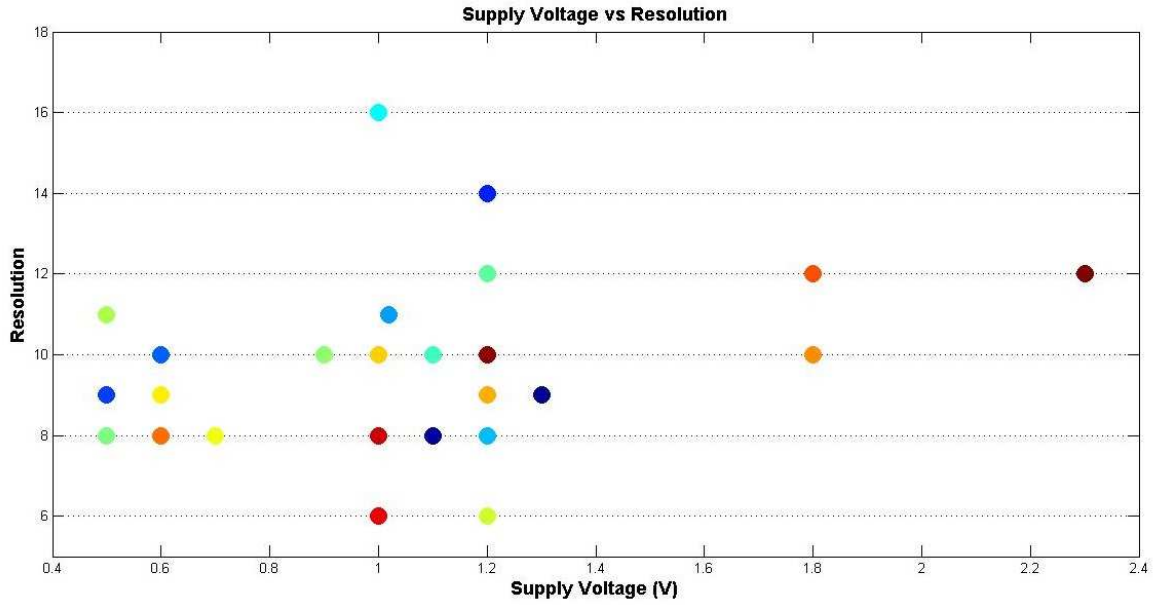

Figure 2.2 Supply Voltage vs Resolution

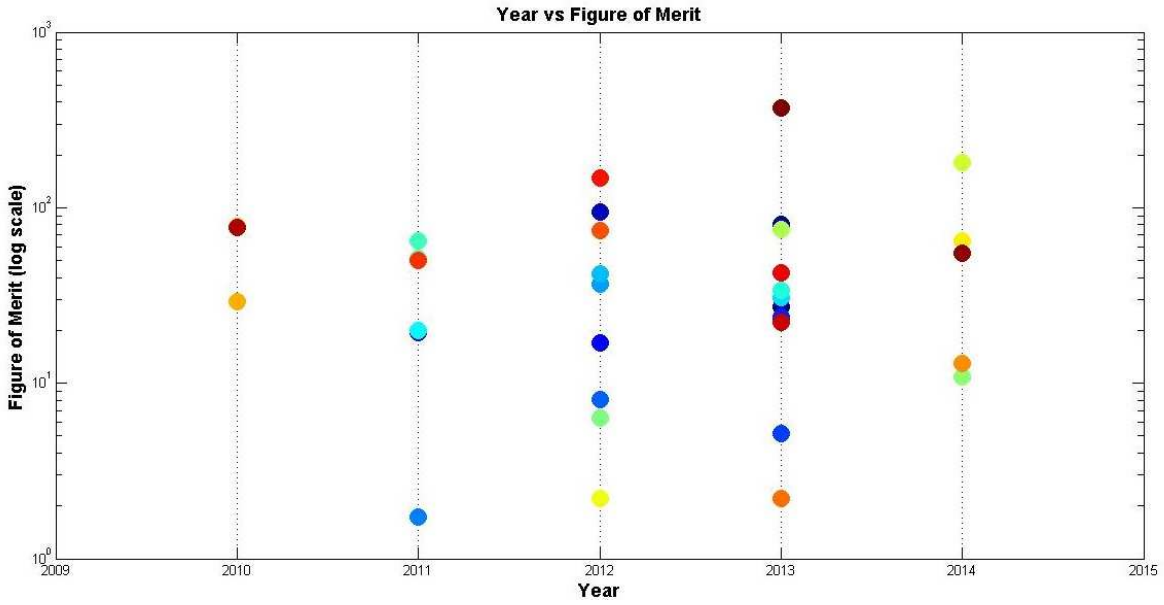

Figure 2.3 Year vs Figure of Merit

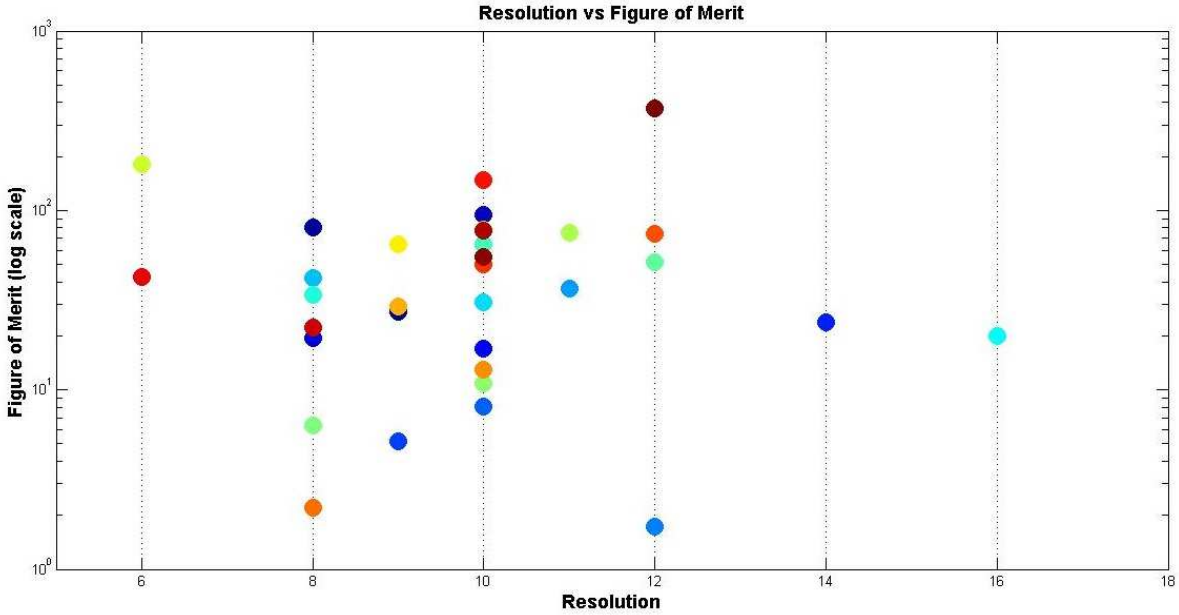

Figure 2.4 Resolution vs Figure of Merit

2.1.1 LOW POWER CAPACITOR SWITCHING SCHEME

The design presented in [3] employs a monotonic switching method for a fully differential DAC capacitor array. Instead of using conventional bottom plate sampling techniques, the top plates of the capacitors are used to sample the input. To minimize charge injection impact and achieve rail-to-rail input range, bootstrapped switches are used as the sampling switch. There are two advantages of using the proposed top plate sampling technique. First, it increases settling speed and input bandwidth since there is smaller parasitic capacitance at the top plate. Second, the MSB conversion can be carried out without charging or discharging any capacitor. Note that the bottom plates of the capacitors are connected to V_{ref} during sampling. During the conversion, the largest capacitor in the higher voltage potential side array is switched to ground and the other capacitors remain unchanged. This operation continues till the LSB conversion. So during one conversion cycle, only one capacitor is switched which significantly reduces charge transfer and transitions, thereby increasing the switching speed. The search process is monotonic based on the inputs. This switching procedure leads to lower switching energy which is reduced by 81%, without splitting or adding capacitances, and a total capacitance reduction of 50%. The overall switching power consumption is reduced to 1mW using 0.13μm CMOS technology.

2.1.2 INCREASING SAR ADC SPEED VIA BYPASS WINDOW TECHNIQUE

Techniques to increase the conversion speed of an SAR ADC are presented in [15]. A bypass window technique is used to skip several conversion steps in an SAR ADC if the ADC input is within the bypass window range. Assume the window size is

$2^M.V_{LSB}$ and the difference between the DAC outputs is V_{diff}. During the conversion process, if the voltage difference between the two comparator inputs in a conversion cycle is smaller than the window size, the conversion can directly jump to the $(N-M)^{th}$ conversion cycle, where N is the ADC resolution. The digital bits associated with the skipped conversion cycles will be assigned to 0.

In this proposed method, the power consumptions of each block are separately calculated for uniformly distributed signals and it is found that a 128LSB window size leads to the least power consumed in such cases. For signals which are mostly non-uniform such as normal distributed signals, ECG signals or neural signals, a much narrower window is found to be suitable and hence a 32-LSB window size is considered. Two comparators, coarse and fine comparators, are used to compare the DAC output voltages with a constant voltage corresponding to the bypass window size. The method is implemented with a supply voltage of 0.6V and sampling frequency of 200 KS/s with 9.34 ENOB.

2.1.3 SAR ADC SELF CALIBRATION TECHNIQUE

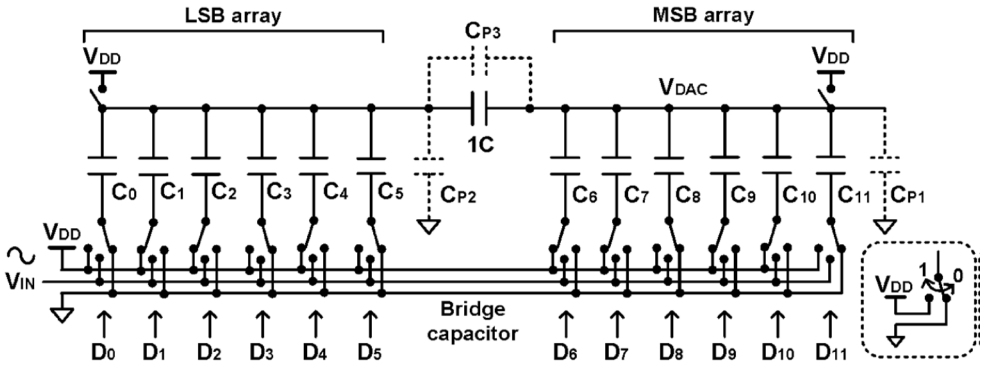

Figure 2.5 The differential type 11.5-bit split-capacitor DAC array used in [27]

The work in [27] presents a self-calibration technique to minimize the inaccuracy caused by capacitor mismatch and parasitic capacitance, C_{P1}, C_{P2} and C_{P3} (caused by overlaps between metal layouts and silicon substrates) as shown in Figure 2.5. It uses one of the split-capacitive DACs to measure the error code of the other array during the calibration process. The error voltages for each DAC capacitor is measured as E_{Vi} for bit i. E_{Ci} is its corresponding error code which is the digital value for average error voltage $0.5\ (E_{VPi} + E_{VNi})$ of the positive and negative C_i branches of the DAC array. The error voltage and error code of a bit are related by the following equation:

$$E_{Ci} = 0.5\ (E_{VPi} + E_{VNi}).\frac{2^{11}}{V_{DD}} \quad (2)$$

The measured codes are stored in a memory. During the normal ADC operation, an 11.5 output code is generated which is a raw output. It is then added to the pre-measured error code, E_{Ci}, to generate the 11-bit calibrated output code. Note that an additional bit of 0.5 LSB is added for the error correction. If a bit D_i from the MSB array is 1 during the conversion process, the corresponding error code E_{Ci} is fetched from the memory and added with the 11.5-bit raw SAR code. Although all the 11.5-bit codes are used for calibration, only six MSB codes are used in error compensation since the sum of the error codes for the six LSB codes is smaller than 0.5 LSB (sum of all error voltages). Consider ΣE_{Ci} is the sum of all measured error codes and $D_{11}D_{10}D_9 \ldots D_0$ is the raw SAR code.

$$\Sigma E_{Ci} = E_{C11} \cdot D_{11} + \cdots + E_{C0} \cdot D_0 \quad (3)$$

$$D_{out} = D_{11}D_{10}D_9 \ldots D_0 + \Sigma E_{Ci} \quad (4)$$

The error correction procedure is done in the following manner. First, the offset compensation of the comparator is performed. Then the error codes are pre-measured

and stored in a memory circuit. The normal ADC conversion is performed which generates the raw 11.5 bit output code and an adder circuit adds the estimated error codes and the raw output to generate the calibrated 11-bit digital code. The design is implemented in a standard CMOS 0.13μm technology with a supply voltage of 0.5V and a sampling rate of 10 KS/s and 9.93 ENOB.

2.2 VOLTAGE CONTROLLED DELAY LINE

In general, three circuit techniques have been widely used in the implementation of Voltage Controlled Delay Lines. They are: shunt capacitor, current-starved and variable resistor techniques. Figure 2.6 shows the block diagram of current starved implementation.

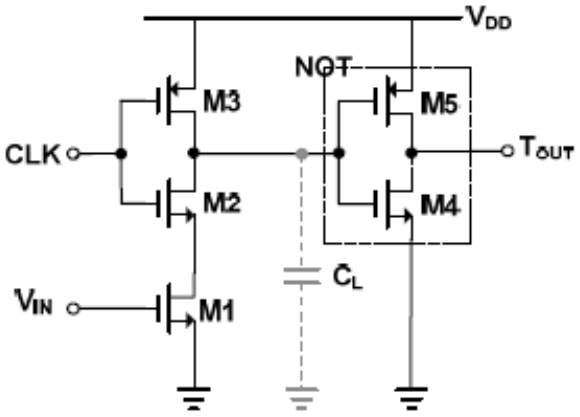

Figure 2.6 Current-starved technique [36]

During the clock low-to-high transition, M2 turns on and the capacitor C_L starts to discharge. The discharging current is controlled by M1 which acts as a current source. The rising delay can be derived as, [36]

$$t_d = \tau \ln \frac{1+\lambda_1 V_{DD}}{1+\lambda_1 \frac{V_{DD}}{2}} \quad (5)$$

where

$$\tau = \frac{C_L}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{IN}-V_T)} \quad (6)$$

μ_n is the mobility of electrons, λ is the channel length modulation parameter, V_T is the threshold voltage of M1 and C_L is the load capacitance. The above equation shows that the delay can be controlled by the size of M1.

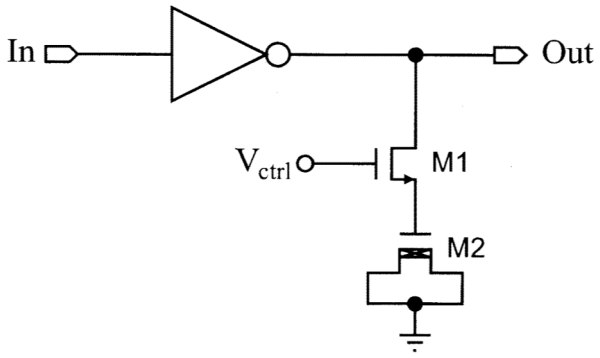

Figure 2.7 Shunt capacitor technique [37]

The shunt capacitor technique is shown in Figure 2.7. Transistor M2 acts as a capacitor while transistor M1 controls the charging and discharging of M2. The gate voltage of M1, V_{ctrl}, controls the charging/discharging current. Hence, the resistance of M1 is directly controlled by V_{ctrl}. As the value of V_{ctrl} increases, the resistance of the shunt transistor M1 decreases and the effective capacitance at the output is large thereby producing larger delay. Thus its delay can be controlled through the control voltage.

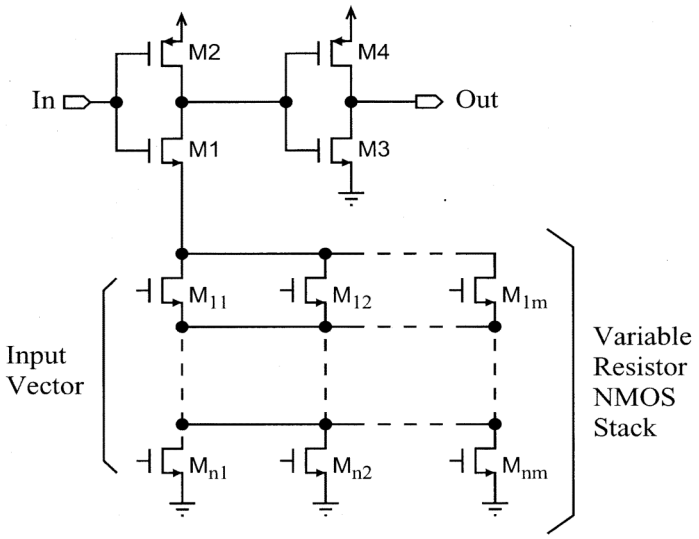

Figure 2.8 Variable resistor technique [37]

A variable resistor technique is shown in Figure 2.8. Variable resistors are used to control a particular transistor for delay in the form of a vector. A stack of n rows and m columns of NMOS transistors is used to make a variable resistor. The resistor stack controls the delay of the circuit. In the circuit, only the rising edge of the output is controlled through the stack. A stack of PMOS transistors can be used to control the falling edge of the delay.

Among these three techniques, the current-starved technique is often preferred since it is less prone to temperature and process variations. To further improve its performance, a temperature compensated voltage controlled delay line is shown in Figure 2.9.

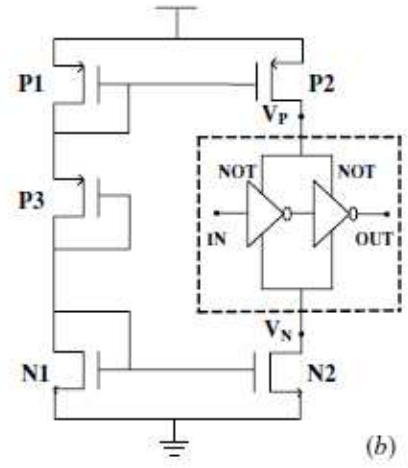

Figure 2.9 Thermal compensation current-starved delay line [38]

The thermal compensation of the delay line is performed through the diode connected transistors P1, N1 and P3 by making the drain current of P3 independent of absolute temperature. The temperature increase directly affects the threshold voltage of the transistors. This decreases the drain current of the transistors and causes the increase of the delay. The threshold voltage V_T expression is given:

$$V_T(T) = V_T(T_0) + \alpha(T - (T_0)) \tag{7}$$

where T_0 and T are reference and practical absolute temperatures, respectively. α is from -0.5 to -3.0 mVK^{-1}, which is the temperature coefficient. For P3, we have:

$$I_{DS3} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)\left(V_{gs} - V_t\right)^2(1 + \lambda V_{gs}) \tag{8}$$

Substituting V_T expression into the above equation,

$$I_{ds3} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)\left(\frac{T}{T_0}\right)^{km} X\,[V_{gs} - V_T(T_0) - \alpha(T - (T_0)]^2(1 + \lambda V_{gs}) \tag{9}$$

where km is thermal conductivity. The term $(1 + \lambda V_{gs})$ will be neglected in the following derivations since its thermal sensitivity is much smaller than that of mobility and threshold voltage. The sizes of P1 and N1 are adjusted to make Vgs of P3 satisfy the equation below.

$$V_{gs3} = V_T(T_0) + \alpha(T - T_0) + 2\frac{\alpha T}{km} \quad (10)$$

$$I_{ds3} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)\left(\frac{T}{T_0}\right)^{km}\left(\frac{2\alpha T}{km}\right)^2(1 + \lambda V_{gs}) \quad (11)$$

when $km = -2$ the current of P3 will become totally independent of temperature as shown below:

$$I_{ds3} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)(\alpha T_0)^2(1 + \lambda V_{gs}) \quad (12)$$

Thus, through the help of current mirrors P1, P2, N1 and N2, the conduction current of NOT gates will be kept thermally insensitive too.

2.3 TIME-TO-DIGITAL CONVERTER

Time-to-digital converters (TDC) are generally used to convert the time information to digital output based on their comparison. Several recently reported time-domain comparators are discussed as follows. A flip-flop can be conventionally used since it is the fastest and simplest circuit. But it has a characteristic of non-zero setup time since a flip-flop has different paths for clock and data. This mismatch contributes to an input-referred offset delay which varies as supply voltage decreases. In [36],a true single edge D Flip-Flop as shown in Figure 2.10 is used as the phase detection circuit. Two inputs, D and CLK, decide the output of the flip flop based on the incoming signals.

It uses a single clock but with the expense of additional transistors. Due to the usage of a clock, it is prone to metastability caused by setup and hold time violations.

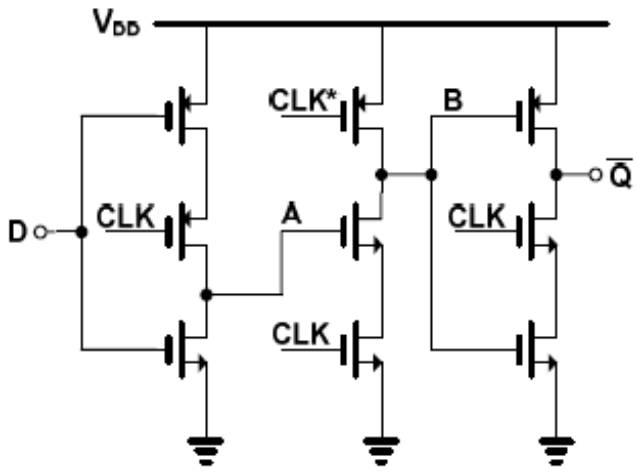

Figure 2.10 Time-domain comparator with DFF [36]

To cope with the above drawback, a Binary Phase Detector is proposed in [39] to convert time to digital code. The PD is shown figure 2.11. The Binary PD has two inputs, two back-to-back connected inverters and a latch. OUT is 1 when IN1 arrives first and vice-versa. The PD achieves fast latch operation with the shortest paths from input to its output.

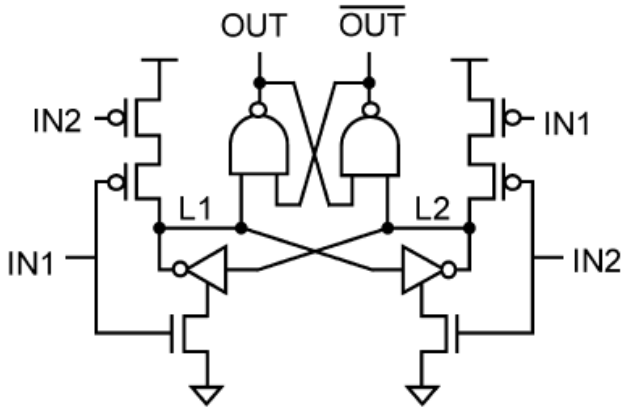

Figure 2.11 Binary Phase Detector [39]

A Vernier type Time-to-Digital converter is presented in [40] which is used to convert the pulse width from a temperature sensor to a corresponding digital code. It is implemented in a 2 stage Vernier type TDC. The first stage of the Vernier type TDC is the conventional inverter based TDC to reduce power consumption. The second stage is the Vernier type TDC for high resolution where the resolution of the second stage is determined by the difference between the gate delays of the two inputs, thereby controlling its resolution. During the first stage operation, when the delay line leads the pulse input, the final time residue or final time remaining becomes the input for the second stage. A similar operation is done in the second stage. Finally, the digital code is determined by controlling the gate delays of both inputs. The design is implemented in a 0.18μm CMOS process technology.

A novel method of converting time to voltage and then converting the voltage to digital output through an ADC is presented in [41]. For converting the time to voltage, a charge-pump based transducer is implemented. A PMOS and an NMOS are connected

together in series with the differential inputs as gate inputs. When the PMOS is on and NMOS is off, the capacitor connected to both the transistors outputs gets charged. The voltage on the capacitor is held and converted to digital output by an ΔΣ ADC. During the hold and conversion process, both the transistors are turned on to make sure that the flowing output current is the same as the input current. Once the voltage is converted, the NMOS turns on and PMOS turns off, thereby discharging the charge from the capacitor. Final resolution is 200ps and power dissipated is 30mW.

CHAPTER 3

PROPOSED ACCELERATED SAR TECHNIQUE

In this chapter, we present a technique that accelerates the SAR process during Analog to Digital conversion. The technique is developed for a Voltage-to-Time based VTC ADC circuit as shown in Figure 3.1.

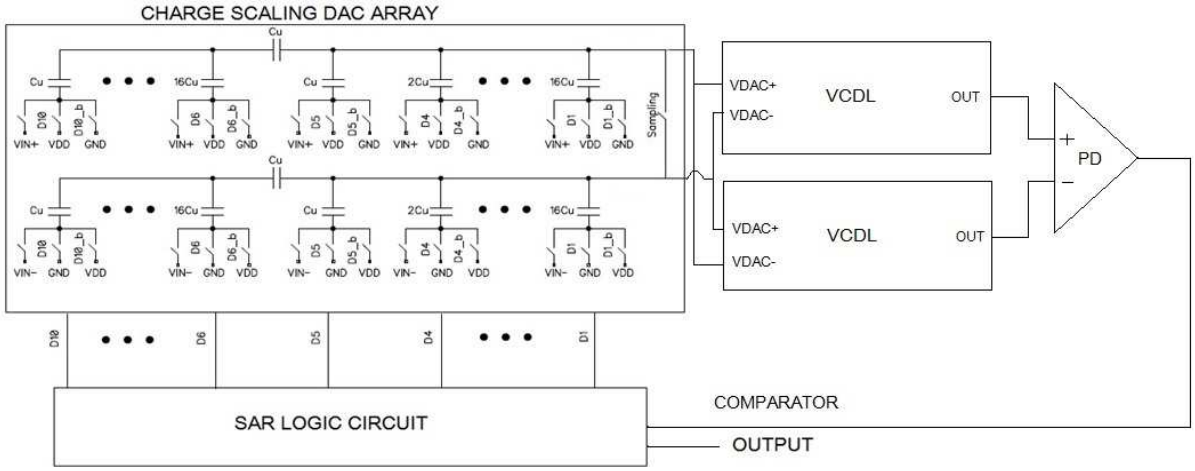

Figure 3.1 Conventional VTC-based SAR ADC

The conventional SAR ADC always updates either the upper or the lower bound to reduce the search space by half. The proposed method updates both the upper and lower bounds in one conversion cycle, thereby reducing the number of conversions and reducing the overall power consumption. To implement this technique, two additional PDs are added along with the existing PD as shown in Figure 3.2. The original PD can be called as the main comparator whose output is P_M. This determines the difference between ${V_{DAC}}^{+}$and ${V_{DAC}}^{-}$. The offset of PD is relatively small after careful circuit design

and calibration [42]. The voltage-to-time gain of the VCDL is large such that a small input voltage can be converted to a large delay. So the offset of the PD is ignored. The PD whose output is referred to as $P_A{}^+$, is an auxiliary PD which compares the delay of the entire top VCDL and a portion of the bottom VCDL. The upper PD is referred to as $P_A{}^-$ which is the negative auxiliary PD which compares a portion of the upper part of the VCDL and the entire bottom VCDL. Unlike the main PD, $P_A{}^+$ and $P_A{}^-$ compare the asymmetric branches of the VCDL, as shown in Figure 3.2. Hence the comparison results are prone to temperature and process variations.

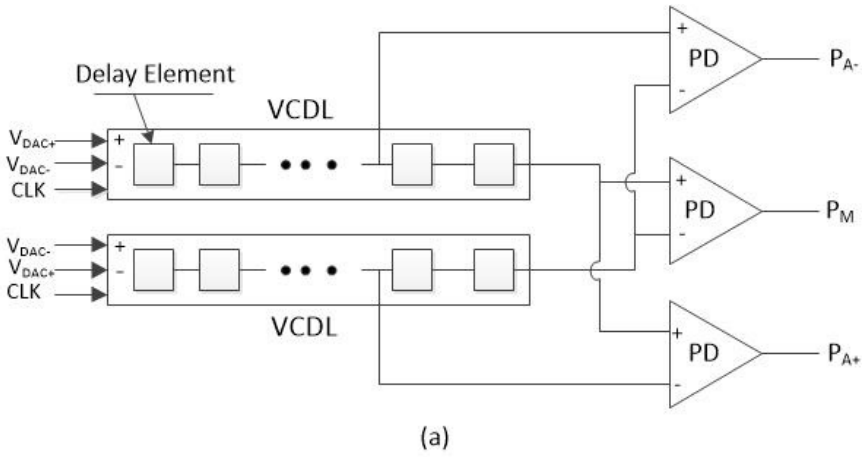

Figure 3.2 A-SAR concept of VCDL with three PDs

V_{DACmin} and V_{DACmax} are used to denote the minimum and maximum values of the uncertain region, where the auxiliary PD produces different results based on the irregularities in process and temperature variations. This uncertain region is termed as $uncertainty\ band\ (uBand)$ and its width is $V_\delta = V_{DACmax} - V_{DACmin}$. We approximately round the V_δ value to a multiple of V_{LSB} since it is the minimum voltage difference that the ADC can detect. The rounded value is called as the $enforced\ uBand$ and denoted

as V_Δ. V_A is used to represent the starting voltage of the enforced uBand. In Figure 3.3, the shaded rectangle is the uBand and the unshaded rectangle is the enforced uBand.

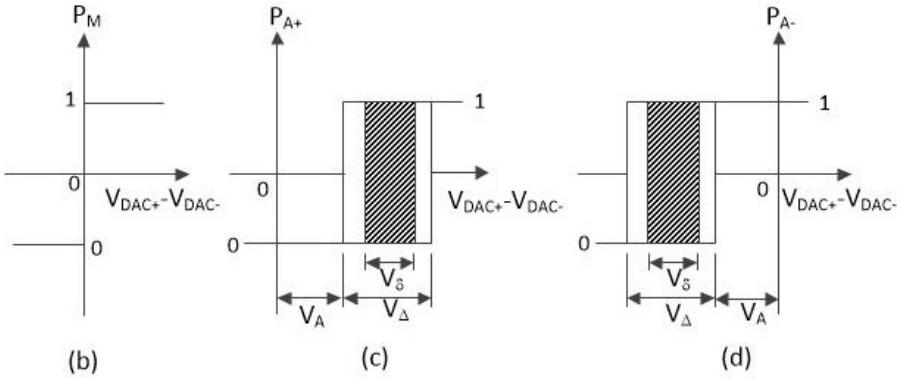

Figure 3.3 Relation between DAC outputs and comparator outputs of (b) P_M (c) ${P_A}^+$ and (d) ${P_A}^-$

The conventional SAR ADC and A-SAR ADC are compared with respect to search space refinement in Figure 3.4. The left side of the figure corresponds to conventional SAR operation which uses only the main PD. If $P_M = 1$, ${V_{DAC}}^+ > {V_{DAC}}^-$, indicating that V_{in} is larger than V_D, which corresponds to the voltage level which is specified by the digital code in the SAR. V_{in} and V_D are connected with the relation [43]:

$$ {V_{DAC}}^+ - {V_{DAC}}^- = V_{in} - V_D \tag{13}$$

In this case, only the lower bound of the search space is updated to V_D. On the contrary, the upper bound of the search space will be updated to V_D in case if $P_M = 0$.

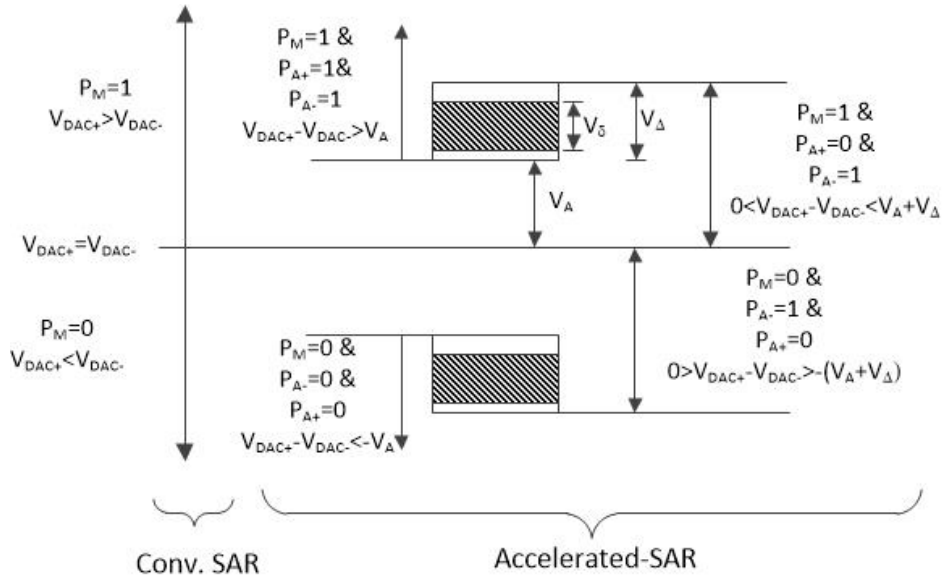

Figure 3.4 Comparative outcomes of Conventional SAR and A-SAR

The right side of the figure corresponds to the A-SAR operation. Based on the relation between the VCDL outputs, there are only four possible combinations of the PD outputs. First case, all the outputs are 1, indicating that

$$V_{DAC}{}^{+} - V_{DAC}{}^{-} = V_{in} - V_D > V_A \tag{14}$$

Also it implies that the new LB should be $V_D + V_A$. In case 2, all outputs are 0., indicating

$$V_{DAC}{}^{+} - V_{DAC}{}^{-} = V_{in} - V_D < -V_A \tag{15}$$

Implying that the new UB should be $V_D - V_A$. In these two cases, the A-SAR updates only one bound of the search space, but it does more aggressively than its conventional counterpart. In case 3, $P_M = 1$, $P_A{}^{+} = 0$ and $P_A{}^{-} = 1$, we have

$$0 < V_{DAC}{}^{+} - V_{DAC}{}^{-} = V_{in} - V_D < V_A + V_\Delta \tag{16}$$

Hence,

$$V_D < V_{in} < V_D + V_A + V_\Delta \tag{17}$$

In case 4, $P_M = 0$, $P_A{}^{+} = 0$ and $P_A{}^{-} = 1$. Hence,

$$V_D - V_A - V_\Delta < V_{in} < V_D \quad (18)$$

In cases 3 and 4, the A-SAR updates both the lower and upper bounds. Thus by aggressive search space update and reduction the A-SAR is capable of producing the digital output in less than the stipulated number of conversion cycles.

3.1 4-BIT EXAMPLE

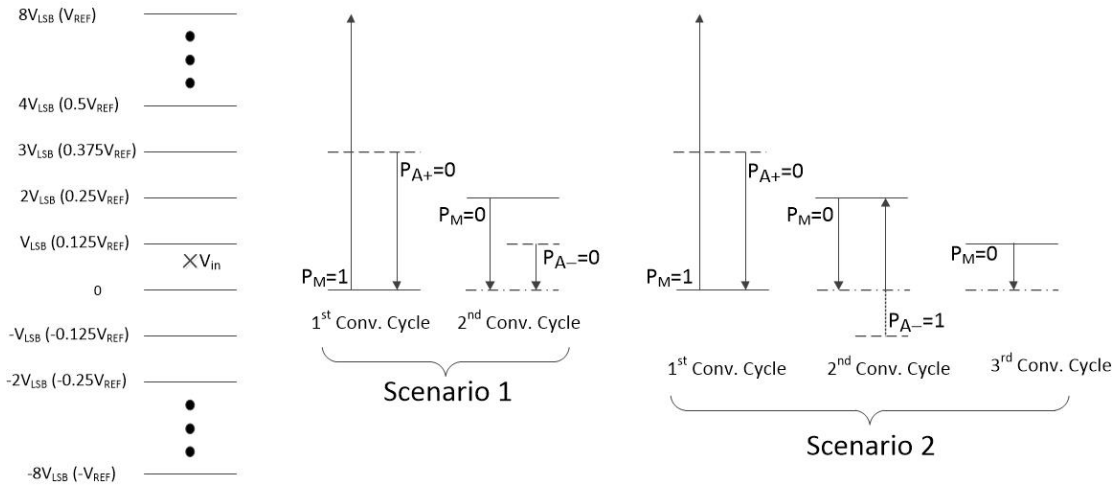

Figure 3.5 Illustrative examples of A-SAR conversion

Let us consider a 4-bit example to explain the search space reduction in the A-SAR scheme as shown in Figure 3.5. The input of the ADC V_{in} is assumed as $0.1V_{REF}$ in the example. The output of the ADC is clearly seen as 1000 (excess-8 code) and it (conventional ADC) should take 4 conversion cycles to complete the conversion. For the A-SAR operation, we assume $V_A = 1V_{LSB}$ and $V_\Delta = 2V_{LSB}$. After the first conversion cycle, comparator output $P_M = 1$ (since $V_{in} > V_D = 0$) and ${P_A}^+ = 0$ since V_{in} is below the enforced uBand of ${P_A}^+$. Now, the UB is updated from V_{REF} to $0.375V_{REF}$ and LB is

updated from $-V_{REF}$ to 0. In the second conversion cycle, the ADC compares V_{in} with $0.25V_{REF}$, the level which will be compared in the conventional ADC. $P_M = 0$ since $V_{in} < 0.25V_{REF}$. But this time V_{in} is located inside the enforced uBand of P_A^-, so P_A^- can be either 0 or 1. In scenario 1, we assume $P_A^- = 0$, which indicates $V_{in} < 0.125V_{REF}$ ($V_D - V_A = 0.25V_{REF} - 0.125V_{REF}$). This information is adequate for the ADC to reach the correct output code and the conversion is complete after two conversion cycles. Scenario 2 assumes $P_A^- = 1$, which indicates $0.25V_{REF}$ (V_D) $> V_{in} > -0.125V_{REF}$ ($V_D - V_A - V_\Delta$). But, LB has been received as 0 in the previous conversion cycle. The $-0.125V_{REF}$ is an underestimate of the LB, due to the uncertainty associated with the uBand. Hence, the final LB and UB must be $0.25V_{REF}$ and 0, respectively, after the second conversion cycle. There is only one level, which is $0.125V_{REF}$, within this search space. The output of the main PD in the third conversion cycle will be adequate to determine the final digital output and the entire conversion is completed in three cycles. Thus, we see that the A-SAR is capable of producing the digital output in less number of conversion cycles than the conventional ADC.

3.2 LOWER BOUND (LB) AND UPPER BOUND (UB) UPDATE CIRCUITS

From the previous section where the A-SAR principle was explained, the search bound update policies in the proposed A-SAR scheme can be easily derived and they are depicted in Figure 3.6.

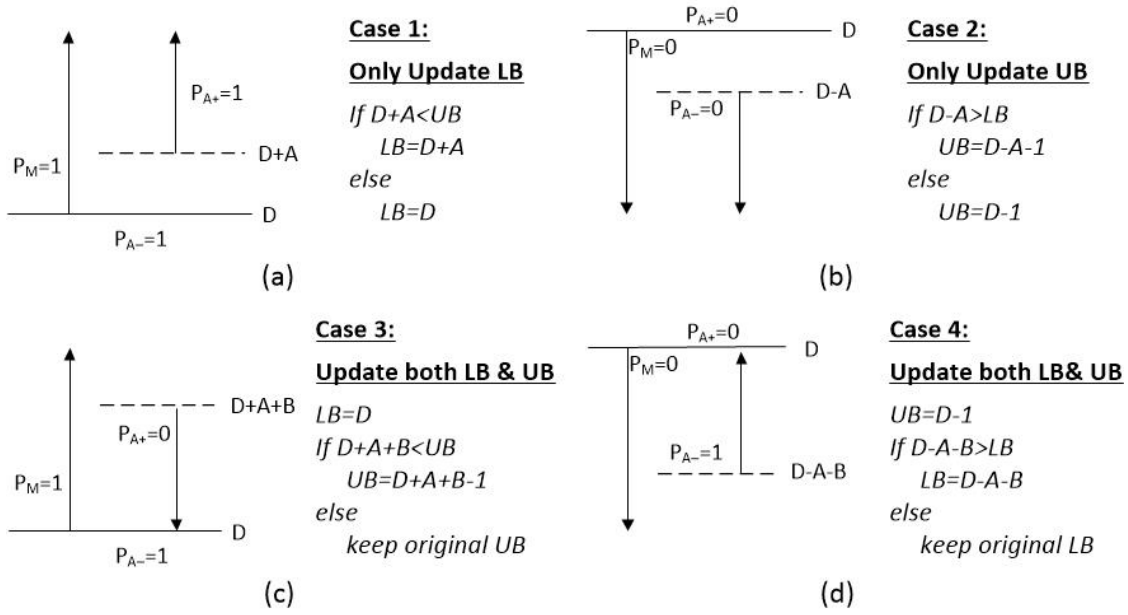

Figure 3.6 Lower and Upper bound update schemes

D represents the digital code from the SAR register; A and B are the digital codes corresponding to V_A and V_Δ respectively. In the UB update process, the newly calculated UB is always one V_{LSB} below the actual voltage level that partitions the search space. This is because if the ADC input is a fraction of V_{LSB} smaller than a voltage level whose corresponding code is d, the ADC output code is $d-1$.

- **Case 1:** This case updates only the lower bound or LB. If the new D+A is less than the previous UB, then the new LB will be D+A, else LB will be the new D. The comparison takes place with the help of a subtractor circuit
- **Case 2:** This case updates only the upper bound or UB. The subtractor circuit compares the new D-A and the previous LB. If the output is 0, then UB will be D-A-1, else UB is D-1
- **Case 3:** This case updates both UB and LB based on the comparison. Here, always the new LB will be the previous D. UB will be compared with

D+A+B. If the output is 1, UB will be D+A+B-1 or else the UB will the same as the previous UB

- **Case 4:** This case also compares both UB and LB. Here, UB is always D-1. LB is compared with D-A-B and new LB is D-A-B if output is 0. LB remains the same if output is 1

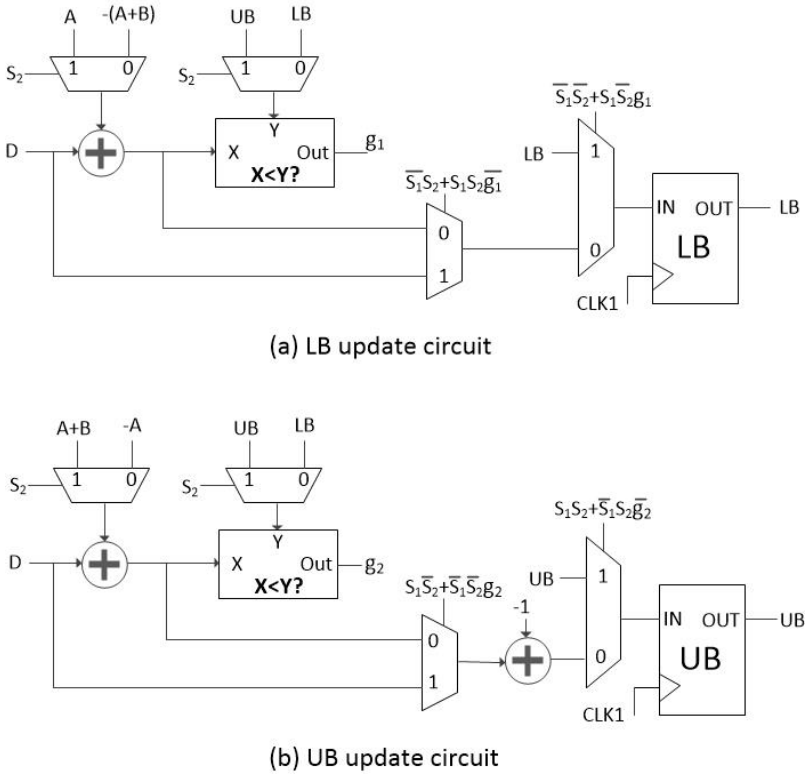

Figure 3.7 (a) LB update circuit and (b) UB update circuit

The logic control circuit for the aforementioned cases, which is responsible to update the lower bound and upper bound, is shown in Figure 3.7. Control signals $S1$ and $S2$ are figured out based on the four cases. Table 3.1 shows the four cases with the

three comparator outputs. It is easy to verify that the circuit functionalities are consistent with LB and UB update policies.

Table 3.1 Cases of comparator outputs in A-SAR

CASE	PHASE DETECTOR OUTPUTS			$S1$	$S2$
	$P_A{}^+$	P_M	$P_A{}^-$	$P_A{}^- . (\overline{P_M} + P_A{}^+)$	$P_M . P_A{}^-$
1	1	1	1	1	1
2	0	0	0	0	0
3	0	1	1	0	1
4	0	0	1	1	0

When implemented in the circuit, both the signals control the lower and upper bound update code for the next cycle. The equations for $S1$ and $S2$ are as follows:

$$S1 = P_A{}^- . (\overline{P_M} + P_A{}^+) \quad (19)$$

$$S2 = P_M . P_A{}^- \quad (20)$$

Figure 3.7 shows that the control signals $S1$ and $S2$ control the two 11-bit 2:1 multiplexers. The digital codes A and B are 11-bit and the output is 11-bit code. The UB and LB signals to the second MUX is from the previous conversion cycle. D is the previous digital code from the SAR register. Signals D and the output from the MUX are added through an 11-bit adder. The MSB of D input of the adder is grounded since the digital output D consists of 10-bits. Also, the C_{in} of the adder is grounded to set it to zero. As seen in the figure, two 10-bit 2:1 multiplexers are responsible for the final

update of both LB and UB values at their respective registers. Their control signals are labeled as SELECT1, SELECT2, SELECT3 and SELECT4 based on the relation between $S1$, $S2$, $g1$ and $g2$ which is derived from the four cases. The relation is shown in Table 3.2. The generation of signals $g1$ and $g2$ are explained in the next section.

Table 3.2 Table listing the logic for SELECT1, SELECT2, SELECT3 and SELECT4

SIGNALS	CIRCUIT	EQUATION
SELECT1	LB UPDATE	$\overline{S1}.S2 + S1.S2.\overline{g1}$
SELECT2	LB UPDATE	$\overline{S1}.\overline{S2} + S1.\overline{S2}.g1$
SELECT3	UB UPDATE	$S1.\overline{S2} + \overline{S1}.\overline{S2}.g2$
SELECT4	UB UPDATE	$S1.S2 + \overline{S1}.S2.\overline{g2}$

3.3 VALUE COMPARISON (X<Y?) CIRCUIT

In Figure 3.7, the component labeled as “X<Y” compares the values of inputs X and Y and produces the output g1 (or g2) as 1 if X<Y. g1 (or g2) is 0 if X>Y. It works like a subtraction circuit and its carry out is the circuit output. In order to explain the operation of the circuit, let us consider an example. After the sampling, the LB register is set to 0000_0000_00, UB is set to 1111_1111_11 and thereby D is set to 1000_0000_00. We shall assume that $S1 = S2 = 1$. From Figure 3.7, input X of the value comparison circuit of the LB register is D+A (1000_1111_10) and Y is UB (1111_1111_11). Note that A = 0000_1111_10 and A+B = 0001_1000_00 which will be explained later why. Clearly, X<Y. So g1 is 1. Thereby from Table 3.2, SELECT1 = 0 and SELECT2 = 0. Now, the LB is updated as D+A. Similarly, for the UB update circuit,

X is D+A+B which is 1001_1000_00 and Y is UB which is 1111_1111_11, thereby g2 = 1. So SELECT3 = 0 and SELECT4 = 1. Hence, the UB stays the same in this conversion.

Let us consider an example where the value of X is negative. That would be the case when $S2$ = 0. We shall consider the UB update circuit for this example. According to Figure 3.7, the input of the value comparison circuit, X, will be D-A which is 1_1111_0000_10 which is negative. Y is UB, 0_1111_1111_11. The value comparison circuit performs the subtraction X-Y and the difference is 0_1111_0000_11 with an additional carry-out of 1. Hence, the difference is negative and g2 should be 1. But, since the circuit is a 11-bit subtractor, the 12th bit is neglected and the circuit assumes the value of g2 as 0. In such a case when the value of X is negative, an error is occurred. To cope with this error, an additional 12th bit is added to the value comparison circuit which takes one input as the carry-out of the 11-bit adder. The difference of the 12th bit is taken as g2. The same measure is considered for the LB update circuit where g1 is considered.

In a summary, the inputs of the LB and UB register include A, B, digital code D, signal 2 , UB and LB values of the previous conversion cycle and signals SELECT1, SELECT2, SELECT3 and SELECT4. The outputs are $g1$, $g2$ and updated LB and UB values $LB9 - LB0$ and $UB9 - UB0$ respectively. The LB and UB registers are controlled by $CLK1$. The LB register is reset to 0 for all 10-bits and UB register is preset to 1 for all 10-bits during the first conversion cycle.

3.4 DIGITAL CODE UPDATE CIRCUIT

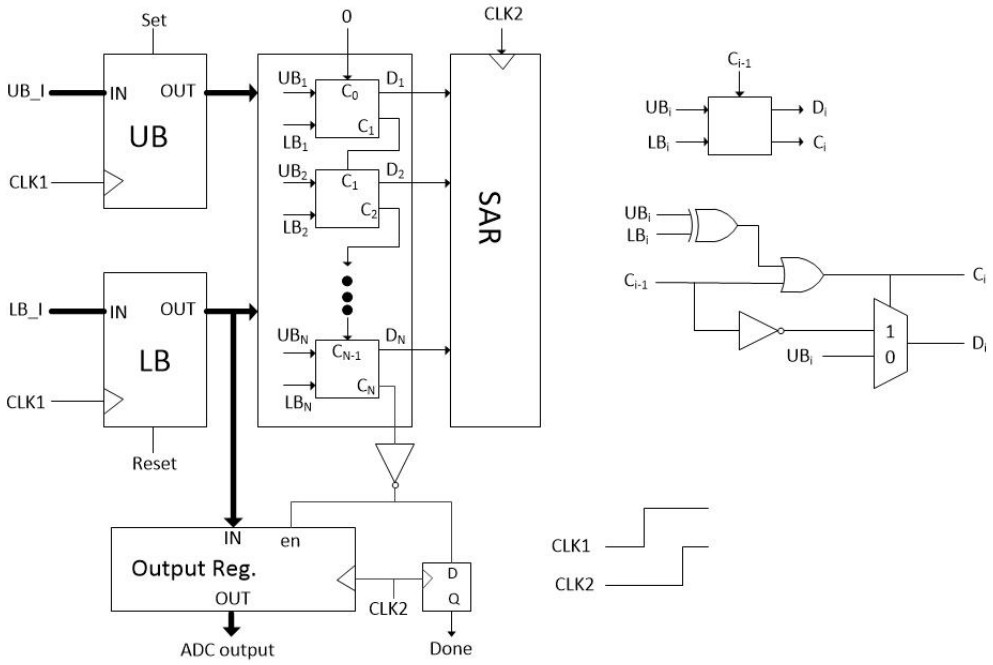

Figure 3.8 A-SAR concept of Ci and SAR register

Figure 3.8 shows the circuit that generates the digital code corresponding to the voltage level to be compared with in the SAR conversion process. In the figure, blocks labeled by LB, UB and SAR are registers to store the current lower bound, upper bound and the D value, controlling the charge scaling capacitor array. The SAR register is updated as follows. First, the UB and LB are compared in bit-wise manner. Assume the k^{th} bit is the first bit that the LB and UB are different, starting from the MSB. The LB (or UB) register bits are partitioned into two groups: all the bits before the k^{th} bit $U_1U_2 \dots U_{K-1}$ and the rest of the bits $U_KU_{K+1} \dots U_N$, assuming that the ADC resolution is N. Since LB and UB agree with each other before the k^{th} bit, $U_1U_2 \dots U_{K-1}$ is the correct ADC output for the first k-1 bits. They will be directly loaded into the SAR register for the next conversion cycle. Also, the k^{th} bit of SAR is set to 1 and rest of the bits are reset to

0. The voltage level specified by SAR will be compared with ADC input in the next conversion cycle to further refine the search space.

The above circuit carries out the above function. It is implemented by cascading N basic cells whose schematic is shown at the right side of the figure. The XOR gate detects if UB_i is different from LB_i. If they are different, the cell output C_i will be 1. C_i is also 1 when its previous cell output C_{i-1} is 1. This is implemented by the OR gate in the cell. If C_i is 0, UB_i is given to cell output D_i which is the input of the SAR. If $C_i = 1$ and $C_{i-1} = 0$, the i^{th} bit is the first bit that LB and UB are different. Thus, the output D_i will be 1. Finally, if $C_i = 1$ and $C_{i-1} = 1$, then $D_i = 0$.

The operation of the above circuit can be further explained using the same 4-bit ADC example provided previously, in Table 3.3. The discussion assumes Scenario 2 takes place during the conversion. Before the first conversion cycle, UB is set to 1111 and LB is reset to 0000. MSB is the first bit that UB and LB are different. Hence, 1000 is loaded into the SAR. These values are tabulated below in the rows “before conv.” group.

Table 3.3 Table showing LB, UB and SAR updates for the 4-bit example

CONV. CYCLE	PD OUTPUT		REGISTER	MSB	MSB-1	MSB-2	LSB
BEFORE CONV.	$P_A{}^+$	X	SAR	1	0	0	0
	P_M	X	LB	0	0	0	0
	$P_A{}^-$	X	UB	1	1	1	1
1	$P_A{}^+$	0	SAR	1	0	1	0
	P_M	1	LB	1	0	0	0
	$P_A{}^-$	1	UB	1	0	1	0
2	$P_A{}^+$	0	SAR	1	0	0	1
	P_M	0	LB	1	0	0	0
	$P_A{}^-$	1	UB	1	0	0	1
3	$P_A{}^+$	0	SAR	X	X	X	X
	P_M	0	LB	1	0	0	0
	$P_A{}^-$	1	UB	1	0	0	0

After the first conversion, the LB and UB are updated to 1010 and 1000, respectively. Hence, the third bit is the first place that UB and LB are different. As a result, 1010 is loaded into the SAR. Similarly, the SAR values at the end of the 2nd and 3rd can be determined. At the end of the third conversion cycle, LB and UB become the same and $C_4 = 0$, indicating the completion of the conversion. The inverted C_4 signal enables the output register to capture the correct ADC output from the LB (or UB) register.

CHAPTER 4

CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The proposed A-SAR technique is implemented and evaluated in this chapter. The implemented SAR ADC consists of a differential charge-scaling capacitor array, two ten-stage VCDLs, three binary phase detectors and the A-SAR logics. The design and circuit evaluation of these circuits are described in the following sections.

4.1 CHARGE SCALING CAPACITOR ARRAY DESIGN

A split-capacitor DAC charge scaling differential array is used in this design. The split-capacitive array consists of a pair of MSB and LSB arrays, each of 5-bits, connected by an attenuation capacitor. The unit capacitance is selected as 10fF. Consecutively, the rest of the bits are increased in powers of 2, where 160fF is the MSB capacitor of the LSB array. Correspondingly, the capacitances of the MSB array are also arranged in the same manner as 10fF, 20fF, 40fF, 80fF and 160fF. The attenuation capacitor (C_S) is chosen as 10fF, same as that of the unit capacitance. A similar architecture is employed for the differential array segment for the input voltage V_{in}^{-} as seen in Figure 4.1.

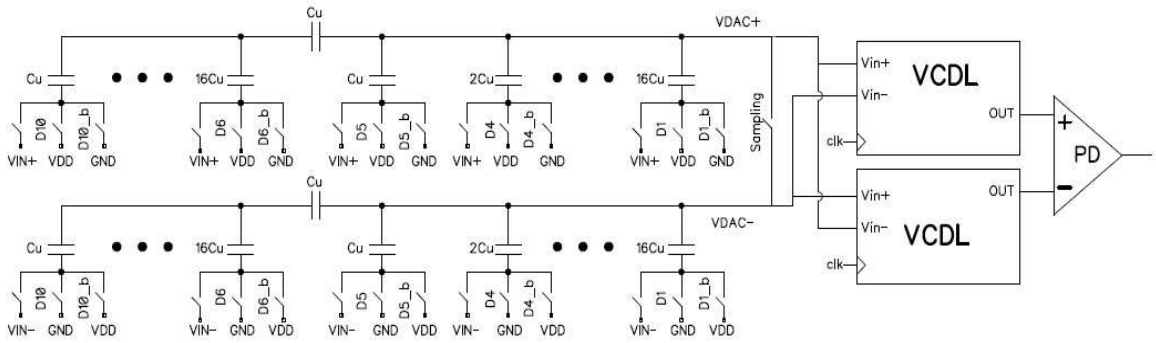

Figure 4.1 Block diagram of split-capacitive DAC array with VCDL and PD

Each capacitor is connected to three different switches: V_{in} switch, V_{DD}switch and GND switch. The V_{in} switch is implemented by a transmission gate (due to varying input and to reduce channel charge injection) for the sampling of the input. The switch connected to V_{DD} is implemented with a PMOS (since it is a good conductor of high voltage) and the switch connected to GND is implemented with an NMOS (since it is a good conductor of low voltage). The equalization switch (ES) which shorts the two capacitor arrays is implemented using a transmission gate. Also, the off-resistance of the V_{in} switch is of no importance because when the V_{in} switch is open, there is always some voltage (V_{DD} or GND) to charge the connected node.

During the sampling phase of the ADC, all the V_{in} switches are turned on. The equalization switch is also turned on. Therefore, the nodes ${V_{DAC}}^{+}$ and ${V_{DAC}}^{-}$, from Figure 4.1, are settled at input common mode voltage, V_{CM}. In the subsequent conversion phases, both the V_{in} switch and the ES are off. The V_{DD} and GND switches are turned on and off according to the SAR register values during the conversion.

To accommodate the operation, a 11-bit shift register, whose output are labeled from $S0 - S10$, is implemented. During the sampling phase, $S0$ = 1. The rest of the shift register outputs are 0. During the conversion phase, the logic 1 value, previously stored at $S0$, is passed as a token along the shift register chain. During the ith conversion phase, the ith bit of the SAR logic, which is denoted as D_i, is set to logic 1. In the capacitor array, whose signal input is Vin^+, the ith capacitor branch should be connected to V_{DD}. Meanwhile, the ith capacitor branch connected to the other capacitor array should be grounded. To realize this configuration, the switch controls are given in Table 4.1.

Table 4.1 Control Switch logic for DAC array switches

	V_{in} SWITCH	V_{DD} SWITCH	GND SWITCH
$V_{in}{}^{+}$ array	$S0$ / $\overline{S0}$	$S0 + \overline{D}$	$\overline{S0}$. $\overline{D}$
$V_{in}{}^{-}$ array	$S0$ / $\overline{S0}$	$S0 + D$	$\overline{S0}$. D

As mentioned earlier, the V_{DD} switch is implemented by a PMOS and the GND switch is implemented by an NMOS. The sizes of the V_{DD} and GND switches are determined through the settling error, which must be less than half of the V_{LSB}voltage which is 0.48828mV. Default sizes (160nm/120nm) are selected for the LSB capacitor switch and consecutively binary weighted for the rest of the capacitor array switches. Two scenarios are to be checked for the settling error criterions which are:

a. V_{in} switches from 0 to V_{DD}

b. V_{in} switches from V_{DD} to 0

A minimum sizing requirement of 2:1 ratio for the PMOS:NMOS criterion is provided and simulated for the above sizes. The settling errors for the LSB capacitor array are tabulated in Table 4.2.

Table 4.2 Settling error for V_{DD}/GND switches

CONDITION	SETTLING ERROR (mV)
0 -> V_{DD}	0.0006
V_{DD} -> 0	0.00006

Both the cases adhere to the settling error requirement. Hence, the LSB switch is given a size of 320nm/120nm for the PMOS and 160nm/120nm for the NMOS. The rest of the switches are binary weighted, owing to the increase in capacitances, as shown in Table 4.3.

Table 4.3 Sizes for V_{DD}/GND switches

CAPACITOR	V_{DD} SWITCH	GND SWITCH
LSB	320nm/120nm	160nm/120nm
MSB-3	640nm/120nm	320nm/120nm
MSB-2	1.28μm/120nm	640nm/120nm
MSB-1	2.56μm/120nm	1.28μm/120nm
MSB	5.12μm/120nm	2.56μm/120nm

The V_{in} switch is implemented by a transmission gate. Its on-resistance reaches the maximum value when the on-resistances of both PMOS and NMOS reach the same value. For the convenience of discussion, we refer to this voltage as critical voltage, $V_{critical}$. Therefore, the worst settling behavior can occur in one of the following four scenarios:

a. V_{in} switches from 0 → V_{DD}
b. V_{in} switches from V_{DD} → 0
c. V_{in} switches from 0 → $V_{critical}$
d. V_{in} switches from V_{DD} → $V_{critical}$

The first two scenarios represent situations that the circuit experiences the largest voltage change. The last two scenarios represent the conditions that the switch experiences the largest on-resistance at the end of sampling phase. The sizes of the V_{in} switches are maintained a ratio of 2:1 (PMOS:NMOS) throughout with default channel lengths. For the LSB capacitor switch size, the width is implemented 4 times that of default width. Consecutively, the rest of the capacitor array V_{in} switches are binary weighted. Figure 4.2 shows the setup used to determine the settling errors of the above cases. It is to be noted that while calculating the settling errors for the V_{in} switch, the V_{DD} and GND switches are also connected to the node.

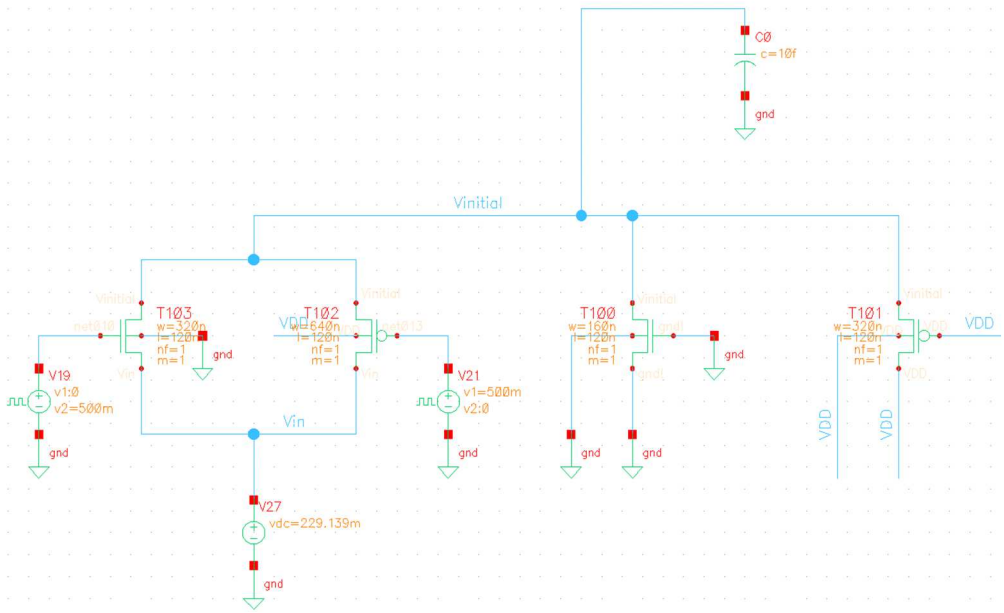

Figure 4.2 Setup to determine the settling error for V_{in} switch

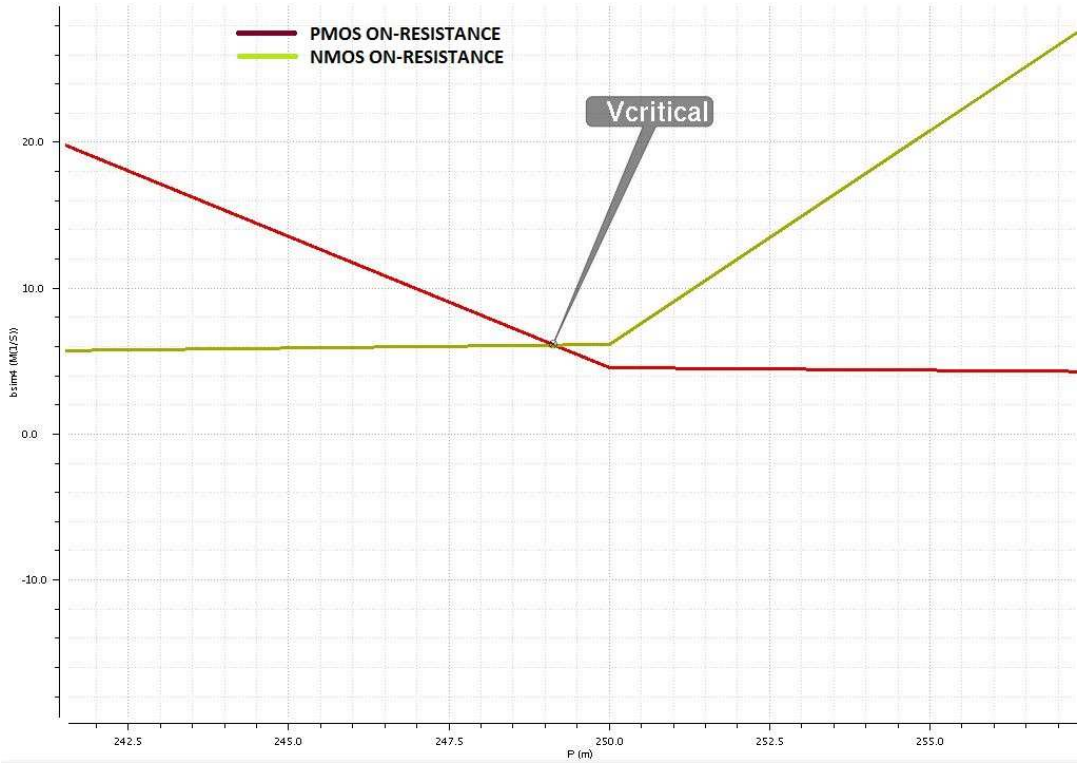

Figure 4.3 Critical voltage of transmission gate

Figure 4.3 shows the simulated on-resistances of PMOS and NMOS devices. The obtained critical voltage stands at 0.2491395V, where both the resistances of PMOS and NMOS are the same, is labeled as $V_{critical}$. Table 4.4 lists the settling error values of each scenario. It is seen that the selected transistor sizes satisfy the settling error requirement and hence the final sizes of the V_{in} switches are given in Table 4.5. The schematic of the MSB capacitor branch with all the switches is given in Figure 4.4.

Table 4.4 Settling errors for various transitions

CONDITION	TRANSITION	SETTLING ERROR (mV)
	V_{DD} -> 0	0.00035
	0 -> V_{DD}	0.003
$\boldsymbol{V_{critical} = 249.1395mV}$	0 -> $V_{critical}$	0.1139
	V_{DD} -> $V_{critical}$	0.1177
$\boldsymbol{V_{critical}' = V_{critical} + 20mV}$	V_{DD} -> $V_{critical}$	0.1016
	0 -> $V_{critical}$	0.1034
$\boldsymbol{V_{critical}' = V_{critical} - 20mV}$	V_{DD} -> $V_{critical}$	0.1003
	0 -> $V_{critical}$	0.0994

Table 4.5 Sizes for V_{in} switches

SWITCH	SIZE [P/N] (L=120nm)
LSB	640nm/320nm
MSB-3	1.28μm/640nm
MSB-2	2.56μm/1.28μm
MSB-1	5.12μm/2.56μm
MSB	10.24μm/5.12μm

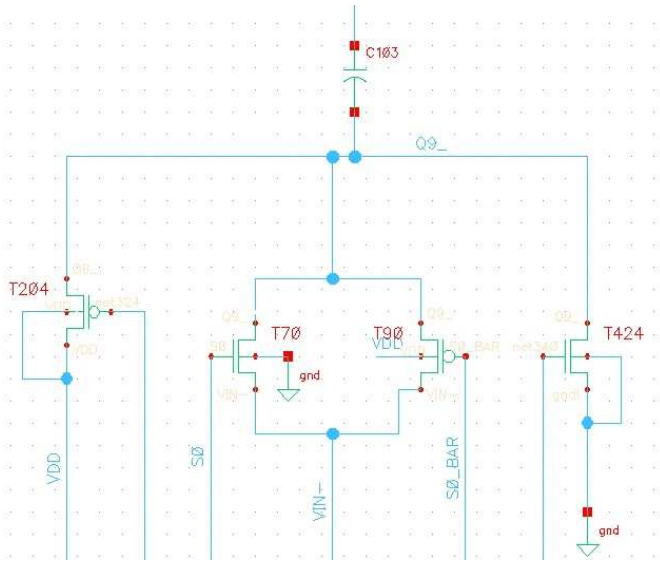

Figure 4.4 MSB of the split-capacitor array showing all the switches

The equalization switch (ES) or the sampling switch is closed during the sampling phase along with the V_{in} switches and open during the conversion phase. At the end of the sampling phase, it is made sure that the ES is open first before the opening of the V_{in} switch in order to neglect the channel charge injection and to make sure that the input is completely sampled and the node voltages equal the input

common mode voltage. So, additional delay is provided to the V_{in} switches to make this happen.

Transmission gate is used for the ES since the voltage connected to the switch is around $V_{DD}/2$. Since the ES is open during all the 10 conversion phases, the leakage of the transmission gate comes into effect and it is necessary to efficiently reduce the leakage current when it is off. Before considering reducing the leakage current, the maximum allowable leakage current is evaluated first. Considering the charge, capacitance and voltage relation:

$$\Delta V = \frac{\Delta Q}{C} \tag{21}$$

where ΔV is the change in voltage. Here, the minimum difference in voltage is half V_{LSB}. ΔQ is the charge associated with the array or the current times the time required for charge and discharge, which is 10μs. C is the total capacitance of one of the differential charge-scaling arrays, which is 320fF. The above equation can be modified as:

$$0.5V_{LSB} = \frac{I_{leakage}*\Delta T}{C} \tag{22}$$

The maximum leakage current can be calculated as 15.62pA from the above condition. It is to be made sure that the leakage current of ES must not exceed the maximum leakage current. To reduce the leakage current, stacked transistors based on [16] are implemented. And to determine their sizes, a basic single transmission gate is considered to calculate the channel length by varying it with the width as twice the channel length and the leakage current is monitored. Figure 4.5 shows the setup used to determine the leakage.

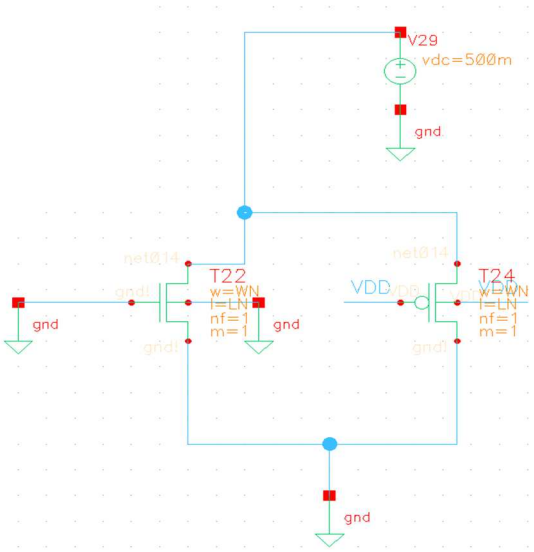

Figure 4.5 Setup to determine leakage current of equalization switch

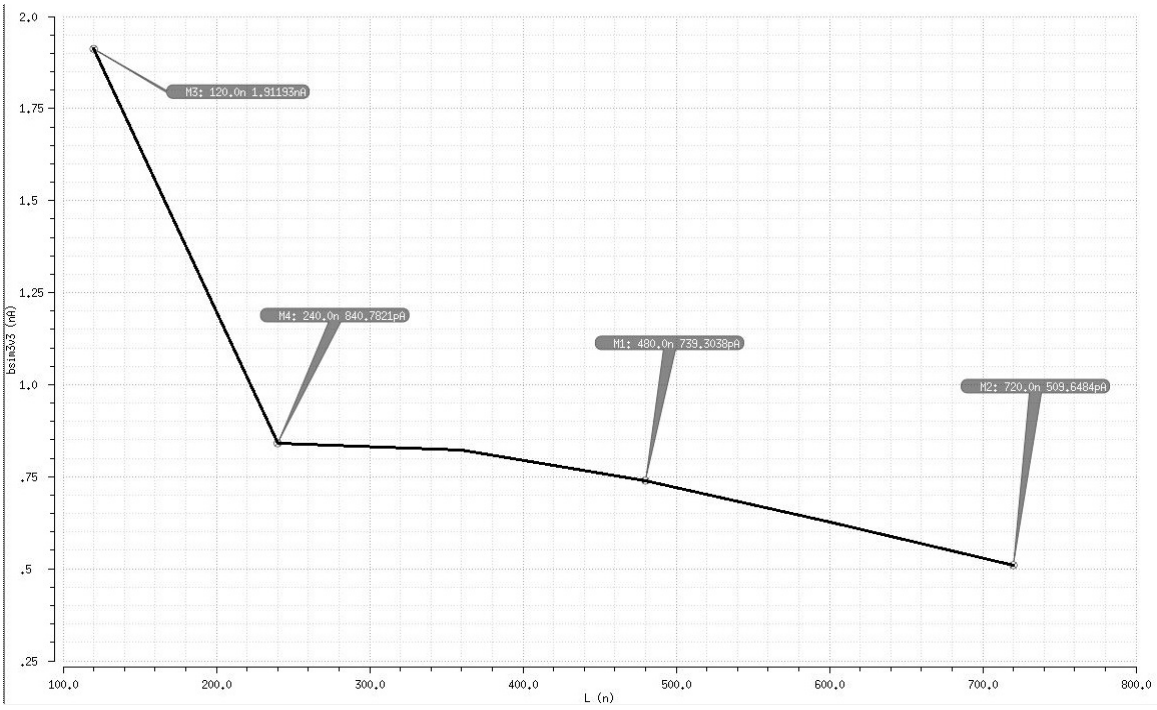

Figure 4.6 Leakage vs Length for W = 2*L

Upon simulating the single transmission gate, it is found that for a maximum leakage current of 15.62pA, the observed channel length is 1.32μm (11*L). Such a large channel length will potentially affect the overall Signal-to-noise ratio (SNR) of the ADC. Owing to the area constraints, the calculated channel length is not feasible, even though it satisfies the criteria of maximum leakage. From Figure 4.6, it is seen that the leakage decreases as the size increases and at the range of 6 times the length, the reduction becomes almost constant. Hence, for future calculations, the length of the transmission gate is fixed as 6*L where L is the default channel length. But, it is seen that the observed leakage current at 6*L is 509.6pA which is more than the calculated maximum leakage current. The width is again varied for W = 3*L and W = 4*L in Figure 4.7 and Figure 4.8 to double-check whether the range of 6*L adheres to all the cases.

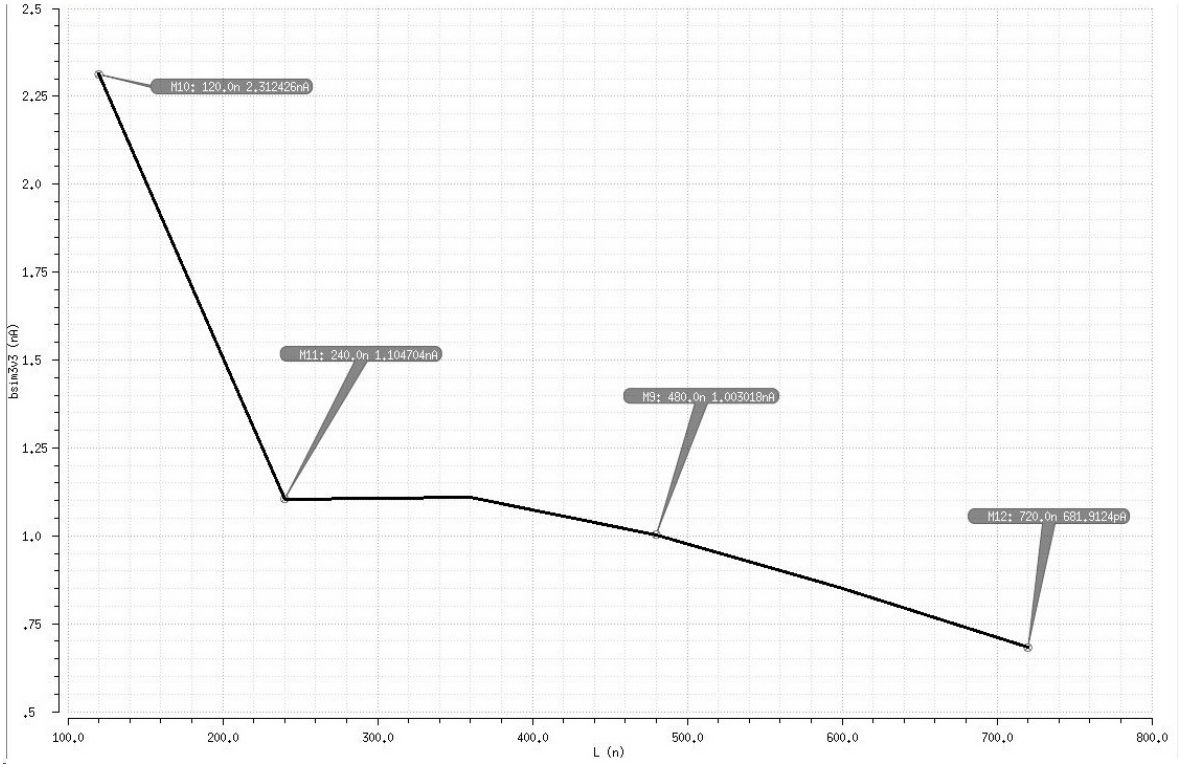

Figure 4.7 Leakage vs Length for W = 3*L

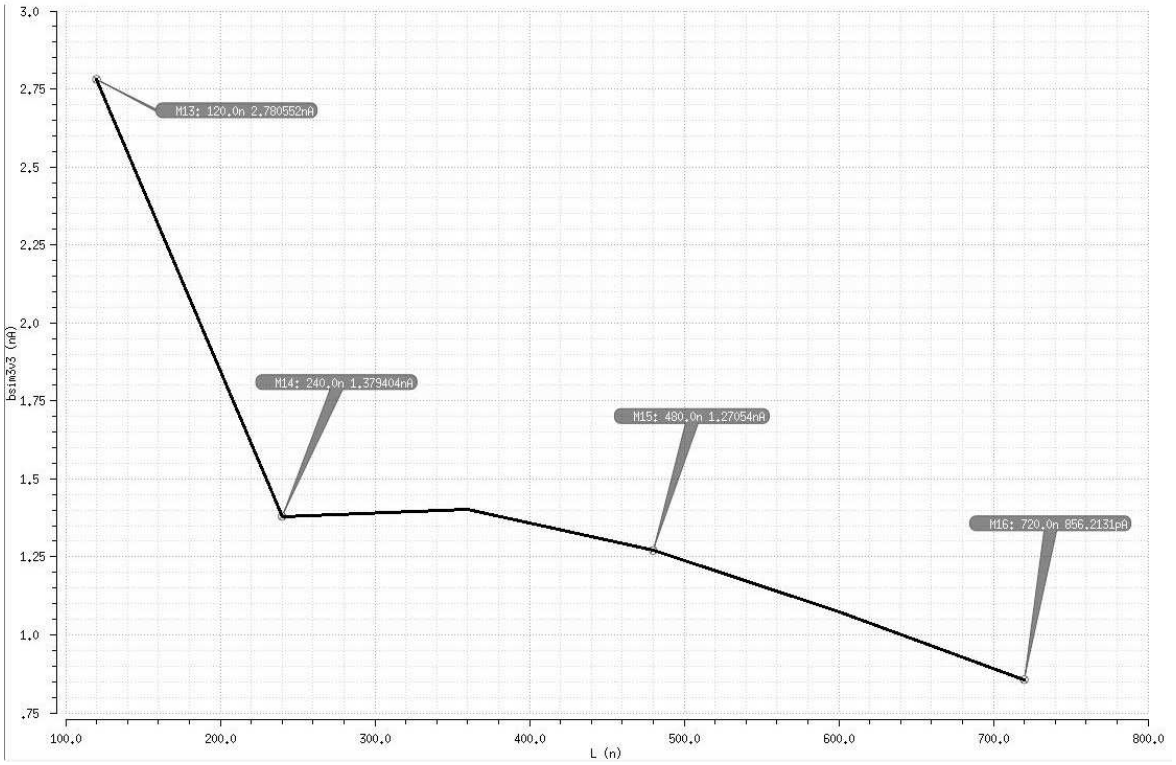

Figure 4.8 Leakage vs Length for W = 4*L

The above figures show that the leakage current becomes constant in the range of 6*L (720nm) for the single transmission gate. Hence, channel length of 3*L (360nm) for each transistor (2 X 3*L) is fixed for the stacked transmission gate which is to be employed as the ES.

In order to determine the width of the ES, the on-resistance needs to be considered. The on-resistance of the equalization switch needs to be very small to sample the input voltages and equalize the node voltages to $V_{DD}/2$. The width of PMOS

is set to two times that of NMOS for nominal sizing and the channel length is set to 3*L, as explained before.

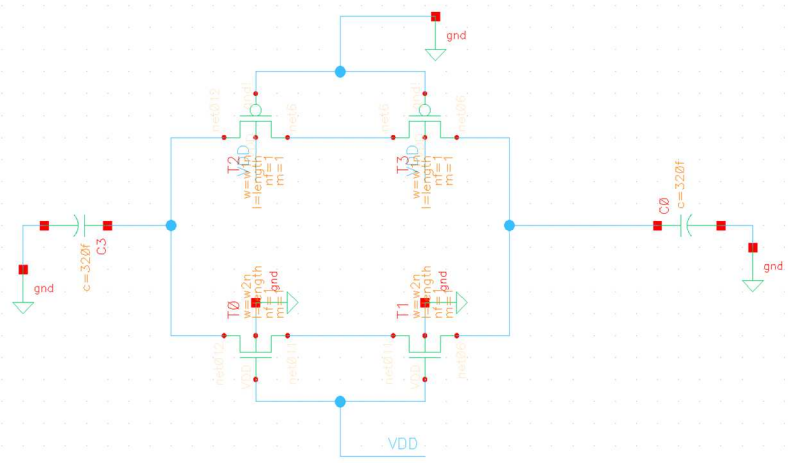

Figure 4.9 Setup to determine the on-resistance of the equalization switch

Figure 4.9 shows the setup to determine the on-resistance of the stacked transmission gate by providing low voltage for the PMOS and high voltage for the NMOS transistors. Both the total array capacitances of 320fF are connected on either side of the switch. The width of the NMOS is varied by plotting the on-resistance of the switch. Figure 4.10 shows the corresponding plot.

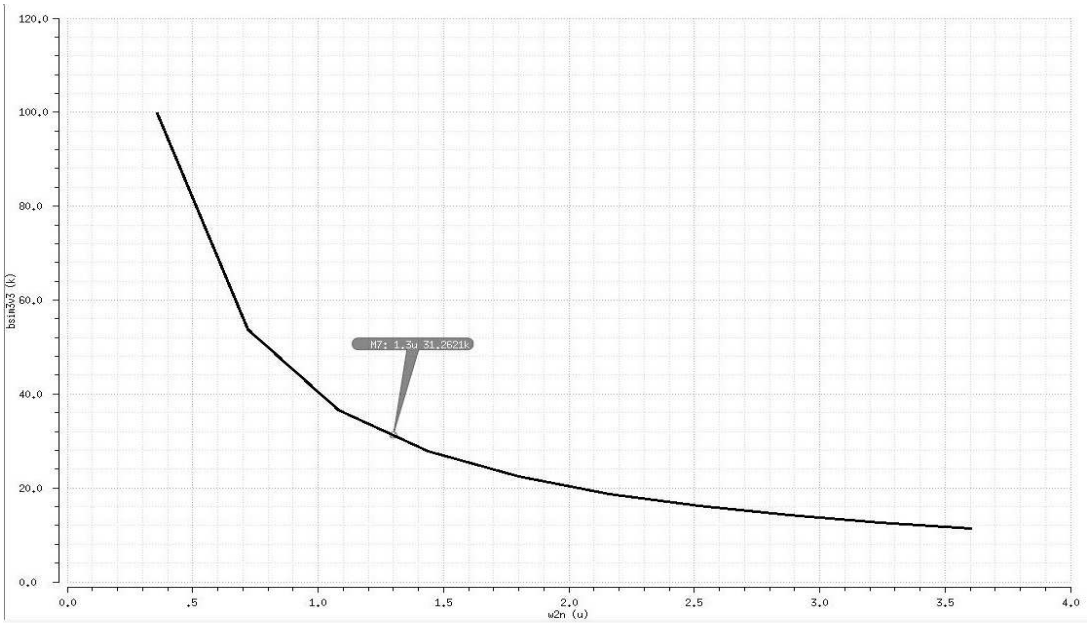

Figure 4.10 On-resistance vs Width with Length = 3*L

From the above waveform, after a certain range, the on-resistance seems to be constant or doesn't show much reduction marginally. The on-resistance reduces gradually around the range of 1μm to 2μm. Considering the settling error requirements, the condition is met for the size of 1.3μm for the NMOS (2.6μm for the PMOS). For the selected width size, the on-resistance is observed as 31.26KΩ. Further refinement of the on-resistance will be done in the future work. The settling error for the selected sizes is plotted in Figure 4.11 and tabulated in Table 4.6.

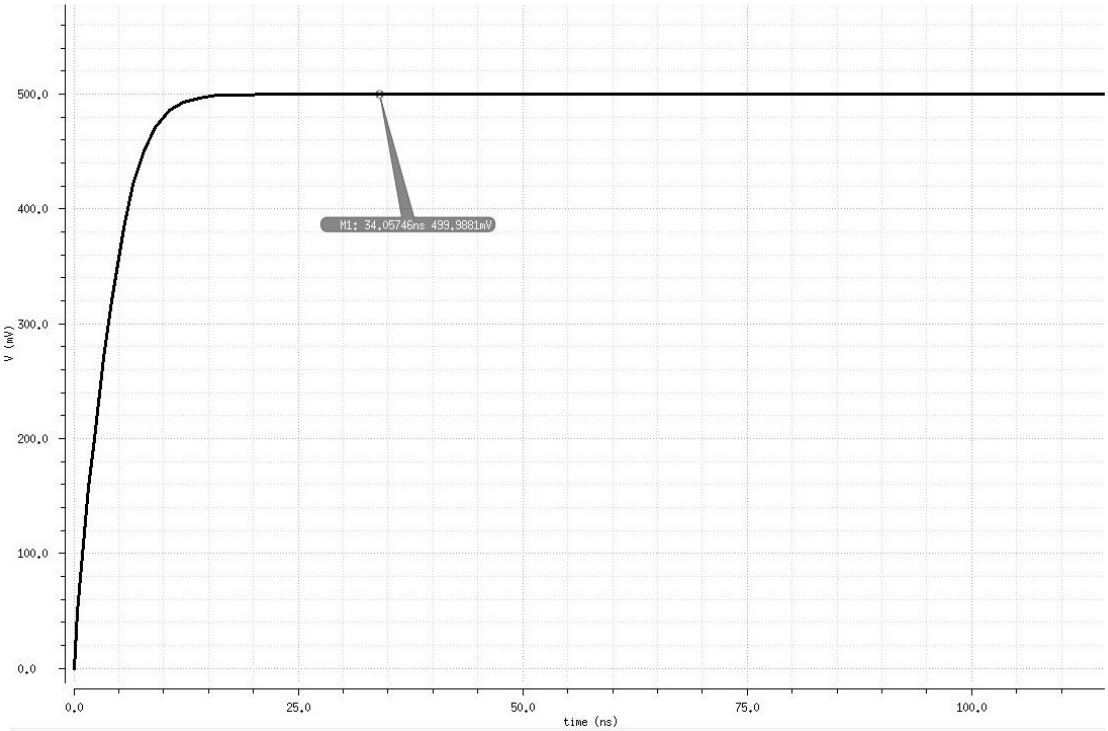

Figure 4.11 Settling error when equalization switch is on

Table 4.6 Settling error for equalization switch

TRANSITION	SETTLING ERROR (mV)
0.5V -> 0	0.013
0 -> 0.5V	0.0127

Table 4.7 Sizes of all control switches and sampling switch

ARRAY NODE	V_{DD} SWITCH (W/L)	GND SWITCH (W/L)	V_{in} SWITCH (P/N) [L=120nm]	EQUALIZATION SWITCH (P/N) [L=360nm]
LSB	320nm/120nm	160nm/120nm	640nm/320nm	2.6μm/1.3μm
MSB-3	640nm/120nm	320nm/120nm	1.28μm/640nm	
MSB-2	1.28μm/120nm	640nm/120nm	2.56μm/1.28μm	
MSB-1	2.56μm/120nm	1.28μm/120nm	5.12μm/2.56μm	
MSB	5.12μm/120nm	2.56μm/120nm	10.24μm/5.12μm	

Table 4.7 tabulates the final sizes of the V_{in}, V_{DD}, GND and equalization switches. The split capacitive digital to analog converter array voltage can be mathematically derived. The split-capacitive array operation is based on the charge conservation principle. During sampling, the charge in the capacitors equal $\left(\frac{V_{DD}}{2} - V_{in}\right) 320f$. The node voltages during conversion process are calculated as $(D.V_{ref} - V_{in})$, where V_{ref} is the reference voltage for the input voltages and D is the digital output. The comparator output is 0 if the following condition is true.

$$D^+.V_{ref} - {V_{in}}^+ > D^-.V_{ref} - {V_{in}}^- \quad (23)$$

$$V_{ref}\,(D^+ - D^-) > {V_{in}}^+ - {V_{in}}^- \quad (24)$$

Where $D^+.V_{ref} - {V_{in}}^+ = {V_{DAC}}^+$ and $D^-.V_{ref} - {V_{in}}^- = {V_{DAC}}^-$. In simple words, if ${V_{DAC}}^+ > {V_{DAC}}^-$, the output is 0. In the following discussion, we assume the sampled inputs ${V_{in}}^+$ and ${V_{in}}^-$ as 0.28V and 0.22V, respectively.

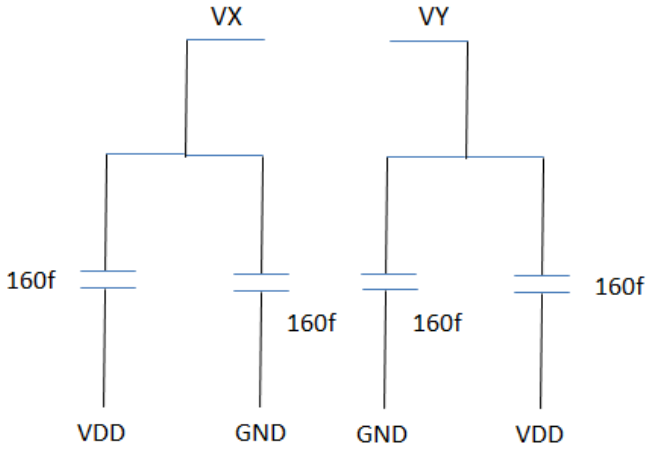

Figure 4.12 I conversion cycle

For the first cycle, the MSB capacitor is always set to 1 for one array and it is inverted for the other array, as shown in Figure 4.12. $D9$ = 1, $D8$ = 0, $D7$ = 0, $D6$ = 0, $D5$ = 0, $D4$ = 0, $D3$ = 0, $D2$ = 0, $D1$ = 0, $D0$ = 0 and $Q9$ = 0, $Q8$ = 1, $Q7$ = 1, $Q6$ = 1, $Q5$ = 1, $Q4$ = 1, $Q3$ = 1, $Q2$ = 1, $Q1$ = 1, $Q0$ = 1 (where $Q = \overline{D}$ for the other differential array).

$$\left({V_{DAC}}^{+} - V_{DD}\right)160f + {V_{DAC}}^{+}160f = \left(\frac{V_{DD}}{2} - {V_{in}}^{+}\right)320f \tag{25}$$

$${V_{DAC}}^{+} = V_{DD} - {V_{in}}^{+} = 0.22V \tag{26}$$

Similarly, ${V_{DAC}}^{-}$ can be derived as $0.28V$. From the above equation, ΔV_{in} is greater and $V_{LSB} = 1$.

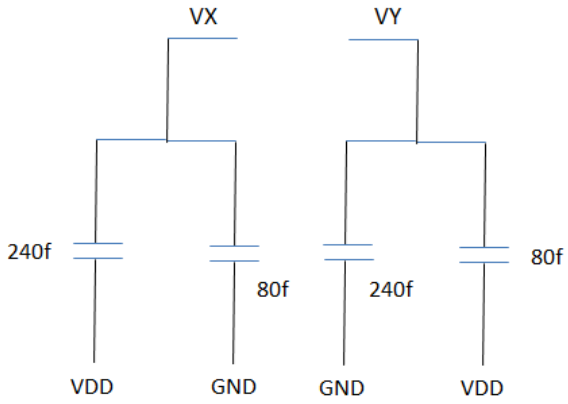

Figure 4.13 II conversion cycle

For the second cycle, MSB-1^{th} capacitor changes to 1 for the D array and MSB-1^{th} capacitor changes to 0 for the Q array (Figure 4.13). $D9$ = 1, $D8$ = 1, $D7$ = 0, $D6$ = 0, $D5$ = 0, $D4$ = 0, $D3$ = 0, $D2$ = 0, $D1$ = 0, $D0$ = 0 and $Q9$ = 0, $Q8$ = 0, $Q7$ = 1, $Q6$ = 1, $Q5$ = 1, $Q4$ = 1, $Q3$ = 1, $Q2$ = 1, $Q1$ = 1, $Q0$ = 1

$$\left({V_{DAC}}^{+} - V_{DD}\right)240f + {V_{DAC}}^{+}80f = \left(\frac{V_{DD}}{2} - {V_{in}}^{+}\right)320f \tag{27}$$

$${V_{DAC}}^{+} = \frac{5V_{DD}}{4} - {V_{in}}^{+} = 0.345V \tag{28}$$

Similarly, ${V_{DAC}}^{-} = 0.155V$. From the above equation, $V_{ref}\ (D^{+} - D^{-})$ is greater than ΔV_{in}. So $V_{LSB} = 0$.

And the DAC operation goes on so forth, based on the comparator output. Totally 10 conversion cycles are consumed for the 10-bit operation. Till the 5th bit conversion, the LSB array is considered as the termination capacitor for the MSB array conversions. From the 6th bit, the conversion mechanism differs.

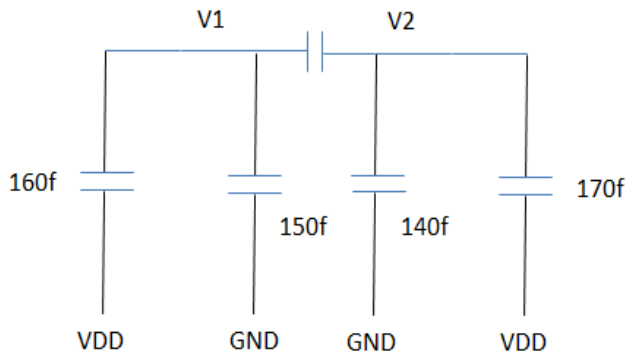

Figure 4.14 VI conversion cycle

The termination capacitor for the MSB array is the split capacitor which is 10fF and there is no need for a termination capacitor for the LSB array, as seen in Figure 4.14. The node voltage $V2$ is calculated as per the below equation.

$$V2 = \frac{V_{DD}}{2} - {V_{in}}^{+} + \frac{1}{1-\left(\frac{1}{2^{10}}\right)}\left[\frac{170}{320}V_{DD} + \frac{10}{320}.\frac{160}{320}V_{DD}\right] \quad (29)$$

$V2$ (${V_{DAC}}^{+}$ of 6th cycle) was calculated as 0.2439V and $V2$ for the other differential array is calculated 0.2557V. Similarly the voltages for the other 4 cycles are calculated.

The node voltages of both the arrays ${V_{DAC}}^{+}$ and ${V_{DAC}}^{-}$ are calculated for the above input voltages. Along with that, the observed or simulated node voltages are also tabulated in Table 4.8 and the comparator output is also given.

Table 4.8 Node voltages and comparator outputs for DAC array operation

CONV. CYCLE	CALCULATED VALUES		SIMULATED VALUES		COMP. OUTPUT
	$V_{DAC}{}^{+}$ (V)	$V_{DAC}{}^{-}$ (V)	$V_{DAC}{}^{+}$ (V)	$V_{DAC}{}^{-}$ (V)	
SAMPLING	0.249	0.249	0.249	0.249	**X**
I	0.2207	0.2788	0.2211	0.2791	**1**
II	0.344	0.155	0.344	0.155	**0**
III	0.282	0.217	0.284	0.218	**0**
IV	0.2516	0.2479	0.2520	0.2482	**0**
V	0.2362	0.2634	0.2366	0.2637	**1**
VI	0.2439	0.2557	0.2443	0.2559	**1**
VII	0.2478	0.2518	0.2482	0.2521	**1**
VIII	0.2497	0.2499	0.25018	0.25019	**1**
IX	0.2507	0.2489	0.2511	0.2492	**0**
X	0.2502	0.2494	0.2506	0.2497	**0**

The final output for the differential input of 60mV (0.28V and 0.22V) is 59.08203125mV (1000_1111_00). In this split-capacitor array DAC, the output voltage $V_{DAC}{}^{+}$ is given to the negative input of the comparator and $V_{DAC}{}^{-}$ is given to the positive input due to the following equations.

$$V_{DAC}{}^{+} = \frac{V_{DD}}{2} - V_{in}{}^{+} - D.V_{ref} \quad (30)$$

$$V_{DAC}{}^{-} = \frac{V_{DD}}{2} - V_{in}{}^{-} - \bar{D}.V_{ref} \quad (31)$$

$$V_{DAC}{}^{+} - V_{DAC}{}^{-} = (\overline{D} - D).V_{ref} - (V_{in}{}^{+} - V_{in}{}^{-}) \quad (32)$$

[Where $V_{ref} = V_{DD}$ and $D^{+}.V_{ref} - V_{in}{}^{+} = V_{DAC}{}^{+}$ and $D^{-}.V_{ref} - V_{in}{}^{-} = V_{DAC}{}^{-}$]. The complete architecture of the split-capacitive charge-scaling differential DAC array is shown in Figure 4.15.

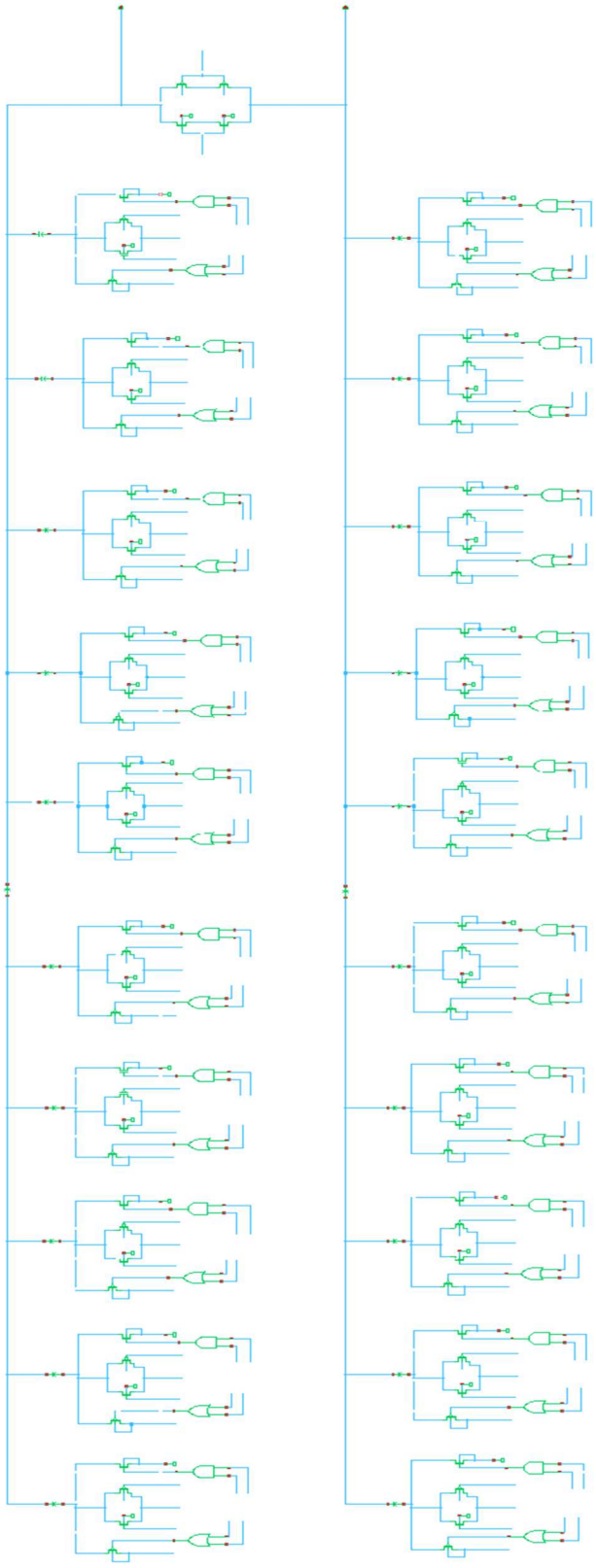

Figure 4.15 Split-capacitive DAC array schematic

4.2 VOLTAGE CONTROLLED DELAY LINES

The current-starved technique is used to design a series of inverter chains, known as Voltage Controlled Delay Lines (VCDL). It is implemented by cascading two types of delay cells, which are basically inverters with current limiting capability. The VCDL used in the design is shown in Figure 4.16. It consists of 10 stages and its control voltage inputs are from the charge scaling DAC. The currents of all the delay cells with odd position numbers are limited by NMOS devices, whose gates are controlled by input $V_{DAC}{}^{+}$. Meanwhile, the delay cells in even positions have PMOS current limiting devices controlled by input $V_{DAC}{}^{-}$. Hence, the total delay of the VCDL is controlled by $V_{DAC}{}^{+} - V_{DAC}{}^{-}$.

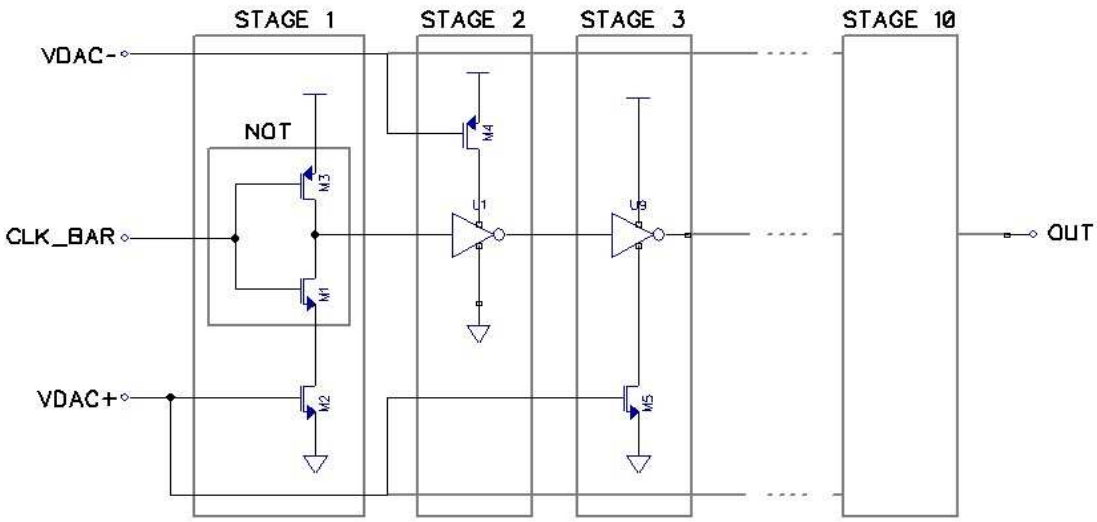

Figure 4.16 Block diagram of Voltage Controlled Delay Line

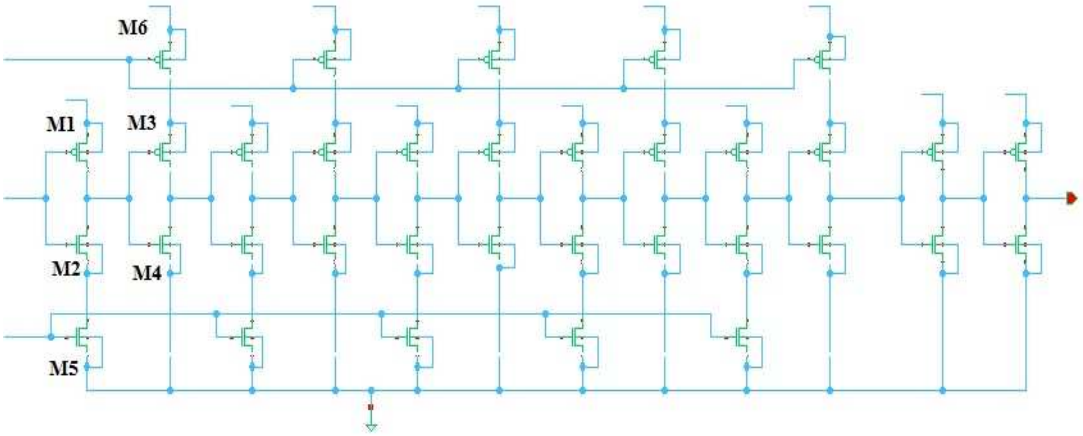

Figure 4.17 Simulated 10-stage VCDL

Proper sizing of the inverters is ensured so as to maintain the linear increase in sensitivity of temperature and process variation. Minimum sizes are used for the CMOS and a ratio of 2:1 is maintained throughout. The sizes for the respective transistors are tabulated in Table 4.9.

Table 4.9 Transistor sizes in VCDL

TRANSISTOR	SIZE (nm)
M1, M2	320/120
M3	640/120
M4	160/120
M5	320/120
M6	640/120
INVERTER PMOS	320/120
INVERTER NMOS	160/120

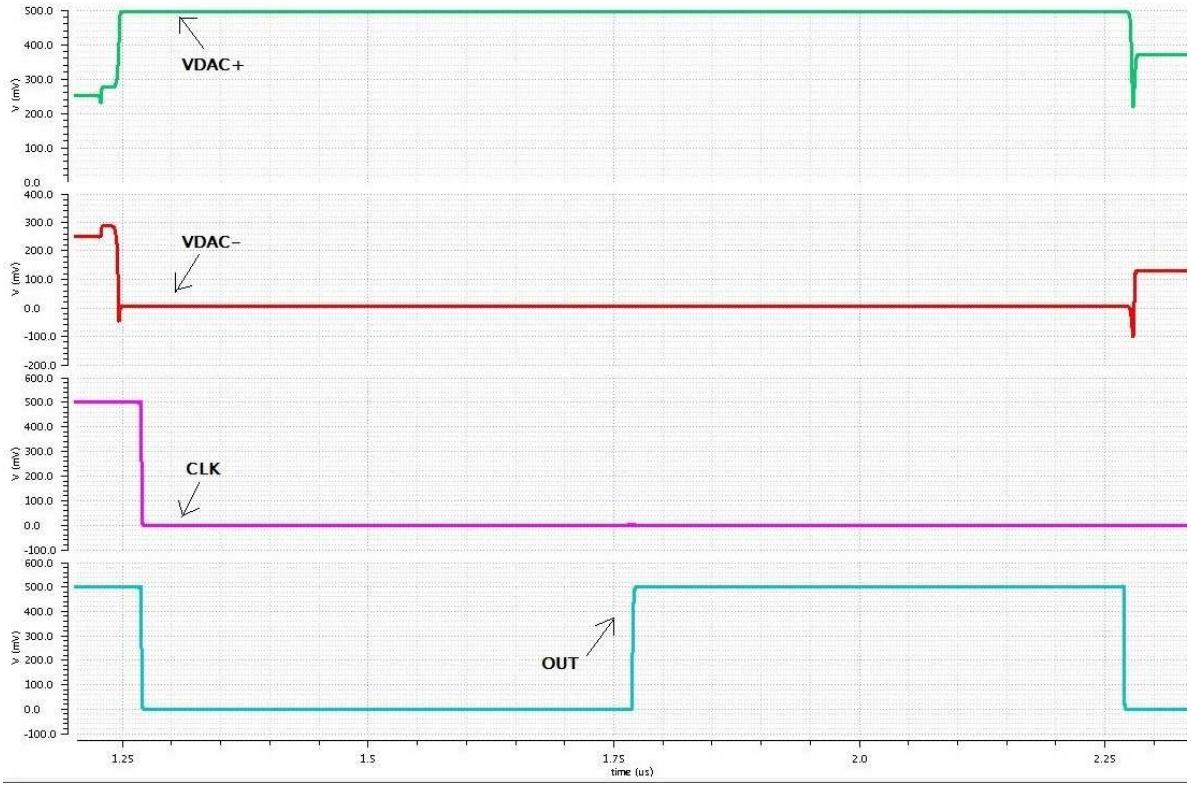

Figure 4.18 Output waveform of VCDL

Figure 4.18 shows the inputs $V_{DAC}{}^{+}$ and $V_{DAC}{}^{-}$ along with the clock input. As seen in the figure, the output waveform rises after a considerable delay from the 10-stage VCDL. The VCDL is simulated at different process corners such as SS, FF and TT corners. The plot is shown in Figure 4.19.

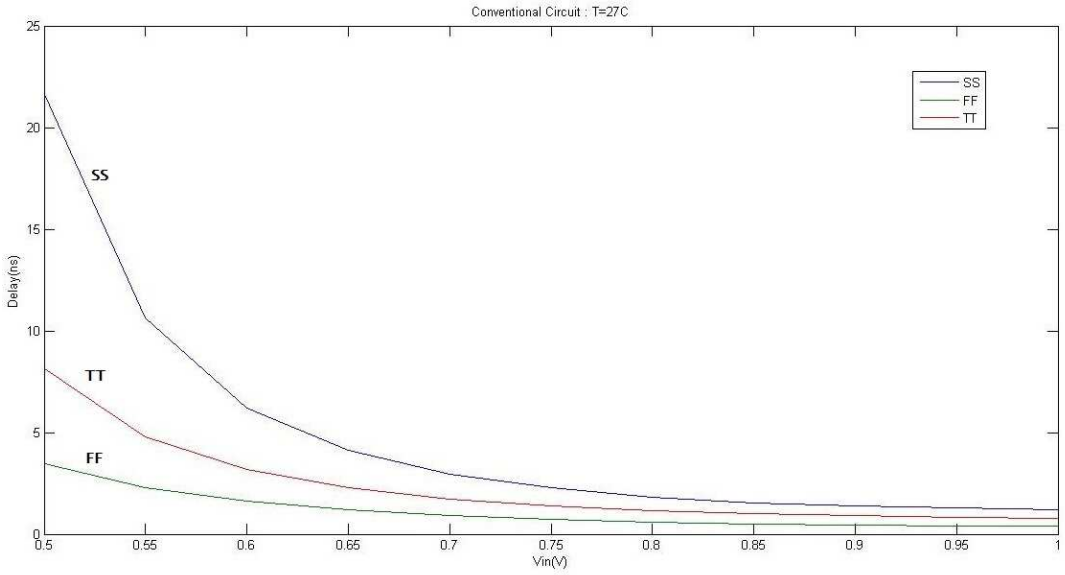

Figure 4.19 Plot showing simulated VCDL for SS, FF and TT process variations

Referring to the VCDL, (Figure 3.2) the portion of the VCDL whose delay is compared with the delay of the entire VCDL by the auxiliary PDs, consists of two delay stages. Circuit simulations have been performed at different process corners as well as different temperatures to find the input voltage values of the VCDL that result in the delay of the portion of VCDL being larger than the entire VCDL delay. Table 4.10 lists the obtained voltages that are rounded and expressed in terms of V_{LSB}.

Table 4.10 Simulated voltages to determine uBand in terms of V_{LSB}

PROCESS CORNERS	**TEMPERATURE (℃)**		
	0	**25**	**85**
TT	64	70	86
FF	68	74	93
SS	63	68	82

Note that the maximum and minimum values are $63V_{LSB}$ and $93V_{LSB}$, respectively. Thus, the uBand V_{δ} is $93V_{LSB}$ - $63V_{LSB}$ = $30V_{LSB}$. In the design, we select the enforced uBand as V_{Δ} = $34V_{LSB}$ and select V_A = $62V_{LSB}$. So, A+B = $V_{\Delta} + V_A$ = $96V_{LSB}$ and B = $62V_{LSB}$.

4.3 BINARY PHASE DETECTOR

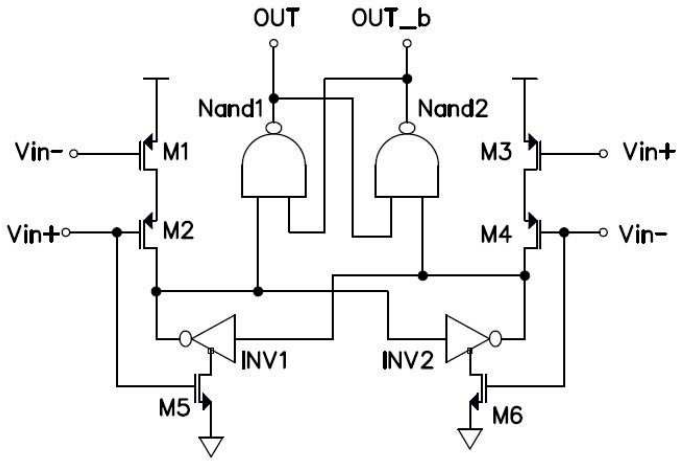

Figure 4.20 Block diagram of Phase Detector [39]

An offset-free analog binary phase detector is used for the detection and comparison of the delay generated from the VCDL. This PD works fast than a flip-flop and eliminates setup/hold time. From Figure 4.20, INV1 and INV2 form a latch-type amplifier that senses the incoming input signals Vin^{+} and Vin^{-}. Transistors M5 and M6 are in series with the discharging path of the inverters. So when inputs are low, M5 and M6 are off thereby disabling the inverters. PMOS M1 – M4 raise the cross-coupled nodes to V_{DD}. When one input raises to V_{DD} before the other, the inverter connected with

it starts to discharge, thereby completing the comparison. The output is stored by the latch of $Nand1$ and $Nand2$. The sizes of transistors for the PD are tabulated in Table 4.11 and the designed schematic is shown in Figure 4.21.

Table 4.11 Transistor sizes in PD

TRANSISTOR	SIZE (nm)
M1, M2	1280/120
INVERTERS, M5	640/120
NAND GATE PMOS	320/120
NAND GATE NMOS	320/120

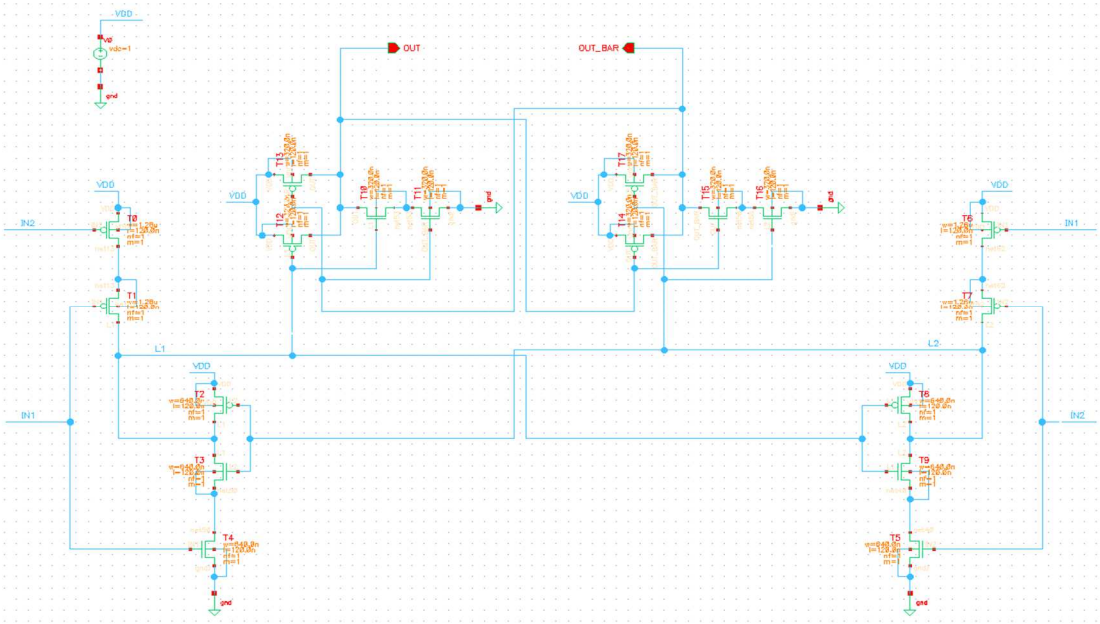

Figure 4.21 Final schematic of PD

Figure 4.22 shows the output of the PD. The first two signals are the PD inputs and third is the output. Clearly, the output is 1 since the positive input, $V_{in}{}^{+}$, rises first.

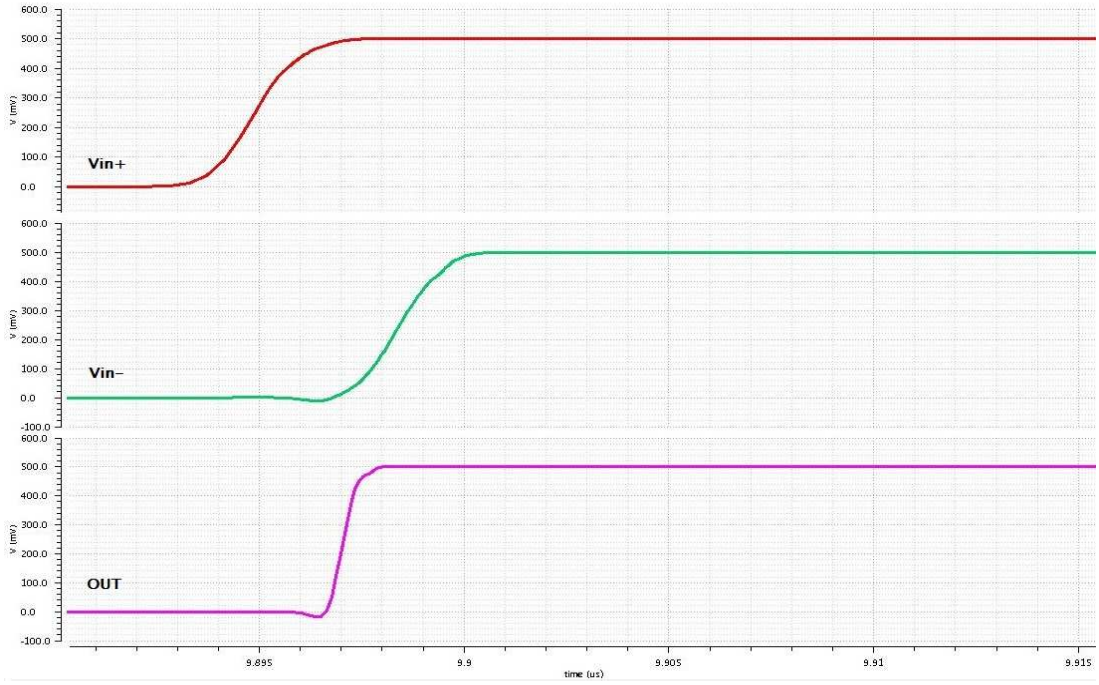

Figure 4.22 Output waveform of PD

4.4 DESIGNED DIGITAL BLOCKS OF A-SAR

Few of the designed blocks of the LB, UB update circuit and Digital code update circuit are shown in this section. Signal O_EN is used to initialize the output register to generate the final digital output of the A-SAR and the $DONE$ signal is used to mark the end of the conversion process, which are also shown.

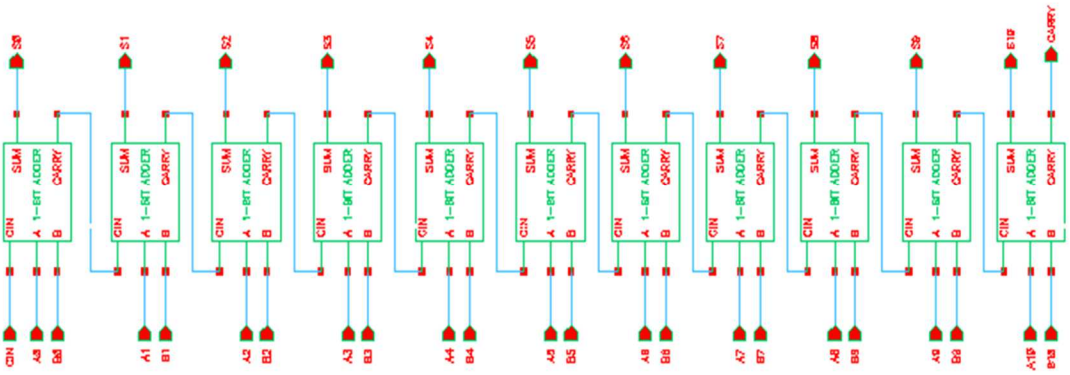

Figure 4.23 11-bit adder schematic

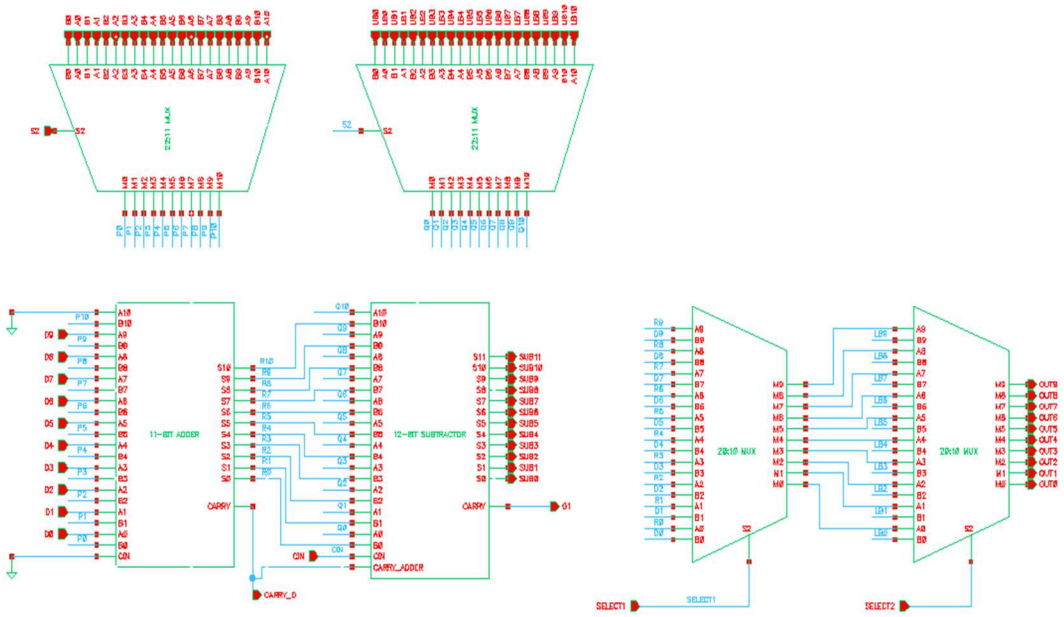

Figure 4.24 LB update circuit

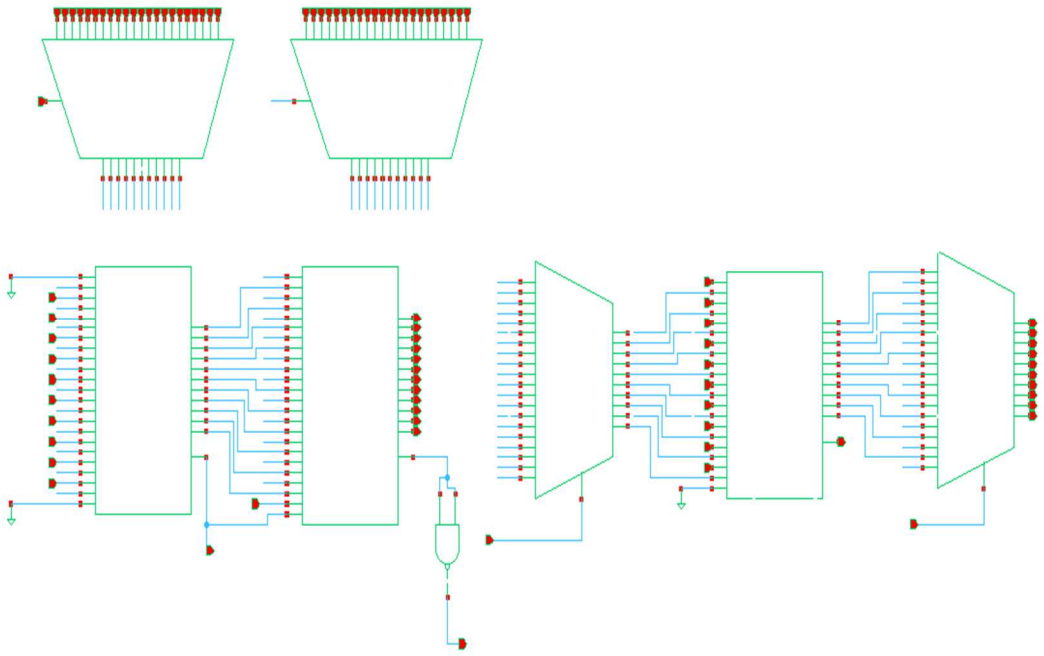

Figure 4.25 UB update circuit

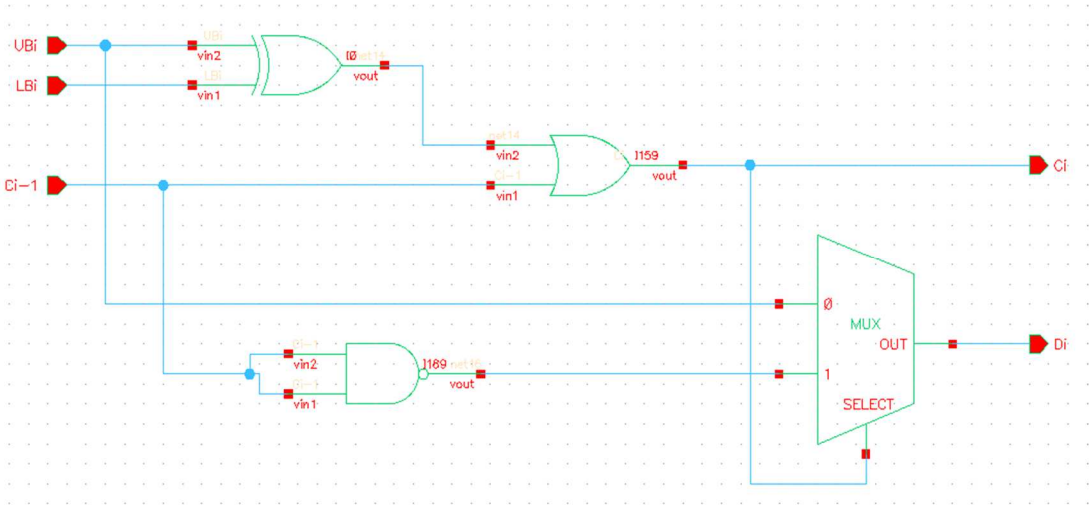

Figure 4.26 Digital code update circuit schematic

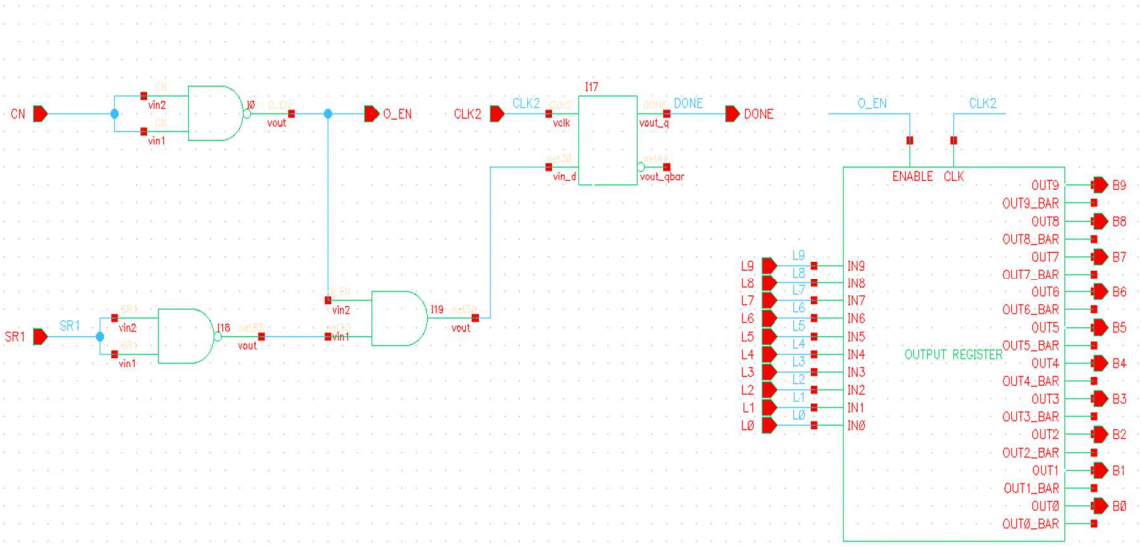

Figure 4.27 Schematic showing O_EN, $DONE$ and output register

The complete architecture and schematic of the Accelerated Successive Approximation Technique is given in Figure 4.28. It consists of the input signals, control signals, Digital to Analog Converter, Voltage Controlled Delay Line and Phase Detector, LB and UB update circuits, LB and UB registers, Digital code update circuit and the output register blocks. The inputs of the A-SAR will be ${V_{in}}^{+}$, ${V_{in}}^{+}$, CLK and $RESET$ and the outputs will be the 10-bit digital output $D_9,\ D_8,\ D_7 \ldots . D_0$, O_EN and $DONE$ signals.

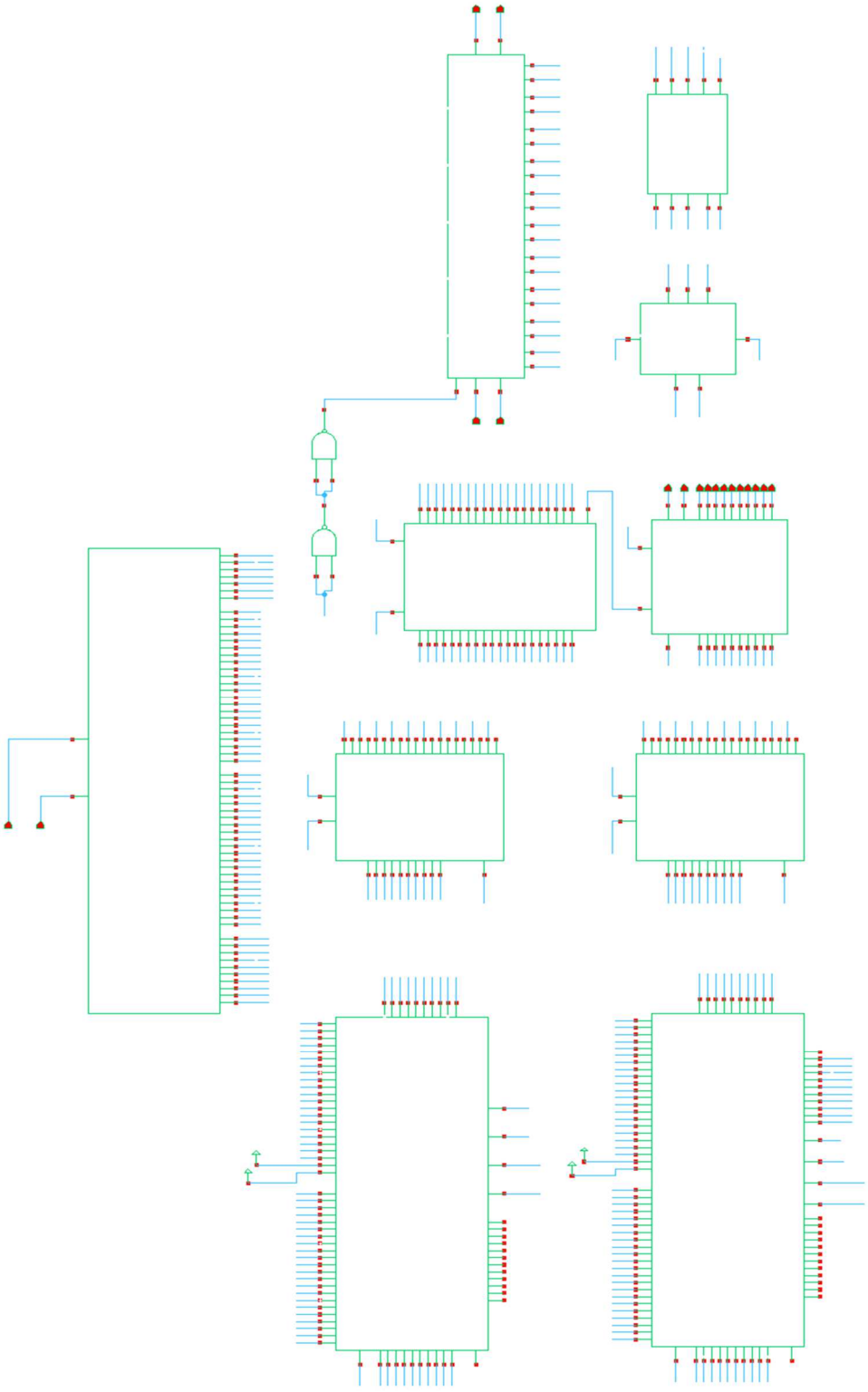

Figure 4.28 Complete A-SAR schematic

4.5 SIMULATION RESULTS

The implemented ADC is simulated with a 0.5V power supply with 100 KS/s sampling rate. Also, the ADC input range is from rail to rail. Figure 4.29 shows a conversion for inputs $V_{in}{}^{+} = 0.28V$ and $V_{in}{}^{-} = 0.22V$. So the differential input is $60mV$ and corresponding digital output code is 1000_1111_00. As one can see, the final ADC output code is obtained after the eight clock cycle itself, and the $DONE$ signal rises immediately showing that the conversion is complete. The ADC being structured for 10-bit resolution produces the output in two cycles less than the stipulated number of conversion cycles. The 10-bit waveforms are labeled as $D_1, D_2 \ldots D_{10}$ where D_1 is the MSB and D_{10} is the LSB. The first clock period is the sampling phase and it is controlled by $S0$ from the shift register, which is controlled by $CLK1$. This samples the input voltage in the capacitors which will be used for the conversion process in the following clock periods. Once the sampling is done, the conversion starts. At the first conversion cycle, the SAR register is set to 1000_0000_00, which is identical to a conventional SAR ADC. Clearly, the A-SAR technique approaches the final ADC output code more quickly.

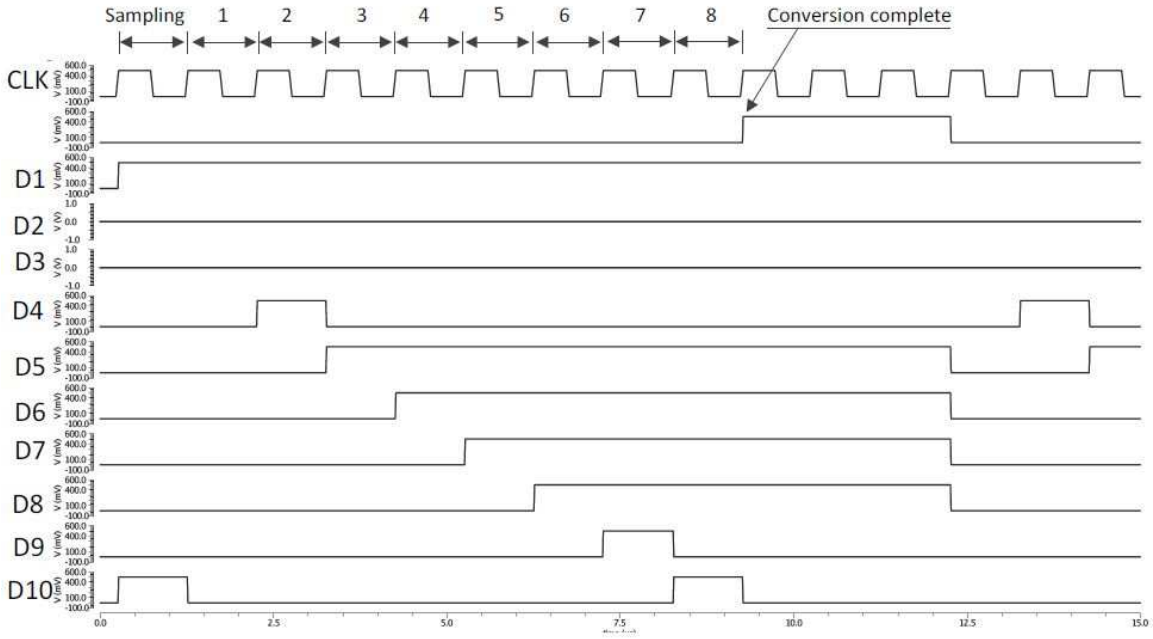

Figure 4.29 A-SAR output waveform

4.5.1 POWER CONSUMPTION

The power consumption of an SAR ADC circuit is dominated by its analog blocks, especially its charge scaling DACs [44]. In this section, the average power consumptions of the analog blocks in the A-SAR and a conventional VTC-based SAR ADC are compared. The two ADCs used in the comparison have the same DAC, VCDL and PD circuits, except that only one PD is used in the conventional ADC. The clock frequency for both the ADCs is 1MHz and power supply is 0.5V.

Table 4.12 Table showing power consumption for each block in A-SAR

COMPONENTS	CONV. SAR ADC (nW)	A-SAR ADC (nW)	POWER SAVING (%)
DAC	53.7 nW	42.2 nW	**21.4%**
VCDL	13 nW	14.5 nW	**-11.5%**
PD	2.1 nW	5.2 nW	**-148%**
TOTAL	**68.8 nW**	**61.9 nW**	**10%**

Table 4.12 lists the power values of the components obtained from circuit simulations. It clearly shows that the DAC power consumption dominates the overall power consumption. The proposed A-SAR reduces the DAC power consumption by 21.4%, mainly due to the reduction in number of clock cycles. The VCDL consumes more power in the A-SAR circuit since it has additional output loads. Also, the proposed ADC has three PD circuits and hence the total power consumption of the three PDs is much higher than the single PD power consumption in the conventional ADC. Also it is to be noted that the PD power consumption is not tripled due to the uncertainties. Due to the dominance of the DAC in power consumption, the overall power consumption is still reduced in the A-SAR by 10%, as mentioned in Table 4.12. And it should be noted that the unit capacitance is 10fF. In designs which use more unit capacitance, the overall power saving can be much higher.

4.5.2 SNR

The Signal-to-Noise Ratio of the ADC is evaluated. Every digital output from the end of the conversion is captured using a write module and the set of digital codes is written into a text file. The swing of the sinusoidal wave is from $-V_{DD}$ to V_{DD}. A total of 1024 points or more are considered for the calculation. To calculate the input frequency of the sinusoidal waveform, the following equation is considered:

$$\frac{f_{in}}{f_s} = \frac{137}{1024} \tag{33}$$

where f_s is the sampling frequency of the ADC, which is 100KHz, and f_{in} is the input frequency for the sinusoidal inputs. From the above equation, the input frequency is calculated as $f_{in} = 13.405539772727KHz$. The sinusoidal input is differential and the signals are at a phase difference of 180. The SNR is seen as 43.43dB and SNDR as 43.01dB (Figure 4.30).

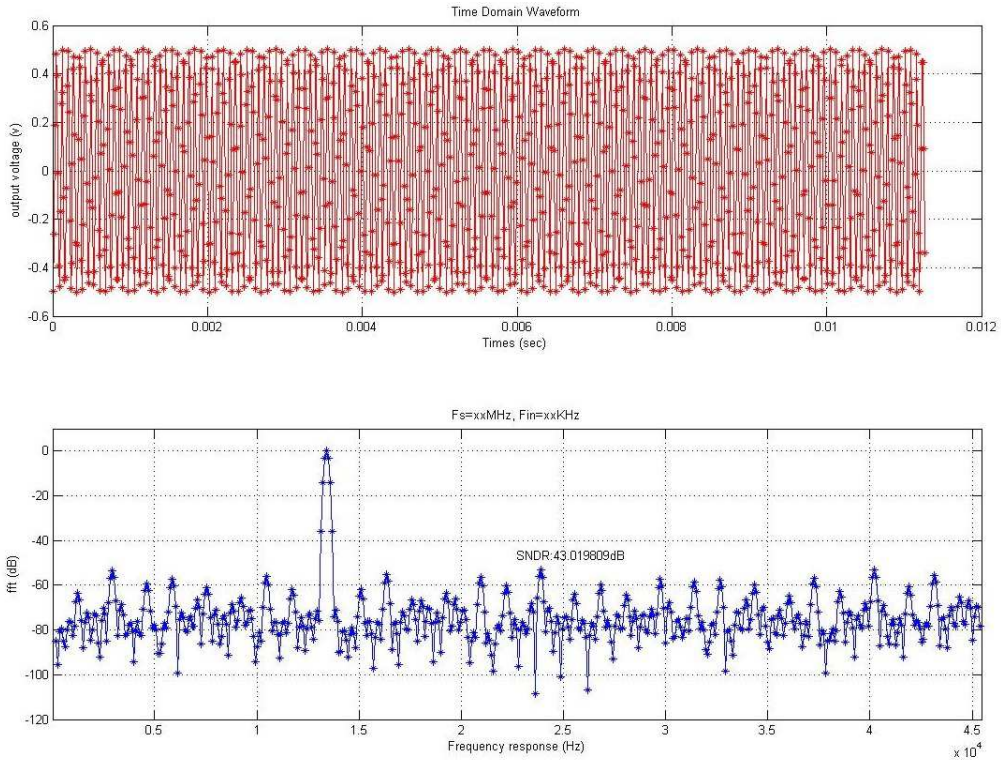

Figure 4.30 SNR of the A-SAR

The effective number of bits (ENOB) is calculated as 6.85 according to the relation:

$$ENOB = \frac{SNDR - 1.76dB}{6.02} \quad (34)$$

4.5.3 INL / DNL

The Differential Non-linearity (DNL) and Integral Non-linearity (INL) of the A-SAR is calculated by providing a ramp input signal from 0 to V_{ref} for 9 occurrences of each conversion. A pulse-width-linear (V_{PWL}) is given as input where at time t=0, the voltage is 0V. The final time is calculated through 9 occurrences * 11 cycles each (1 sampling and 10 conversions) * 1024 conversions, which is 101.376ms, where the voltage is V_{ref}. A sample input is shown below:

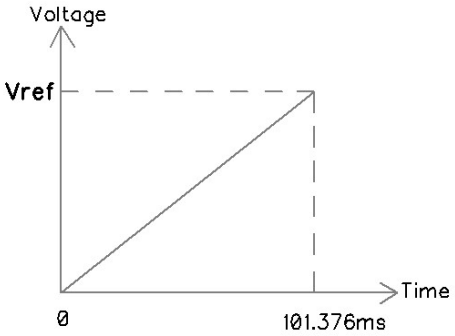

Figure 4.31 Ramp signal to calculate INL/DNL

The output provides a linearly increasing output code with 9 occurrences for each code. It is dumped into a text file and simulated through MATLAB. FFT analysis is performed on the output. Ideally, the difference between each of the codes is V_{LSB}. The maximum/minimum DNL stands at +0.1106/-0.1115 V_{LSB} and the maximum/minimum INL stands at +3.0000/-0.6681 V_{LSB}. Both the corresponding plots are shown below:

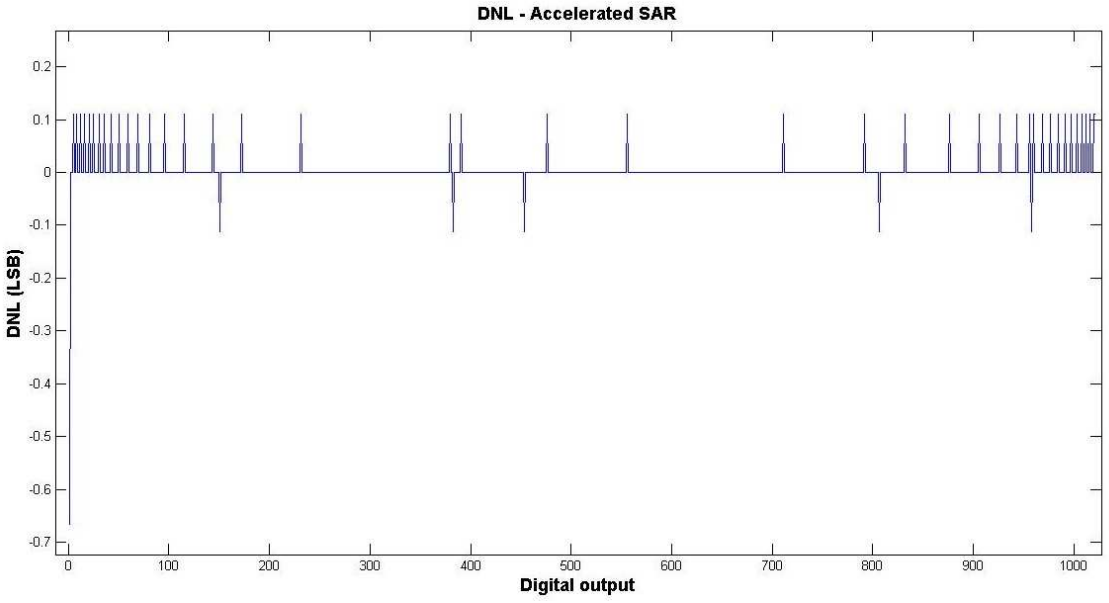

Figure 4.32 DNL of A-SAR

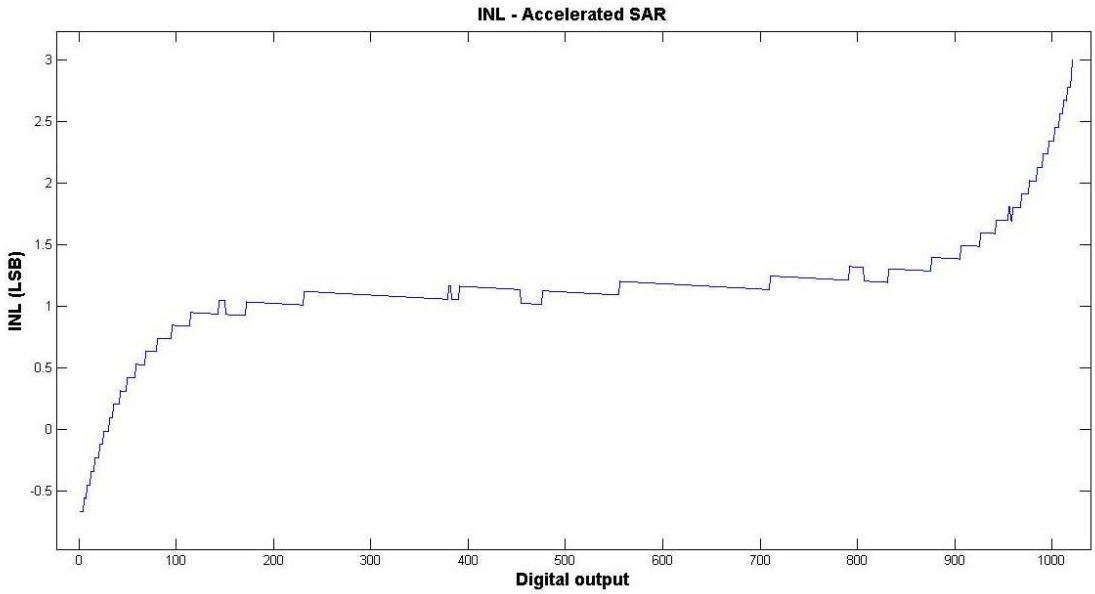

Figure 4.33 INL of A-SAR

4.5.4 REDUCED NUMBER OF CONVERSION CYCLES

The output of the A-SAR is simulated for 1024 conversions and the number of each conversion cycles, in which the output is generated, is seen. In particular, the $DONE$ signal is seen for every operation. Clock cycles of 10, 8 and 7 were seen as a result. The percentage split for the corresponding data is tabulated in Table 4.13.

Table 4.13 Percentage split of number of conversions

NO. OF	PERCENTAGE
10	**67.578%**
9	**0%**
8	**10.644%**
7	**21.778%**

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

This thesis work presents a novel technique to reduce the number of conversion cycles in an SAR ADC, thereby making it faster. As a result, output can be generated in less than N clock cycles for an N-bit SAR ADC by this method which is called as the Accelerated Successive Approximation Register (A-SAR) technique. Compared to a conventional SAR ADC which updates only one bound, either the upper or lower bound, in a single conversion cycle, the proposed technique updates both the upper and lower bounds in a single conversion cycle, thereby producing the digital output much sooner than the conventional counterpart. Circuit techniques to implement the A-SAR technique are also developed and implemented using a 0.13μm CMOS technology. The validity of the proposed technique is demonstrated by circuit simulation results.

The proposed ADC topology has three phase detectors (PD). However, there are only four valid combinations of the three PD outputs. This leads to an interesting opportunity to perform online built-in-self-testing (BIST) operation for the ADC circuits, which will be investigated in our future works. Also, the SNR of the implemented ADC is much lower than the ideal value. Additional circuit optimization is needed to reduce the leakage of equalization switch and potentially improve the ADC performance. Furthermore, the layout of the circuit can be designed for fabrication and subsequently hardware measurements can be conducted to characterize the ADC performance.

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