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Published in:

I E E E Microwave and Wireless Components Letters

DOI (link to publication from Publisher):

[10.1109/LMWC.2014.2332057](https://doi.org/10.1109/LMWC.2014.2332057)

Publication date:

2014

Document Version

Peer reviewed version

[Link to publication from Aalborg University](#)

Citation for published version (APA):

Shen, M., Yin, Y-Z., Jiang, H., Tong, T., & Mikkelsen, J. H. (2014). A 3-10 GHz IR-UWB CMOS Pulse Generator With 6-mW Peak Power Dissipation Using A Slow-Charge Fast-Discharge Technique. I E E E Microwave and Wireless Components Letters, 24(9), 634-636. DOI: 10.1109/LMWC.2014.2332057

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A 3-10 GHz IR-UWB CMOS Pulse Generator With 6-mW Peak Power Dissipation Using A Slow-Charge Fast-Discharge Technique

Ming Shen, *Member, IEEE*, Ying-Zheng Yin, Hao Jiang, Tong Tian, and Jan H. Mikkelsen, *Member, IEEE*

Abstract—This letter proposes a UWB pulse generator topology featuring low peak power dissipation for applications with stringent instantaneous power requirements. This is accomplished by employing a new slow-charge fast-discharge approach to extend the time duration of the generator’s peak current so that peak value of the current is significantly reduced, while maintaining the waveform of the generated UWB pulse signal. A prototype pulse generator has been implemented using the UMC 0.18 μm CMOS process for validation. The pulse generator offers a 3-10 GHz bandwidth, a maximum pulse repetitive rate of 1 Gpps, a minimum peak power consumption of 6 mW, and a low energy consumption of 5 pJ/pulse. The fabricated pulse generator measures 0.16 mm².

Index Terms—Charge, discharge, IR-UWB, pulse generator, peak power dissipation.

I. INTRODUCTION

IMPULSE radio ultra wideband (IR-UWB) has been considered a promising technology for short range applications with stringent power consumption requirements, such as battery-less wireless sensor networks (WSN) based on energy harvesting [1], [2]. In an IR-UWB system the pulse generator is the key component in generating short pulses for low duty cycle operation and low power consumption. Thus it has attracted considerable research attention in recent years [3]–[7]. According to FCC’s regulation, a UWB signal should have a minimum bandwidth of 500 MHz or a minimum fractional bandwidth of 20% [8]. Therefore the time duration of a UWB pulse signal is usually at the order of 1-2 ns or less. Existing UWB pulse generators based on CMOS circuits can easily achieve pulse widths of a few hundreds ps due to the fast switching capability of CMOS transistors [3]–[7]. However, CMOS circuits mainly dissipate power during switching. This results in a high peak power dissipation typically at the order of tens of mW or higher (90 mW in [4]). For devices powered by energy harvesters, which usually only can provide an output power at the order of a few mW or less [2], the peak power dissipation in existing designs is too high. As

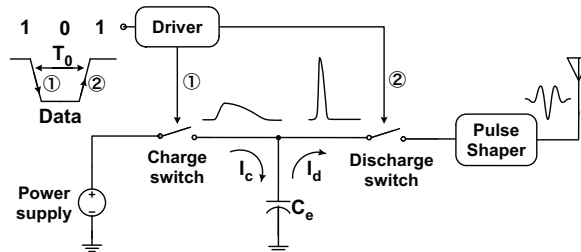


Fig. 1. The proposed IR-UWB pulse generator topology.

a consequence high performance power management circuits, big energy storage capacitors and long energy storage time are required (250 μF and charging time of 13 seconds in [1]), which lead to high cost and low feasibility. To enable low cost implementation of battery-less WSN nodes based on energy harvesting, UWB pulse generators with not only low average power consumption but also low peak power consumption are highly desired. This paper proposes a circuit topology for the implementation of UWB pulse generators aiming at both low instantaneous power dissipation and low energy consumption per pulse. A slow-charge fast-discharge approach is used to reduce the peak of the power supply current, while the energy consumption per pulse is minimized as well.

II. THE PROPOSED UWB PULSE GENERATOR

The proposed IR-UWB pulse generator topology is shown in Fig. 1. It consists of an energy storage capacitor, C_e , two switches, a driver stage and a pulse shaper. This topology is suitable for on-off keying (OOK) with return-to-zero coding. At every falling edge of the input data, the charge switch is turned on and starts charging C_e during the period of T_0 (stage ① in Fig. 1) while the discharge switch is off. And at every rising edge of the input the discharge switch is turned on to discharge the stored energy (stage ②) with a short time discharge current I_d . I_d is then fed to a pulse shaper and subsequently the antenna. The pulse shaper is a high pass filter that reduces the low frequency spectrum components of the generated UWB pulse signal to fulfill FCC’s mask. It should be noted that the starting time of charging and discharging are separated with a time interval of T_0 . Therefore the charging can be done slowly during the whole period of T_0 , resulting in a low peak value of the current. Different from existing duty cycled systems, where the energy is stored for a burst of data, the proposed approach stores energy

Manuscript received January 27, 2014; revised April 17, 2014; accepted June 12, 2014. Date of publication **, **, 201*; date of current version **, **, 201*. This study was supported by the Danish Research Council for Technology and Production Sciences (FTP).

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Digital Object Identifier ***

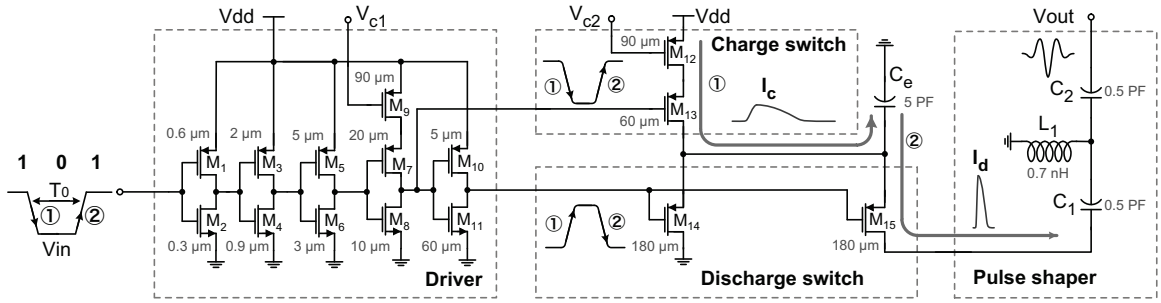


Fig. 2. CMOS implementation of the proposed IR-UWB pulse generator topology in Fig. 1.

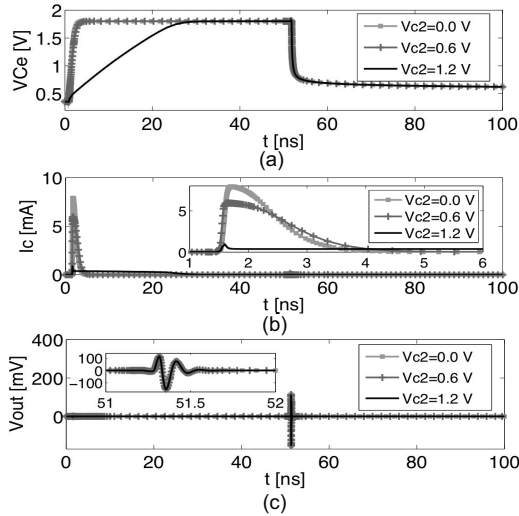


Fig. 3. Simulated (a) voltage on C_e , (b) charging current and (c) the generated UWB pulse waveform ($V_{c1} = 0$, $T_0 = 50$ ns).

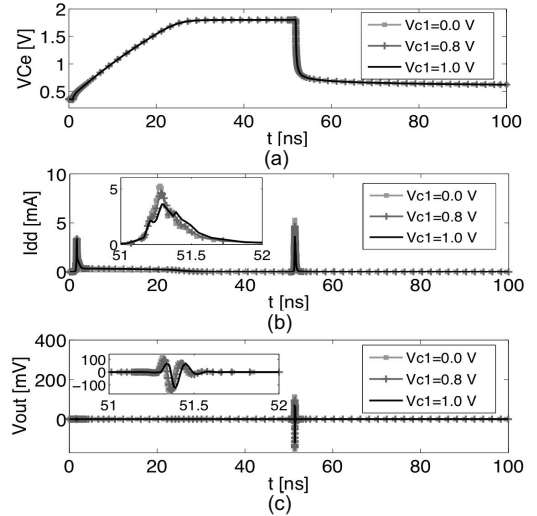


Fig. 4. Simulated (a) voltage on C_e , (b) total current and (c) the generated UWB pulse waveform ($V_{c2} = 1.2$, $T_0 = 50$ ns).

only for one pulse generation. Therefore, the value of C_e is significantly smaller than the capacitors in existing methods and the required charging time is much shorter.

The design implemented in the UMC 0.18 μm CMOS process is shown in Fig. 2. The value of C_e is designed to 5 pF to achieve a storage capability of 8 pJ when charged to 1.8 V. The driver is implemented using a 5-stage inverter chain (M_1 - M_{11}). V_{c1} is used to control the falling slope of the signal driving M_{14} and M_{15} for tunable pulse width. The charging switch is implemented using two cascaded PMOS transistors (M_{12} and M_{13}). The gate of M_{12} is controlled by V_{c2} so that the amplitude of the charging current I_c can be adjusted. The discharging is done by M_{14} and M_{15} . The discharging current flowing through M_{15} is used for the generation of the pulse signal. To guarantee a short time duration of I_d and consequently a wide bandwidth of the generated UWB pulse signal, a relatively big size of M_{15} (180 μm) was chosen. M_{14} directly discharges part of the energy on C_e to ground. This is necessary to keep the discharging speed high, since the pulse shaper and the load antenna (50 Ohm) present a high discharging impedance. Including V_{c1} and V_{c2} in the design enables tuning capability of the UWB pulse generator under different operation scenarios [9].

The simulated voltages on C_e , charging currents and UWB pulse waveforms with a pulse repetitive rate (PRR) of 10 MHz

are shown in Fig. 3. The input data signal falls at 0 ns, and rises at 50 ns. By using relatively small transistors (M_{12} and M_{13}) the amplitude of the charging current is only 8 mA when both V_{c1} and V_{c2} equal to 0 V. By increasing V_{c2} from 0 V to 1.2 V the peak of I_c can be reduced to less than 1 mA. It should be noted that the energy stored on C_e is the same since C_e is charged to the same voltage value V_{dd} even though the charging currents are different (Fig. 3(a)). Thus the generated UWB pulse signals are maintained identical (Fig. 3(c)). The simulated total current consumption I_{dd} , including both I_c and the current consumption in the driver, is shown in Fig. 4. In this simulation, $V_{c2} = 1.2$ V and V_{c1} varies from 0 V to 1.0 V. Similarly, by increasing the value of V_{c1} the peak value of I_{dd} at the time of discharging (mainly contributed by M_7 and M_9) can be reduced. In addition, the width of the generated UWB pulse signal is extended as V_{c1} increases. This is because V_{c1} changes the falling slope of the input to the discharge switch and hence changes the discharge speed. In the frequency domain, the PSD of the generated pulse can be shifted by applying different values of V_{c1} [9].

III. EXPERIMENTAL VALIDATION

The fabricated prototype chip is shown in Fig. 5. The size of the design without measurement pads is 0.4×0.4 mm². The

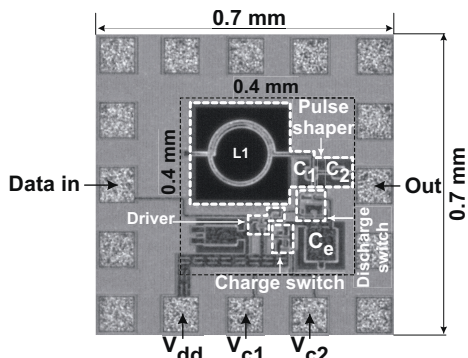
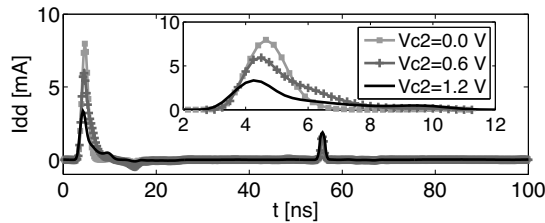


Fig. 5. Microphotograph of the fabricated prototype chip.

Fig. 6. Measured total current of the UWB pulse generator at a PRR of 10 Mpps ($V_{c1}=1.0$ V).

total current of the generator was measured from the voltage across a 10 Ohm series resistor connected between the power supply and the V_{dd} node of the generator (Fig. 6). The peak current of the pulse generator is only 3.3 mA while $V_{c1}=1.0$ V and $V_{c2}=1.2$ V, corresponding to a peak power dissipation of 6 mW and an energy consumption of 18 pJ/pulse with the power supply of 1.8 V. Fig. 7 shows the measured PSD of the generated UWB pulse signal at a PRR of 250 MHz. It can be seen that the PSD has a -10 dB bandwidth (BW) of 6.75 GHz (3.75-10.5 GHz) with a maximum magnitude of -40 dBm/MHz, which fulfills FCC's UWB mask. An added benefit of the pulse generator is that as the PRR increases, the time slot T_0 available for charging C_e is reduced, and so is the energy stored on C_e . Therefore the pulse generator can operate with a high PRR up to 1 Gpps ($V_{c1}=1.0$ V, $V_{c2}=1.0$ V) without violating FCC's radiation limit. The performance of the proposed UWB pulse generator is summarized in Table I and compared with previously published designs. It is clear that the proposed UWB pulse generator features low peak power dissipation (PP), broad bandwidth, low energy consumption (EP), and compact chip size compared to previous work.

IV. CONCLUSION

A UWB pulse generator topology is presented in this letter. A slow-charge fast discharge approach is proposed to achieve low peak power dissipation as well as low energy consumption per pulse. The proposed design has been validated by a prototype UWB pulse generator fabricated using the UMC 0.18 μm CMOS process. The fabricated UWB pulse generator offers a 3-10 GHz full bandwidth coverage with a minimum peak power dissipation of 6 mW (PRR = 10 Mpps). The energy consumption is 5 pJ/pulse at 1 Gpps, and the size of the core circuit is only 0.16 mm^2 . The proposed UWB pulse generator

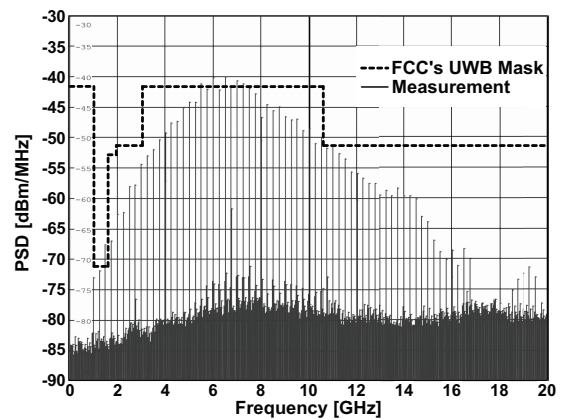
Fig. 7. Measured PSD of the UWB pulse signal with a PRR of 250 Mpps ($V_{c1}=0.9$ V $V_{c2}=1.0$ V). The resolution bandwidth is 1 MHz.

TABLE I
COMPARISON OF MEASURED PERFORMANCE

Ref	CMOS [μm]	PRR [Mpps]	EP pJ/pulse	BW [GHz]	PP [mW]	Area [mm^2]
[3]	0.18	250	20	3-5	N/A	0.08
[4]	0.13	100	9	6.8	90	0.54
[5]	0.18	100	18	0.53	N/A	0.4
[6]	0.13	50	48	3.1-4.8	N/A	0.11
[7]	0.09	400	65	5.5	N/A	1.9
This work	0.18	250	14.6	6.75	10.0	0.16
		1000	5.0*	6.0	10.4*	

*: Simulation

is suitable for short-rang applications with tight instantaneous power constrain such as battery-less self-sustainable wireless sensor networks based on energy harvesting.

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