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Abstract—The grid voltage phase and frequency are crucial information in control of most grid connected power electronic based equipment. Most often, a phase-locked loop (PLL) is employed for this purpose. A PLL is a closed-loop feedback control system that the phase of its output signal is related to the phase of its input signal. Arguably, the simplest PLL is a type-1 PLL. The type-1 PLLs are characterized by having only one integrator in their control loop and therefore having a high stability margin. However, they suffer from a serious drawback: they cannot achieve zero average steady-state phase-error in the presence of frequency drifts. To overcome this drawback of type-1 PLLs, and at the same time, to achieve a fast dynamic response and high filtering capability, a modified PLL structure is proposed in this letter. The proposed PLL has a similar structure to a type-1 PLL, but from the control point of view is a type-2 control system. For this reason, it is called the quasi-type-1 PLL (QT1-PLL). The effectiveness of the proposed PLL is confirmed through simulation and experimental results and comparison with standard PLLs.

Index Terms—Phase-locked loop (PLL), synchronization.

I. INTRODUCTION

The grid voltage phase and frequency are crucial information in control of most grid connected power electronic based equipment. Most often, a phase-locked loop (PLL) is employed for this purpose [1]. A PLL is a closed-loop feedback control system that its output phase is related to its input phase. While a wide variety of PLLs have been proposed in literature, almost all of them consist of three distinct parts: a phase detector (PD), a loop filter (LF), and a voltage controlled oscillator (VCO) [2].

Undoubtedly, the type-2 PLLs (a type-N PLL has N poles at the origin in the open-loop transfer function of its linearized model) are the most common PLLs within the areas of power electronics and power systems mainly because they are able to achieve zero average steady-state phase error under both phase angle jumps and frequency drifts. In its simplest form, a type-2 PLL can be realized by employing a proportional-integral (PI) controller as LF [3]. This controller, however, is not able to effectively block the grid disturbances in the PLL control loop. To tackle this problem, additional filters are typically employed in conjunction with the PI controller

inside the PLL's control loop. The notch filter [4], the moving average filter (MAF) [5]-[7], the *dq*-frame cascaded delayed signal cancellation operator [8]-[10], the repetitive regulator [11], and the conventional low-pass filters (LPFs) are typical choices for this purpose. Another approach is to employ some filtering stages before the input of the PLL [12]-[14].

The type-1 PLLs are characterized by presence of only one integrator in their control loop and therefore having a high stability margin [2]. Despite this interesting feature, they suffer from a major drawback: they cannot provide zero average steady-state phase error when the grid voltage frequency deviates from its nominal value [3], [15]. That is the reason why the type-1 PLLs are not usually employed. A detailed analysis of a typical type-1 PLL and a brief overview of state-of-the-art techniques are presented in the next section.

Inspired by the proposed approach in [16] which allows to view high order, high-type PLLs as a natural extension of a low order type-1 PLL, a modified structure to tackle the tracking error of type-1 PLLs under off-nominal grid frequencies is proposed in this letter. The proposed structure, in addition to provide a zero average steady-state phase error in the presence of frequency drifts, guarantees a fast transient response and high disturbance rejection capability. The suggested structure is called the quasi-type-1 PLL (QT1-PLL) as it has a similar structure to a type-1 PLL, but from the control point of view is a type-2 control system. The effectiveness of the proposed QT1-PLL is confirmed through simulation and experimental results and comparison with standard PLLs.

II. OVERVIEW AND ANALYSIS

A. Overview of State-of-the-Art

This section provides a brief overview of recent advances in the field.

Fig. 1 shows the proposed PLL structure in [18], which is referred to as the all digital PLL (ADPLL). The ADPLL is actually a traditional digital PLL (DPLL) in which a frequency detector adjusts its center frequency. Notice that the up/down counter and resettable accumulator (RACC) act as a proportional regulator in this PLL, so the ADPLL can be understood as a type-1 or quasi-type-1 PLL.

Fig. 2 shows the proposed PLL structure in [19] which is actually a hybrid type-1/type-2 PLL. In this PLL, the reconstructor continuously monitor the value of error signal *e*. Under nominal frequency condition, the steady-state value of this signal is zero. In this condition, the reconstructor disconnects the PI controller (which acts as frequency detector) from the initial-phase angle detector and, therefore, the PLL behaves as a type-1 PLL. However, when the grid frequency deviates from its nominal value, the error signal *e* becomes
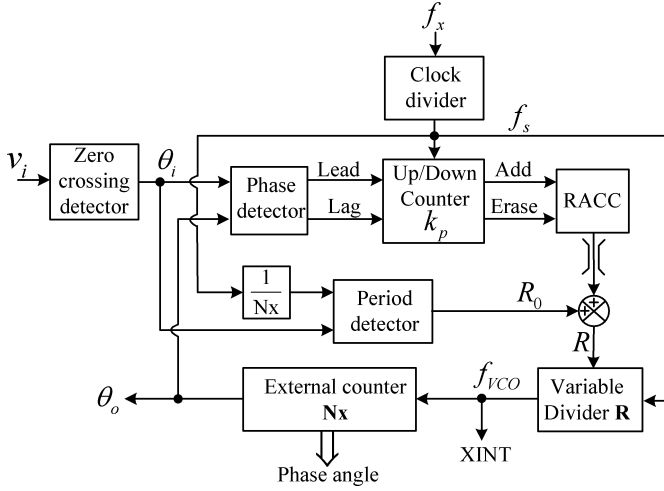
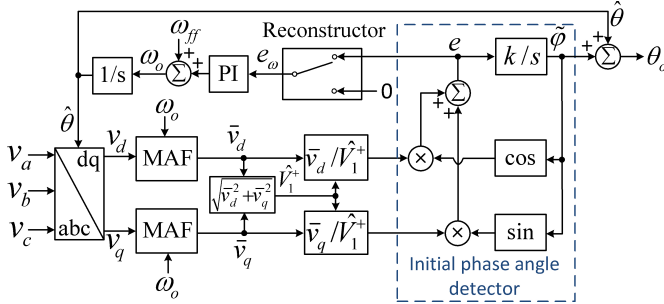Fig. 1. Block diagram structure of the ADPLL [18].

Fig. 2. Proposed PLL structure in [19].

nonzero. To remove this tracking error, the reconstructor connects the initial-phase angle detector to the PI controller. In this condition, the PLL behaves as a type-2 PLL. The reported simulation and experimental results in [19] shows that this PLL has a fast transient response and high disturbance rejection capability.

B. Analysis of a Typical Type-1 PLL

Fig. 3 shows the structure of a typical three-phase type-1 PLL (hereafter called the type-1 PLL) in which ω_{ff} is the VCO's center frequency and is equal to the nominal frequency, $\omega_o = \omega_{ff} + \Delta\omega_o$ is the estimated frequency, and

$$\theta_o = \int^t \omega_o\left(\tau\right)d\tau = \omega_{ff}t + \underbrace{\int^t \Delta\omega_o\left(\tau\right)d\tau}_{\Delta\theta_o} \quad (1)$$

is the estimated phase angle. For the sake of generality, a lead/lag controller with the continuous transfer function shown in Fig. 3 is considered as the LF in this PLL, as for $T_1 = 0$ it turns to a lag filter, and for $T_1 = T_2 = 0$ it turns to a simple gain[1].

A common trend in analysis of the type-1 PLL and determination of its steady-state tracking error is to base the study on

[1]A simple gain, a lag filter, and a lead/lag filter are typical choices for LF of a type-1 PLL [2].
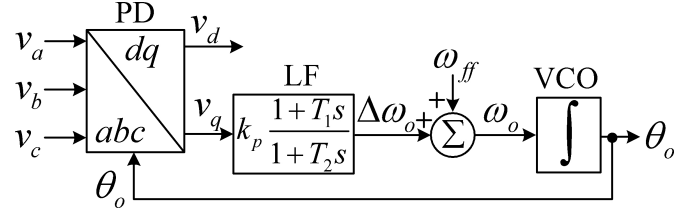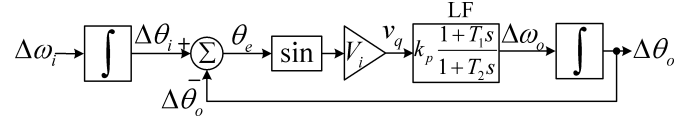

Fig. 3. Schematic diagram of a typical type-1 PLL.

Fig. 4. Nonlinear model of the type-1 PLL.

its linearized model. The linearized model, however, cannot accurately predict the type-1 PLL's tracking error particularly when the bandwidth is low. This fact can be easily verified by comparing the predicted results by nonlinear model which is shown in this section with those of linearized model which can be found in [2] and [3].

Let the three-phase input voltages of the type-1 PLL be of the form

$$\begin{aligned} v_a(t) &= V_i\cos\left(\theta_i\right) \\ v_b(t) &= V_i\cos\left(\theta_i - \tfrac{2\pi}{3}\right) \\ v_c(t) &= V_i\cos\left(\theta_i + \tfrac{2\pi}{3}\right) \end{aligned} \quad (2)$$

where V_i is the input voltage's amplitude and

$$\theta_i = \int^t \omega_i\left(\tau\right)d\tau = \omega_{ff}t + \underbrace{\int^t \Delta\omega_i\left(\tau\right)d\tau}_{\Delta\theta_i} \quad (3)$$

is the input phase-angle, and ω_i and $\Delta\omega_i$ denotes the input frequency and its deviation from the nominal frequency, respectively.

Applying the Clarke ($abc \rightarrow \alpha\beta$) transformation and then the Park ($\alpha\beta \rightarrow dq$) transformation to the three-phase input voltages yield the dq-coordinate voltage as

$$\begin{aligned} v_d(t) &= V_i\cos\left(\theta_i - \theta_o\right) = V_i\cos\left(\Delta\theta_i - \Delta\theta_o\right) \\ v_q(t) &= V_i\sin\left(\theta_i - \theta_o\right) = V_i\sin\left(\Delta\theta_i - \Delta\theta_o\right). \end{aligned} \quad (4)$$

Using (1), (3) and (4), the nonlinear model of the type-1 PLL can be obtained as shown in Fig. 4. Using this model, the differential equation describing the behavior of the type-1 PLL can be obtained as

$$T_2\frac{d^2\theta_e}{dt^2} + \left[1 + T_1 k_p V_i\cos\left(\theta_e\right)\right]\frac{d\theta_e}{dt} + k_p V_i\sin\left(\theta_e\right)$$
$$= T_2\frac{d^2\left(\Delta\theta_i\right)}{dt^2} + \frac{d\left(\Delta\theta_i\right)}{dt} \quad (5)$$

where $\theta_e = \theta_i - \theta_o = \Delta\theta_i - \Delta\theta_o$.

Under a phase locked condition, the phase error θ_e should be constant [17]. Therefore, the phase-locked solution of (5) for a step change in the phase angle and a step change in the frequency can be obtained, respectively, as

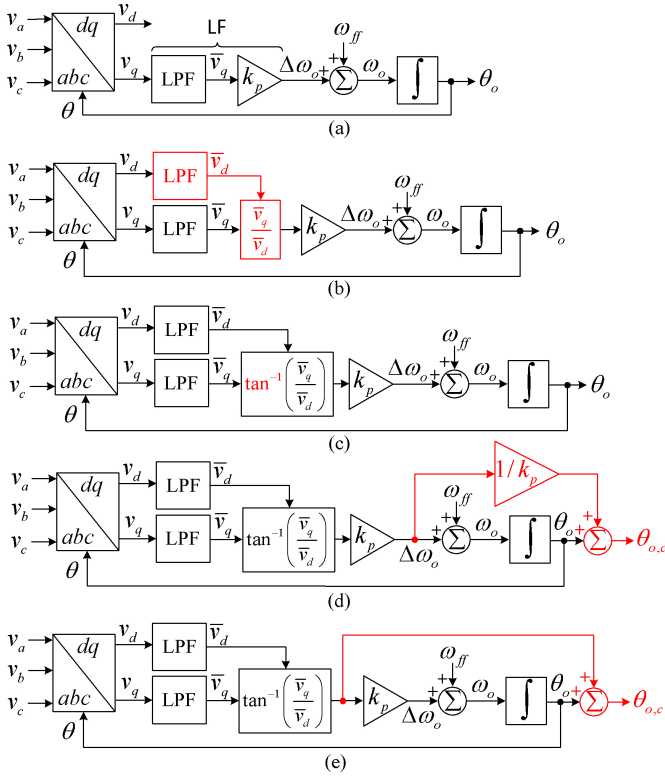$$k_p V_i\sin\left(\theta_e\right) = 0 \Rightarrow \theta_e = 0 \quad (6a)$$

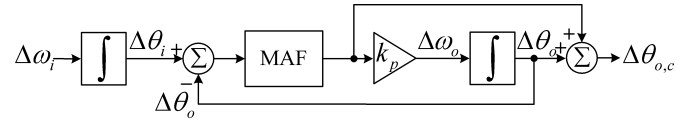Fig. 5. Step-by-step procedure towards realizing the proposed QT1-PLL.

Fig. 6. Small-signal model of the QT1-PLL.

amplitude normalization scheme (ANS) is included in the PLL structure [20]. As highlighted in Fig. 5(b), the ANS is realized by passing the d-axis voltage component through LPF in order to provide an estimation of V_i and dividing $\bar{v}_q$ (the output signal of the q-axis LPF) by this estimation. It is worth mentioning that, in addition to remove the dependency of the PLL's tracking error on the input voltage amplitude, the ANS also makes the PLL's dynamic and stability insensitive to input voltage amplitude variations, which is a very desirable feature.

To remove the nonlinearity of control loop, the arctangent function is incorporated into control loop, as shown in Fig. 5(c). As a result, the phase tracking error becomes linearly proportional to $\Delta\omega_i$, i.e.,

$$\theta_e = \frac{\Delta\omega_i}{k_p}. \tag{8}$$

Finally, the phase tracking error at the output of type-1 PLL is compensated by online calculation of (8), as highlighted in Fig. 5(d), and adding the result to the output of PLL. Notice that under locked condition the average value of $\Delta\omega_o$ is equal to $\Delta\omega_i$. Alternative mathematically-equivalent representation of Fig. 5(d) is shown in Fig. 5(e) that is the proposed QT1-PLL.

As mentioned before, the proposed QT1-PLL is actually a type-2 control system. This issue is proved in Appendix.

IV. SMALL-SIGNAL MODEL AND PARAMETERS DESIGN GUIDELINES

A. Small-Signal Model

Fig. 6 shows the small-signal model of the proposed QT1-PLL. Derivation of this model is straightforward, so the details of derivation are not presented here for the sake of brevity. The accuracy of this model, however, is examined in the following.

To evaluate the accuracy of this model, a performance comparison between the QT1-PLL and the model is carried out. The values of control parameters are listed in Table I. As shown in this Table, two different values for the gain k_p are considered to ensure the PLL's bandwidth has no effect on the accuracy of the model. The obtained results are shown in Fig. 7. It can be observed that regardless of the value of k_p, the small-signal model accurately predicts the behavior of the QT1-PLL.

B. Parameters Design Guidelines

The first step of design procedure is to select the MAF's window length. By substituting $s = j\omega$ into (7), the magnitude of MAF can be expressed as

$$|\mathrm{MAF}(j\omega)| = \left|\frac{\sin(\omega T_w/2)}{\omega T_w/2}\right|. \tag{9}$$

$$k_p V_i \sin(\theta_e) = \Delta\omega_i \Rightarrow \theta_e = \sin^{-1}\left(\frac{\Delta\omega_i}{k_p V_i}\right). \tag{6b}$$

Equation (6a) shows that the type-1 PLL accurately tracks a step change in the phase angle. However, as shown in (6b), it cannot track a step change in grid frequency. Clearly, this tracking error can be reduced by selecting a high value for gain k_p. This selection, however, is not practical under distorted and unbalanced grid conditions as increasing k_p increases the type-1 PLL's bandwidth and therefore reduces its filtering capability.

It should be emphasized here that all conclusions drawn in this section are also valid when a lag filter or a simple gain is used as the type-1 PLL's LF.

III. PROPOSED QUASI-TYPE-1 PLL (QT1-PLL) STRUCTURE

The proposed QT1-PLL is based on the structure shown in Fig. 5(a), which is a type-1 PLL similar to that considered in previous section, but with a lag filter (a LPF with dc gain k_p) as LF. In order to achieve a high filtering capability, a MAF is considered as the LPF in this structure. The MAF is a linear phase filter that can act as ideal LPF if certain conditions hold [5]. It can be described in s-domain as

$$\mathrm{MAF}(s) = \frac{1 - e^{-T_w s}}{T_w s} \tag{7}$$

where T_w is the MAF's window length.

Equation (6b) shows that the type-1 PLL's phase tracking error under off-nominal grid frequency depends on the input voltage amplitude V_i. To remove this dependency, an
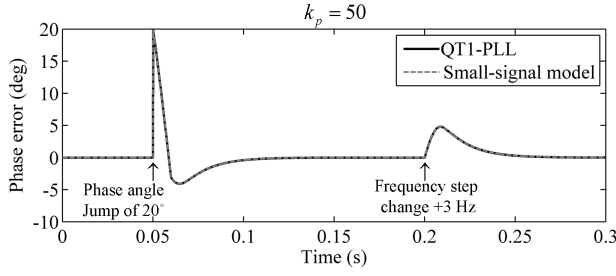
Fig. 7. Accuracy assessment of the QT1-PLL's small-signal model.
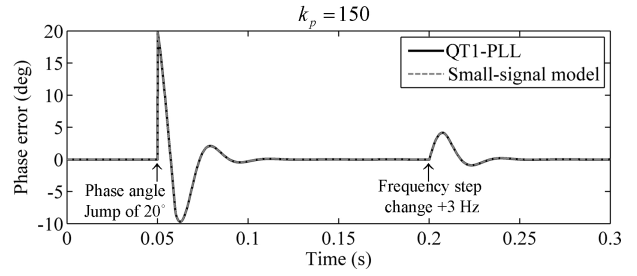
TABLE I
QT1-PLL's Parameters.

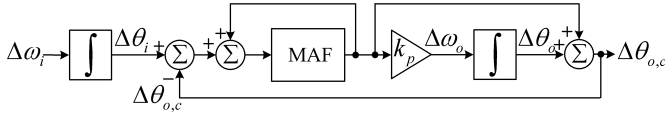| Parameter	Value
Proportional gain, k_p	50, 150
MAF's window length, T_w	0.01 s
Input voltage amplitude, V_i	1 pu
Sampling frequency, f_s	10 kHz
Nominal frequency, ω_{ff}	$2\pi 50$ rad/s

Fig. 8. The standard form of the small-signal model shown in Fig. 6.

Using (9) it can be shown that the MAF provides unity gain at zero frequency and zero gain at frequencies n/T_w ($n = \pm1, \pm2, \pm3, \cdots$) in hertz. This means that the MAF passes the dc component and completely blocks the frequency components of integer multiples of $1/T_w$ in hertz. Therefore, the MAF's window length can be simply selected according to the anticipated harmonic components in the PLL's input voltage. In most practical cases, the odd harmonics are the dominant harmonic components in the grid voltage, and the dc component and even harmonics are negligible compared to them. Therefore, $T_w = T/2 = 0.01$ s (T is the grid fundamental period) is selected in this letter.

The next step of design procedure is to select a proper value for the gain k_p. Having a sufficient stability margin, for sure, is a crucial requirement for any feedback control system including PLLs. Therefore, we select k_p such that the proposed QT1-PLL have a sufficient stability margin.

Using the block diagram algebra, the standard form of Fig. 6 can be simply obtained as shown in Fig. 8. Based on this model, the QT1-PLL's open-loop transfer function can be obtained as

$$G_{ol}(s) = \frac{\Delta\theta_{o,c}(s)}{\Delta\theta_i(s) - \Delta\theta_{o,c}(s)} = \left(\frac{\text{MAF}(s)}{1 - \text{MAF}(s)}\right)\left(\frac{s + k_p}{s}\right).$$
(10)

Using (10), the QT1-PLL's phase margin (PM) variations as a function of k_p can be simply achieved as shown in Fig. 9. It can be observed that the PM decreases with increasing k_p. In most control texts, a PM within the range of $30° - 60°$ is recommended to ensure the stability. In this letter, a PM in the middle of this range, i.e., $\text{PM} = 45°$, is considered that
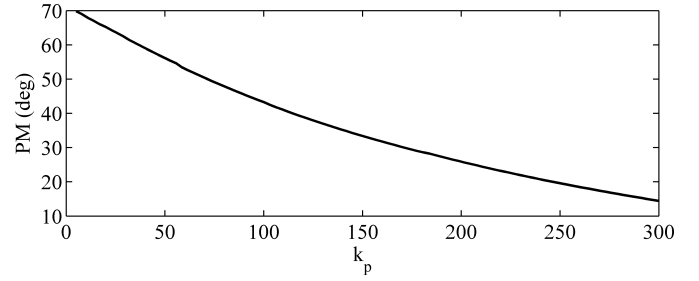

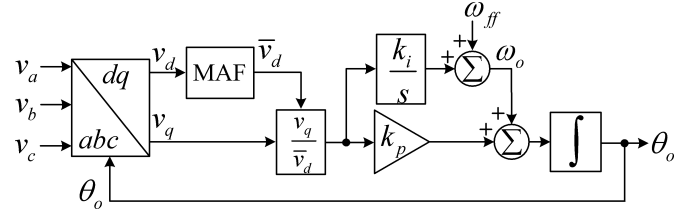Fig. 9. PM variations as a function of k_p.

Fig. 10. Block diagram description of the conventional SRF-PLL.

corresponds to $k = 92.34$.

V. Simulation and Experimental Results

To evaluate the effectiveness of the proposed QT1-PLL, some simulation and experimental results are presented in this section. Simulations are carried out in Matlab/Simulink environment and experimental results are obtained using dSpace DS1401 controller board. Throughout the simulation and experimental studies, $f_s = 10$ kHz, $\omega_{ff} = 2\pi 50$ ras/s, and $V_i = 1$ pu are considered.

To further highlight the effectiveness of proposed PLL, the conventional synchronous-reference frame PLL (SRF-PLL) shown in Fig. 10 and the SRF-PLL with in-loop MAF (hereafter called the MAF-PLL) shown in Fig. 11 are also implemented and compared with the proposed PLL.

For the case of the SRF-PLL, the proportional and integral gains are selected such that the closed-loop poles have an optimum damping factor of 0.707, and the bandwidth is the same as that of the QT1-PLL. For the case of the MAF-PLL, special care must be taken when designing the control parameters, as selecting a high bandwidth for this PLL may lead to stability problems. As recommended in [5], the symmetrical optimum method is used to select the control parameters of the MAF-PLL. The selected values of the control parameters for all
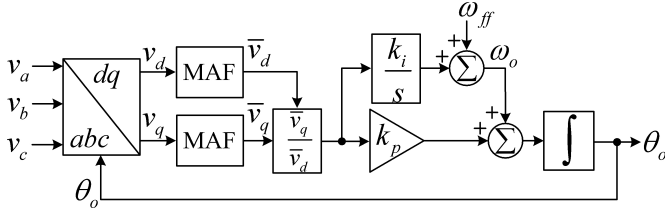
Fig. 11. Block diagram description of the conventional SRF-PLL with in-loop MAF (MAF-PLL).

TABLE II
PLLs' CONTROL PARAMETERS

	QT1-PLL	SRF-PLL	MAF-PLL
MAF's window length, T_w	0.01 s	0.01 s	0.01 s
Proportional gain, k_p	92.34	191	83.33
Integral gain, k_i	——	18250	2893.5

PLLs are listed in Table II and the open-loop Bode plots of them are shown in Fig. 12.

Fig. 13 and 14 show the obtained results when the grid voltage undergoes a frequency-step change of +3 Hz and a phase angle-jump of +40°, respectively. It can be observed that the QT1-PLL and the SRF-PLL have fast dynamic responses. The MAF-PLL, however, has a rather slow dynamic response. The detailed results are summarized in Table III.

Fig. 15 shows the numerical results under distorted and unbalanced grid conditions. The parameters of input voltage are summarized in Table IV. A step change of +3 Hz in the grid frequency is also programmed in this test. The detailed results are summarized in Table III. It can be observed that regardless of the value of grid frequency, the SRF-PLL has a poor disturbance rejection capability and the MAF-PLL has an excellent disturbance rejection capability. The disturbance rejection capability of the QT1-PLL, however, depends on the value of grid frequency; the QT1-PLL provides a great disturbance rejection capability when the grid frequency is at its nominal value, however its disturbance rejection capability decreases with increasing the grid frequency deviation from its nominal value. Despite this fact, the performance of the proposed QT1-PLL is acceptable for most practical cases as the grid frequency variations are limited by international standard [21]. It is worth mentioning that the disturbance rejection capability of the QT1-PLL under off-nominal grid frequency condition can simply be improved by making the MAFs frequency adaptive [5], [19].

The last row in Table III compares the PM of all PLLs. All PLLs, particularly the SRF-PLL, have good stability margins.

VI. CONCLUSION

In this letter, a PLL called the quasi-type-1 PLL (QT1-PLL) is proposed. The proposed PLL has a similar structure to a type-1 PLL, but from the control point of view is a type-2 PLL. The small-signal modeling and control design guidelines for the proposed PLL are presented, and its effectiveness is evaluated through simulation and experimental results and comparison with standard PLLs. The obtained results show that the proposed PLL has a fast transient response (a settling
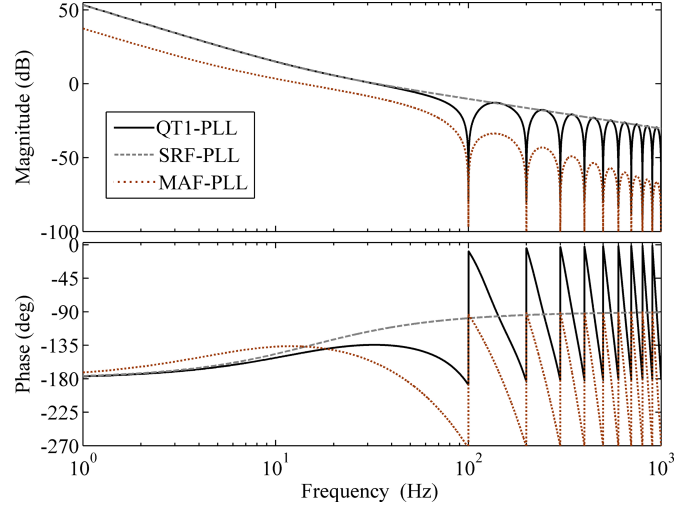

Fig. 12. The open-loop Bode plots of the QT1-PLL (solid line), the SRF-PLL (dashed line) and the MAF-PLL (dotted line). The values of control parameters are listed in Table II.

TABLE III
SUMMARY OF RESULTS

	QT1-PLL	SRF-PLL	MAF-PLL
+3 Hz frequency step change			
settling time	35 ms (1.75 cycles)	44 ms (2.2 cycles)	60 ms (3 cycles)
frequency overshoot	0.1 Hz (3.33%)	0.13 Hz (4.33%)	0.03 Hz (1%)
peak phase error	4.5°	3.67°	11.42°
+40° phase-angle jump			
settling time	30 ms (1.5 cycles)	36 ms (1.8 cycles)	74 ms (3.7 cycles)
phase overshoot	13.5° (33.75%)	8.42° (21.05%)	14.46° (36.15%)
peak frequency error	8.75 Hz	6.94 Hz	3.43 Hz
Distorted and unbalanced Grid			
peak-to-peak phase error (freq.=50 Hz)	0°	3.24°	0°
peak-to-peak phase error (freq.=53 Hz)	1.34°	3.05°	≈ 0°
Phase margin (PM)	45°	65.5°	43.3°

time of less than two cycles of the fundamental frequency), a good stability margin, and a good disturbance rejection capability.

APPENDIX

Proposed Quasi-Type-1 PLL (QT1-PLL) Is a Type-2 PLL

Approximating the delay term $e^{-T_w s}$ in (7) by first-order Pade approximation, i.e.,

$$e^{-T_w s} = \frac{e^{-T_w s/2}}{e^{+T_w s/2}} \approx \frac{1 - T_w s/2}{1 + T_w s/2} \quad \text{(A-1)}$$

and substituting the result into (7) yields

$$\text{MAF}(s) \approx \frac{1}{\frac{T_w}{2} s + 1}. \quad \text{(A-2)}$$

(A-2) shows that the MAF transfer function can be approximated by a first-order LPF with a time-constant $T_w/2$.

By substituting (A-2) into (10), we can obtain

$$G_{ol}(s) \approx \left(\frac{\frac{1}{\frac{T_w}{2} s + 1}}{1 - \frac{1}{\frac{T_w}{2} s + 1}} \right) \left(\frac{s + k_p}{s} \right) = \frac{\frac{2}{T_w} (s + k_p)}{s^2}. \quad \text{(A-3)}$$

The open-loop transfer function (A-3) has two poles at the origin, which means the proposed QT1-PLL is a type-2 PLL.
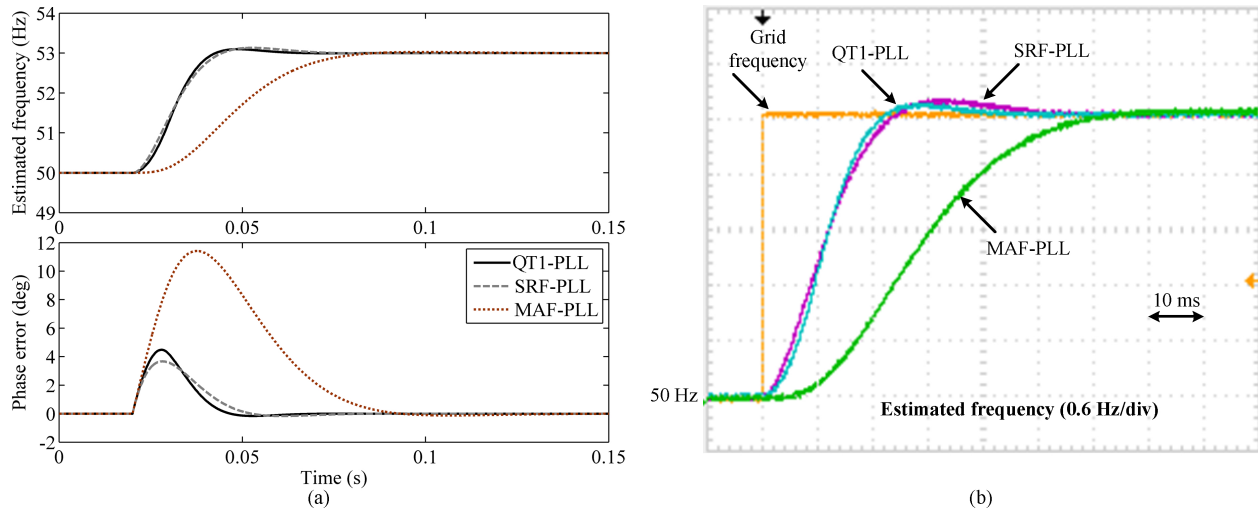
Fig. 13. (a) Simulation results and (b) experimental results when the grid voltage undergoes a frequency step change of +3 Hz.
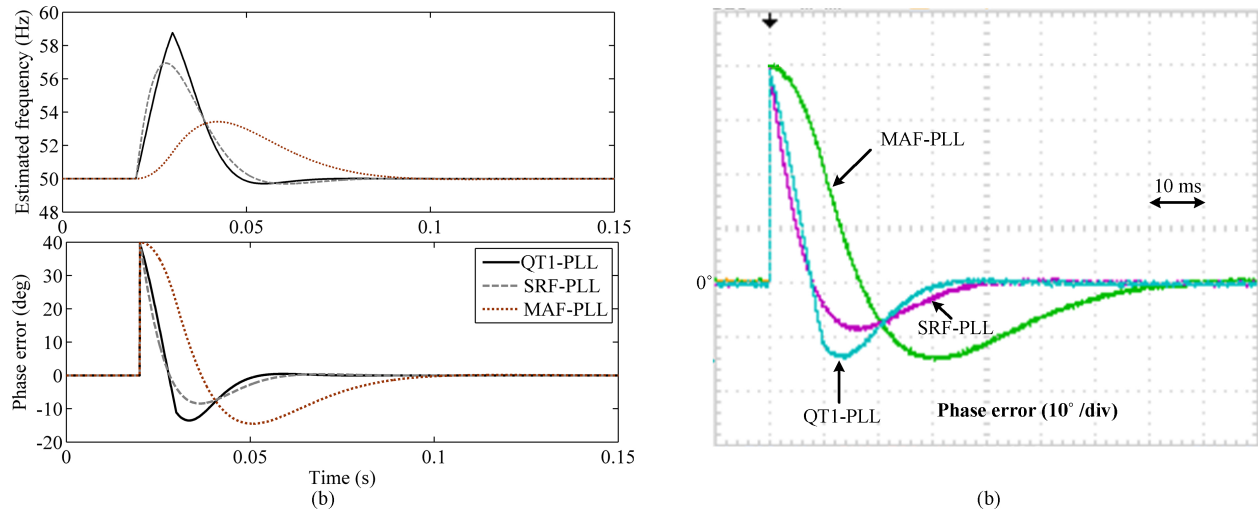

Fig. 14. (a) Simulation results and (b) experimental results when the grid voltage undergoes a phase-angle jump of $+40°$.
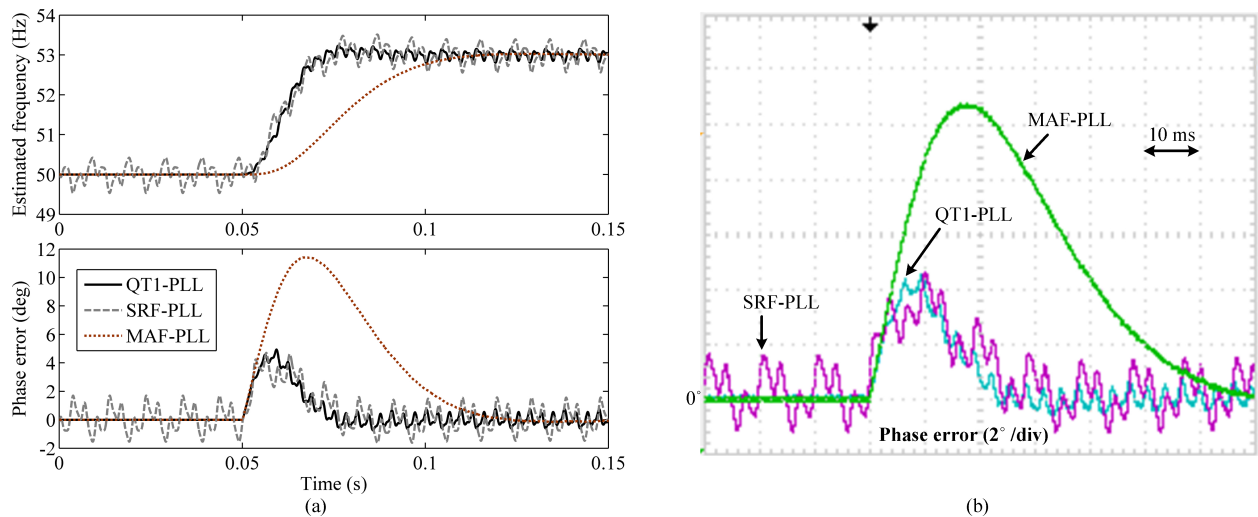

Fig. 15. (a) Simulation results and (b) experimental results under distorted and unbalanced grid condition.

TABLE IV
PARAMETERS OF DISTORTED INPUT VOLTAGE

Voltage component	Amplitude (p.u.)
Fundamental positive sequence	1
Fundamental negative sequence	0.05
5th harmonic negative sequence	0.1
7th harmonic positive sequence	0.1
11th harmonic negative sequence	0.05
13th harmonic positive sequence	0.05

REFERENCES

[1] M. Karimi Ghartemani, *Enhanced phase-locked loop structures for power and energy applications.* WileyIEEE Press, 2014.

[2] F. M. Gardner, *Phaselock Techniques.* 3rd ed. Hoboken, NJ: Wiley, 2005.

[3] K. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 431-438, May 2000.

[4] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Trans. Ind. Electron.*, vol. 59, no. 6, pp. 2718-2731, Jun. 2012.

[5] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750-2763, Jun. 2014.

[6] N. R. N. Ama, F. O. Martinz, L. Matakas, and F. K. Junior, "Phase-locked loop based on selective harmonics elimination for utility applications," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 144-153, Jan. 2013.

[7] I. Carugati, S. Maestri, P. Donato, D. Carrica, and M. Benedetti, "Variable sampling period filter PLL for distorted three-phase systems," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 321-330, 2012.

[8] Y. F. Wang, and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1987-1997, Jul. 2011.

[9] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1067-1080, Apr. 2011.

[10] S. Golestan, M. Ramezani, J. M. Guerrero, and M. Monfared, "dq-frame cascaded delayed signal cancellation-based PLL: analysis, design, and comparison with moving average filter-based PLL," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1-15, Apr. 2014.

[11] M. Rashed, C. Klumpner, and G. Asher, "Repetitive and resonant control for a single-phase grid-connected hybrid cascaded multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2224-2234, May 2013.

[12] F. Neves, H. de Souza, F. Bradaschia, M. Cavalcanti, M. Rizo, and F. Rodriguez, "A space-vector discrete Fourier transform for unbalanced and distorted three-phase signals," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2858-2867, Aug. 2010.

[13] P. Rodriguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," *in Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, Jun. 2006, pp. 1-7.

[14] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194-1204, Apr. 2011.

[15] F. D., Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of Phase-Locked Loops for Power Converters Under Distorted Utility Conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp 2039-2047, Nov./Dec. 2009.

[16] A. Carlosena, A. Manuel-Lazaro, "General method for phase-locked loop filter analysis and design," *Circuits, Devices & Systems, IET*, vol. 2, no .2, pp. 249-256, Apr. 2008.

[17] A. Suarez and R. Quere, *Stability Analysis of Nonlinear Microwave Circuits.* New Jersey: Artech House, 2003.

[18] H. Geng, D. Xu, and B. Wu, "A novel hardware-based all-digital phase-locked loop applied to grid-connected power converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1737-1745, May 2011.

[19] L. Wang, Q. Jiang, L. Hong, C. Zhang, and Y. Wei, "A novel phase-locked loop based on frequency detector and initial phase angle detector," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4538-4549, Oct. 2013.

[20] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Design and tuning of a modified power-based PLL for single phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no.8, pp. 3639-3650, Aug. 2012.

[21] *European Standard EN-50160. Voltage Characteristics of Public Distribution Systems,* CENELEC Std., November 1999.