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Reduction of DC-link Capacitor in Case of Cascade Multilevel Converters by means of Reactive Power Control

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Abstract—A new method to selectively control the amount of dc-link voltage ripple by processing the desired reactive power by a DC/DC converter in an isolated AC/DC or AC/DC/AC system is proposed. The concept can reduce the dc-link capacitors used for balancing the input and output power and thereby limiting the voltage ripple. It allows the use of a smaller dc-link capacitor and hence a longer lifetime and at the same time high power density and low cost can be achieved. The isolated DC/DC converter is controlled to process the desired reactive power in addition to the active power. The control system to achieve this selective degree of compensation is proposed and verified by Simulations.

I. INTRODUCTION

AC/DC/AC conversion systems with a Medium Frequency (MF) transformer is proposed for many applications, such as Solid State Transformer (SST) [1]–[3], adjustable speed Medium Voltage (MV) motor drives [4], and back-to-back connection of MV networks [5]. The transformer size reduction due to MF operation makes it attractive for offshore applications, such as wind farm integration, and oil & gas exploration platforms [6]. The inverter stage can be omitted in applications where the dc power can be directly utilized. Traction power electronics transformer [7], [8], power converter to integrate wind generator to multi-terminal dc collection network are few such examples. The basic block diagram of such an MF system is shown in Fig. 1.

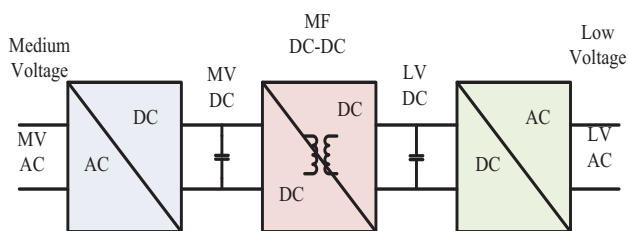


Fig. 1. Basic block diagram of isolated AC/DC/AC system using a medium frequency transformer.

Due to the limited voltage handling capability of the state of the art silicon based IGBTs, the use of multilevel converter structure is inevitable. Cascade Multilevel Converter (CMC) is often employed due to its simple structure [9], scalability [10], and low cost [11] compared to other multilevel converter

topologies. Because of the inherent single phase structure of CMC, the double frequency component of AC power on MV dc-link is unavoidable in both single phase and three phase applications [12]. If a single phase converter is used on the Low Voltage (LV) side, the same phenomenon will be observed on the LV dc-link as well. Often large capacitors are used to guarantee small ripple voltage on the dc-link, and to avoid interactions with the control loop, which otherwise will deteriorate the quality of AC current waveforms if a suitable control is not implemented [13]. With more stringent reliability constrains, the design of dc links encounters the following challenges: a) capacitors are one kind of the stand-out components in terms of failure rate [14], [15]; b) cost reduction pressure from global competition dictates minimum design margin of capacitors without undue risk; c) capacitors are to be exposed to more harsh environments (e.g. high ambient temperature, high humidity, etc.) in emerging applications, and d) constrains on volume and thermal dissipation of capacitors with the trends for high power density power electronic systems [16].

A capacitor size reduction technique in AC/DC/AC system with the equal supply and load frequency has been studied in [17], [18]. Input and output AC powers are synchronized to reduce the dc-link power, thus capacitor size reduction can be achieved. A six switch solution for non-isolated AC/DC/AC system is proposed in [13], where the phase difference between the inverter and rectifier modulation waveforms is varied. A similar approach of power synchronization in isolated AC/DC/AC system for single phase SST application is followed in [19], [20]. The isolated DC/DC converter is used for processing the reactive power. A Dual Active Bridge (DAB) feed forward power ripple control method is used in [19] and a proportional integral resonant controller is employed to obtain closed loop control [20]. However, there are many three phase application which uses single phase structure (CMC) and gives either dc or three phase AC output. The capacitor size reduction issue in such a system is addressed in this paper.

This paper proposes a technique to selectively control the reactive power processed by the DC/DC converter, and therefore the dc-link voltage ripple. The single phase and three phase system considered for the study are depicted in Fig. 2 and Fig. 3, respectively. Earlier studies [19], [20] on

capacitor size reduction in single phase systems focus only on the control techniques. However, the effect of reactive power processing by the DC/DC converter stage on the converter efficiency and design requirements are not addressed. The system overview and modulation of DAB is discussed in Section II. In Section III, capacitor size reduction technique is presented. A detailed analysis on losses and component stresses is given in Section IV. Simulation results are finally presented in Section V followed by a conclusion.

II. SYSTEM OVERVIEW

Fig. 2 shows the system configuration of one of the possible power electronics interface of a single phase MV AC network to LV AC network. A CMC is used as a MV-side converter and it consists of several H-bridge cells connected in cascade. The number of levels in CMC depends on the MV-side voltage level and the voltage handling capability of the semiconductor device used. A bidirectional DC/DC converter is connected to individual dc links of the CMC to facilitate bi-directional power flow. A MF transformer is used to provide galvanic isolation, and it aids to achieve the desired voltage transformation. DAB is often employed because of its symmetrical structure and it offers simpler control for seamless power transfer in both directions. High power density can be achieved using Dual Active Bridge (DAB) [4], [21]. Requirement of very few passive components and soft switching properties are the major advantages offered by DAB. Also depending upon the dc gain of the converter, Zero Voltage Switching (ZVS) can be achieved over a wide load range. This is an important feature as high voltage semiconductor devices are used on MV-side of DAB. The outputs of DABs are connected in parallel to utilize the advantages of interleaving. A single phase DC/AC converter is used to feed the LV AC loads.

Fig. 3 depicts the three phase isolated AC/DC/AC system. The rectifier uses the same CMC structure as that of the single phase system. The outputs of the DABs from each phase groups are connected in parallel to form a LV dc-link. A three phase inverter is used to provide the desired three phase AC voltages at the LV AC side. The inverter stage can be omitted in applications where the dc power can be directly utilized.

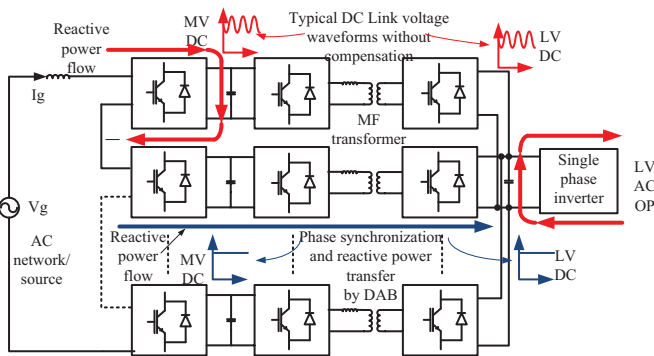


Fig. 2. Single phase isolated AC/DC/AC system with reactive power transfer.

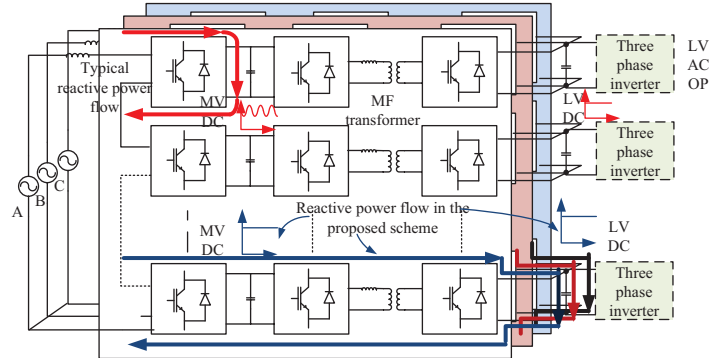


Fig. 3. Three phase isolated AC/DC/AC system with reactive power transfer.

A. Dual active bridge

The circuit configuration of a DAB is shown in Fig. 4. It consists of two H bridges, a MF transformer and an inductor. Depending on the value of the inductance required, the possibility of integrating the inductance into the transformer exists [22]. In its simplest form of operation, both H-bridges are operated with 50% duty ratio and voltages are phase displaced by an angle δ . This scheme is known as phase shift modulation and the value of δ along with inductance value, switching frequency and voltages; determine the amount and direction of power transfer. Let the dc voltage gain be:

$$Kv_{dc} = \frac{n * V_{dcLV}}{V_{dcMV}} \quad (1)$$

where, n is transformer turns ratio, V_{dcLV} is voltage at LV dc-link and V_{dcMV} is MV dc-link voltage output at each CMC module. For $Kv_{dc} = 1$, ZVS over the whole power range

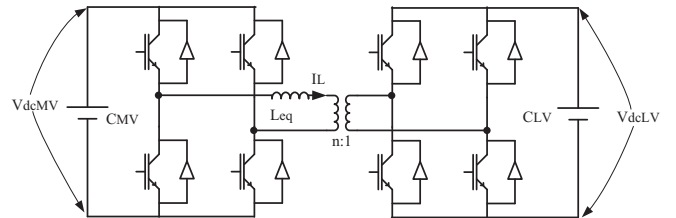


Fig. 4. Dual active bridge (DAB).

can be achieved. This is an important feature, especially in applications where high voltage semiconductor devices are used and both input and output voltages of the DAB are tightly controlled. Generally the turn-on and turn-off energy of the device for a given current rating increases with increase in voltage rating and if the device is hard switched, the switching loss is substantial. Appropriate transformer turns ratio can be chosen to achieve ZVS over a wide load range. However using the conventional phase shift modulation scheme with a given n to achieve ZVS over wider load range, it may result into high transformer current, and also capacitor RMS current increases. This could decrease the efficiency.

Considerable transformer current reduction is achieved using triangular current mode modulation [23], [24]. The power

transfer depends on the effective voltage difference of both bridges and hence it suffers from limited power transfer capacity in such scheme. Trapezoidal modulation scheme is proposed [23], [24] to improve the power transfer capacity. The efficiency can be improved by adopting an optimum modulation scheme for expanding the soft switching range [25] or to reduce the conduction loss [26]. However, the schemes are beyond the scope of this paper and the discussion is mainly focused on the use of single PWM control [25], also popularly known as $D1$ and δ control.

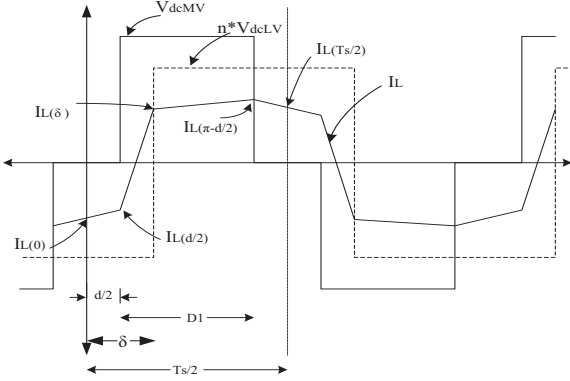


Fig. 5. DAB inductor current and MF transformer primary and secondary voltages.

B. Dual Active Bridge Modulation

The transformer voltages and inductor current for a $D1$ and δ control are shown in Fig. 5. The power transfer from MV-side to LV-side is considered for discussion and the same analysis would apply for reverse direction of power flow as well. Considering a loss less system, the power transfer P_{dab} for a given δ is given by:

$$P_{dab} = \frac{nV_{dcLV}V_{dcMV}\delta}{X_L} \left(\frac{\pi - |\delta|}{\pi} \right) - \frac{nV_{dcLV}V_{dcMV}\delta}{X_L|\delta|} \left(\frac{d^2}{4\pi} \right) \quad (2)$$

For $\frac{d}{2} < \delta < \pi$. Where, $X_L = 2\pi f_s L_{eq}$, f_s is the switching frequency, L_{eq} is the equivalent inductance, d is the free-wheeling period. The first term in (2) is the same as the power flow in DAB when a phase shift modulation is used. The maximum power transfer is:

$$P_{dab,max} = \frac{nV_{dcLV}V_{dcMV}}{4\pi X_L} (\pi^2 - \delta^2), \text{ for } \delta = \pi/2 \quad (3)$$

From (2), the phase shift required for transferring given power is:

$$\delta = \frac{\pi}{2} \left[1 - \sqrt{1 - \left(\frac{8P_{dab}f_s L_{eq}}{nV_{dcLV}V_{dcMV}} + \frac{d^2}{\pi^2} \right)} \right] \quad (4)$$

The inequalities due to manufacturing tolerances result into the flow of a dc bias current in a MF transformer. This leads to a dc offset in the flux density swing and cumulative effect can drive the magnetic core into saturation region. This could lead to more losses into both semiconductor devices and transformer core. Air gapped cores [27] can be used at the expense of

additional losses. A magnetic transducer [28] can also be used to correct the dc bias current. A current mode control is traditionally used to avoid dc bias in push-pull and full bridge dc-dc converters and further extended for DAB control in this paper. Phase angle information from (4) is translated into current domain (see Fig. 5), and it is given as:

$$I_L(\delta) = \frac{1}{2X_L} [(nV_{dcLV} - V_{dcMV})\pi + 2V_{dcMV}\delta] \quad (5)$$

$$I_L\left(\pi - \frac{d}{2}\right) = \frac{1}{2X_L} [(nV_{dcLV} - V_{dcMV})\pi + 2V_{dcLV}\delta - (V_{dcMV} - nV_{dcLV})d] \quad (6)$$

The transformer current is alternating in the DAB. Positive and negative current wave-shape can be made similar by updating the reference current value once in each switching period T_s . The $I_L(\delta)$ is used to obtain the required phase shift to cater the power demand and $I_L(\pi - \frac{d}{2})$ is controlled to ensure volt-sec balance. This can avoid core saturation and ensures effective utilization of the magnetic core.

III. CAPACITOR VOLTAGE RIPPLE AND IT'S REDUCTION TECHNIQUE

Considering a balanced three phase system, analysis for one phase is presented and then extended to three phase system. Assuming that the CMC rectifier is switched at sufficiently higher frequency and the filter is designed to make the harmonic content in the grid current to be zero. Then the grid voltage and the rectifier current are given as $\sqrt{2}V_a \sin \omega t$ and $\sqrt{2}I_a \sin(\omega t - \phi)$, respectively. A ϕ is the power factor angle. The input power of A phase is given by:

$$P_{in}(t) = V_a I_a \cos \phi - V_a I_a \cos(2\omega t - \phi) \quad (7)$$

Assuming zero losses in the filter inductor, the reactive power contribution of the filter is:

$$P_{Lf}(t) = I_a^2 \omega L_f \sin(2\omega t - 2\phi) \quad (8)$$

The MV dc-link voltage is controlled by CMC rectifier and the task of maintaining a stable LV dc-link is assigned to DAB. Assuming a lossless system, the power balance is maintained by making the power flow through DAB the same as the active power processed by the rectifier. This implies:

$$V_a I_a \cos \phi = N P_{dabactive}(t) \quad (9)$$

where, N is the number of cascade connected modules and $P_{dabactive}$ is the power flowing through DAB.

The reactive power circulates through the MV dc-link capacitor. This causes a ripple in dc-link voltage. The capacitor voltage is composed of a dc value overlapped by an AC component. The AC component frequency is nearly twice that of the supply frequency. This double frequency component of reactive power demands, larger capacitor to restrict the ripple within allowable limit.

Let the DAB designed and controlled to process desired

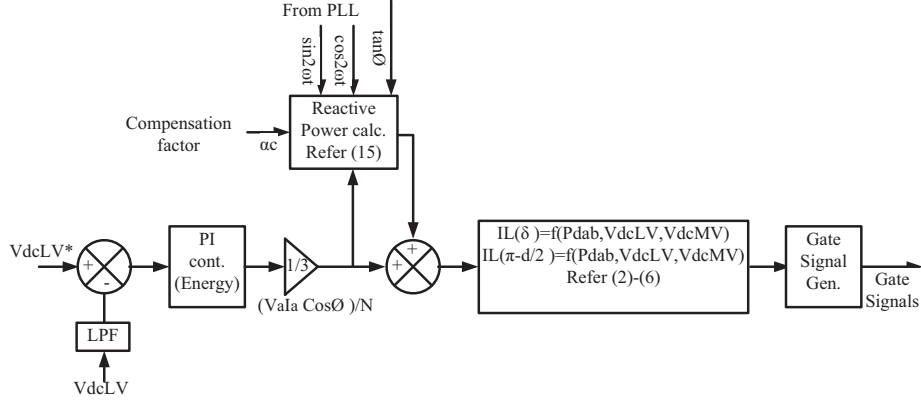


Fig. 6. Proposed control scheme for selective reactive power transfer through DAB

amount of input reactive power in addition to the input active power, and the power flowing through the DAB is:

$$P_{dab}(t) = P_{dabactive}(t) + P_{dabreactive}(t) \quad (10)$$

Where, $P_{dabreactive}$ is the desired fraction of the rectifier reactive power of one module. Due to the multi-level voltage waveforms, a small filter is required in CMC to meet the current THD requirement. It implies that $I_a \omega L_f$ and the reactive power consumption of the filter inductor can be neglected. This gives;

$$P_{dabreactive}(t) = -\alpha_c \frac{V_a I_a}{N} \cos(2\omega t - \phi) \quad (11)$$

where, α_c is a compensation factor and can be selectively chosen for desired dc-link voltage ripple cancellation. Using power balance in steady state, the oscillating power in MV dc-link capacitor is given as:

$$\tilde{P}_{cmv}(t) = (\alpha_c - 1) \frac{V_a I_a}{N} \cos(2\omega t - \phi) \quad (12)$$

The double frequency component of the power stores/withdraws energy during a quarter cycle of the fundamental frequency and from (12), the capacitance required to maintain the desired ripple in the the MV dc voltage is given as:

$$C_{mv} = \frac{(1 - \alpha_c) V_a I_a}{\omega N V_{dcmv} \Delta V_{dcmv}} \quad (13)$$

where, V_{dcmv} is the MV dc-link voltage and ΔV_{dcmv} is peak to peak ripple voltage. From (13), it is apparent that the capacitance required to maintain a voltage ripple in a desirable limit reduces as α_c increases. In a three phase system, the power output at the DAB terminals is;

$$\begin{aligned} P_{daba}(t) &= \frac{V_a I_a}{N} \cos \phi - \alpha_c \frac{V_a I_a}{N} \cos(2\omega t - \phi) \\ P_{dabb}(t) &= \frac{V_b I_b}{N} \cos \phi - \alpha_c \frac{V_b I_b}{N} \cos(2\omega t + \frac{2\pi}{3} - \phi) \\ P_{dabc}(t) &= \frac{V_c I_c}{N} \cos \phi - \alpha_c \frac{V_c I_c}{N} \cos(2\omega t - \frac{2\pi}{3} - \phi) \end{aligned} \quad (14)$$

In balance three phase system, the reactive power flowing through DAB of from each phase group will have an equal

magnitude and phase displacement of 120° of double frequency. The output are connected to a common dc-link at LV-side as shown in Fig. 3 and addition of reactive power becomes zero. Therefore, the ripple on MV dc-link can be canceled with a negligible effect on the voltage ripple at LV dc-link.

IV. CONTROL SYSTEM AND DESIGN IMPLICATIONS

The desired MV dc-link voltage ripple reduction can be achieved by precisely controlling the DAB reactive power. From (11), the reactive power component processed by the DAB can be rewritten as:

$$P_{dabreactive}(t) = -\alpha_c \frac{V_a I_a \cos \phi}{N} [\cos 2\omega t + \sin 2\omega t \tan \phi] \quad (15)$$

Fig. 6 depicts the block diagram of the proposed control system. The LV dc-link voltage is sensed and compared with the reference value. The error is passed through a PI controller, and the output is the power required to maintain the power balance at LV dc-link. As all three phases contributes to the power at LV dc-link, the power command for the individual DAB is one third of the total power required. The compensation factor can be chosen based on the application and availability of the devices. The choice of compensation factor also affects the selection of semiconductor devices, transformer core size, efficiency, and reliability of the system. The input reactive power that is required to be processed by DAB is calculated using (15). The $\sin 2\omega t$ and $\cos 2\omega t$ are obtained for each phase from the rectifier phase locked loop. The power factor angle is known to the controller and hence $\tan \phi$ can be easily obtained. The $D1$ and δ control is used and with $Kv_{dc} < 1$, the freewheeling period is introduced on MV-side waveforms. The freewheeling period d is chosen to be equal to $\pi(1 - Kv_{dc})$ for maximizing the ZVS range as demonstrated in [25]. Current mode control is used to generate PWM and $I_L(\delta)$ is used to obtain the required phase shift to cater the power demand.

In order to facilitate the dc-link capacitor reduction, the DAB should be designed to allow additional power flow through it. In normal operation(without compensation), only

input active power flows through DAB, whereas in the proposed scheme; a fraction of the input reactive power (decided by the compensation factor) in addition to active power is processed by the DAB. This in-turn will increase the semiconductor device rating and size of the MF transformer. It may not be viable to have full compensation and hence a design compromise has to be done. Several factor may influence the design, which includes cost, efficiency, reliability and availability of the components. Other possible approach without any implications on the cost, is to exploit the full capacity of the converter at part load. The compensation factor can be determined based on the converter capacity and the amount of input active power being flowing through it. This can help in reducing the stress on the MV dc-link capacitor and improve the lifetime of the dc-link capacitor. Also this allows the DAB to operate at its full capacity, and an appropriate design ensures improvement in the overall efficiency.

The maximum value of compensation factor at full load should be decided at the design stage. For a given modulation scheme, the semiconductor switch current rating varies linearly with the compensation factor. The Area-Product (AP) of the transformer for different design depends on the selection of compensation factor, and it is shown in Table. I for different values of compensation factor. The transformer size increases and MV dc-link capacitance decreases with increase in compensation factor. It is important to note that the size of MF transformer is inversely proportional to the DAB switching frequency, whereas the capacitance is determined by the grid frequency. With the use of Silicon carbide (SiC) semiconductor switches, reduction in capacitance can be achieved without much increase in to the overall converter size. For three phase applications (refer Fig. 3), the MF transformer from each phase group can be combined to form a three phase transformer. The appropriate interleaving of the gate signals for the DABs ensures cancellation of some of the flux components which are 120° phase-shifted. This leads to a reduction in size compared to the use of three individual MF transformers.

The design parameters of the DAB for different degree of compensation for 300 kVA, 11 kV/400 V SST system is given in Table. I. The design approach is influenced by the availability of the components. The maximum phase shift is limited to 0.5 rad by choosing an appropriate value of the inductor. Considering a high voltage low current application, more number of turns are selected to limit the peak flux density to a low value. The window area is effectively utilized by choosing more copper area and reduced current density in the conductor. This reduces the resistive losses. The efficiency optimized design of the transformer can be achieved by a proper selection of peak flux density and number of turns. The efficiency curves for all five design cases are shown in Fig. 7. The active power flow through DAB in all cases is same. An improved generalized Steinmetz equation is used to evaluate the core losses. The higher turn off loss of IGBTs on MV-side bridge is the main reason for the lower efficiency during part loads, and hence the design in this case is more focused on extending the ZVS range.

TABLE I
DESIGN PARAMETERS OF DAB FOR DIFFERENT VALUES OF COMPENSATION FACTOR

Compensation factor α_c	Case1 $\alpha_c = 0$	Case2 $\alpha_c = 0.25$	Case3 $\alpha_c = 0.5$	Case4 $\alpha_c = 0.75$	Case5 $\alpha_c = 1$
Inductance L (mH)	6.5	5.2	4.4	3.7	3.3
Area Prod. (cm^4)	487	529	551	588	636
MV dc-link cap. (μF)	110	82.5	55	27.5	15
Core size	AMCC 500	AMCC 630	AMCC 630	AMCC 800A	AMCC 800A
Primary winding	440 turns 26/30	392 turns 26/30	392 turns 26/30	320 turns 42/30	320 turns 42/30
Secondary winding	110 turns 5X22/30	98 turns 5X22/30	98 turns 5X22/30	80 turns 7X24/30	80 turns 7X24/30
Peak flux density (T)	0.475	0.42	0.42	0.425	0.425

Switching frequency: 3 kHz, Due to limited availability of IGBTs for this voltage rating, the same switches are used in all cases. The phase shift angle is restricted to 0.5 rad in all cases.

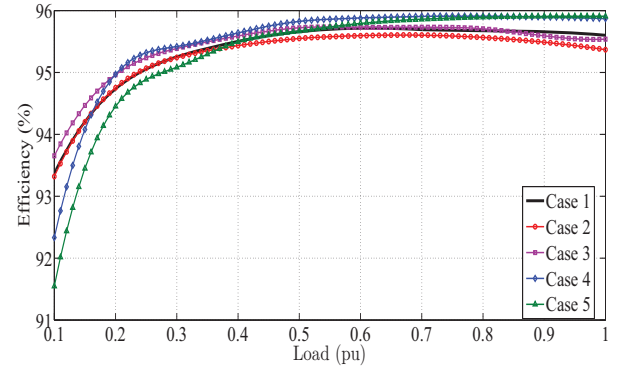


Fig. 7. Efficiency curves for different designs, considering the degree of compensation as a parameter (refer to Table I).

V. SIMULATION RESULTS

A three phase 300 kVA, 11 kV/400 V SST system (refer Fig. 3) is used for simulation studies. The front-end CMC rectifier is connected to the 11 kV 3-phase MV AC supply. The CMC converters are star connected. The voltage on the MV AC side is assumed to vary between -10% to +5% range and hence maximum phase voltage across CMC is 6.66 kV. The filter inductor is designed to restrict current harmonics within 5%. For a rated phase current of 16 A, the filter inductor is chosen to be 62.9 mH. Four H-bridges each with a 4.5 kV IGBTs (ABB-5SNG0150P450300) are connected in cascade and switched at 1.5 kHz. The reference dc-link voltage for each module is chosen to be 2.71 kV. The $110\mu F$ capacitance is used and it gives 10% voltage ripple at full load.

The DAB consists of two H bridges and a MF transformer. The MV-side bridges uses 4.5 kV IGBTs (ABB-5SNG0150P450300) and 1.2 kV (Infinion-FF300R12ME4)

IGBT is used as a switch in LV-side bridge. The rated power of each DAB is 25 kW without compensation and taken as a base case for analysis. With full compensation, DAB is required to process the full reactive power in addition to the active power and hence the peak power that would flow through it is 50 kW. The DAB switching frequency is taken as 3 kHz. For a 25 kW design, AMCC500 is selected as a transformer core, whereas AMCC800A is used for the full compensation case. Considering the availability of the semiconductor devices and to reduce the transformer copper loss, the turns ratio is chosen to be 4. The dc voltage gain is close to unity and the ZVS can be achieved over the full power range. 1000 V, 900 μF (AVX-FFLI6L0907K-) with ESR of 2.9 $m\Omega$ is used as a LV-side dc-link capacitor.

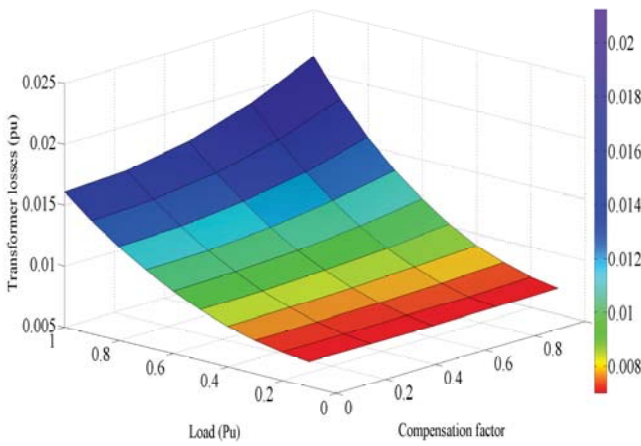


Fig. 8. Variation in the transformer losses (expressed in Pu with rated active power as a base value) as a function of load and compensation factor.

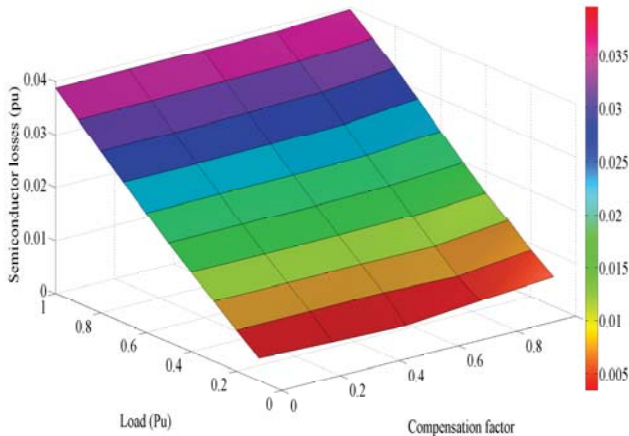


Fig. 9. Variation in the semiconductor losses (expressed in Pu with rated active power as a base value) as a function of load and compensation factor.

For AMCC800A, the net cross sectional area is 17.4 cm^2 and the window area is 34 cm^2 . The maximum flux density in this case is taken as 0.425 T and the window area utilized by the windings is 13.6 cm^2 . The variation in a

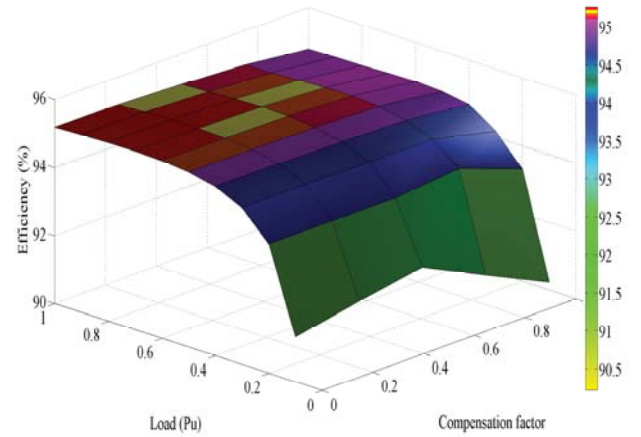


Fig. 10. DAB efficiency as a function of load and compensation factor.

transformer losses is depicted in Fig. 8. It is observed that the copper loss in transformer at full load rises sharply as the compensation factor approaches unity. This is because of the nature of the power transfer characteristic of the DAB. The maximum phase shift angle is restricted to 0.5 rad in this case by selecting a proper inductance value. If DAB is designed for larger value of the maximum phase shift angle, the transformer copper loss rises more sharply due to the increased reactive power in the DAB. The combined semiconductor losses of both MV-side H-bridge and LV-side H-bridge is shown in Fig. 9. The switching loss of the MV-side bridge is a major contributor. Although, zero voltage transition at device turn-on is achieved over full operating power range, turn-off losses still occur. Due to the use of high voltage IGBTs on the MV-side and larger silicon area (Due to limited availability of the IGBT in this voltage range), the switching loss in MV-side bridge dominates the conduction losses. The efficiency of the DAB converter as a function of active power and compensation factor is depicted in Fig. 10.

Fig. 11 shows the simulation results of the three phase system. The system is operated at rated load and the MV dc-link voltage has a double frequency pulsation. The CMC rectifier is commanded to maintain an average MV dc voltage of 2710 V. As the MV dc-link capacitor value is chosen for 10% peak-peak voltage ripple, the peak to peak ripple of 270 V is observed. The compensation starts at 0.3s with a factor of 0.5 ($\alpha_c = 0.5$) and DAB starts transferring 50% of the input reactive power from MV dc-link to LV dc-link. As a result, the MV dc-link voltage ripple is reduced by 50% (peak to peak ripple is 130 V) as analytically shown in (13). The outputs of the DABs from all three phases are connected to a common dc-link. The reactive power outputs of DABs have equal magnitude and phase displacement of 120 degrees of double frequency. The parallel operation on the LV-side makes the summation of double harmonic component to be zero and hence there is a negligible effect on the voltage ripple on

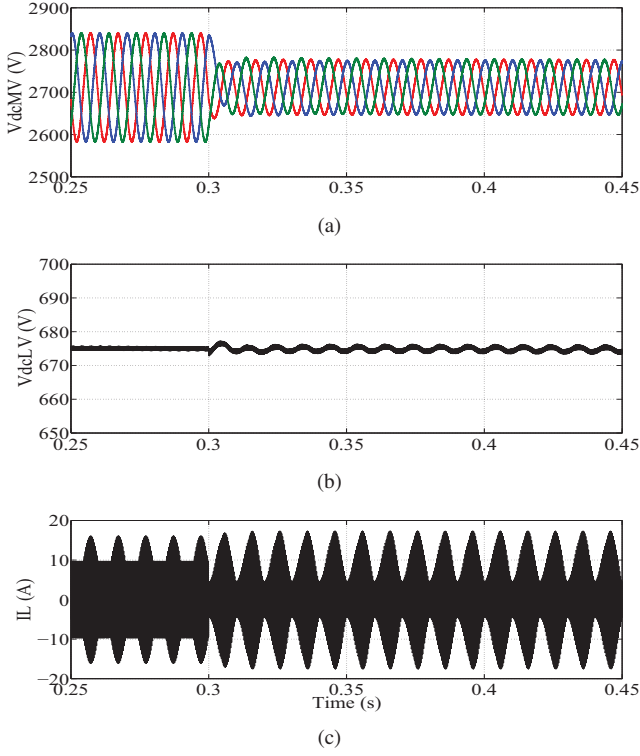


Fig. 11. Simulation results for a compensation factor of 0.5. (a) Medium voltage dc-link voltage, (b) Low voltage dc-link voltage, and (c) DAB inductor current.

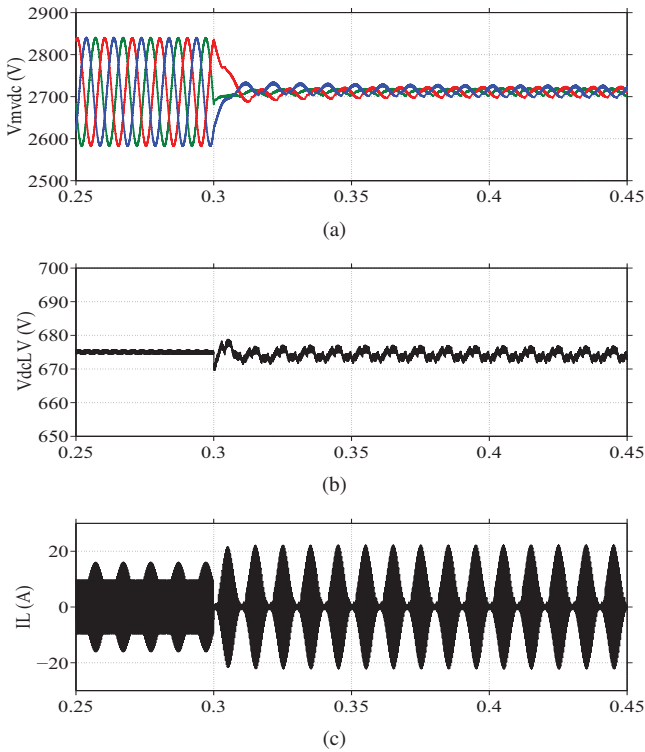


Fig. 12. Simulation results for a full compensation case. (a) Medium voltage dc-link voltage, (b) Low voltage dc-link voltage, (c) DAB inductor current.

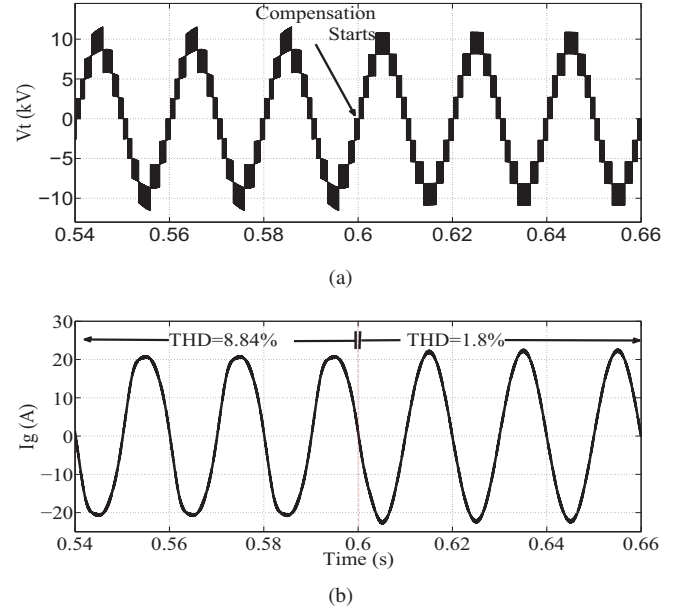


Fig. 13. Phase A rectifier waveforms with half MV dc-link capacitor (a) The PWM voltage at CMC terminal and (b) Grid current

LV dc-link. The profile of the inductor current for the given case is also shown in Fig. 11(c). The MV and LV dc-link voltage waveforms for a full compensation case ($\alpha c = 1$) is shown in Fig. 12(a). and 12(b). The compensation starts at 0.3 s. The ripple on the MV dc-link almost becomes zero with negligible effect on the LV dc-link voltage waveforms. The peak current through DAB is increased as shown in Fig. 12(c).

Due to the lower switching frequency of the CMC rectifier, and small MV dc-link capacitor, the assumption of constant MV dc-link voltage over a switching cycle is not valid. The double frequency pulsation on the MV dc-link results into unwanted low order harmonics in the grid current, specially the 3^{rd} harmonic. The CMC rectifier controller can be designed to limit the unwanted harmonic components. However, in order to highlight the improvement in grid current waveform solely by the proposed method, it is not used in this study. The grid current waveforms before and after the start of the compensation is shown in Fig. 13. The THD is within a specified limit and shows that the scheme can be implemented without any detrimental effects on the grid current.

VI. CONCLUSION

Isolated AC/DC/AC conversion system with a MF transformer is an attractive option for many modern applications. The CMC is most preferred converter for MV ac interface due to its simple structure and scalability. However, due to the inherent single phase structure of CMC, the double frequency pulsation on dc-link side is unavoidable. Often large capacitors are used to guarantee small ripple voltage on dc-link. A

method to reduce the dc-link capacitor in isolated AC/DC or AC/DC/AC systems is proposed. The DAB processes the desired reactive power set by a compensation factor. In a balance three phase system, the reactive power output of DAB of from each phase group will have equal magnitude and phase displacement of 120° of double frequency. As the outputs are connected to a common dc-link at the LV-side, an addition of reactive power becomes zero. Therefore the ripple on MV dc-link can be canceled with negligible effect on the voltage ripple at LV dc-link. The simulation results verify that the dc-link ripple at the CMC/single phase rectifier output is significantly reduced and becomes almost negligible with compensation factor of 1. It allows a smaller dc-link capacitor to be used. The implications of the proposed scheme on the design of the converter is also discussed.

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