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LOW-POWER TECHNIQUES FOR SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG-TO-DIGITAL CONVERTERS

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by

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A Thesis
Submitted in Partial Fulfillment of the Requirements for the
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THESIS APPROVAL

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MAJOR PROFESSOR: Dr. Haibo Wang

In this work, we investigate circuit techniques to reduce the power consumption of Successive Approximation Register Analog-to-Digital Converter (SAR-ADC). We developed four low-power SAR-ADC design techniques, which are: 1) Low-power SAR-ADC design with split voltage reference, 2) Charge recycling techniques for low-power SAR-ADC design, 3) Low-power SAR-ADC design using two-capacitor arrays, 4) Power reduction techniques by dynamically minimizing SAR-ADC conversion cycles. Matlab simulations are performed to investigate the power saving by the proposed techniques. Simulation results show that significant power reduction can be achieved by using the developed techniques. In addition, design issues such as area overhead, design complexity associated with the proposed low-power techniques are also discussed in the thesis.

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INTRODUCTION

1.1 Objectives and Motivation

Data converter circuits are widely used as interface between analog and digital circuits. Although more and more signal processing functions are performed in digital domain, many signals that need to be processed in real world are analog signals. This creates great demands for data converter circuits. In general, data converter circuits can be classified into two categories: Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC). As indicated by their names, an ADC converts analog signals to binary words and a DAC performs the opposite operations. ADCs can be further classified as serial or parallel ADCs. Serial ADCs produce digital output with one bit at a time, and parallel ADCs produce all digital output bits at the same time.

With the wide use of battery-powered portable electronic devices, there are great interests in low-power design techniques for ADC and DAC circuits. In literature various low-power circuit techniques for modern data converter circuits have been reported. Many of them have been already used in commercial devices. Nevertheless, the development of new low-power techniques for data converter circuits is never ended, mainly due to the following reasons. First, the advancement of semiconductor devices and IC fabrication processes continuously create new possibilities of new circuit techniques. Second the never-ending demands for further reducing electronic device power consumption relentlessly drive the development of more power efficient circuits. As a result, low-power ADC design techniques remain a very active research field.

Among various low-power ADC implementations, Charge Redistribution Successive Approximation Register Analog to Digital converter (CR-SAR-ADC) architecture is particularly appealing due to its low-power consumption and low hardware requirement to implement [6, 10]. A CR-SAR-ADC sample the input signal and performs the binary search using a charge scaling capacitor array. The CR-SAR-ADC is one of the most commonly used serial ADC architectures which have low-power consumption, medium speed and medium-to-high accuracy. In this work, techniques to further minimize the power consumed by charging the capacitor array during the ADC conversion processes is investigated.

1.2 Contributions

Four new low-power techniques are developed in this work. They are briefly discussed as follows.

Low-Power SAR-ADC design with Split Voltage Reference: In this design, the capacitors in the capacitor array switches between two voltage references, rather than switching with a single voltage reference as a traditional ADC. It is designed to consume zero energy for the most significant bit (MSB) and charge the capacitor to half of the reference voltage during the conversion.

Charge Recycling Techniques for Low-power SAR-ADC Design: This method re-utilizes the charge stored in the capacitors of DAC array from the previous conversion to reduce the energy consumption for the current conversion.

Low-Power SAR-ADC Design using Two-capacitor Arrays: It Utilizes two-capacitor arrays of unequal size and switches with half the reference voltage to perform the SAR

conversion. The switching sequence drastically reduces the power consumption of the ADC.

Power Reduction Techniques by Dynamically Minimizing SAR-ADC Conversion Cycles: The algorithms proposed in this method save energy by retaining the MSBs that are generated in the previous conversion and perform a traditional binary search for the remaining bits.

1.3 Organization of the thesis

The rest of the thesis is organized as follows. Chapter 2 reviews the fundamentals of CR-SAR-ADCs along with the explanation of how the energy equations being calculated when capacitors are switched in the capacitor array. This chapter also provides a brief survey on previously proposed low-power techniques for CR-SAR-ADC design. Chapters 3, 4, 5, 6 explain the proposed low-power techniques. Matlab simulation results are also presented to demonstrate the power reduction by using the proposed techniques in each corresponding chapter. The scope of future work is discussed in chapter 7.

CHAPTER 2

LITERATURE REVIEW

2.1 Basic Operation of Successive Approximation Register ADC

An SAR-ADC produces the equivalent digital output for a sampled analog input using the principle of binary search algorithm [10]. Its block diagram is shown in Figure 1. In each iteration, the binary search algorithm equally divides the search space in two sub space and identifies which sub space needs to be further searched. The final output can be generated in N steps for an N-bit SAR-ADC. The search operation of a SAR-ADC is illustrated in the flow chart shown in Figure 2.

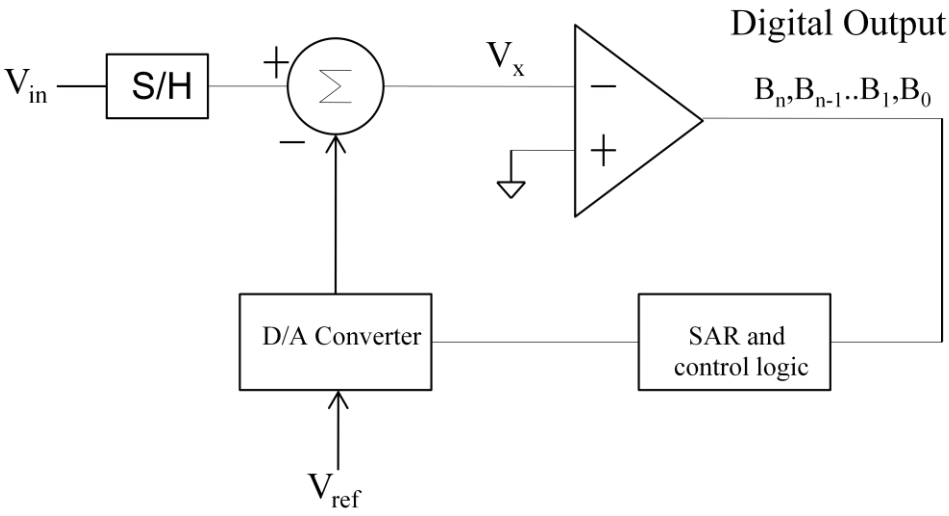


Figure 1: Block diagram of Traditional SAR-ADC

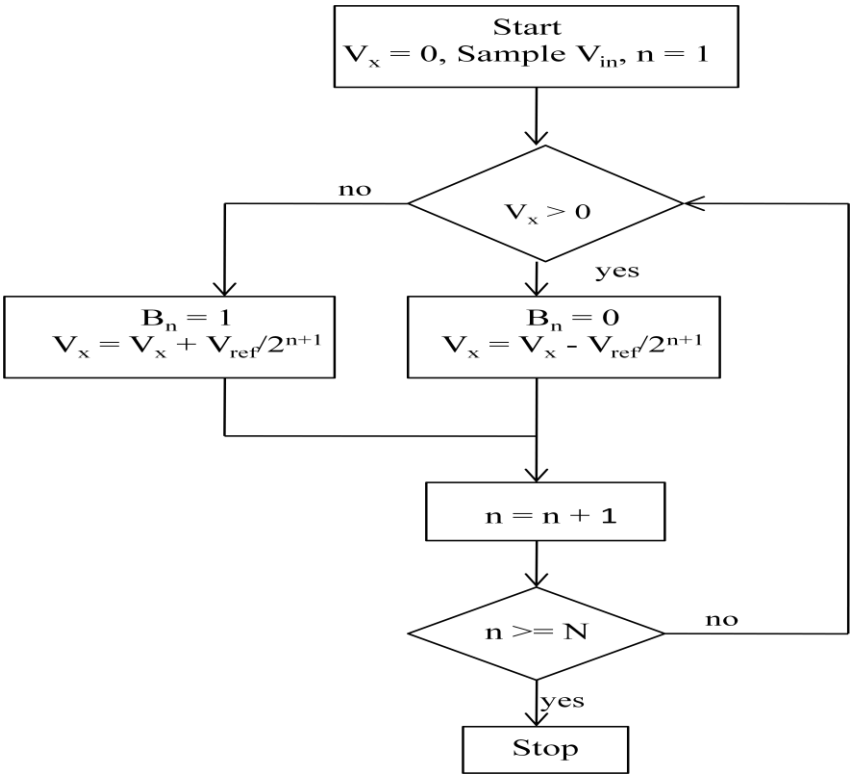


Figure 2: Flow chart of SAR ADC operation

A Charge Redistribution Successive Approximation Register (CR-SAR) Analog to Digital Converter [10] represents an implementation of the above SAR-ADC architecture. It combines the DAC, subtraction circuit, sample and hold circuit into a switch capacitor array. The schematic of a CR-SAR-ADC is shown in Figure 3. The operation of a CR-SAR-ADC can be divided into three modes, namely sampling mode, hold mode and redistribution mode. The operations of the three modes are explained as follows.

Sampling Mode: During the sampling mode S_1 is connected to input signal and node A is being reset through S_2. The comparator acts as an operational amplifier when S_2 is closed

and makes the node voltage (V_x) to zero. The bottom plates of all the capacitors in the array are connected to input voltage (V_{in}) through switches b_1, b_{n-1}, b_n.

Hold Mode: During this mode, S_1 is switched back to V_{ref} and the comparator is taken out of the voltage follower mode by opening S_2. Then the bottom plates of all the capacitors in the array are grounded through switches b_1, b_{n-1}, b_n. This causes node voltage V_x to be $-V_{in}$, thereby holding the input signal on the capacitor array.

Redistribution Mode: This mode produces the necessary voltages to be compared with the input signal and approximates the analog signal in terms of digital bits. It starts by producing the most significant bit (MSB) by connecting the largest capacitor in the array whose value is ($2^{N-1}C_0$) to V_{ref} through b_1, where C_0 is the unit capacitor in the array. This switching causes the voltage at node A (governed by the law of charge conservation) to rise to

$$V_x = -V_{in} + \frac{V_{ref}}{2}$$

This node voltage is compared with signal ground (equivalently comparing V_{in} with $V_{ref}/2$) and subsequently the ADC produces the most significant bit B_1. If the voltage at node A is lesser than ground voltage, it implies that V_{in} is greater than $V_{ref}/2$ and the MSB is "1". Similarly if the voltage at node is greater than the ground voltage, it shows that V_{in} is lesser than $V_{ref}/2$ and the MSB is "0". The comparator output controls the next switch transition. If B_1 is high, the MSB capacitor remains connected to V_{ref} and the next largest capacitor in the array whose value is $2^{N-2}C_0$ is connected to V_{ref}, raising V_x. If B_1 is low, causes MSB capacitor will be switched back to ground and the next largest

capacitor is connected to V_{ref}, lowering V_x. The above process is repeated for N times until the digital outputs are produced.

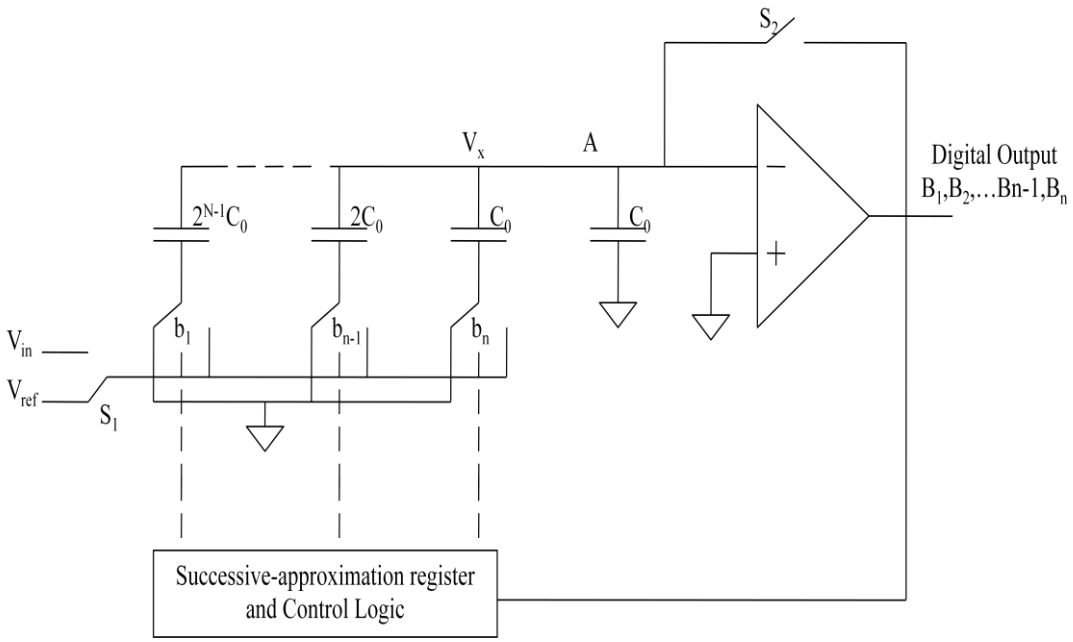


Figure 3: N-bit Capacitive DAC based SAR-ADC

The equivalent circuit of the charge-redistribution DAC during the redistribution mode is shown in Figure 4. The node voltage V_x during each switching activity in the redistribution mode is determined by the law of charge conservation. This can be equated as $Q_{current} = Q_{inp}$. $Q_{current}$ is the charge stored in the array during current switching and Q_{inp} is the charge stored in the array during sampling operation. To compute voltage V_x in Figure 4, we have

$$C_v * (V_x - V_{ref}) + C_g * V_x = (-2^N C * V_{in})$$

By solving this equation we have

$$V_x = -V_{in} + \frac{C_v V_{ref}}{\sum C}$$

Where $C_v = \sum_{n=1}^{N} C_n b_n$

$$\sum C = 2^N C_0$$

C_v = group capacitance connected to $V_{ref,}$

C_g = group capacitance connected to ground

N = Resolution of the converter

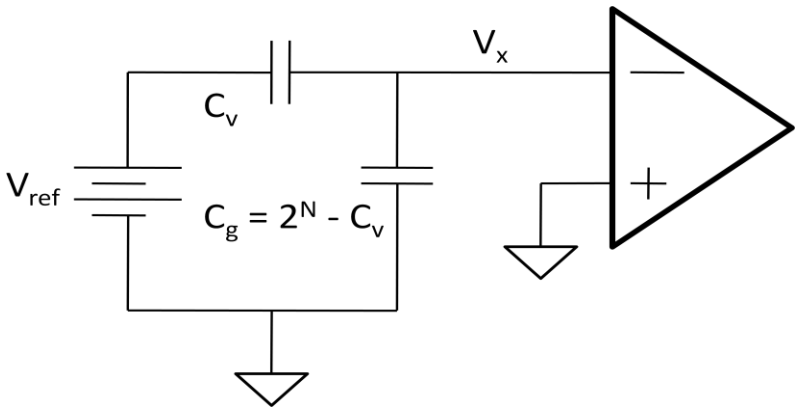


Figure 4: Equivalent circuit of N-bit Capacitive DAC during charge redistribution

We can observe that SAR-ADC mainly depends on the performance of capacitive DAC array. Even though this ADC consumes less power, it has its own limitations which are discussed as follows. The major limitations of this type of architecture are slow speed due to the large node capacitance seen at the inverting terminal of the comparator and being sensitive to parasitic capacitance. The parasitic capacitance plays an important role in determining the accuracy of a charge scaling DAC. Figure 5 portrays a capacitor along with parasitic capacitance associated with it. A binary weighted capacitor C_{bi} is formed

by the enclosure of two polysilicon (metal) layers poly1 (metal1) and poly2 (metal2) for the top and bottom plates respectively. A substantial parasitic capacitance C_{p2} exists when the substrate below the bottom plate is connected to analog ground. This C_{p2} may be as large as 20 percent of C_{bi}, where as C_{p1} accounted from the top plate due to the interconnect lines may vary from 1 to 5 percent of C_{bi}.

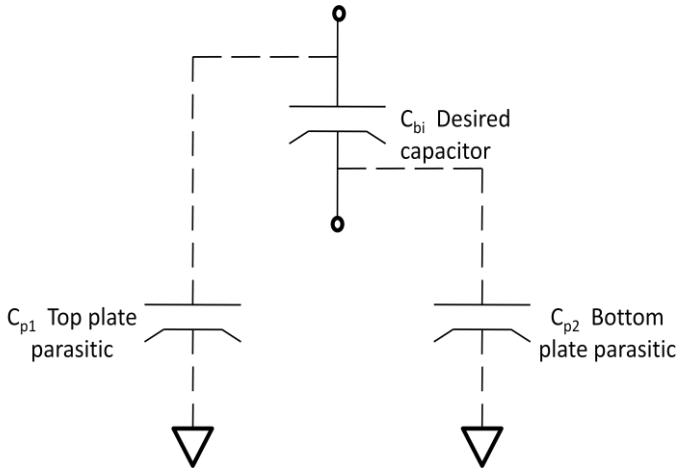


Figure 5: Model of integrated capacitor along with parasitic capacitance

The switch induced error in a DAC circuit is another contributor to the performance limitation. As MOS transistors are used as switches to connect top and bottom plate of a capacitor, these are affected by the channel charge injection as well as clock feedthrough effect. Increase in the converters resolution, requires large capacitor values which in turn increases area and power consumption. To minimize the parasitic capacitance effect, bottom plates of the capacitors are connected to V_{ref} and not to the comparator input.

2.2 Estimation of CR-SAR-ADC power consumption

The energy consumption of a SAR-ADC is mainly attributed by charging capacitors to V_{ref} in the DAC capacitor array. This section explains how to estimate the energy consumed by charging these capacitors. When constructing an N-bit capacitive DAC as shown in Figure 6, (N+1) capacitors are required to have total capacitance of $2^N C_0$ rather than $(2^N-1) C_0$. We use a 2-bit CR-SAR-ADC circuit in the analysis, whose capacitor array is shown in Figure 7. The equations presented here can be generalized to an arbitrary size capacitor array.

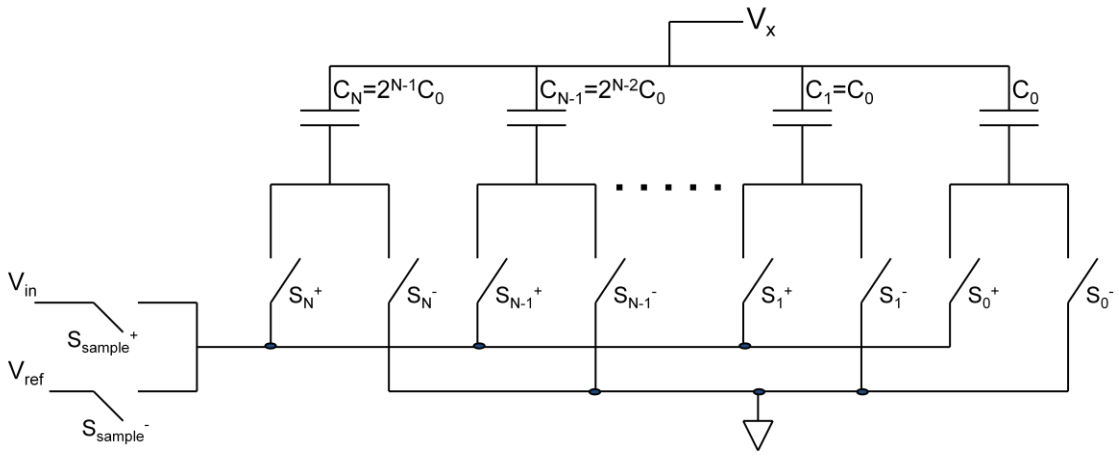


Figure 6: N-bit capacitive DAC

Initially the input signal V_{in} is sampled by the 2-bit capacitor array through switches S_{sample}^+, S_2^+, S_1^+, and S_0^+ while the node voltage V_x is being reset. After sampling, the DAC array holds the input signal by grounding the bottom plates of all the capacitors in the array through S_2^-, S_1^-, and S_0^- (Figure 8 (a)). Before the redistribution mode starts, Switch S_{sample}^- is closed for providing comparison with reference voltage V_{ref}. The bottom

plate of the C_2 is switched to V_{ref} through S_2^+ as shown in Figure 8 (b) causing V_x to settle to

$$V_{x[1]} = -V_{in} + \frac{V_{ref}}{2}$$

$V_{x[1]}$ is the voltage at node X during time 1 when the MSB capacitor (C_2) in the array is switched to V_{ref}. If $V_{x[1]}$ is less than zero, then the input voltage is greater than half of the reference voltage ($V_{in} > V_{ref}/2$) making MSB B_1 as 1 and C_2 is left connected to V_{ref}. Otherwise B_1 is assigned to be 0 and C_2 is reconnected to ground. Similar to the above process, to determine the next bit, the next largest capacitor (C_1) is connected to V_{ref} causing $V_{x[2]}$ to settle to some value depending on the previous bit value (Figure 8 (c), 8 (d)).

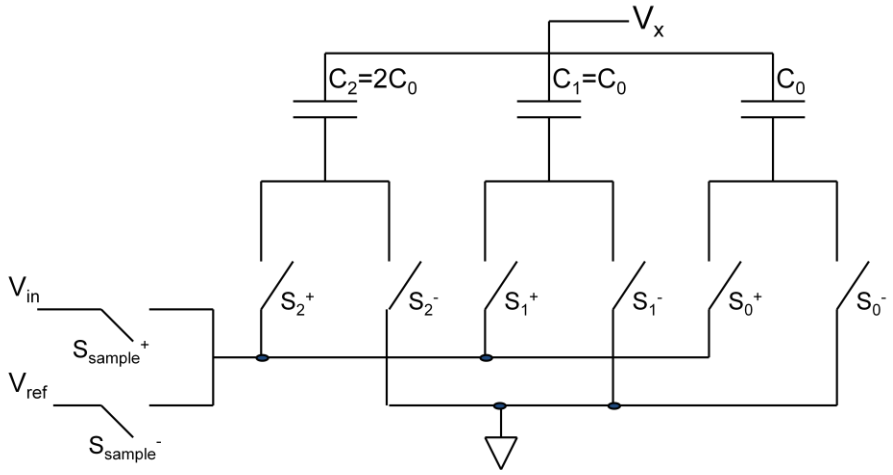


Figure 7: 2-bit capacitive DAC

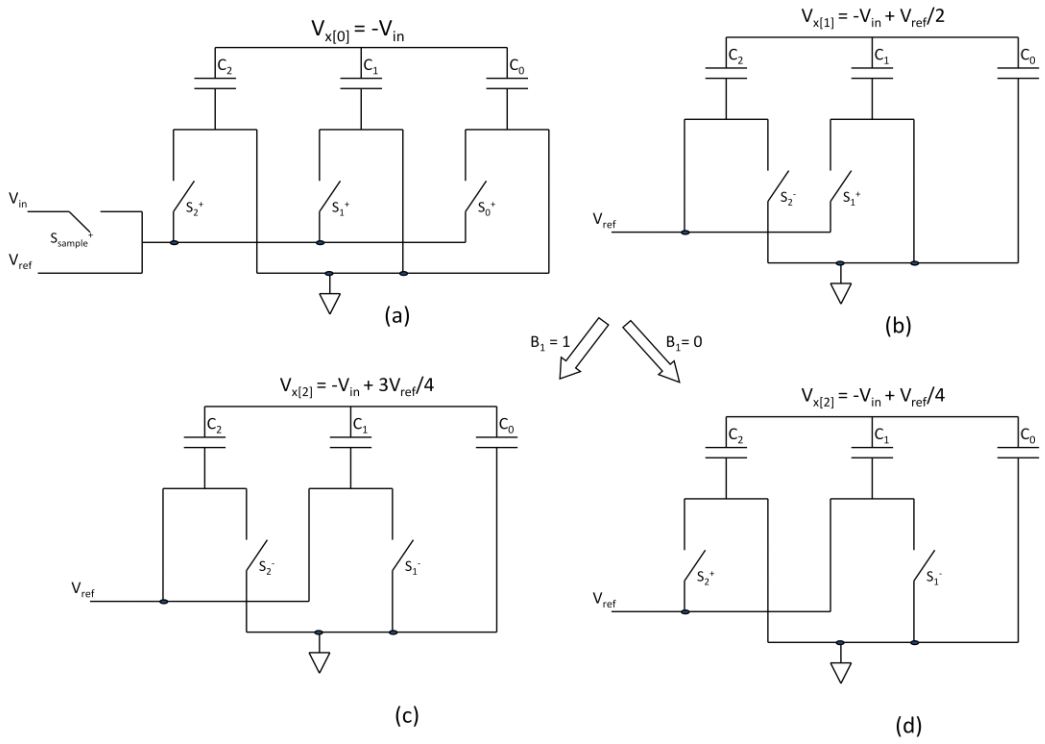


Figure 8: Operation of 2-bit capacitive DAC

A detailed energy expression for CR-SAR-ADC is presented in literature [1]. Here we briefly discuss the key points presented in [1]. Energy can be expressed as:

$$E = V_{ref} * Q$$

Where Q is the charge moved from voltage reference source to charge the capacitor. The value of Q is expressed as capacitance times the difference in voltage across the capacitor during the current and previous operation. With respect to Figure 8 (b), charge stored in the array when C_2 is connected to V_{ref} can be expressed as

$$Q = 2C_0\{(V_{ref} - V_{x[1]}) - (0 - V_{x[0]})\}$$

Where $V_{x[1]} = -V_{in} + V_{ref}/2$

$V_{x[0]} = -V_{in}$

Substituting these values in above equation, we get

$$Q = 2C_0 \left\{ \left(V_{ref} + V_{in} - \frac{V_{ref}}{2} \right) - V_{in} \right) \right\}$$

By substituting the value of charge in the energy equation, we obtain

$$E_{0\to1} = V_{ref} * 2C_0 * \left\{ \left(V_{ref} + V_{in} - \frac{V_{ref}}{2} \right) - V_{in} \right) \right\} = \mathbf{C_o V_{ref}^2}$$

Where $E_{0\to1}$ is the energy consumed when the largest capacitor in the array is connected to V_{ref}. At the end of the first period of redistribution operation, $V_{x[1]}$ is compared with ground voltage producing B_1. If B_1 is 1, the next largest capacitor 'C_1' is connected to V_{ref} as shown in Figure 8 (c). The total energy drawn from V_{ref} during this time

$$E_{1\to2} = V_{ref} \{ (2C_0 + C_0) * (V_{ref} - V_{x[2]}) - 2C_0 * (V_{ref} - V_{x[1]}) - C_0 * (0 - V_{x[1]}) \}$$

$$= \frac{\mathbf{C_o V_{ref}^2}}{\mathbf{4}}$$

Where $V_{x[2]} = -V_{in} + \frac{3V_{ref}}{4}, V_{x[1]} = -V_{in} + \frac{V_{ref}}{2}$

$E_{1\to2}$ is the energy consumed when the second largest capacitor in the array is connected to V_{ref}. However if B_1 is 0, C_2 is switched down and C_1 capacitor is switched up as shown in Figure 8 (d).

$$E_{1\to2} = V_{ref} * C_0 * \{ (V_{ref} - V_{x[2]}) - (0 - V_{x[1]}) \} = \frac{\mathbf{5C_o V_{ref}^2}}{\mathbf{4}}$$

$$\text{Where } V_{x[2]} = -V_{in} + \frac{V_{ref}}{4}, V_{x[1]} = -V_{in} + \frac{V_{ref}}{2}$$

Where $V_{x[2]}$ is the node voltage when C_1 is switched to V_{ref}. We can generalize the equations as

$$E_{0\to1} = V_{ref} * 2^{n-1}C_0 * \{ (V_{ref} - V_{x[1]}) - (0 - V_{x[0]}) \}$$

$$E_{1\to2} = V_{ref}\{ B_{1*}2^{n-1}C_0[(V_{ref} - V_{x[2]}) - (V_{ref} - V_{x[1]})] + 2^{n-2}C_0[(V_{ref} - V_{x[2]}) - (0 - V_{x[1]})] \}$$

Similarly, for a 3-bit SAR-ADC, the energy consumption during the third conversion cycle can be expressed as:

$$E_{2\to3} = V_{ref}\{ B_1 * 2^{n-1}C_0 + B_2 * 2^{n-2}C_0[(V_{ref} - V_{x[3]}) - (V_{ref} - V_{x[2]})] + 2^{n-3}C_0[(V_{ref} - V_{x[3]}) - (0 - V_{x[2]})] \}$$

For a N-bit ADC we use $E_{n_{\to}n+1}$ to represent the energy equation when switching takes place and n is the resolution. From the above equations we can analyze that if there is a bit increase, there is an additional term in the energy equation.

$$E_i = V_{ref} * C_0 * \left[\left(\sum_{i=1}^{m-1} b_i * 2^{N-i} \right) + 2^{N-m}(V_{ref} - V_{x[m]}) - \left(\sum_{i=1}^{m-1} b_i * 2^{N-i} \right)(V_{ref} - V_{x[m-1]}) - 2^{N-m}(0 - V_{x[m-1]}) \right]$$

Where **N** = Resolution of the ADC

m = number of energy calculations required (m=N)

i = loop variable

b = Digital output obtained during each conversion

$\mathbf{V_{ref}}$ = Voltage reference

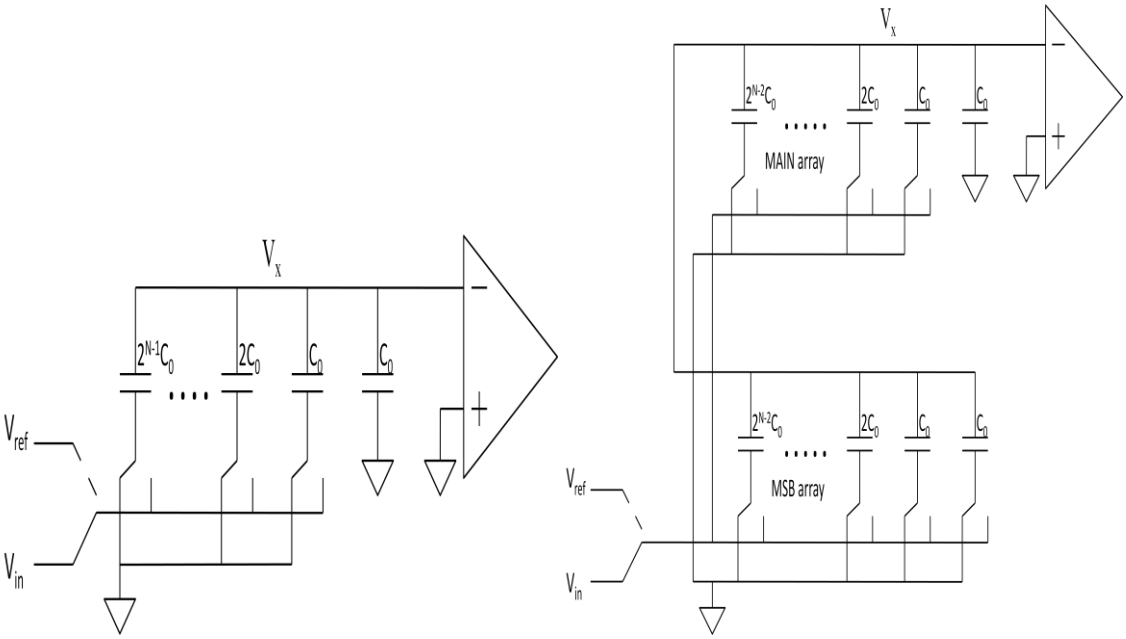
$\mathbf{C_0}$ = Unit capacitance

$\mathbf{V_x}$ = Node voltage

2.3 Previously proposed techniques for low-power SAR-ADC

To reduce power consumed by charging the capacitor array during conversion, several low-power techniques are proposed in [1]. Among them, an attractive approach is the capacitor split technique. It splits the MSB capacitor into N-1 binary weighted sub-capacitors and saves energy up to 37% compared to a conventional switching method. Figure 9 (b) displays an N – bit split capacitor array approach. It is evident that the MSB capacitor is split into N-1 binary weighted sub capacitors (replica of the rest of the binary weighted capacitors). At the beginning of a conversion, the analog input signal is sampled by the capacitor array similar to the traditional circuit. The operation of split capacitor array is similar to traditional converter during up transition and differs only during down transition. The up transition refers to charging the next largest capacitor in the array when the input voltage is greater than the previous node voltage. The down transition represents charging the next largest capacitor in the array when the input voltage is lesser than previous node voltage. For i^{th} up transitions, the i^{th} capacitor in the main array is switched to V_{ref}, while for the corresponding down transitions, i^{th} capacitor in the MSB array is switched to ground. Thus the split capacitor array approach avoids

throwing away the charge that has been stored on to the array by charge re-utilization during the down transition.



(a): A conventional N-bit CR-SAR-ADC

(b): An N-bit split capacitor array CR-SAR-ADC

Figure 9: Conventional Vs Split capacitor array CR-SAR-ADC

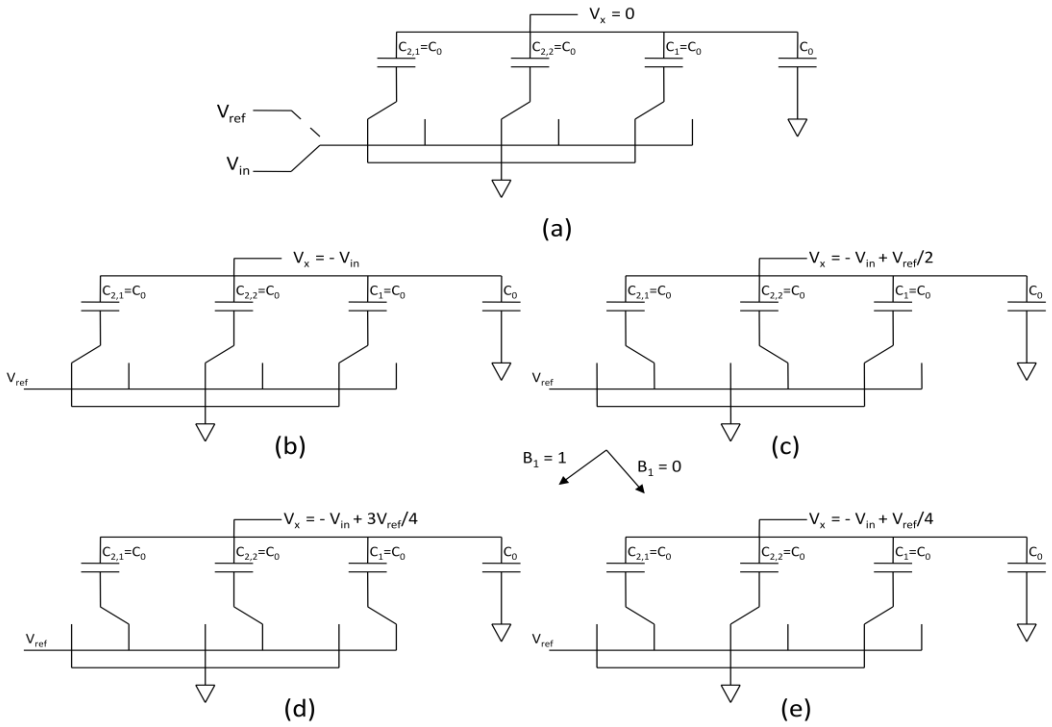


Figure 10: Operation of 2-bit split capacitor array SAR-ADC

To further illustrate the power saving by capacitor splitting technique, the energy consumption of a 2-bit ADC with capacitor splitting technique is discussed in the following. In figure 10, V_x represents the node voltage (node connected to negative terminal of the comparator), V_{in} & V_{ref} are the analog input signal and voltage reference respectively, C_0 and C_2 denote the unit capacitor and MSB capacitor which is split into $C_{2,1}$ and $C_{2,2}$ respectively. At the beginning of a conversion, the analog input signal is sampled by the capacitor array similar to the traditional circuit. The MSB array which has two unit size capacitors is charged to $V_x = - V_{in} + V_{ref}/2$ as shown in Figure 10 (c). The energy required to charge the MSB capacitor is:

$$E_{0\rightarrow1} = \mathbf{C_o V_{ref}^2}$$

Let's consider the caseof MSB = 1, then C_1 charges up to produce the necessary node voltage (Figure 10 (d)). The energy consumed in this step is:

$$E_{1\to2} = \frac{\mathbf{C_o V_{ref}^2}}{\mathbf{4}}$$

If MSB = 0, traditionally converters discharges C_2 and charges C_1. Thus energy consumed is:

$$E_{1\to2} = \frac{\mathbf{5C_o V_{ref}^2}}{\mathbf{4}}$$

It is seen that the energy consumed in down conversion is five times more than that in the up conversion. In the split capacitor array architecture, instead of discharging the entire C_2 or MSB in this case, one of the unit capacitors in the MSB array (either $C_{2,1}$ (or) $C_{2,2}$) is discharged to get corresponding node voltage (Figure 10 (e)). The energy consumed in this step is

$$E_{1\to2} = -V_{ref} * C_0 * \{ V_{x[2]} - V_{x[1]} \} = \frac{\mathbf{C_o V_{ref}^2}}{\mathbf{4}}$$

Where $V_{x[2]} = -V_{in} + \frac{V_{ref}}{4}, V_{x[1]} = -V_{in} + \frac{V_{ref}}{2}$

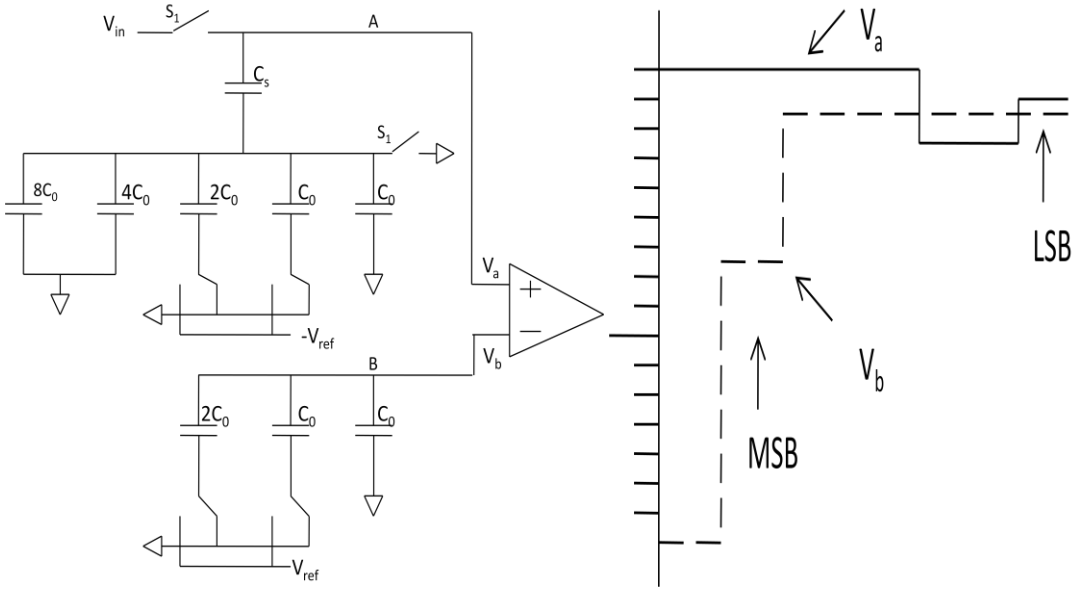
So the energy consumed is the same as that the traditional up conversion, but is less when compared to the traditional down conversion. The generalized energy equation for up and down conversions for a capacitor splitting ADC is:

$$E_1 = \frac{\mathbf{2^n C_o V_{ref}^2}}{\mathbf{4}}$$

$$E_{2(up)} = \frac{\mathbf{2^n C_o V_{ref}^2}}{\mathbf{16}} \, , E_{2(down)} = \frac{\mathbf{2^n C_o V_{ref}^2}}{\mathbf{16}}$$

The energy consumption for determining the rest of the bits can be analyzed using the same method. Energy can be significantly saved for output codes with smaller values where more down transitions take place in the array during the conversions. But for other codes that have larger values, energy saving is not significant (follows the traditional switching approach) because more up transitions occur. This architecture requires double the number of switches, but it should have roughly the same area and consumes low power when compared to capacitive-DAC array. Employing additional CMOS switches potentially make the circuit more prone to the effect of channel charge injection and clock feedthrough.

Another low-power SAR-ADC design is presented in [2]. It utilizes two separate capacitor arrays with unequal sizes to determine more significant bits and less significant bits respectively. It dramatically reduces the total capacitance that need to be charged during conversion. The operation of this approach can be explained with a 4-bit ADC circuit as shown in Figure 11 (a).



(a) (b)

Figure 11: 4-bit two step low energy SAR-ADC with negative voltage reference

During the Sampling mode, switches labeled as S_1 are closed. During this time, input (V_{in}) is sampled to node A while node B is being reset. The node voltage V_a holds the input signal and the bottom capacitor array is charged/ discharged to determine the first two bits which are MSBs. This operation is called coarse-level search and utilizes a total capacitance $2^{N/2}C_0$ (N=4 in this case) which is far lesser than the traditional 2^NC_0. After the coarse-level conversion, the top capacitor array is charged and discharged to shift V_a while keeping V_b unchanged to determine the last two bits which are LSBs. This operation is called fine- level search and requires total capacitance of 2^NC_0 to provide the necessary voltage swing ($V_{ref}/8$, $V_{ref}/16$). Out of the 2^NC_0, the N/2 largest capacitors of the array are always grounded just to provide necessary voltage swing. Since top array is only used to determine the LSBs, the voltage swing in node A is always smaller when

compared to node B. A graph in Figure 11(b) explains this concept. It can be observed that a negative voltage reference is used to shift down V_a. In order to avoid using the negative voltage reference, a voltage boosting technique was proposed as shown in Figure 12. At the end of the coarse-level search, node B is further boosted up by $V_{ref}/2^{N/2}$, by connecting C_b to V_{ref}. C_b is called as a boosting capacitor and it produces voltage equivalent to V_{LSB} in the coarse-level array DAC. By this technique the voltage V_a is always smaller than V_b, thus eliminating the need for negative reference voltage. The energy consumed by boosting technique is small as C_b is small.

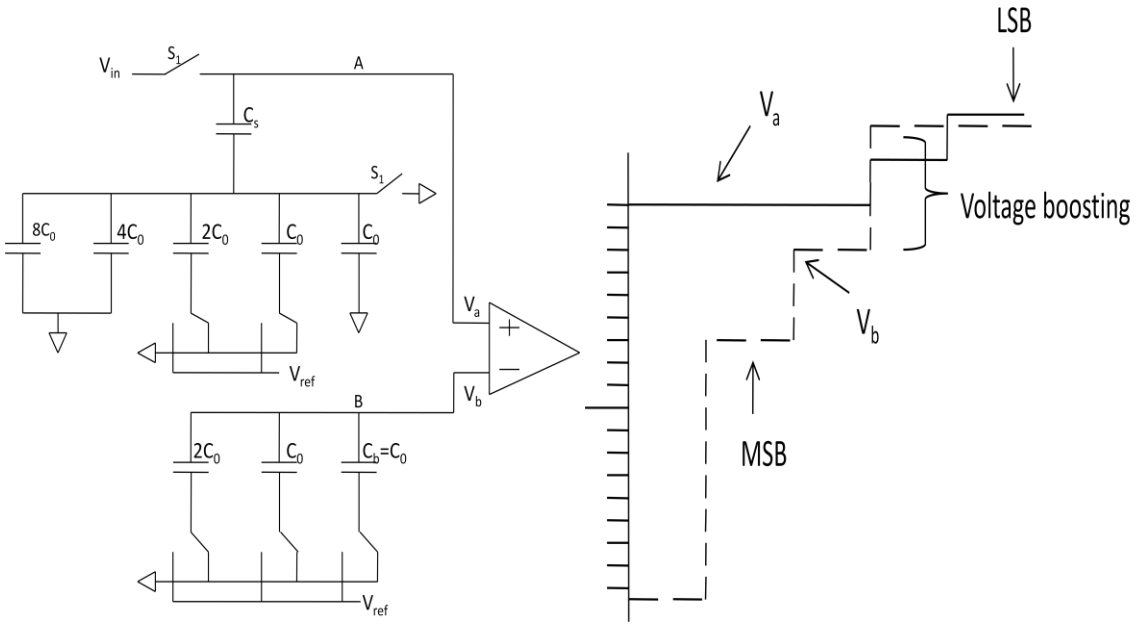


Figure 12: 4-bit two step low energy SAR-ADC with voltage boosting

So the energy required to charge the MSB capacitor

$$E_{0\to1} = \mathbf{C_o V_{ref}^2}$$

If MSB = 1, the bottom array performs up transition (Figure 11 (a)).

$$E_{1\to2} = \frac{\mathbf{C_o V_{ref}^2}}{\mathbf{4}}$$

If MSB = 0, the bottom array performs down conversion

$$E_{1\to2} = \frac{\mathbf{5C_o V_{ref}^2}}{\mathbf{4}}$$

Similarly the LSBs are generated using the top array with very low energy consumption when compared to bottom array. This is because only small sized capacitors are used for switching. From a N-bit two step architecture, it can be observed that the energy required to sample V_{in} is given by

$$E_0 = \mathbf{C_s V_{in}^2}$$

The energy required to charge MSB capacitor in the bottom array is given by

$$E_1 = \mathbf{2^{N-M-2} C_0 V_{ref}^2}$$

Energy for up transistion

$$E_{2(up)} = \mathbf{2^{N-M-4} C_0 V_{ref}^2}$$

Enrgy for down transistion

$$E_{2(down)} = \mathbf{2^{N-M-4} 5 C_0 V_{ref}^2}$$

Where N = converter resolution, M = N/2

By employing two-capacitor arrays of unequal sizes, the total number of capacitors ($2^N C_0$ + $2^{N/2} C_0$) required is greater when compared to traditional SAR-ADC. The voltage boosting technique causes reliabitlity problem when $V_{ref} = V_{dd}$, Since V_a can swing greater than Vdd. Further more the sampling capacitor which is connected to node A in

Figure 12 is floating during the fine-level search. This floating capacitor adds parasitic capacitance (C_p) which affects the conversion accuracy. The impact of C_p on the accuracy of the ADC conversion can expalined as follows with the help of Figure 13

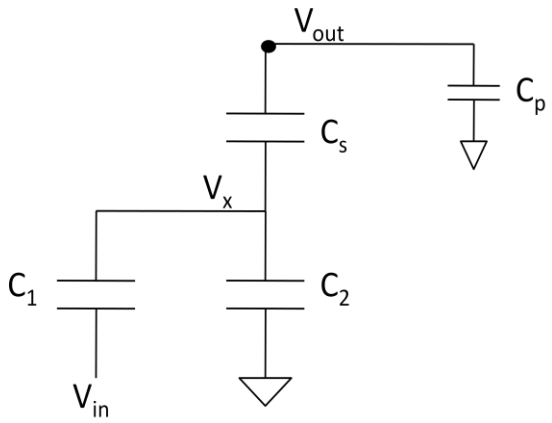


Figure 13: Effect of parasitics on capacitors connected in series fashion

According to charge conservation, the node voltage V_x can be derived as

$$C_1 * (V_{in} - V_x) = \left(C_2 + \frac{C_s C_p}{C_s + C_p}\right) * V_x$$

$$V_x = \frac{C_1 * V_{in}}{C_1 + C_2 + \frac{C_s C_p}{C_s + C_p}}$$

In addition, V_{out} can be expressed as

$$V_{out} = \frac{C_s * V_x}{C_s + C_p}$$

By substituting the value of V_x in the above equation, we get

$$V_{out} = \frac{C_1 * C_s * V_{in}}{C_1 + C_2(C_s + C_p) + C_s C_p}$$

$$\text{Ideally } V_{out} = \frac{C_1 * V_{in}}{C_1 + C_2}$$

Compared with the ideal equation we can observe that the parasitic capacitance affects the output node voltage.

Very recently, two control algorithms that can adaptively adjust the searching range during ADC conversion are investigated to reduce SAR-ADC power consumption [3]. Both control algorithms reduce dynamically the number of conversion steps. It has been shown that up to 25% energy saving per conversion cycle can be achieved.
The basic assumption used in these approaches is that the difference between two successive samples is smaller than δ (band size)

$$\left|V_{a,k-1} - V_{a,k}\right| < \delta$$

Where $V_{a,k-1}$ and $V_{a,k}$ corresponds to previous and next (current) analog input values. Rather than performing a full conversion for each new sample, these algorithms utilize δ to determine the most significant bits of the previous converted digital value that will be kept in the current conversion. The two algorithms differ from how the parameter δ (band size) is determined. In the *Range checking algorithm (RCA)*, the band size is an externally defined constant input where as in *Variable range algorithm (VRA)*, the band size adjusts dynamically by the algorithm itself to accommodate the current signal dynamics.

Figure 14 shows the general flow chart of the algorithms proposed in [3] and an example to illustrate the algorithm. We assume the algorithm takes previously converted digital value N_{k-1}, digital equivalent of the band size is d and converter resolution is n. The algorithm starts by calculating the upper (N_{k-1} + d) and lower bounds (N_{k-1} – d). An

XOR operation is performed on the calculated bounds to determine m, which is the number of bits to be retained for the next operation. Leading number of zeroes gives the m value. Since the MSBs have been determined, n-m conversion steps are required to generate LSBs, starting from the bit position n-m-1. Finally a condition is checked to detect the whether the converted value is within the range.

$$\text{i.e.} \quad N_{k-1} + d \leq N_k \geq N_{k-1} - d$$

If the converted value is out of range, a new conversion starts from the beginning, resulting in more clock cycles and large energy consumption. Unlike the RCA algorithm, the delta (d) for the VRA algorithm is determined by the difference between the last two samples. Thus δ may change for each conversion cycle. So a large delta leads to band enlargement, while a small δ leads to band compression. Band size is inversely proportional to m. So if band size is large then m is small, which means less energy is saved and vice-versa. The above algorithms are based on the fact that any two successive samples should be within the calculated boundaries. But in real world, input signals vary randomly. If the converted value is out of range then more clock cycles and additional energy consumption are required to convert an analog value which makes it worse than a traditional conversion.

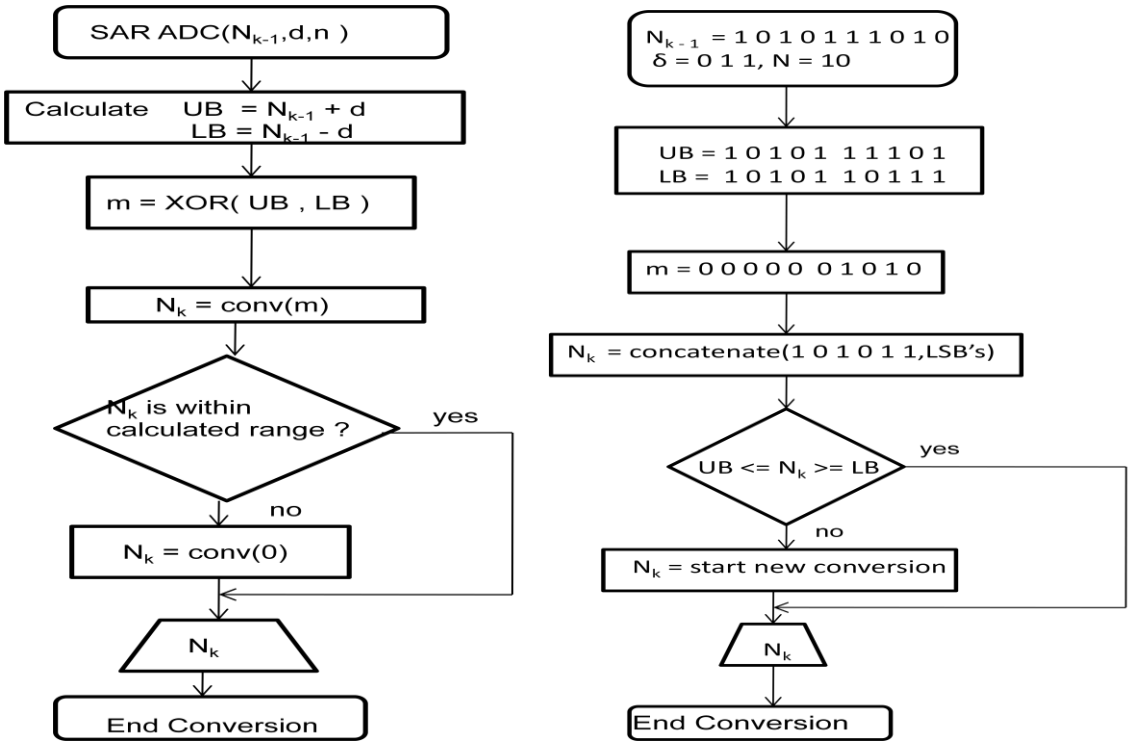


Figure 14: Flow chart of control algorithms in [3]

In [4], Lampinen et al. proposed techniques to reduce SAR-ADC energy consumption and speed up the conversion by a double successive approximation algorithm. This algorithm has two phases. The first phase uses non-linear range selection to determine the coarse-level of the signal logarithmically and the second phase relies on a linear binary tree search similar to traditional method to determine the fine-level of the signal. By logarithmically finding the coarse-level of the signal, it requires less capacitors to be charged, hence reducing energy consumption.

Furthermore, Chang et al. proposed an energy saving switching sequence to maximize the energy savings during MSB conversion in a fully differential SAR-ADC circuit [5]. In a

traditional differential mode operation of an SAR-ADC, causes the largest energy consumption is due to producing MSB. With the proposed method in [5], almost no energy is consumed in charging the capacitor array for determining MSB. This is achieved by the following circuit technique: after sampling the input signal, instead of switching the MSB capacitors, the entire capacitor array is grounded to determine MSB.

CHAPTER 3

LOW-POWER SAR-ADC DESIGN WITH SPLIT VOLTAGE REFERENCE

In a traditional SAR-ADC the capacitor array switches between ground and voltage reference level V_{ref}. Since the energy consumption for charging a capacitor is proportional to the square of the voltage level. If the voltage level that the capacitor needs to be charged can be reduced by a half, the power consumption of the charge scaling DAC can be reduced by 75%. In this chapter, we propose a low-power SAR-ADC implementation whose voltage reference is separated into two references with each level being half of the original voltage reference level. As a result, the voltage swing of the capacitor array is reduced by two. Also the total capacitance in the capacitor array is reduced by half and its power consumption is only 12.5% of the power consumption of the traditional ADC. Note that the proposed ADC has the same dynamic range as the traditional ADC with a voltage reference of V_{ref}.

3.1 Proposed ADC implementation with Split Voltage Reference

The proposed ADC is a single-ended implementation. It assumes the input signal has an input range varying from 0 to V_{ref}. The schematic of the implementation is shown in Figure 15

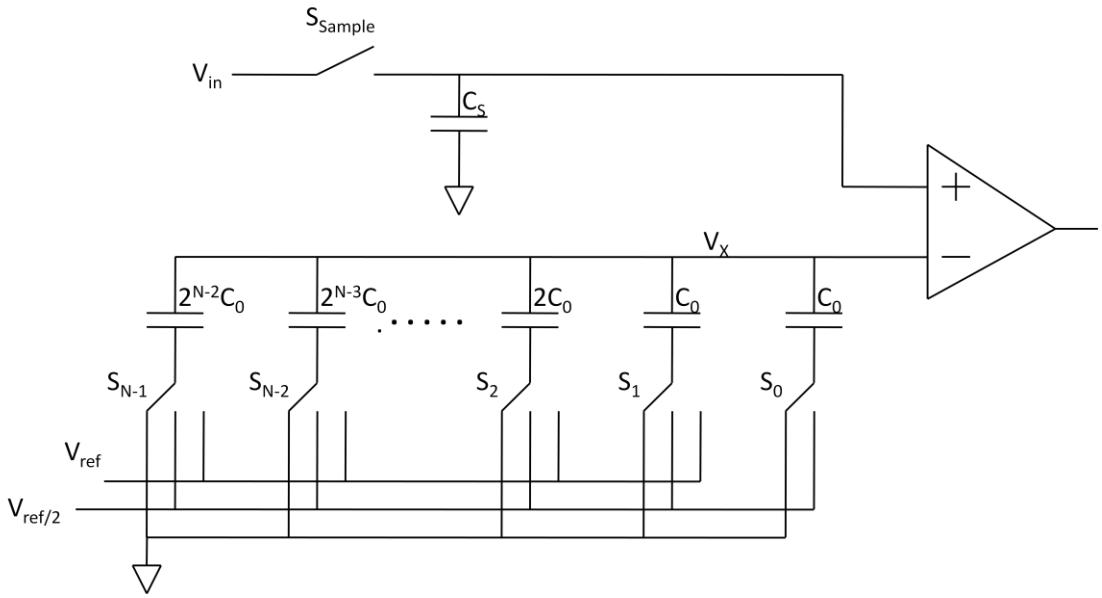
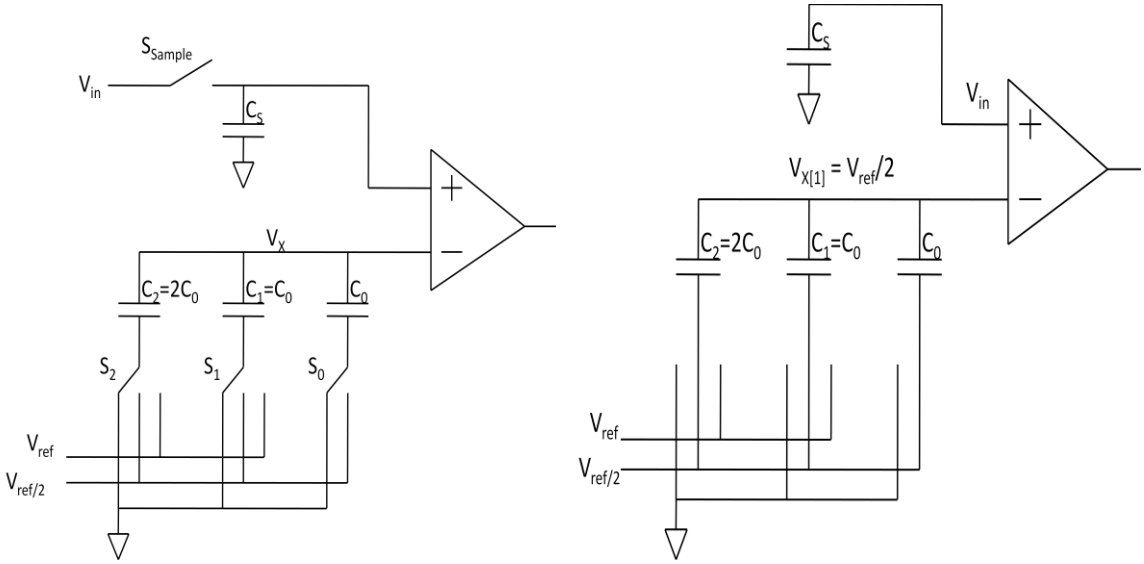


Figure 15: N-bit SAR-ADC with Split voltage references

The operation of the proposed ADC is very much similar to the traditional ADC except on how to determine the MSB and configure switches between two reference voltages. The operation of the proposed ADC can be explained with a help of 3-bit ADC as shown in Figure 16 (a).

Sample and Hold Mode: In this mode, switch S_{sample} is closed to sample the input signal to capacitor C_s, while the DAC capacitor array is grounded through switches S_2, S_1 and S_0. Unlike a traditional SAR-ADC, in which the entire capacitor array is used to sample the input, here the input signal charges a small capacitor. Thus energy consumed by the sampling capacitor is very small. At the end of sampling operation, Switch S_{sample} opens and the capacitor holds the input voltage until the next conversion.

Redistribution Mode: Before the redistribution mode starts, all the capacitors in the capacitor array is connected to $V_{ref}/2$ to determine MSB. As shown in Figure 16 (b), node voltage V_x changes to $V_{ref}/2$. This node voltage is compared with input signal and produces MSB accordingly. If $V_{in} < V_{ref}/2$, the comparator produces MSB (B_1) as '0' which makes the capacitive DAC to switch between $V_{ref}/2$ and signal ground. If on the other hand, comparator yields MSB as '1', it makes the capacitive DAC to switch between $V_{ref}/2$ and V_{ref}. Thus the capacitor array has to discharge when V_{in} is less than $V_{ref}/2$ and has to charge to V_{ref} when V_{in} is greater than $V_{ref}/2$. So the switching of capacitors in the array is opposite in above two cases.



(a): 3-bit example of Split voltage reference SAR-ADC

(b): Determination of MSB in 3-bit Split voltage reference SAR-ADC

Figure 16: Split voltage reference SAR-ADC

First, we assume that the MSB is ‘0’ which means that input signal is lesser than $V_{ref}/2$. The largest capacitor which corresponds to the second bit (i.e. C_2 in this example) is switched to signal ground from $V_{ref}/2$ (Figure 17 (a)). This makes the node voltage reduce to $V_{ref}/4$. If V_{in} is greater than $V_{ref}/4$, capacitor C_2 is reconnected to $V_{ref}/2$ and B_2 is assigned to be ‘1’ (Figure 17 (c)). Otherwise, C_2 is left connected to signal ground and B_2 is taken to be ‘0’ (Figure 17 (b)). Similarly rest of the bits are determined.

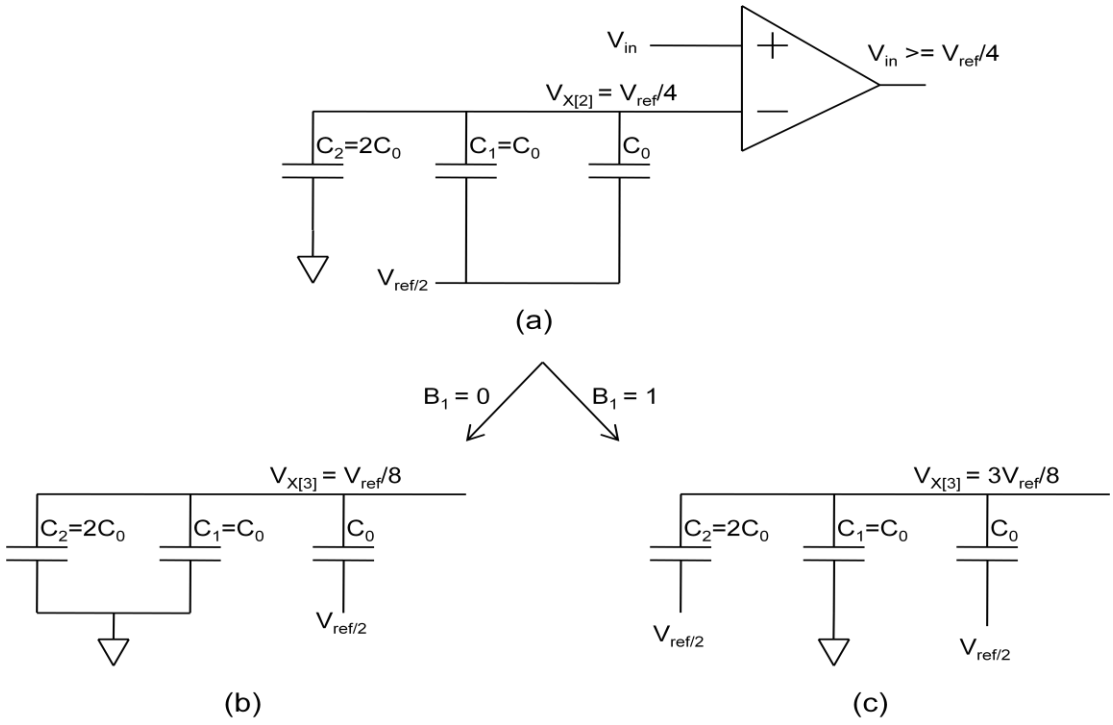


Figure 17: Operation of SAR-ADC with split voltage reference when MSB (B_1) is zero

Now let’s assume that the MSB to be ‘1’, implying that input signal is greater than $V_{ref}/2$. Thus largest capacitor (i.e. C_2 in this example) is switched to V_{ref} from $V_{ref}/2$ (Figure 18 (a)). This switching raises the node voltage V_x to $3V_{ref}/4$. If V_{in} is greater than $3V_{ref}/4$, capacitor C_2 is left connected to V_{ref}. Also B_1 is considered to be ‘1’ (Figure 18 (c)).

Otherwise, the MSB capacitor is reconnected to $V_{ref}/2$ and B_1 is taken to be '0' (Figure 18 (b)). The rest of the bits are determined in the similar manner. In a traditional N-bit ADC, a capacitor array of $2^N C$ is required, while in the proposed design only $2^{N-1} C$ is required. As the MSB capacitor is eliminated, area and energy are saved in the proposed method.

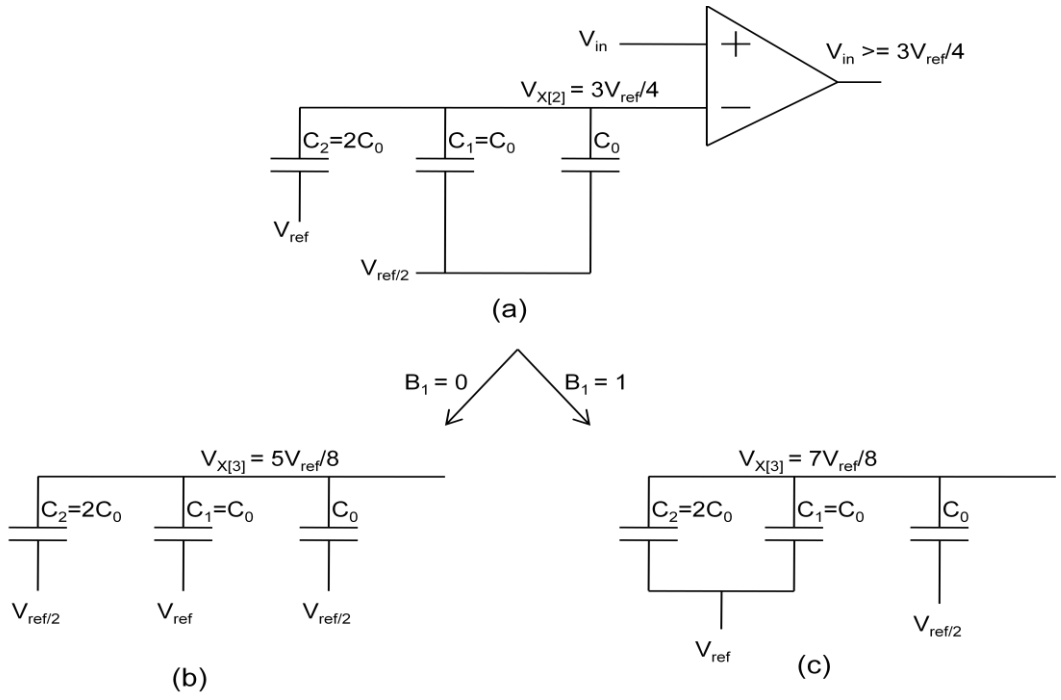


Figure 18: Operation of SAR-ADC with split voltage reference when MSB (B_1) is one

The flowchart of the proposed ADC operation is shown in Figure 19. The flowchart starts with sampling the input voltage and subsequently determining the MSB. According to the MSB output, the capacitive DAC array is made to switch between two voltage references. The iteration continues until all the bits are converted.

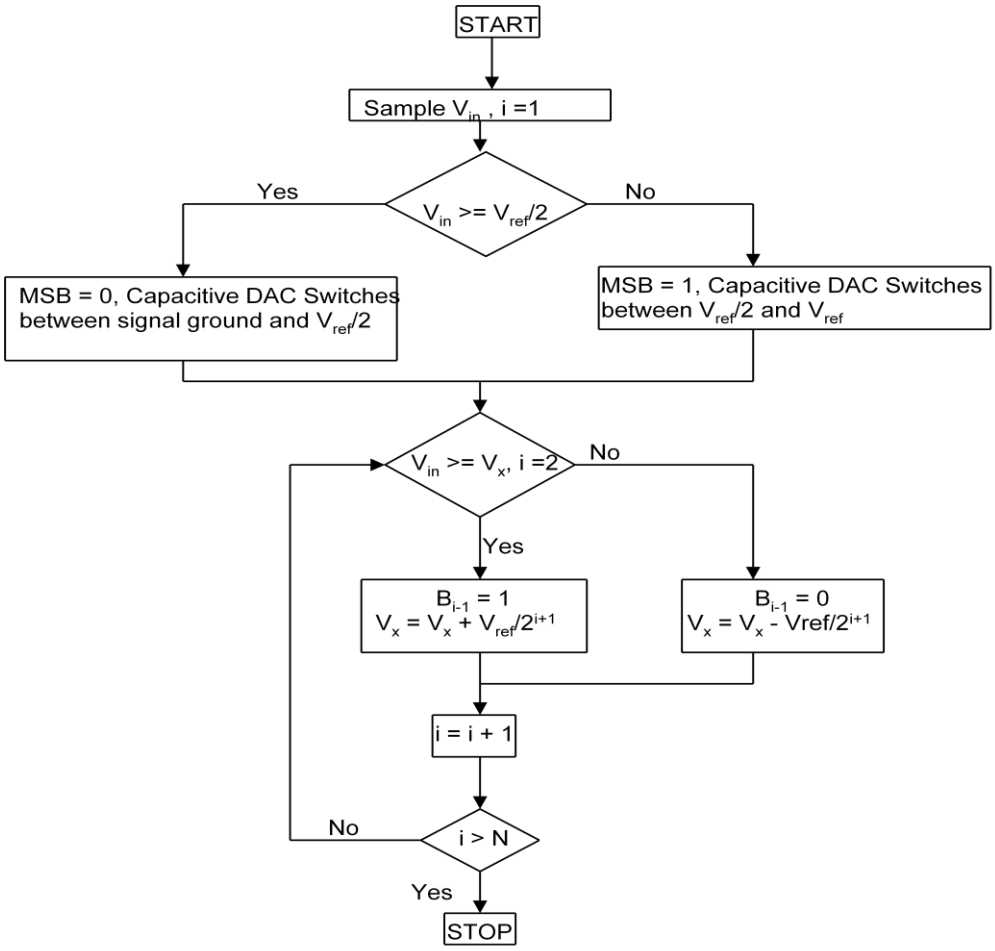


Figure 19: Flow chart of SAR-ADC with split voltage reference

3.2 Switching energy analysis

This section discusses the energy calculation for the proposed 3-bit ADC with reference to [1]. As discussed in the previous section the energy required to determine the MSB is "zero" (Figure 16 (b)). This is evident from equation [1].

$$E_{0\to1} = -\frac{V_{ref}}{2} * (4C_0) * \left\{ \left(V_{x[1]} - \frac{V_{ref}}{2} \right) - V_{x[0]} \right\} = \mathbf{0} - - - (1)$$

$$V_{x[1]} = \frac{V_{ref}}{2}, V_{x[0]} = 0 \ (\ node\ is\ being\ reset)$$

Where $V_{x[1]}$ is the node voltage when all the capacitors in the array is connected to $V_{ref}/2$ and $V_{x[0]}$ is the node voltage during the sampling mode. The effect of parasitic capacitance is usually small and is generally neglected. Assuming the MSB is "0", we can compute the energy consumption for rest of two bits when the capacitive DAC switches between $V_{ref}/2$ and ground.

$$E_{1\to2} = -\frac{V_{ref}}{2} * (2C_0) * \left\{ \left(V_{x[2]} - \frac{V_{ref}}{2} \right) - \left(V_{x[1]} - \frac{V_{ref}}{2} \right) \right\} = \frac{\boldsymbol{C_0 V_{ref}^2}}{\boldsymbol{4}} \quad ---(2)$$

$$V_{x[2]} = \frac{V_{ref}}{4}, V_{x[1]} = \frac{V_{ref}}{2}$$

$V_{x[2]}$ is the node voltage when C_2 is switched to ground (Figure 17 (a)). This C_2 switching would produce the next bit which is B_2. If B_2 is assumed to be one, which implies that the input signal is greater than node voltage. C_2 is switched back to $V_{ref}/2$ and C_1 is connected to ground. The energy computation is shown in equation [3]. Depending upon the input signal B_2 takes zero or one as its output value. The energy equations are shown below

$$E_{2\to3} = -\frac{V_{ref}}{2} * C_0 * \left\{ \left(V_{x[3]} - 0 \right) - \left(V_{x[2]} - \frac{V_{ref}}{2} \right) \right\} = \frac{\boldsymbol{5C_0 V_{ref}^2}}{\boldsymbol{16}} \quad ---(3)$$

$$V_{x[3]} = \frac{3V_{ref}}{8}, V_{x[2]} = \frac{V_{ref}}{4}$$

$V_{x[3]}$ is the node voltage when C1 is switched to ground. If B_2 is assumed to be zero, which implies that the input signal is lesser than node voltage. C_2 is maintained connecting to ground and C_1 is connected to ground. The energy computation is shown in equation [4].

$$E_{2\to3} = -\frac{V_{ref}}{2}\left\{2C_0\left[\left(V_{x[3]}-0\right)-\left(V_{x[2]}-0\right)\right]+C_0\left[\left(V_{x[3]}-0\right)-\left(V_{x[2]}-\frac{V_{ref}}{2}\right)\right]\right\}$$

$$= \boldsymbol{\frac{C_0V_{ref}^2}{16}} \quad ---(4)$$

$$V_{x[3]} = \frac{V_{ref}}{8}, V_{x[2]} = \frac{V_{ref}}{4}$$

Assuming the MSB is "1", we can similarly compute the energy consumption for the rest of the two bits when the capacitive DAC switches between $V_{ref}/2$ and $V_{ref.}$

$$E_{1\to2} = -V_{ref} * (2C_0) * \left\{\left(V_{x[2]}-V_{ref}\right)-\left(V_{x[1]}-\frac{V_{ref}}{2}\right)\right\} = \boldsymbol{\frac{C_0V_{ref}^2}{2}} ---(5)$$

$$V_{x[2]} = \frac{3V_{ref}}{4}, V_{x[1]} = \frac{V_{ref}}{2}$$

If B_2 is assumed to be 1, it implies that the input signal is greater than the corresponding node voltage and causes C_1 switched to V_{ref}

$$E_{2\to3} = -V_{ref}\left\{2C_0\left[\left(V_{x[3]}-V_{ref}\right)-\left(V_{x[2]}-V_{ref}\right)\right]\right.$$

$$\left.+C_0\left[\left(V_{x[3]}-V_{ref}\right)-\left(V_{x[2]}-\frac{V_{ref}}{2}\right)\right]\right\} = \boldsymbol{\frac{C_0V_{ref}^2}{8}} ---(6)$$

$$V_{x[3]} = \frac{7V_{ref}}{8}, V_{x[2]} = \frac{3V_{ref}}{4}$$

If B_2 is assumed to be 0, it implies that the input signal is lesser than the corresponding node voltage and causes C_1 switched to V_{ref} while C_2 being switched back to $V_{ref}/2$

$$E_{2\to3} = -V_{ref} * C_0 * \left\{\left(V_{x[3]}-V_{ref}\right)-\left(V_{x[2]}-\frac{V_{ref}}{2}\right)\right\} = \boldsymbol{\frac{5C_0V_{ref}^2}{8}} ---(7)$$

$$V_{x[3]} = \frac{5V_{ref}}{8}, V_{x[2]} = \frac{3V_{ref}}{4}$$

3.3 Simulation Results

MATLAB simulations are performed to compare the power saving by the proposed technique with other low-power ADC techniques. The above proposed switching method is applied to a 10-bit capacitor array. The unit capacitance is taken to be 100fF with parasitic bottom plate capacitance of 20fF. The proposed method is compared with four switching methods presented in [1]. The simulated results are plotted in Figure 20.

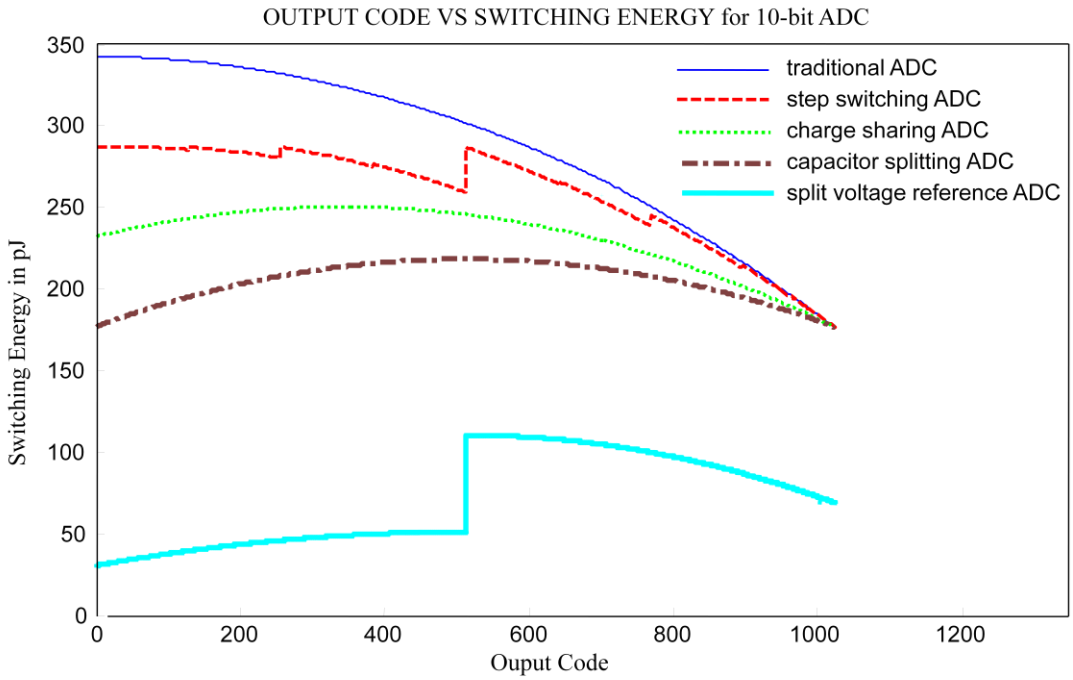


Figure 20: Switching energy for 10-bit ADC for various switching methods

As we can note from Figure 20, there is an increase in the energy consumption for the proposed one at code 512. This is due to the fact that the capacitor array switches between V_{ref} and $V_{ref}/2$ when $V_{in} > V_{ref}/2$. For each method average switching energy is

calculated for the corresponding 10-bit capacitor array and the results are tabulated in Table 1.

Table 1: Average switching energy for different switching methods

ADC Implementation	Average Switching Energy (pJ)
Traditional Switching	287.15
Step Switching	259.50
Charge Sharing	231.96
Capacitor Split	204.36
Voltage Split (proposed one)	70.34

3.4 Discussion

Although the proposed ADC implementation requires two voltage reference levels $V_{ref}/2$ and V_{ref}, it does not increase the circuit complexity in many design cases. In many single ended circuits the signal swing is from 0 to V_{dd} and $V_{dd}/2$ is used as signal ground. In such circuits, the already available V_{dd} and $V_{dd}/2$ can be used as the two voltage reference. Furthermore the need for V_{ref} level can be eliminated with minor modification of the proposed ADC circuit. The modified 3-bit circuit is shown in Figure 21 and its operation is explained briefly in the following.

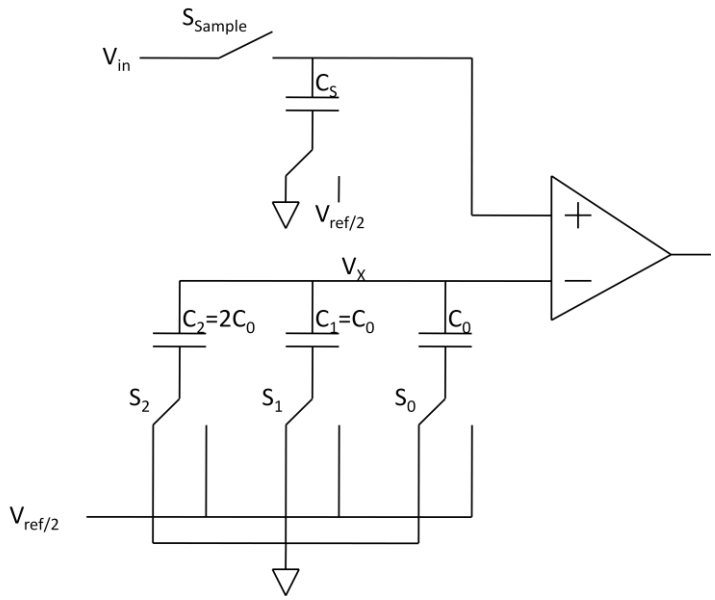


Figure 21: 3 bit ADC which eliminates the use of two reference voltages

During the sampling mode, the bottom plate of the sampling capacitor is connected to $V_{ref}/2$ and C_s samples the input signal. To determine the MSB, all the capacitors in the bottom array are connected to $V_{ref}/2$. This connection increases the node voltage V_x to $V_{ref}/2$. If the input signal is smaller than the node voltage, then capacitors in the bottom array switch to signal ground similar to section 3.2 to produce rest of the bits. If the input signal is greater than the node voltage, bottom plate of the sampling capacitor is connected to ground which reduces the input signal to $V_{in} – V_{ref}/2$. Then the capacitors in the bottom array are switched to ground similar to section 3.2 to produce the rest of the bits. This method has advantages like reduced capacitance, and reduced energy consumption, output swinging rail to rail with half the reference voltage.

CHAPTER 4

CHARGE RECYCLING TECHNIQUES FOR LOW-POWER ADC DESIGN

In all the charge scaling ADC circuits reported in literature, the capacitor arrays are fully discharged after a conversion. When a new conversion starts, the MSB capacitor needs to be charged again. If the charge stored in the capacitor array at the end of the previous conversion cycle can be recycled in the process to charge the MSB capacitor in the current conversion, the energy consumption of the charge scaling ADC can be reduced. This chapter presents circuit techniques to implement the above recycling techniques in charge scaling ADC circuits.

4.1 Proposed circuit implementation for Charge Recycling techniques

The schematic shown in Figure 22 represents an N-bit charge recycling SAR-ADC. The architecture is similar to the split capacitor array explained in [1]. In addition to charge recycling, the architecture works with the principle of capacitor splitting technique for switching down during a conversion. This section explains two charge recycling techniques: namely a) Recycling the charge stored only in the MSB array, b) Recycling the charge stored in entire array. The architecture remains unchanged for the above two cases with slight variations in the switch configuration.

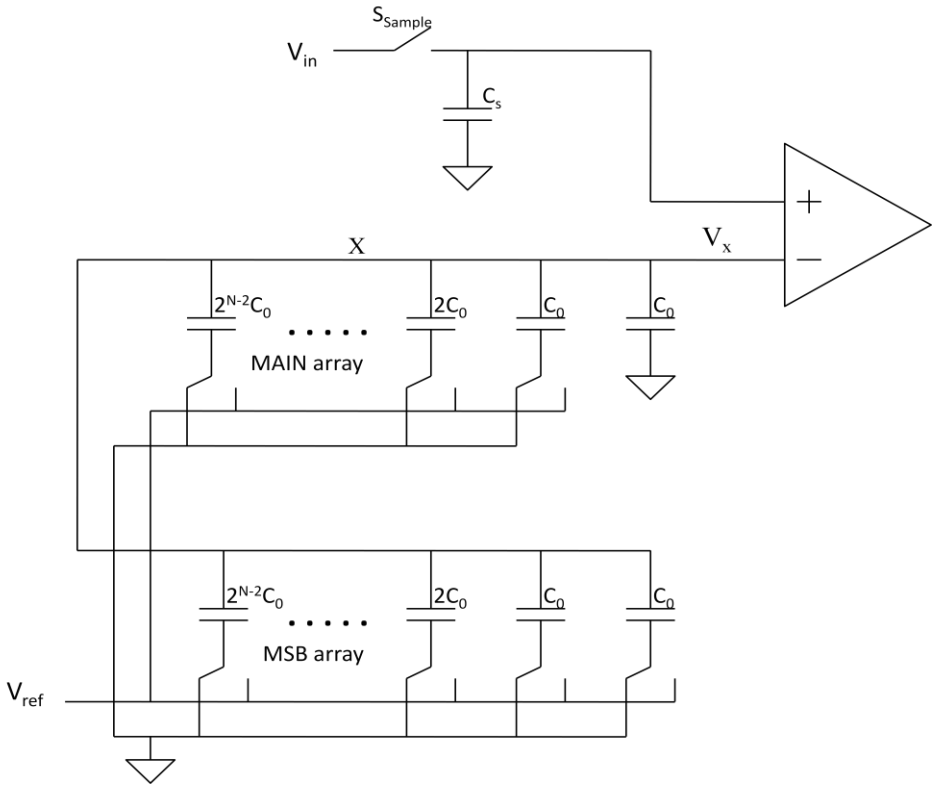


Figure 22: N-bit charge recycling SAR-ADC

4.1.1 Recycling the charge stored only in the MSB capacitor array

During sampling mode, switch S_{sample} is closed to sample the input signal (V_{in}) to sampling capacitor C_s. This capacitor holds the input voltage until the next conversion. At the same time node X is reset (or) grounded to zero. This resetting operation takes place only once during the entire ADC operation. In the redistribution mode, capacitors in the DAC array switch according to the capacitor splitting technique [1] to get the corresponding digital output for the analog input signal. Figure 23 shows how many capacitors are charged in a four bit example in the previous conversion for a 4-bit ADC.

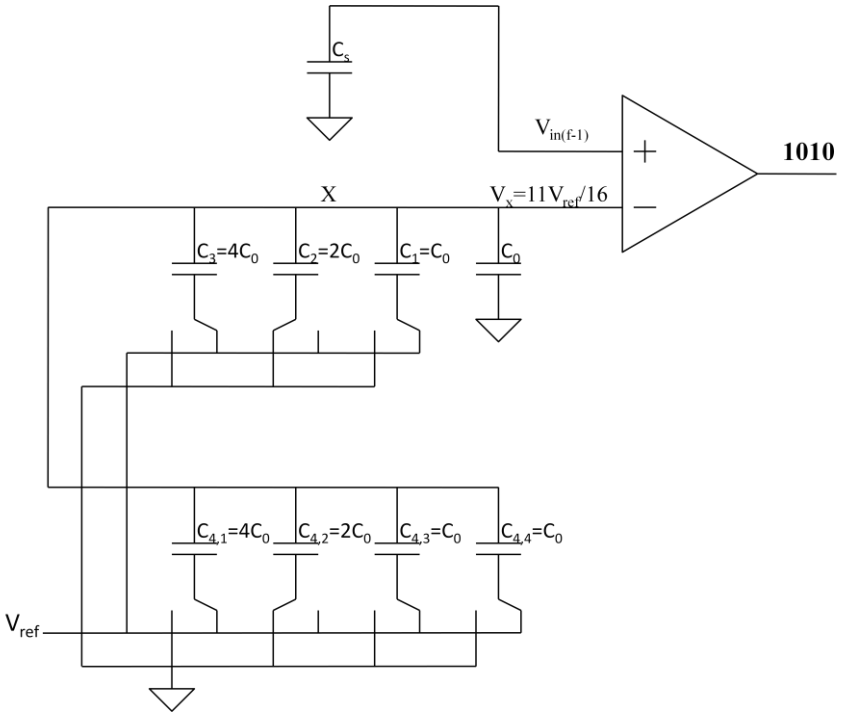


Figure 23: 4-bit ADC with capacitors charged in the previous conversion

We could observe that in Figure 23, a total of 11 capacitors are charged after converting an analog input whose corresponding digital code is 1010. Charge recycling can be performed by making a particular capacitor remain connected to V_{ref} during both current and previous conversion rather than re-charging for every new conversion. Out of these 11 charged capacitors, 6 charged capacitors are contributed by the MSB array. During the next conversion it is sufficient to charge $2C_0$ ($2C_0$ was grounded during the previous conversion) in the MSB array to determine the most significant bit. This operation is shown in Figure 24. The rest of the 5 charged capacitors in the main array in Figure 23 are grounded. Twice the number of switches is required to perform this MSB charge re-utilization when compared to the traditional switching scheme.

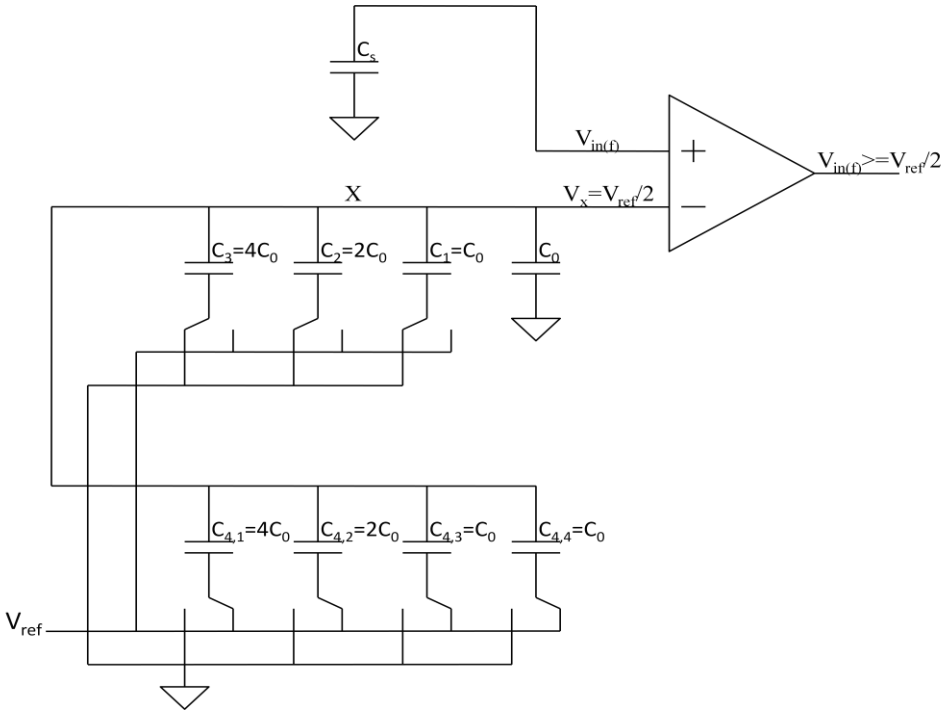


Figure 24: 4-bit ADC with charge recycling approach in the current conversion

4.1.2 Recycling charge stored in the entire capacitor array

This method almost has everything in common with respect to previous method, with only one difference of re-utilizing the charge stored in the entire array. For this recycling to happen effectively the circuit in Figure 23 is slightly modified by replacing all the capacitors in the charge recycling array with equivalent sum of unit capacitors as shown in Figure 25. For example capacitor C_3 ($4C_0$) is replaced by a parallel connection of four unit capacitors (C_0). Figure 25 shows how many capacitors are charged to V_{ref} in the conversion that produces output code 1010

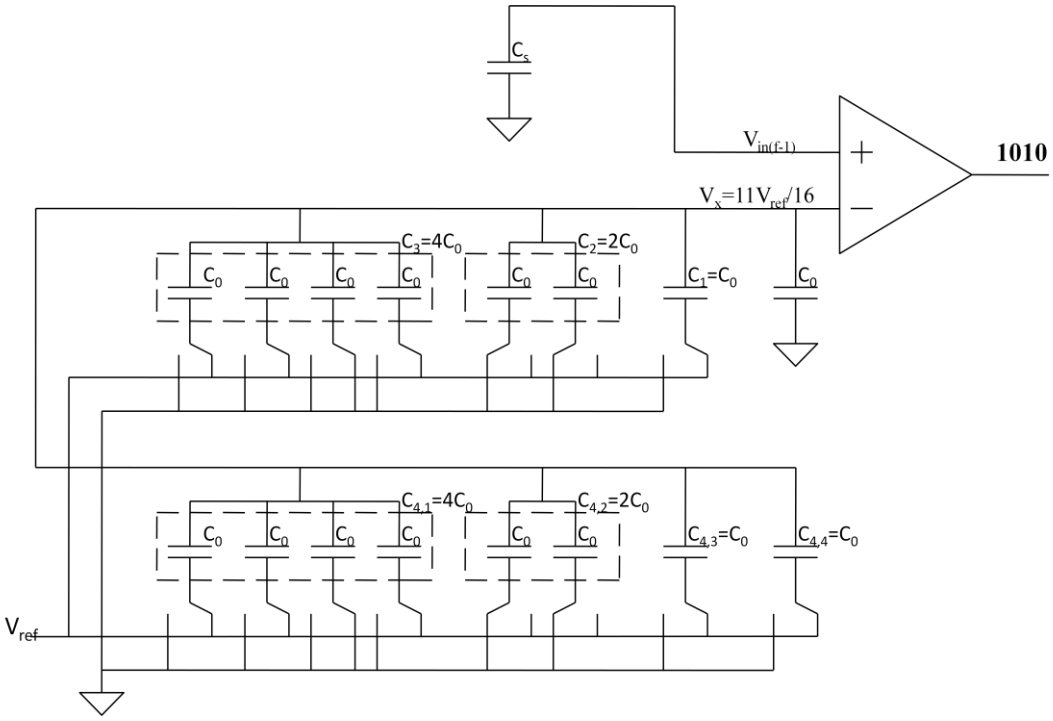


Figure 25: 4-bit ADC with entire capacitor array charge recycling in the previous conversion

From Figure 25, 8 charged capacitors can be recycled (or) used to determine MSB in the next conversion. Thus charging $2C_0$ required in the previous program can be avoided by making two of the unit sized capacitors from capacitor C_3 remain connected to V_{ref} during the next conversion (Figure 26). A comparable amount of energy can be saved by re-utilizing the charge stored in the entire capacitor array.

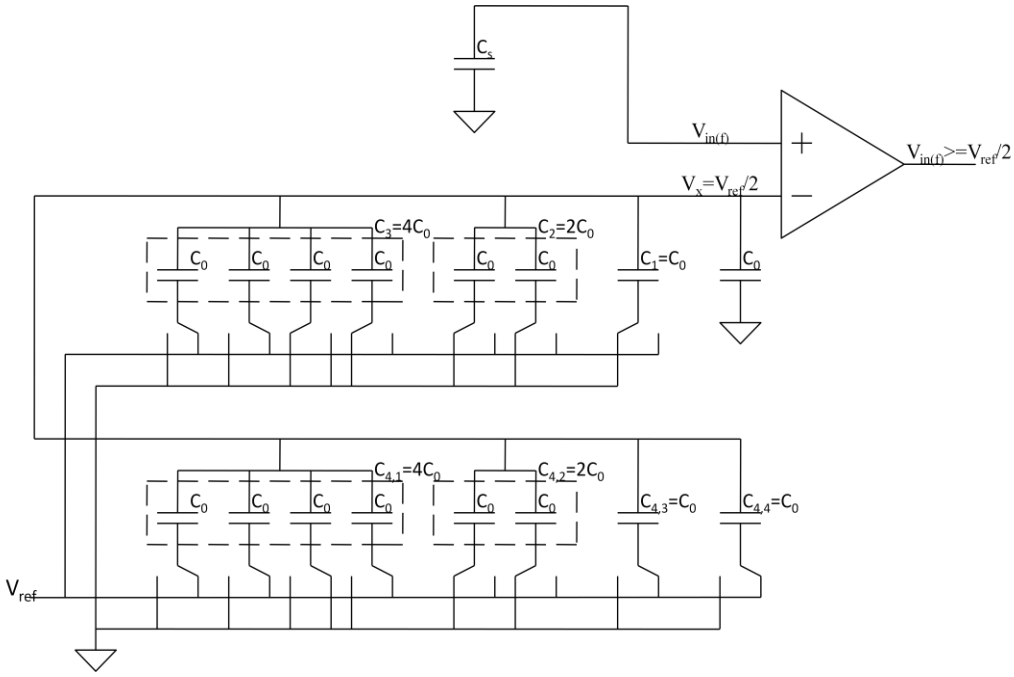


Figure 26: 4-bit ADC with entire capacitor array charge recycling in the current conversion

This method becomes more flexible and energy saving, when all the capacitors in the charge recycling array are represented by unit capacitors (C_0). Table 2 shows how the switching energy for 10 bit ADC is varied if the size of unit capacitor used to represent charge recycling array is varied. Here C_0 is taken as 1pF along with voltage reference level of 12.V. Energy saving decreases as the size of the unit capacitor increases. From Figure 27, we can observe that $2C_0$ is used as unit capacitor to represent the charge recycling array. Number of switches is directly proportional to number of unit capacitors employed in the array.

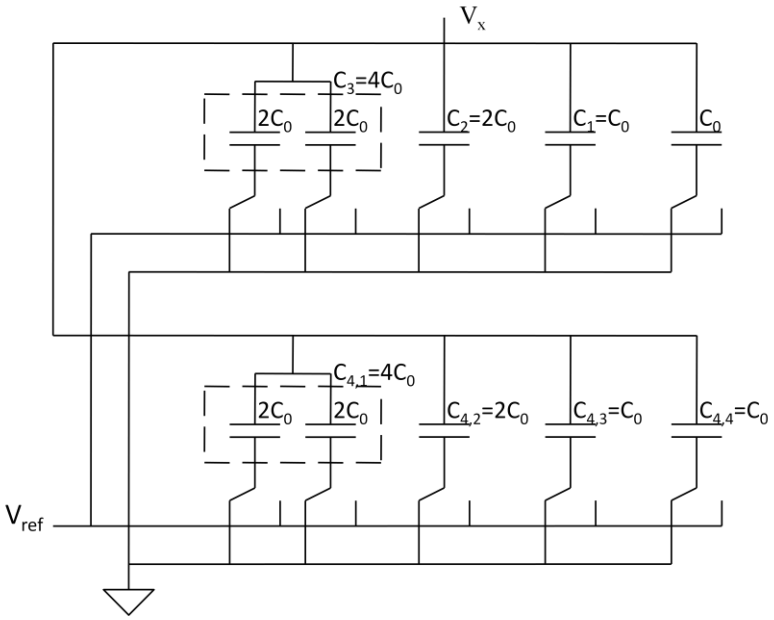


Figure 27: 4-bit ADC with entire capacitor array charge recycling having $2C_0$ as unit capacitor

Table 2: Number of switches versus average energy for charge recycling approach

Unit capacitor	C_0	$2C_0$	$4C_0$	$8C_0$	$16C_0$	$32C_0$	$64C_0$	$128C_0$	$256C_0$	$512C_0$
Avg Energy (pJ)	337.5	337.9	338.2	339.0	340.4	343.3	349.0	360.6	383.6	429.7
No. of switches	1023	512	257	130	67	36	21	14	11	10

4.2 Analysis of energy consumption

The switching energy calculation is similar to the capacitor splitting technique [1], with only little difference in calculating the energy for the most significant bit. Thus

energy required to charge the capacitors in MSB array in the current conversion (considering only the charge in the MSB array) is given by the following equation

$$E_{0\to1} = -V_{ref} * (2^{n-1}C_0 - b) * \{ (V_{x[1]} - V_{ref}) - V_{x[0]} \}$$

Where b - The number of capacitors charged in the previous operation in MSB array

V_{ref} – Voltage reference

n – resolution of the converter

C_0 – unit capacitor

$E_{0->1}$ – Energy required for charging the MSB array in the current conversion

Vx – node votlages

To generate the MSB, a capacitive DAC array needs to have $2^{(N-1)}$ capacitors (N is the resolution of the converter) to be charged in order to provide $V_{ref}/2$. The energy required to determine MSB by considering the charge stored in the entire capacitor array is given by the following condition.

$\boldsymbol{if}\ (\boldsymbol{b \geq 2^{n-1}C_0})$

$E_{0\to1} = 0$

$\boldsymbol{else}$

$E_{0\to1} = -V_{ref} * (2^{n-1}C_0 - b) * \{ (V_{x[1]} - V_{ref}) - V_{x[0]} \}$

$\boldsymbol{end}$

Where b = number of capacitors charged in the entire array in the previous operation

n = Resolution of the converter

If the number of charged capacitors in the previous conversion is greater or equal to $2^{(N-1)}C_0$, the energy required to determine MSB would be zero. Additional capacitors which are charged in the previous conversion are wasted or not utilized.

4.3 Simulation Results

Matlab codes are developed to estimate the energy consumption of the proposed charge recycling approach to a 10 bit ADC. In matlab simulation, an input ramp signal is fed to the ADC. The unit capacitance of the ADC is 1pF and the voltage reference level is 1.2V. Figure 28 shows the switching energy results of the charge recycling approach along with the traditional switching scheme and the approach in [1].

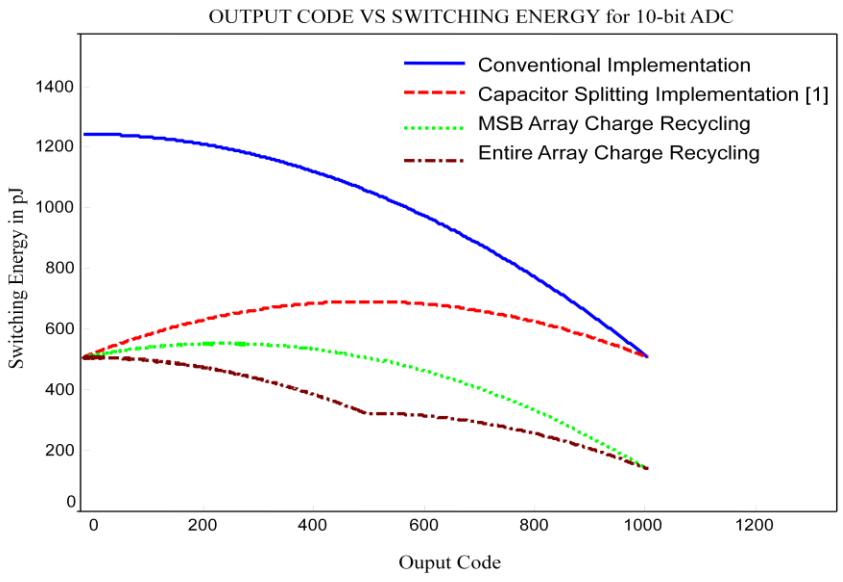


Figure 28: Switching energy for charge recycling approach with step signal input

It is clear from Figure 28 that as the input signal increases, the switching energy reduces. This is because the increase of the input signal, results in the number of charged capacitors increasing during each conversion. Table 3 tabulates the average energy consumed by different ADC implementations for a ramp input signal.

Table 3: Average energy for various switching methods with step signal for 10-bit ADC

ADC Implementation	Average Switching Energy (pJ)
Traditional Conversion	981.60
Capacitor Splitting [1]	613.68
MSB array charge recycling	429.36
Entire array charge recycling	337.56

Table 4 shows the average energy consumption by different ADC implemetations with sin wave input. Sampling frequency is taken to be twice of the natural frequency of the ADC. There is no much difference in energy consumption with step and sin wave signal.

Table 4: Average energy for various switching methods with sine wave for 10-bit ADC

ADC Implementation	Average Switching Energy (pJ)
Traditional Conversion	950.91
Capacitor Splitting [1]	582.99
MSB array charge recycling	398.48
Entire array charge recycling	332.02

Figure 29 shows the plot of average energy consumption of charge recycling over various sampling frequency of the ADC. It is evident from the plot that by varying the sampling frequency of the sine wave doest change the average energy consumption of the proposed charge recycling approach. So the charge recycling approach is not significantly affected by the different sampling rates. Figure 30 shows the variation of the average energy consumption with various amplitudes of the sine wave.

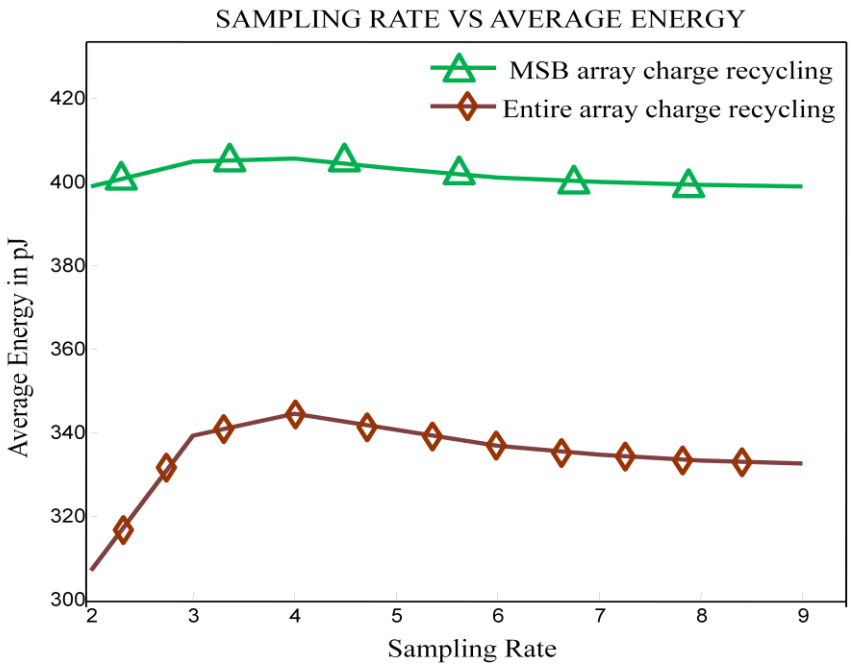


Figure 29: Plot of average energy over sampling rate for charge recycling approach

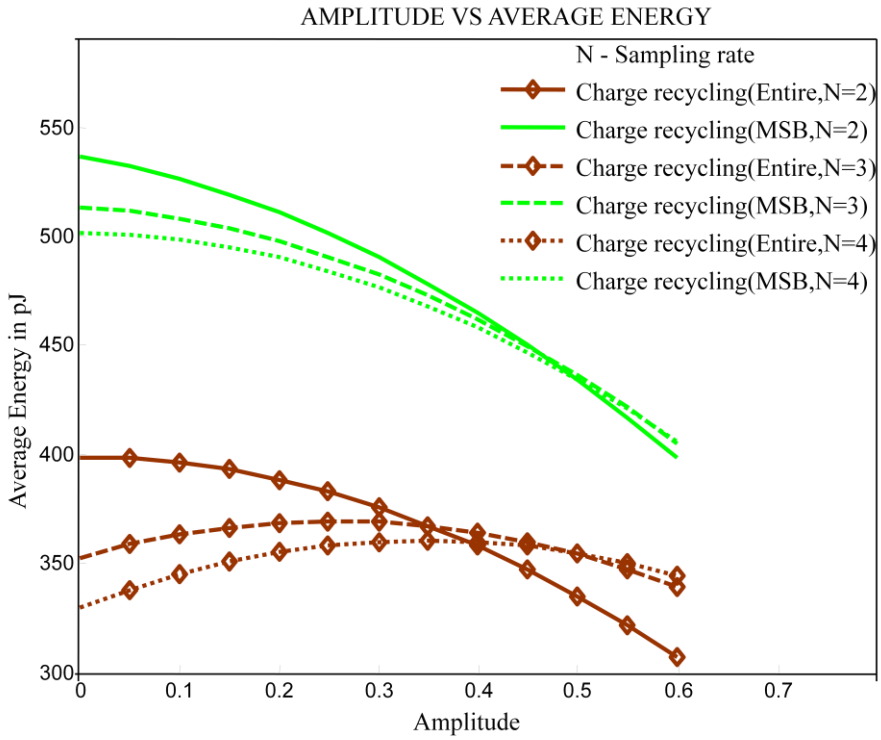


Figure 30: Plot of average energy versus amplitude for different sampling rates for charge recycling approach

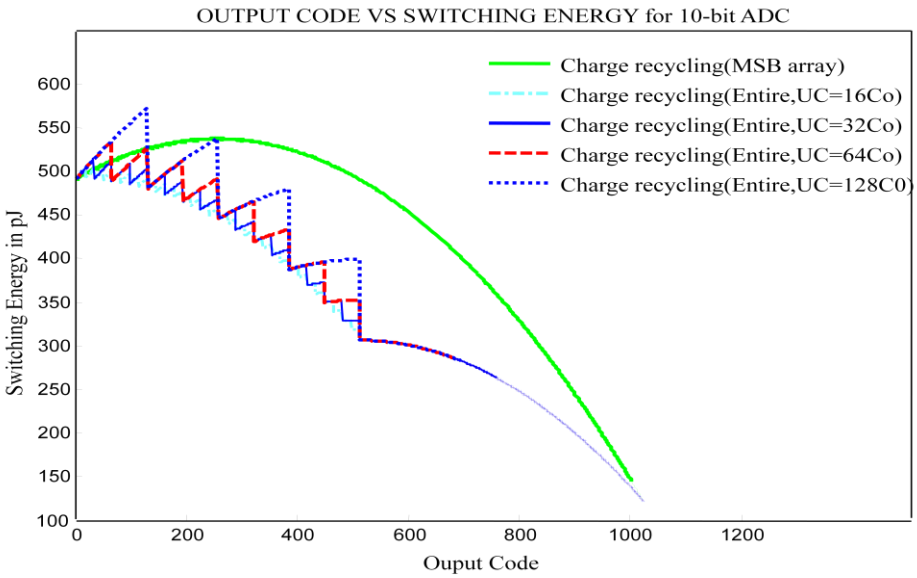


Figure 31: Variation of Switching Energy for various unit capacitor

Figure 31 shows how switching energy of the charge recycling approach varies when the charge recycling array is designed with different unit capacitors. The charge recycling approach becomes effective when we represent the charge recycling array with smallest capacitor (C_0, least weigh capacitor in the array). The spike in the recycling entire array approach shown is shown in Figure 31 is due to the utilization of different unit capacitors. With the help of Table 4, a graph (Figure 32) is plotted to show the percentage of energy that can be saved with number of switches employed in the DAC array. Thus we can conclude that by utilizing the concept of charge recycling the switching energy can be reduced considerably at the cost of increased number of switches in the DAC array.

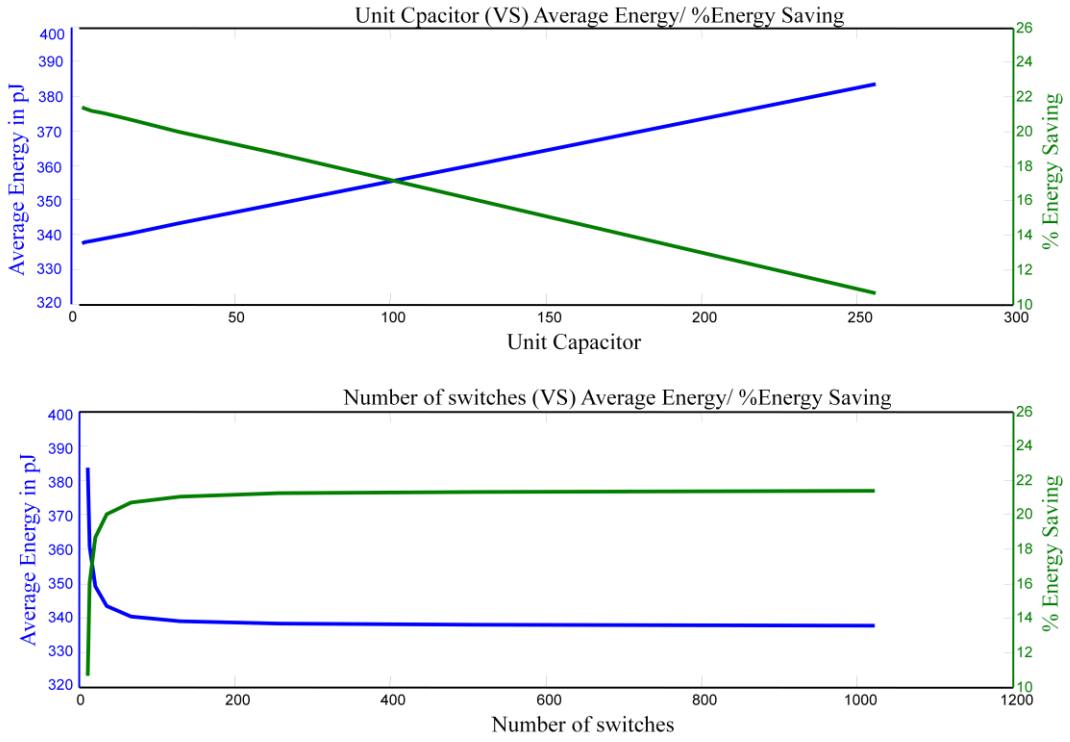


Figure 32: Percentage energy saving versus number of switches utilized in the DAC array

4.4 Discussion

Two charge recycling techniques are presented. These techniques can be used in any CR-SAR-ADC circuits. The energy saved by the MSB capacitor and entire capacitor array charge re-utilization is about 56.25% and 65% of the total energy consumption compared to traditional method. The energy saving is maximum when the entire capacitor array is replaced with equivalent sum of LSB capacitors. Having more equivalent sum of capacitors in the array provides more flexibility for re-utilizing the charge stored in the array for the next conversion. The energy saving provided by these techniques are obtained at the cost of increased number of switches, SAR registers and complex digital logic. The digital circuit required for switching the capacitors in the array will be large when compared to traditional switching. Even though the area occupied by the switches, registers and digital logic will increase compared to the traditional ADC, this penalty is minimal compared to area occupied by the DAC array.

CHAPTER 5

LOW-POWER SAR-ADC DESIGN USING TWO-CAPACITOR ARRAYS

Energy consumed in CS-SAR-ADC depends mainly on capacitance switched and reference voltage employed. Reducing the capacitance needed for switching can considerably minimize the power consumption, but this reduction would affect the resolution of the converter. Methods discussed in [1, 3] utilize entire capacitor array of size 2^NC (N is the resolution of the converter) to determine the bits. As N increases, the size of the capacitor array increases, which, increases the energy required to determine the bits. The method proposed in this chapter utilizes a very small sized capacitor array to determine the MSBs (coarse-level search) and a large sized capacitor array to determine the LSBs (fine-level search), respectively. The proposed method is similar to the approach in [2]. But several improvements are proposed in this design.

5.1 Proposed circuit implementation with Two-Capacitor Arrays

The implementation of two-capacitor array technique reduces the capacitance required for switching, without affecting the converters resolution. Figure 33 shows an N – bit two-capacitor array SAR-ADC which is a further advancement of the approach in [2]. The above converter has the advantage of low energy, input swinging rail to rail, requiring half the reference voltage for the DAC operation. Two input configurations of the two-capacitor array approach have been discussed similar to [2] namely a) two-

capacitor arrays with negative voltage reference b) two-capacitor arrays with voltage-boosting technique.

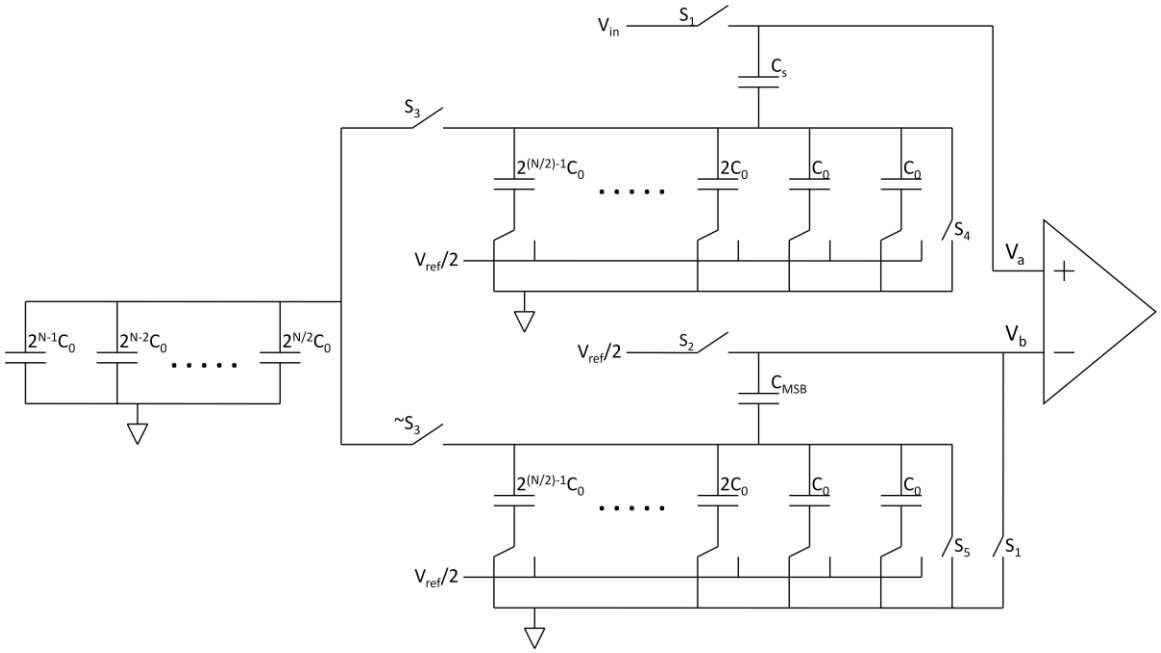


Figure 33: N-bit capacitive SAR-ADC with two-capacitor arrays of unequal size

5.1.1 Two-capacitor array approach with negative voltage reference

A 4 bit ADC example is shown in Figure 34 to explain the operation of the proposed two-capacitor array SAR-ADC. Initially all the capacitors are grounded before the operation starts. Similar to the traditional SAR-ADC operation, steps involved in the conversion are Sampling and Redistribution mode.

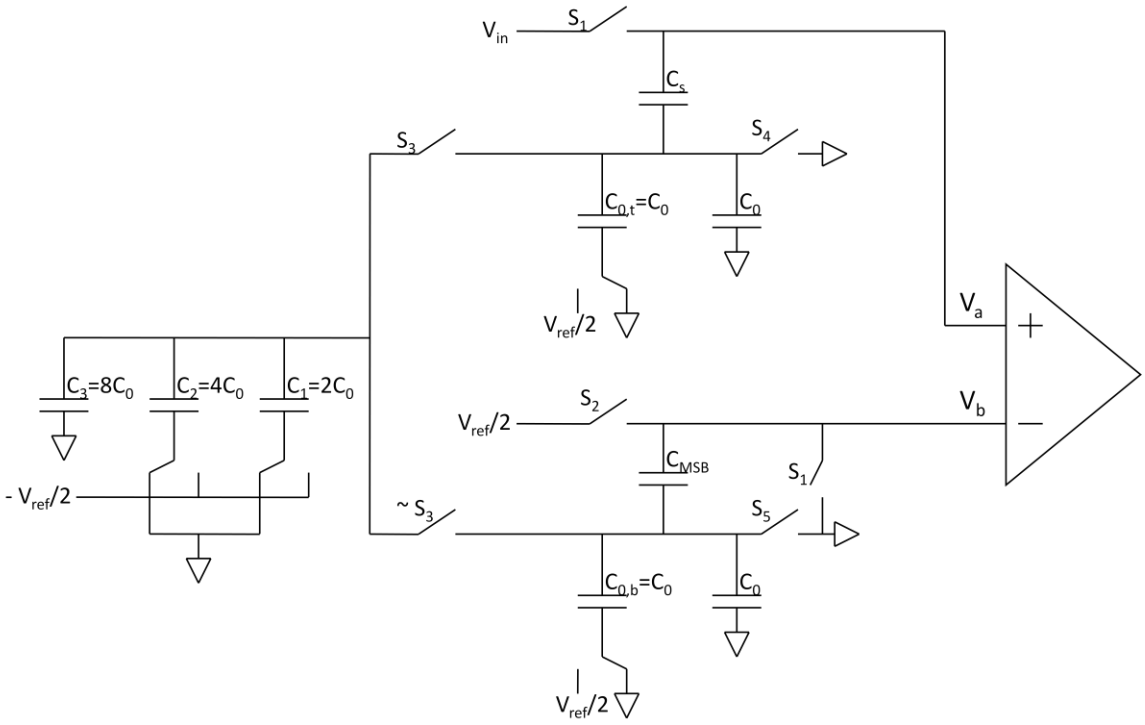
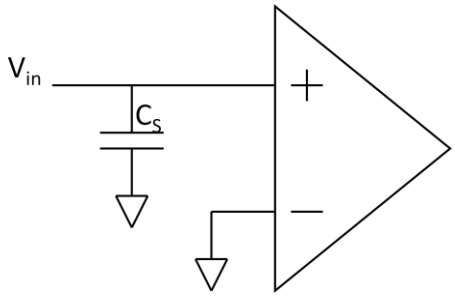


Figure 34: 4-bit example of two-capacitor array with negative voltage reference

Sampling mode: During this mode, switches with label S_1, S_4 are closed and input voltage V_{in} is sampled to the sampling capacitor (C_s). V_b is reset to zero by S_1. The equivalent circuit after switching is shown in Figure 35. From this configuration, energy required during sampling mode to charge the sampling capacitor is minimized drastically, as the input voltage has to charge only a small capacitor.



Figur 35: Sampling operation in two-capacitor array approach

Redistribution mode: This mode starts by opening the switches labeled S_1, S_4 and closing the switches S_2 and S_5. $V_{ref}/2$ is sampled to C_{MSB} to determine the MSB (Figure 36). Since only a small capacitor is used to determine MSB, the energy required to determine the MSB is drastically reduced when compared to the traditional and many other proposed SAR-ADCs.

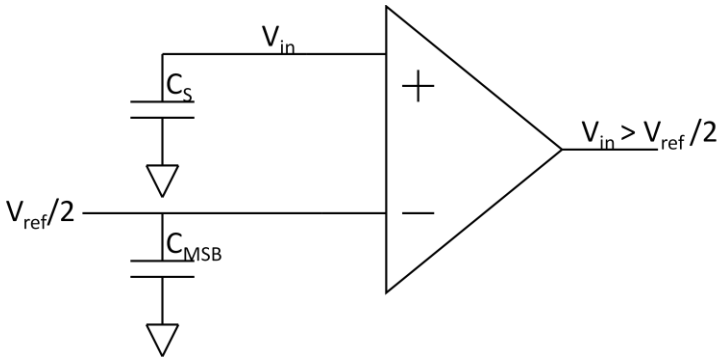


Figure 36: Determination of MSB in two-capacitor array approach

In any conversion, both top and bottom arrays are utilized for both fine-level and coarse-level search. The above operation would determine MSB. If the produced MSB is 1, then the bottom array is used to determine the more significant bits and the less significant bits

are determined using the top array. The capacitor ($C_{0,b}$) in the bottom array (Figure 37) is switched to $V_{ref}/2$, thus pushing the node voltage V_b to $3V_{ref}/4$. We can consider the scenario as two batteries connected in series and their voltages adding up. In the similar fashion, the rest of the capacitors in the bottom array (for N-bit case) would charge/discharge until the most significant bits are produced.

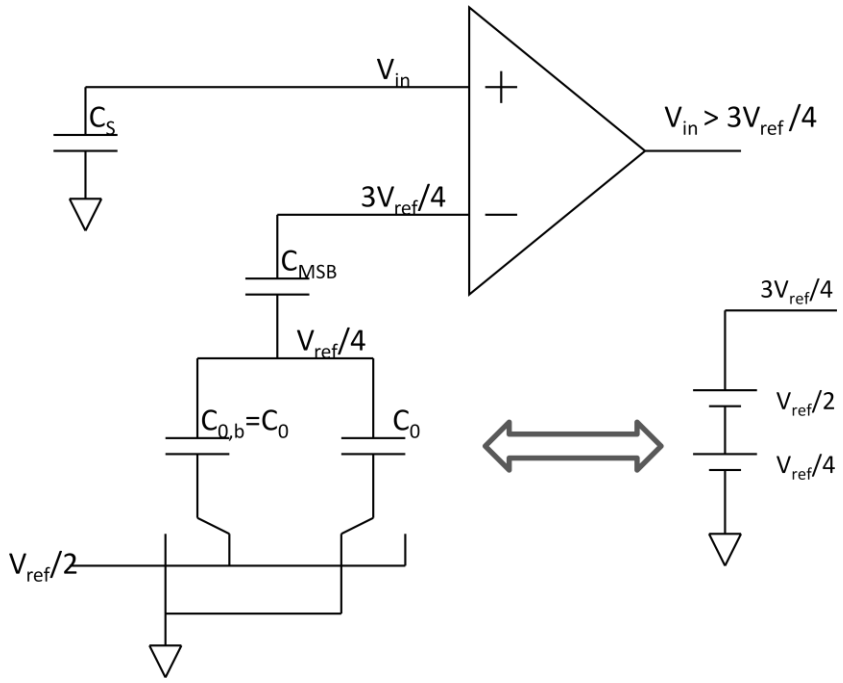


Figure 37: Determination of most significant bits in two-capacitor array approach

After the MSBs are determined, the top array is used to find the LSBs. To provide the necessary voltage swing, the top capacitor array operates with a total size of 2^NC_0 similar to the conventional one, which is now capable of generating the finest resolution of $V_{ref}/2^N$. The size 2^NC_0 is obtained by closing S_3 to the top capacitor array. Since the top capacitor array has to generate voltages from $V_{ref}/2^{N/2}$ to $V_{ref}/2^N$, N/2 largest capacitors

are always connected to ground throughout a conversion. Since V_a is always greater than the V_b, a negative reference voltage is used to bring the top node voltage down. This is explained graphically in Figure 11 (b). The capacitors in the top array charge/discharge to determine the LSBs (Figure 38). If the determined MSB was zero, MSBs are determined by top array and LSBs are determined by the bottom array.

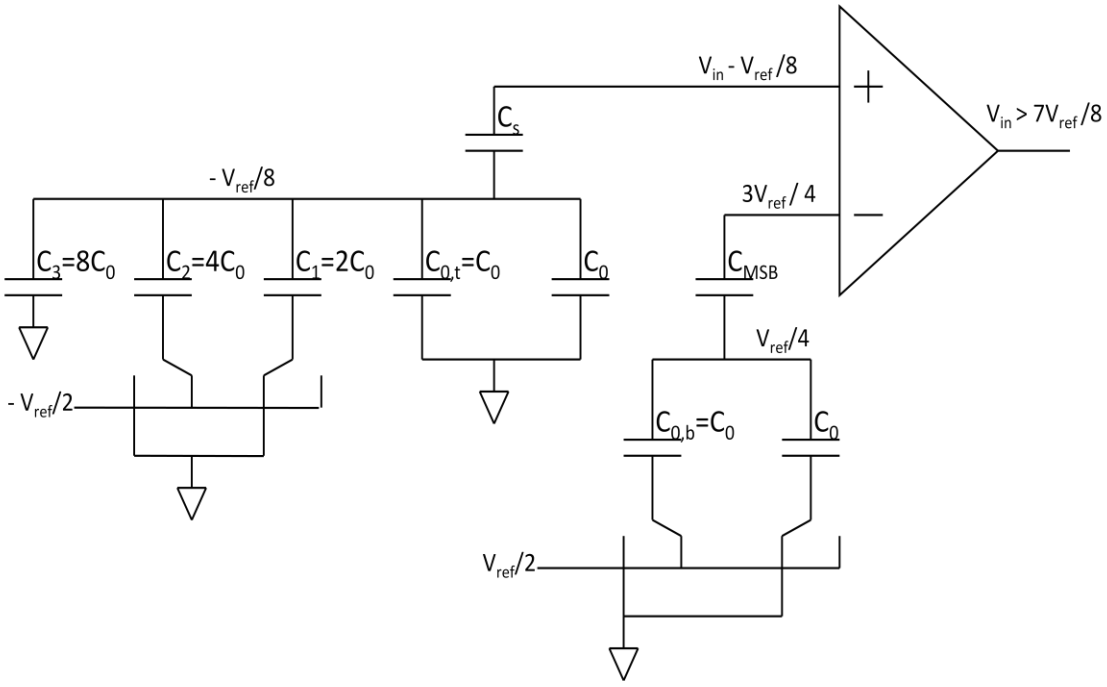


Figure 38: Determination of least significant bits in two-capacitor array approach

5.1.2 Two-capacitor array approach with voltage boosting technique

Instead of using a negative voltage reference to reduce V_a, the technique of voltage boosting is used as discussed in [2]. The operation of this technique is similar to what is discussed in section 5.1.1 with modifications of boosting the node voltage at the end of

course-level search and using a positive reference voltage in the fine-level search. A four bit example is shown in Figure 39 to explain the voltage boosting technique with two-capacitor array approach. Assuming that MSB is one, makes the bottom and top array to be used in coarse-level and fine-level search respectively. After the coarse-level search is done, V_b is further increased by ΔV ($V_{ref}/2^{n/2}$), by connecting capacitor $C_{b,b}$ in the bottom array to $V_{ref}/2$. In this example, the bottom node voltage is boosted up by $V_{ref}/2.2^2$. This boosting technique guarantees that V_a is always smaller than V_b (Figure 12 (b)) and thus avoids using negative reference voltage (Figure 40). After the node voltage is boosted, the LSBs are found using the top array.

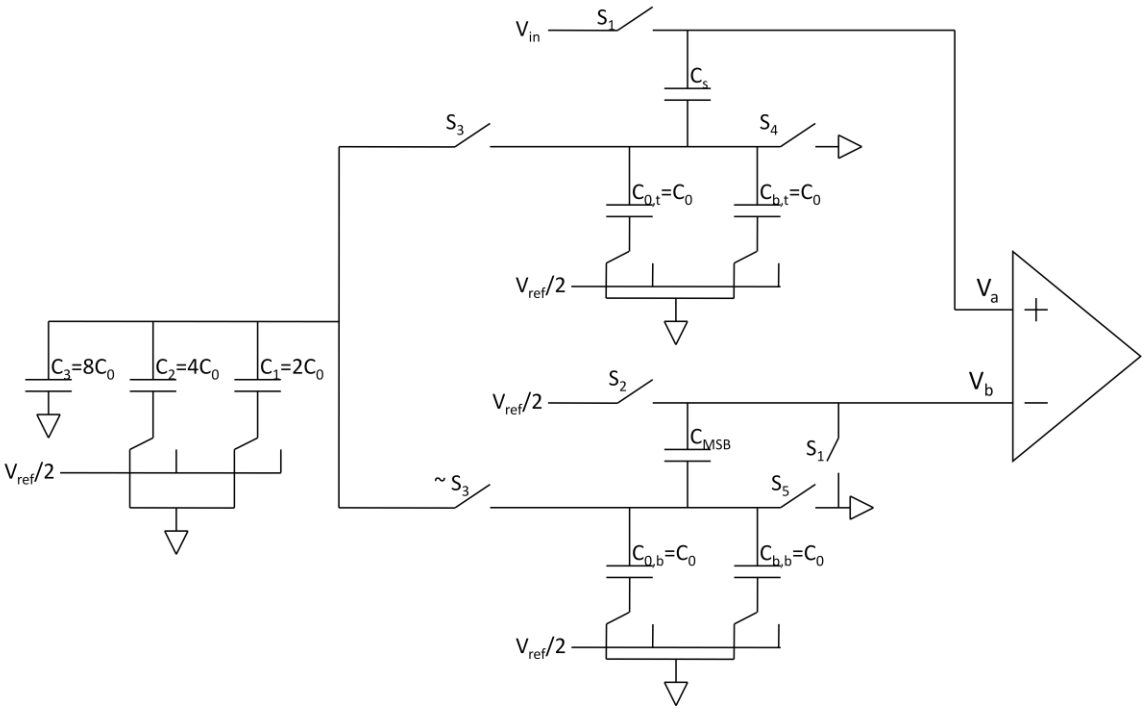


Figure 39: 4-bit example of two-capacitor array with voltage-boosting technique

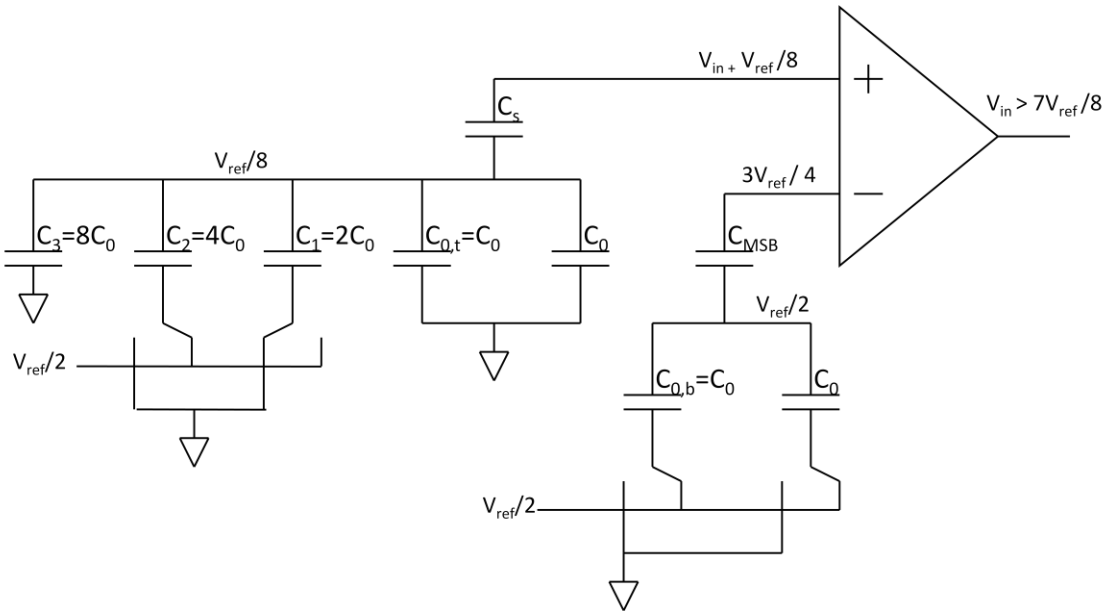


Figure 40: Determination of least significant bits with voltage-boosting

5.2 Switching energy analysis

Rather than having a large capacitor array to sample the input signal as in traditional switching, the input signal is sampled to a dedicated sampling capacitor which can be a small sized capacitor. The energy consumed is given by

$$E_0 = C_s V_{in}^2$$

Here the energy is given as product of capacitance and square of the voltage reference. The energy required to determine MSB is given by

$$E_1 = \frac{C_{MSB} V_{ref}^2}{4}$$

The energy required for boosting the node voltage is also small, as C_b is the smallest capacitor in the array. Table 5 shows the energy consumption in each conversion cycles

of different ADCs. From the table the energy required for determining MSB and the 6th bit has drastically reduced when compared with other two methods. The energy consumed by the rest of the bits is reduced by half when compared with [2]. The energy saving is due to reduction in both capacitance required for switching and reference voltage. Similar to section 2.2, energy equations can be derived to obtain the energy consumption of the proposed two-capacitor array approach for rest of the bits.

Table 5 Tabulation of switching energy of two-capacitor array in comparison with other methods for 10-bit ADC

Bit	V_{in}	1	2	3	4	5	6	7	8	9	10
Traditional switching	$1024CV^2_{in}$	$512CV^2_{ref}$	$256CV^2_{ref}$	$128CV^2_{ref}$	$64CV^2_{ref}$	$32CV^2_{ref}$	$16CV^2_{ref}$	$8CV^2_{ref}$	$4CV^2_{ref}$	$2CV^2_{ref}$	CV^2_{ref}
Two step switching[2]	$C_sV^2_{in}$	$16CV^2_{ref}$	$8CV^2_{ref}$	$4CV^2_{ref}$	$2CV^2_{ref}$	CV^2_{ref}	$16CV^2_{ref}$	$8CV^2_{ref}$	$4CV^2_{ref}$	$2CV^2_{ref}$	CV^2_{ref}
Proposed switching	$C_sV^2_{in}$	$CV^2_{ref}/4$	$4CV^2_{ref}$	$2CV^2_{ref}$	CV^2_{ref}	$CV^2_{ref}/2$	$CV^2_{ref}/4$	$4CV^2_{ref}$	$2CV^2_{ref}$	CV^2_{ref}	$CV^2_{ref}/2$

5.3 Simulation Results

Matlab codes are used to estimate the energy consumption of the proposed two-capacitor array approach to a 10 bit ADC. In matlab simulation, an input ramp signal is fed to the ADC. The unit capacitance of the ADC is 1pF and the voltage reference level is 1.2V. Figure 41 shows the switching energy results of the two-capacitor array approach along with the two step low energy switching scheme in [2]

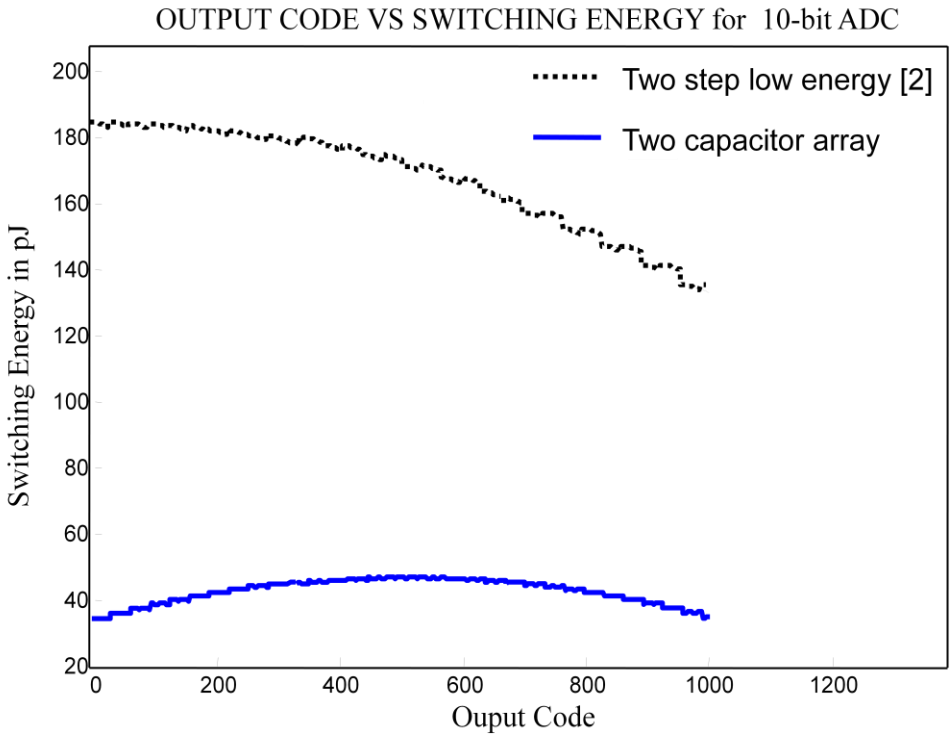


Figure 41: Switching Energy of proposed two-capacitor array SAR-ADC

The average energy results tabulated in Table 6 shows the reduced energy consumption of the proposed two-capacitor approach over approach in [2]. The proposed switching has 74.64% reduced energy consumption when compared to the approach in [2].

Table – 6: Average switching energy for different switching methods for 10-bit ADC

ADC Implementation	Average Switching Energy (pJ)
Two step low energy [2]	165.27
Two-capacitor array	41.90

This ADC has the advantages of achieving rail-to-rail signal swing with requiring half the reference voltage for DAC operation. This configuration has increased number of capacitors which is obvious from Table 7. This capacitor increase leads to increase in area, mismatch between capacitors, and degradation of performance of the converter.

Table 7: Number of switches required for two-capacitor array approach

Traditional switching	Two step low energy [2]	Two-capacitor array
2^N	$2^N + 2^{N/2} + 1$	$2^N + 2^{N/2} + 2$

5.4 Discussion

Configurations discussed in section 5.2 have two limitations which are discussed as below. CMOS Switches can be used to charge and discharge a capacitor effectively with minimal error. Whereas the same switches provide error when used to connect between the different nodes. For example switch S_3 in Figure 34 might not effectively combine the two-capacitor arrays even when the switch size is large. Switch induced error can be more pronounced in these cases and hence can have the ADC producing incorrect digital outputs. Another performance limitation is having the node voltage V_a swinging greater than V_{dd} when $V_{in} = V_{dd}$. To alleviate the above two limitations, configurations discussed in section 5.2 can be modified as shown in Figure 42. The operation of the modified circuit is briefly explained.

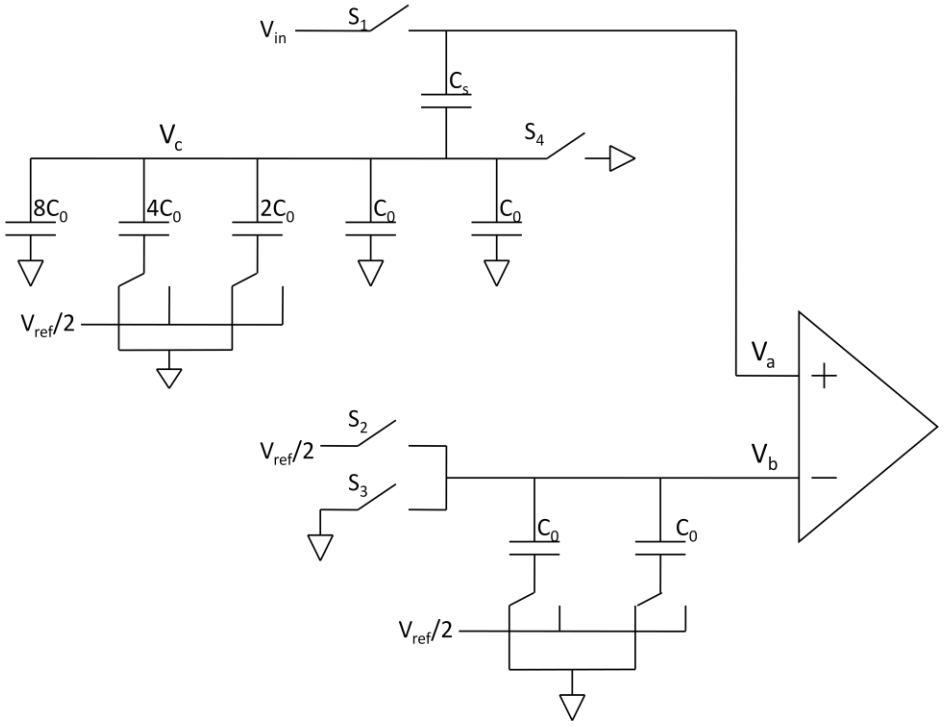


Figure 42: Architecture to avoid the problems in two-capacitor array approach

Similar to the approach in [2], the modified configuration has MSBs determined by the bottom array and LSBs determined by top array. As discussed in section 5.2, input voltage V_{in} is sampled to the sampling capacitor C_s through switches S_1 while S_4 and S_3 are closed. S4 remains closed until the start of fine-level search. To determine the MSB, $V_{ref}/2$ is sampled to the bottom capacitor array through S_2. The bottom array now charges/discharges to produce the MSBs. In order to eliminate the voltage swing problem, the technique of voltage boosting is neglected. Rather than boosting the node voltage V_b at the end of the coarse-level search, the capacitors which are used in the fine-level search are connected to $V_{ref}/2$. Finally the capacitors are selectively discharged/charged to

determine the LSBs. As we could see that C_{MSB}, switch S_3 and voltage boosting are neglected in the modified configuration.

CHAPTER 6

POWER REDUCTION TECHNIQUES BY DYNAMICALLY MINIMIZING SAR-ADC CONVERSION CYCLES

In the view of the fact that the most significant bit consumes the most energy during any conversion, it is better to reuse the previous MSB conversion results rather than finding the new values, if possible. With any two consecutive samples, MSBs rarely change and it's only the LSBs that vary in most cases. With the introduction of charge recycling concept in chapter 4, the charge stored in the capacitor array during previous conversion is re-utilized to determine the MSB in the next conversion. By extending the concept of charge recycling, the charge stored in the capacitive DAC array throughout previous conversion is re-utilized to determine the most significant bits in the current conversion rather than just determining the MSB. By this approach, energy and clock cycles could be considerably saved. This chapter deals with approaches which are further advancement of charge recycling approach. This chapter presents two modified algorithms based on approaches in [3].

6.1 Proposed design

The techniques proposed in [3] is useful one only when two successive samples are within the expected range (band size).

$$\left|V_{a,k-1} - V_{a,k}\right| < \delta$$

Where $V_{a,k-1}$ - Previous analog input signal

$V_{a,k}$ - Current analog input signal

δ – Maximum difference between two successive samples

If the two successive samples are not within the expected range (δ), more clock cycles and energy are required to convert an analog value. In this case, the approach in [3] is worse than the traditional conversion. The algorithms in [3] convert an analog input signal to binary data and check a condition to see whether the decoded value is within the boundary. If it is out of range, the conversion has to start from the beginning similar to the traditional conversion, thus consuming more energy and clock cycles. The proposed methods in this chapter are an effort to overcome the disadvantages discussed above.

6.1.1 Algorithm with boundary conditions checked at the beginning

As an alternative of checking the condition at the end, the proposed method has the boundary conditions checked at the beginning before the conversion starts. The assumption that two successive samples should be within expected range in the proposed approach is not as critical as that in the previous approach. If the input signal is a random varying one which means that difference between two successive samples could be out of range, this can be determined at the beginning and the conversion would start like a traditional one. Figure 43 shows the algorithm with the proposed changes. The energy

and clock cycles are saved at the cost of two analog comparisons from the comparator. The energy consumed for the two comparisons is minimal when compared to energy consumed by 2N conversions.

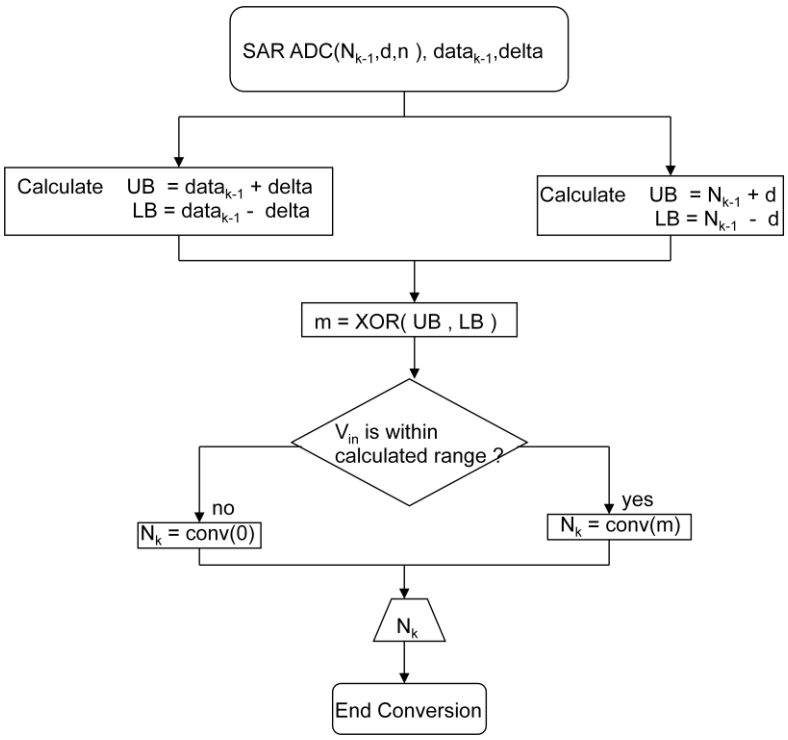


Figure 43: Flow chart of proposed control algorithm with boundaries checked at the beginning

A short explanation of the operation of the algorithm is provided below. Apart from the previously converted digital value N_{k-1}, digital equivalent of band size d and converter resolution, n, previous analog input and band size (delta) in analog terms are given as inputs to the algorithm. The algorithm calculates both digital and analog, upper and lower bounds. The m value is obtained as discussed in chapter 2 and it is inversely proportional to d. In the proposed approach delta (d) is an externally defined input similar to the

Range Checking Algorithm (RCA) used in [3]. In order to have the maximum energy saving the delta (d) should be large to accommodate all the signal variations. A condition is checked whether the current analog input sample is within the calculated bounds. If the condition is true, then n – m conversion steps are required to compute the LSBs, starting from the bit position n – m – 1. If the condition is false, then conversion starts from the beginning. The maximum number of clock cycles associated with this approach is N + 2 clock cycles.

6.1.2 Algorithm with single boundary condition checked at the beginning

The method discussed in section 6.1.1 checks two boundaries, i.e. Upper and lower boundary. But in real cases checking two boundaries would be unnecessary task. The method proposed in this section is to check single boundary depending upon the value of the input signal in the current conversion. This method produces the same result as the previous method. A flowchart is shown in Figure 44 with a minor modification of checking one boundary at the beginning.

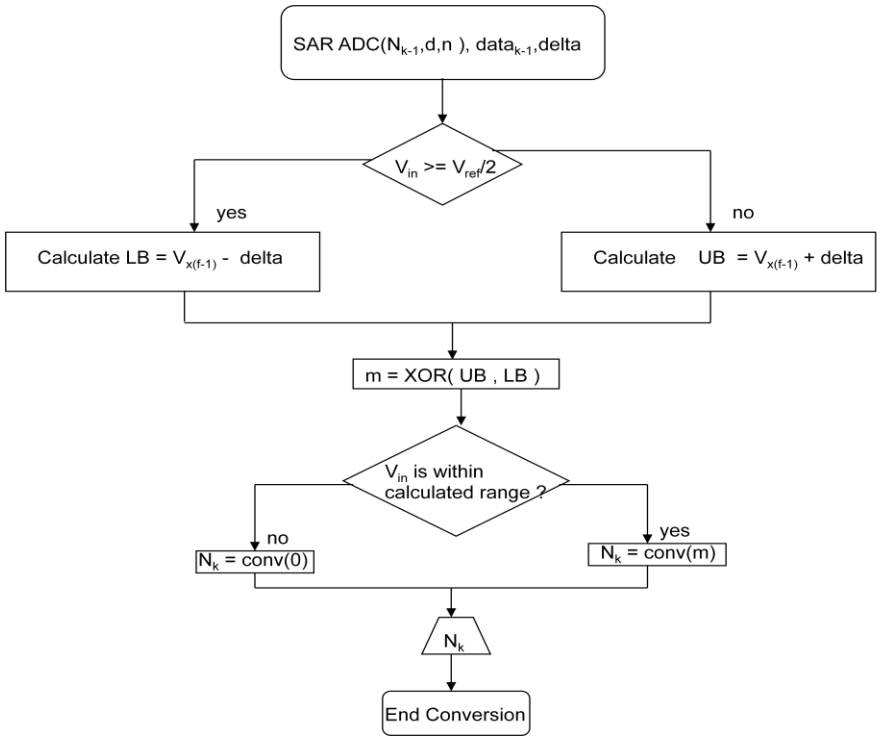


Figure 44: Flow chart of proposed control algorithm with single boundary condition checked at the beginning

A simple 5-bit circuit configuration shown in Figure 45 is used to explain the proposed method of single boundary check. Adding or subtracting delta to determine the boundaries can be done by charging or discharging a capacitor in an array. The circuit shown in Figure 45 is similar to charge recycling method presented in Chapter 4. After the boundary check, the converter performs conversions following the traditional scheme explained in chapter 2.

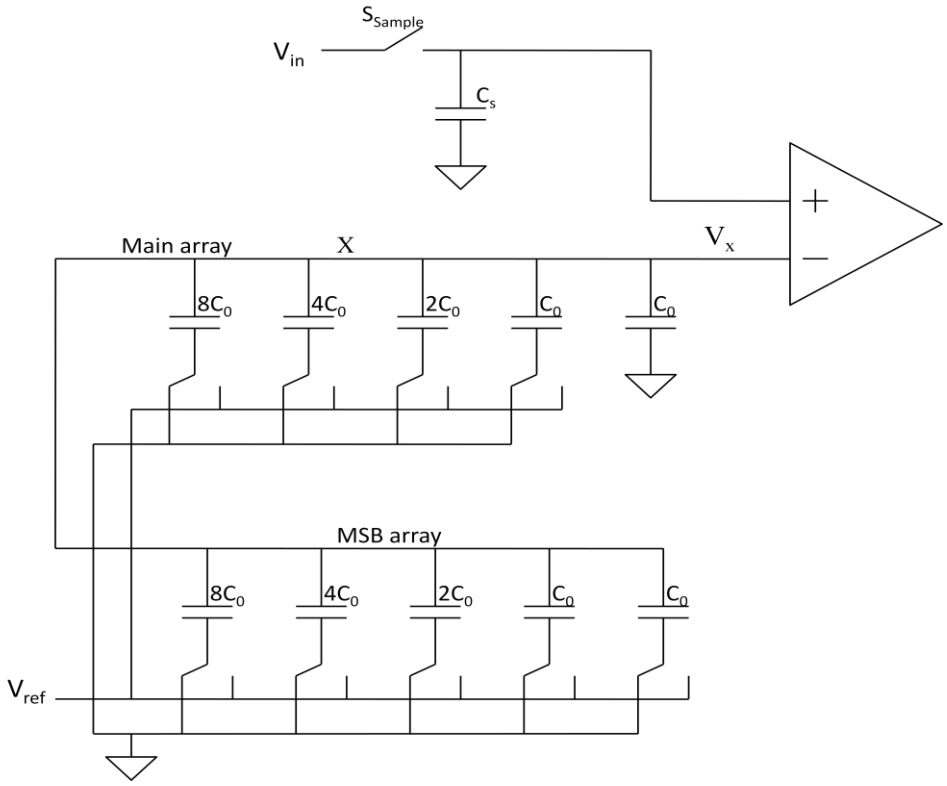


Figure-45: 5-bit split capacitive DAC based SAR-ADC

Figure 46 and 48 show how many capacitors are charged with respect to previous sample. Before computing the boundaries, a condition is checked to see whether the input signal is greater or lesser than the half of the reference voltage. If greater, lower bound is calculated by discharging the delta capacitor as shown in Figure 47. After that node voltage V_x is compared with the current input signal. If it is within the boundary, then the conversion takes place with previous bits restored. If it is out of boundary, then the conversion starts from the beginning. If V_{in} is out of boundary, the top capacitor array is discharged to ground, maintaining (without disturbing) the MSB array connected to V_{ref}. This would make the energy consumption required to determine MSB as zero for the new conversion.

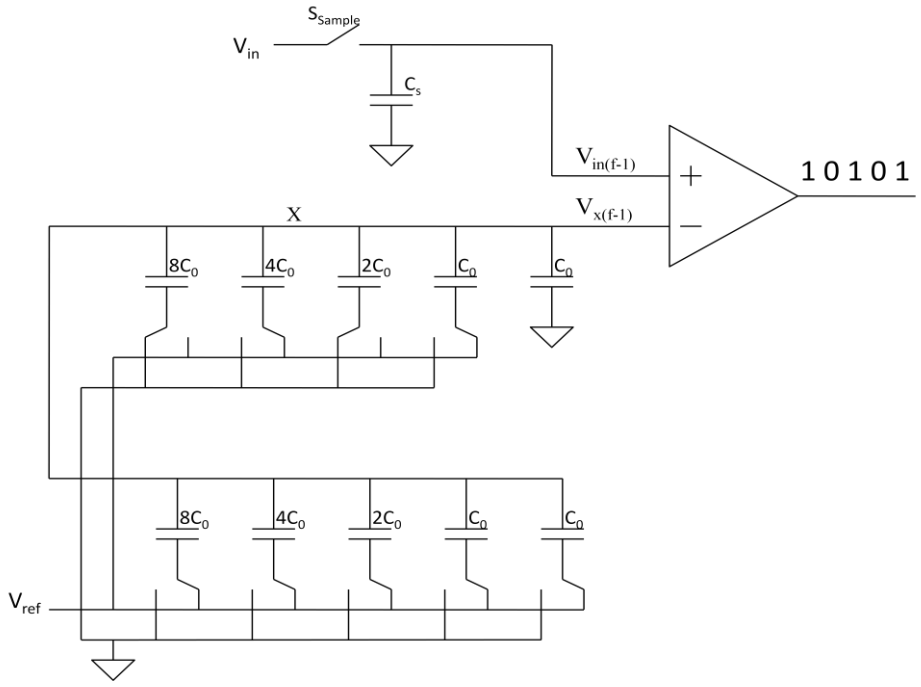


Figure 46: Conversion during previous operation when $V_{in} > V_{ref}/2$

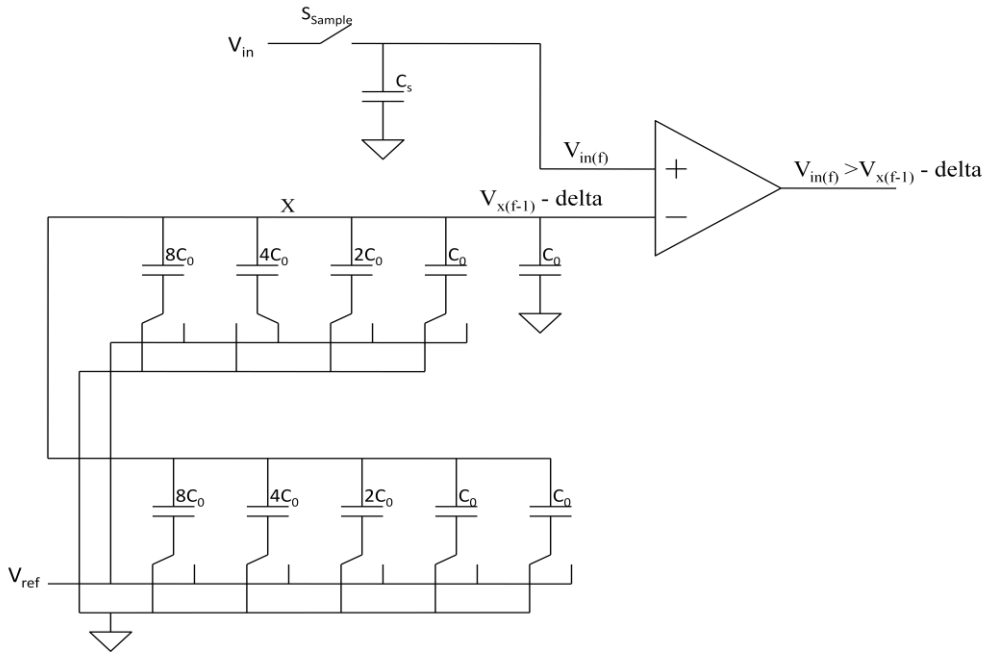


Figure 47: Operation of the circuit with single boundary checked during the current conversion

If the input signal is lesser than half of the reference voltage, upper boundary is calculated by charging the delta capacitor as shown in Figure 49. Then V_x is compared with the current input signal. If it is within the boundary, conversion takes place with previous bits restored. If it is out of boundary then, conversion starts from the beginning. If V_{in} is out of boundary, then the top capacitor array is charged to V_{ref}, maintaining (without disturbing) the MSB array connected to ground. This would make the energy consumption required to determine MSB as zero. With this approach we can interchange the MSB and main arrays in the conversion process.

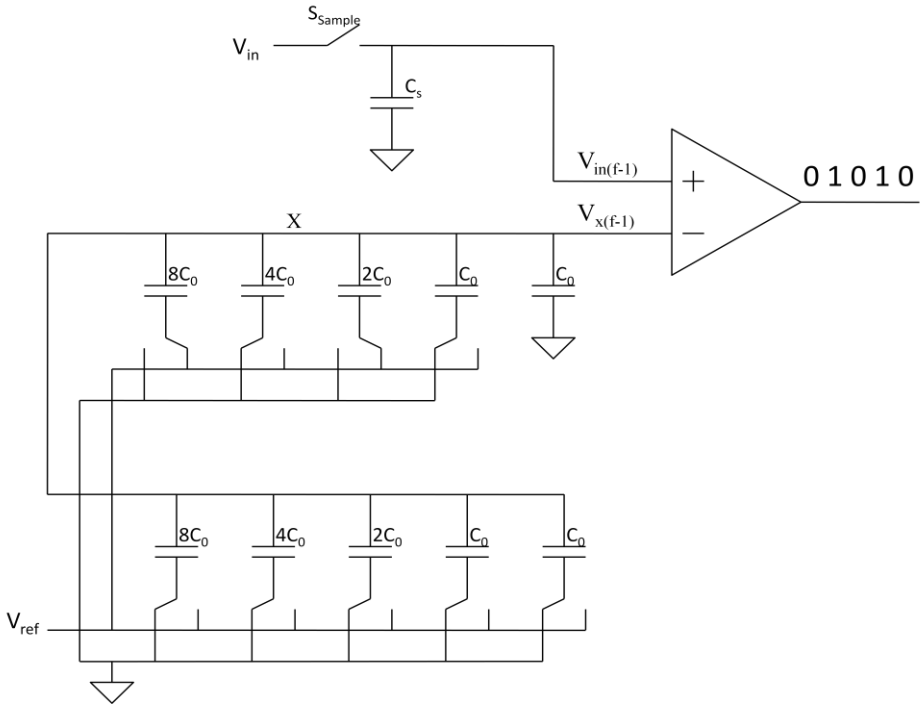


Figure 48: Conversion during previous operation when $V_{in} < V_{ref}/2$

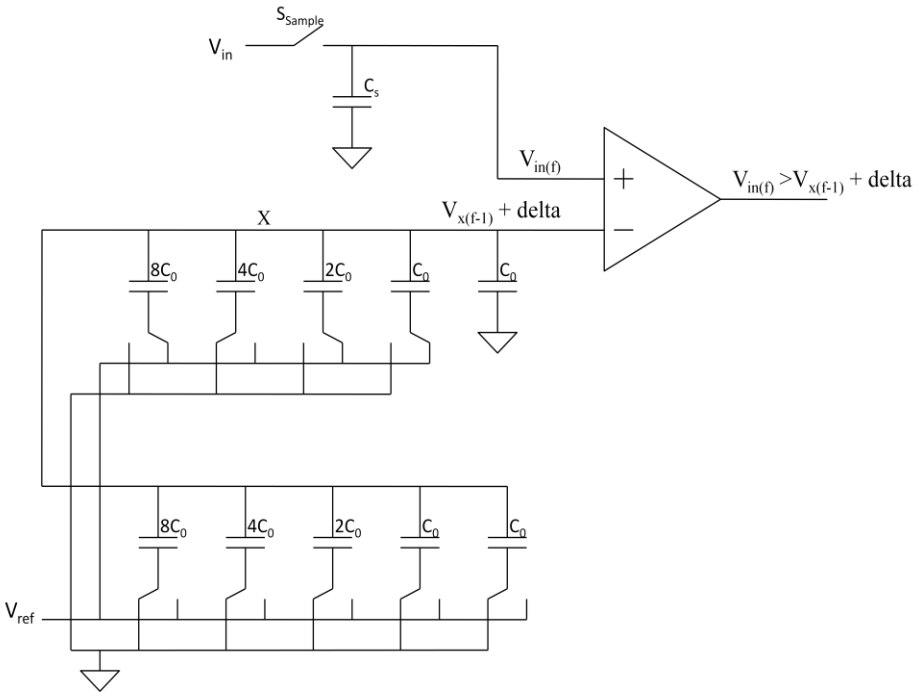


Figure 49: Circuit operation with single boundary checked during the current conversion

6.2 Simulation Results

Matlab models are developed to estimate the energy consumption of the proposed algorithms in a 10 bit ADC. Energy equations used in the code follow the equations explained in chapter 2. In matlab simulation, a sine wave input signal is used. Also, the unit capacitor of the ADCis 1pF and its reference voltage is 1.2V. Table 8 shows the switching energy results of the proposed method along with method proposed in [3]. It shows that for different sampling frequency maximum delta results in the same energy consumption for all the methods. When delta is within a certain range, the proposed methods can save energy. N+2 clock cycles are required for a single conversion when the input signal is not within the calculated boundaries.

Table-8: Switching energy of proposed methods along with methods in [3] for various delta values for 10 bit ADC

Delta		Method proposed in [3]	Algorithm with conditions checked at the beginning	Algorithm with only one boundary checked
N=5	128	507.31	507.31	535.66
	64	835.10	596.70	449.88
	32	985.79	754.53	512.24
N=7	32	228.98	228.98	235.76
	16	675.78	596.74	325.86
	8	855.50	767.36	462.22
N=10	4	50.33	50.33	54.04
	2	437.26	567.22	263.09
	1	690.63	773.12	444.96

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In this work, several low-power design techniques for charge scaling based SAR-ADCs are presented. Particularly, the proposed techniques focus on minimizing the power consumed by charging the capacitor arrays in SAR-ADCs. One of the approaches is to reduce the voltage swing of the capacitors during the ADC conversion cycles. By reducing the capacitor array swing from V_{ref} to $V_{ref}/2$, the power consumed by charging array is reduced by 75%. Note that this is achieved without sacrificing the dynamic range of the ADC circuits. The second approach reduces power consumption by recycling the charges that have stored in the capacitor arrays in the previous conversion cycle. We investigated the power saving efficiency with different unit capacitor value in the charge recycling capacitor array. Also an improved double-array SAR-ADC circuit is presented. Furthermore techniques that can dynamically minimize SAR-ADC conversion cycles are investigated in the thesis. In summary, the proposed low power circuit techniques can be easily implemented without significant area overhead. In addition, they can be combined with other low power circuit techniques in low power ADC circuit design.

7.2 Scope for future work

In this work, only MATLAB simulations are performed to compare power consumption of different circuits. As an extension of this work, the ADC circuits can be implemented at transistor circuit level and the power consumption can be compared by SPICE simulations. In addition, the design circuits can be fabricated and the proposed power saving techniques can be verified by measurement results from the fabricated circuits. The focus of this work is limited to techniques that reduce the power consumption of the capacitor arrays. Future efforts can be directed towards low power techniques for other components of the ADC circuits.

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