Secondary Voltage Unbalance Compensation for Three-Phase Four-Wire Islanded Microgrids

Tang, Fen; Zhou, Xiao; Meng, Lexuan; Guerrero, Josep M.; Vasquez, Juan Carlos

Published in:
Proceedings of the 11th International Multi-Conference on Systems, Signals and Devices, SSD 2014

DOI (link to publication from Publisher):
10.1109/SSD.2014.6808856

Publication date:
2014

Document Version
Early version, also known as pre-print

Secondary Voltage Unbalance Compensation for Three-Phase Four-Wire Islanded Microgrids

Fen Tang, Xiao Zhou
School of Electrical Engineering
Beijing Jiaotong University
Beijing, China
ftang_nego@126.com, 09117346@bjtu.edu.cn

Lexuan Meng, Josep M. Guerrero, Juan C. Vasquez
Dept. of Energy Technology
Aalborg University
Aalborg, Denmark
lme@et.aau.dk, joz@et.aau.dk, juq@et.aau.dk

***Abstract*—This paper proposes a secondary voltage unbalance control approach that compensate voltage unbalances in three-phase four-wire islanded microgrid systems. It is implemented in the secondary control level of the microgrid hierarchical control structure. By sending information through low-bandwidth communication links to the primary control level, the required unbalanced factors at sensitive buses are achieved. Also, negative and zero sequence equivalent circuits and unbalance compensation principle are derived. Finally, real-time hardware-in-the-loop results show the feasibility of the proposed approach for different islanded scenarios.**

***Keywords*—hierarchical control; microgrid; three-phase four-leg converter; unbalance compensation**

I. INTRODUCTION

Nowadays, the microgrid (MG) concept is attracting much attention due to advantages such as flexibility, reliability and high quality power. In IEEE Std 1547.4-2011, a microgrid is considered as a cluster of distributed resources (DRs), i.e. distributed generation (DG), distributed storage (DS) or hybrid DG/DS units, and local loads able to operate in both grid-connected and islanded modes [1].

However, due to the presence of single-phase and/or three-phase unbalanced DRs/loads unbalanced voltage may appear in the microgrid, which may result in adverse effects such as efficiency reduction, instability, inappropriate protection actions, and interference problems. Moreover, in some cases, some loads such as induction machines are sensitive to voltage unbalances. Even though in some cases 2% or 3% voltage unbalance factor can be achieved but unbalanced current may reach more than 50%, which is enough to trip the overload protections [2]-[4]. On the other hand, passive loads may not be so sensitive to voltage unbalance. Therefore, we can have loads with different levels of unbalanced voltage sensitivities. In this way, loads with similar sensitive level can be connected to the same sensitive buses [5].

In order to meet the requirements of different control objectives and time scales, the hierarchical unbalance control structure is proposed in [6] and [7]. The objective of secondary control level is to ensure a specific range of negative unbalanced factors at sensitive buses, as presented in [6]. However, this method needs to take a sort of actions to reset the integrators; otherwise they may lead to negative saturation or inappropriate regulation.

In addition, in many commercial and industrial installations electrical power is distributed through a three-phase four-wire system, where a neutral connection is needed. Thus not only negative sequence but also zero-sequence components should be managed.

In the literature, there are three common ways to provide a neutral connection: (i) a zigzag or a delta-star (Δ-Yn) transformer, which prevents from zero sequence components propagation; (ii) three-leg split-capacitor structure, which retains a three-leg structure but splitting the dc link with a pair of capacitors to provide the fourth wire [8]; and (iii) three-phase four-leg topology [9], which provides a path for the neutral current by an additional fourth leg.

Due to the existence of a line-frequency transformer, this solution is bulky and costly, and zero sequence is decided by the loads, being less controllable. On the other hand, although the split-capacitor approach is simpler, zero-sequence current can cause large dc voltage differences between split capacitors, thus needing voltage balancing controllers or large dc-link capacitors [8]. In addition, this solution suffers from poor dc voltage utilization. The four-leg topology, due to the extra degree of freedom provided by the fourth leg, the three phases become independent. In addition, a 3-D space vector modulation will maintain the dc voltage utilization [9].

In a more general application like an islanded microgrid system, four-leg converters may be used as basic interfaces. In addition, in order to meet the high quality requirements at sensitive buses, a secondary voltage unbalance compensation strategy in islanded microgrids is proposed. This paper is organized as follows. In Section II the zero-sequence and negative-sequence equivalent circuits are derived and the unbalance compensation principle is presented as well. In Section III a new secondary voltage unbalance-compensation control approach is derived based on this model. Then, real-time hardware-in-the-loop (HiL) results are carried out in Section IV. Finally Section V presents the conclusion.

II. SYSTEM MODELING

A four-wire microgrid configuration based on three-phase four-leg converters is shown in Fig. 1. There are three types of buses in the microgrid: local buses (LB), sensitive bus (SB) and AC bus. In the SB, a sort of sensitive loads is connected. Also, we can have other types of converters, such as three-

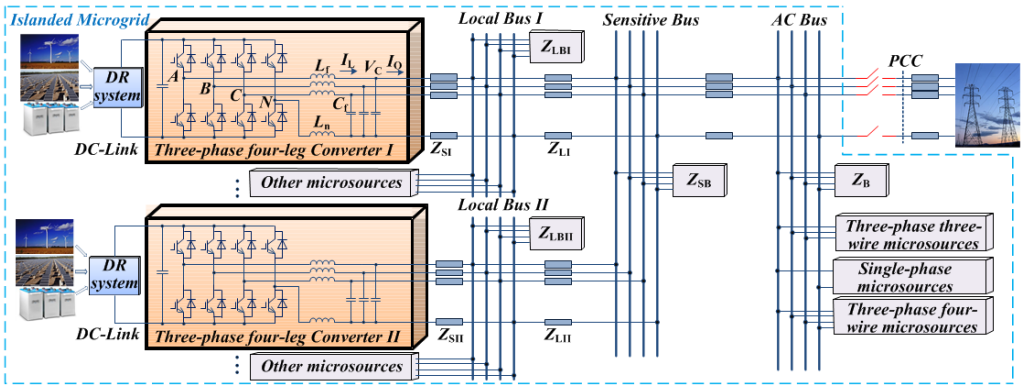

Fig. 1. Microgrid configuration based on three-phase four-leg converters.

phase three-leg converters and/or single-phase converters that connect DRs to those buses, which are named *microsources*. In order to simplify the analysis, only three-phase four-leg converters are under the scope of this paper.

During islanded mode, microgrid is expected to provide voltage and frequency management, maintaining supply and demand power balance, and offering the required power quality [7]. In this paper, in a certain SB, both voltage negative-sequence and zero-sequence unbalance factors are limited to a certain level, e.g. 0.5%. Here we assume that all the LBs have the same power quality restrictions, e.g. unbalanced factors limited to 3%.

To achieve these unbalance requirements, in this Section, the zero-sequence and negative-sequence equivalent circuits are firstly derived and the unbalance compensation principle is presented as well.

A. Sequence Equivalent Circuits

The relationships between phase admittance $\mathbf{Y}_p$ and sequence admittance $\mathbf{Y}_s$ can be obtained as

$$\mathbf{Y}_s = \mathbf{T}^{-1}\mathbf{Y}_p\mathbf{T} \tag{1}$$

where the transformation matrix $\mathbf{T}$ can be given as

$$\mathbf{T} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}, \quad a = e^{\mathrm{j}\frac{2\pi}{3}}$$

Two main kinds of passive loads (*RLC*) connections are shown in Fig. 2, where Y_{an}, Y_{bn}, Y_{cn} are equivalent loads connected between A, B, C and N; Y_{ab}, Y_{bc}, Y_{ca} are equivalent loads connected between phases.

For Y-connected load, the sequence admittance matrix can be derived as

$$\mathbf{Y}_{sy} = \frac{Y_{an}}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} + \frac{Y_{bn}}{3}\begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} + \frac{Y_{cn}}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \tag{2}$$

If Y_{an}=Y_{bn}=Y_{cn}= Y_y, then

$$\mathbf{Y}_{sy} = \mathbf{Y}_{py} = Y_y\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{3}$$

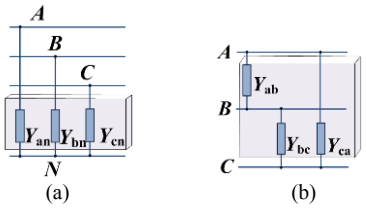

Fig. 2. Two kinds of loads. (a): Y-connected load; (b): delta-connected load;

From (3), the equivalent load for each sequence is the same and the loads are balanced. However, if there are differences between Y_{an}, Y_{bn}, or Y_{cn}, the system is unbalance, which will result in negative and zero sequence components.

For delta-connected load, the sequence admittance matrix can be given as

$$\mathbf{Y}_{sd} = Y_{ab}\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & -a \\ 0 & -a^2 & 1 \end{bmatrix} + Y_{bc}\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & -1 \\ 0 & -1 & 1 \end{bmatrix} + Y_{ac}\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & -a^2 \\ 0 & -a & 1 \end{bmatrix} \tag{4}$$

From (4), zero-sequence is omitted. If Y_{ab}=Y_{bc}=Y_{ca}=Y_d, then

$$\mathbf{Y}_{sd} = \mathbf{Y}_{pd} = 3Y_d\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{5}$$

Usually, negative and zero components in the bus voltage can be neglected since they are smaller compared to positive sequence voltage. Connecting these two kinds of loads to the same bus and assuming bus voltage $\mathbf{V}_p$=[v^0 v^+ v^-]^T, sequence current can be derived as

$$\mathbf{I}_s = \begin{bmatrix} i^0 \\ i^+ \\ i^- \end{bmatrix} \approx \frac{v^+}{3}\begin{bmatrix} Y_{an} + a^2Y_{bn} + aY_{cn} \\ Y_{an} + Y_{bn} + Y_{cn} \\ Y_{an} + aY_{bn} + a^2Y_{cn} \end{bmatrix} + v^+\begin{bmatrix} 0 \\ Y_{ab} + Y_{bc} + Y_{ac} \\ -a^2Y_{ab} - Y_{bc} - aY_{ac} \end{bmatrix} \tag{6}$$

From (6), the negative and zero sequence currents are mainly influenced by the positive voltage. For the sake of simplicity, here we can model the unbalanced passive loads as current sources.

For the electrical distribution lines, we assume that the admittances are balanced. Based on (3) and (5), the negative and zero sequence voltage drops are only related to corresponding sequence components.

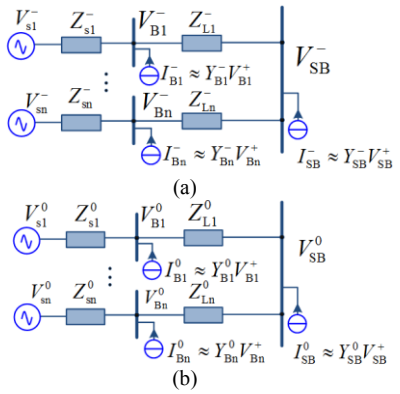

Fig. 3. Simplified negative and zero sequence circuits. (a) negative sequence; (b) zero sequence

From the above analysis, each *microsource* is represented by using Thévenin circuit, then the simplified negative and zero sequence circuits are obtained as shown in Fig. 3, where Z_s and Z_L are source impedance and distribution line impedance respectively; V_s, V_B, V_{SB} are respectively source voltage, local bus voltage and sensitive bus voltage; I_B and I_{SB} are respectively local load current and sensitive bus load current; superscripts *+*, *–*, *0* denote positive sequence, negative sequence and zero sequence respectively; subscript *n* denotes *n*-th *microsource*. For induction machine loads, they can be similarly analyzed as DR sources using Thevenin or Norton equivalent circuits.

B. Voltage Unbalance Compensation Principle

Define the source total negative sequence impedance and admittance as

$$\begin{cases} Z_{\mathrm{tk}}^{-} = Z_{\mathrm{sk}}^{-} + Z_{\mathrm{Lk}}^{-} \\ Y_{\mathrm{tk}}^{-} = 1/Z_{\mathrm{tk}}^{-} \end{cases} \qquad k = 1...n \tag{7}$$

Based on the superposition theorem, the source currents, local and sensitive bus voltages can be derived as

$$\begin{cases} I_{\mathrm{sj}}^{-} = \dfrac{V_{\mathrm{sj}}^{-} - (Z_{\mathrm{xj}}^{-} + Z_{\mathrm{Lj}}^{-}) I_{\mathrm{Bj}}^{-}}{Z_{\mathrm{tj}}^{-} + Z_{\mathrm{xj}}^{-}} - \dfrac{Z_{\mathrm{xx}}^{-} I_{\mathrm{SB}}^{-}}{Z_{\mathrm{tj}}^{-}} \\ \qquad - \dfrac{1}{Z_{\mathrm{tj}}^{-}} \displaystyle\sum_{k=1,k\neq j}^{n} \dfrac{Z_{\mathrm{xk}}^{-} V_{\mathrm{sk}}^{-} + Z_{\mathrm{sk}}^{-} Z_{\mathrm{xk}}^{-} I_{\mathrm{Bk}}^{-}}{Z_{\mathrm{tk}}^{-} + Z_{\mathrm{xk}}^{-}} \qquad ,(\mathrm{j}=1...\mathrm{n}) \\ V_{\mathrm{Bj}}^{-} = \dfrac{(Z_{\mathrm{xj}}^{-} + Z_{\mathrm{Lj}}^{-})(V_{\mathrm{sj}}^{-} - Z_{\mathrm{sj}} I_{\mathrm{Bj}}^{-})}{Z_{\mathrm{tj}}^{-} + Z_{\mathrm{xj}}^{-}} - \dfrac{Z_{\mathrm{sj}}^{-} Z_{\mathrm{xx}}^{-} I_{\mathrm{SB}}^{-}}{Z_{\mathrm{tj}}^{-}} \\ \qquad - \dfrac{Z_{\mathrm{sj}}^{-}}{Z_{\mathrm{tj}}^{-}} \displaystyle\sum_{k=1,k\neq j}^{n} \dfrac{Z_{\mathrm{xk}}^{-} V_{\mathrm{sk}}^{-} + Z_{\mathrm{sk}}^{-} Z_{\mathrm{xk}}^{-} I_{\mathrm{Bk}}^{-}}{Z_{\mathrm{tk}}^{-} + Z_{\mathrm{xk}}^{-}} \qquad ,(\mathrm{j}=1...\mathrm{n}) \\ V_{\mathrm{SB}}^{-} = \displaystyle\sum_{k=1}^{n} \dfrac{Z_{\mathrm{xk}}^{-} V_{\mathrm{sk}}^{-} + Z_{\mathrm{sk}}^{-} Z_{\mathrm{xk}}^{-} I_{\mathrm{Bk}}^{-}}{Z_{\mathrm{tk}}^{-} + Z_{\mathrm{xk}}^{-}} - I_{\mathrm{SB}}^{-} Z_{\mathrm{xx}}^{-} \end{cases} \tag{8}$$

where parallel impedances

$$Z_{\mathrm{xk}}^{-} = 1/\sum_{i=1,i\neq k}^{n} Y_{\mathrm{ti}}^{-} \quad \text{and} \quad Z_{\mathrm{xx}}^{-} = 1/\sum_{i=1}^{n} Y_{\mathrm{ti}}^{-}$$

Negative-sequence current-sharing between converters can be obtained by setting the same negative-sequence voltage reference V_s^-, and the same source impedance Z_s^- while keeping them much larger than the line impedance Z_L^-. In practical system, the same source impedance Z_S^- can be guaranteed by implementing virtual impedance at the primary control level [10], and the same reference can be ensured by the secondary control level, which will be explained in Section III. If all V_s^- and Z_s^- values are equal, the sensitive bus voltage and source currents can be simply represented by

$$\begin{cases} V_{\mathrm{SB}}^{-} = V_{\mathrm{s}}^{-} - \dfrac{Z_{\mathrm{s}}^{-} I_{\mathrm{SB}}^{-}}{n} + \displaystyle\sum_{k=1}^{n} \dfrac{Z_{\mathrm{s}}^{-} I_{\mathrm{Bk}}^{-}}{n} = V_{\mathrm{s}}^{-} - V_{\mathrm{SBL}}^{-} \\ I_{\mathrm{sj}}^{-} \approx -\dfrac{I_{\mathrm{SB}}^{-}}{n} - \displaystyle\sum_{k=1}^{n} \dfrac{I_{\mathrm{Bk}}^{-}}{n} \quad ,(\mathrm{j}=1...\mathrm{n}) \end{cases} \tag{9}$$

Thus, if V_s^- is regulated and the secondary control can react to unbalanced load changes, high power quality can be achieved in the sensitive bus. In addition, negative sequence current-sharing can also be guaranteed.

In terms of zero sequence, similar conclusion and performance can be obtained.

III. PROPOSED CONTROL STRATEGY

The objective of secondary control level is to actively compensate deviations in the microgrid voltage and frequency caused by the primary controls, restoring their values to the nominal ones or tracking grid values [7]. At the same time, this control level also can be used to compensate voltage unbalances at sensitive bus to meet the specified unbalanced voltage requirements [6]. The proposed control structure of secondary level is shown in Fig.4.

In this control level, the sensitive bus voltage is measured and decomposed into positive, negative, and zero components. Among different proposals, the band-pass filter based on Park transformation can achieve good performance [11], which is used for sequence component extraction. To overcome the limits of low-bandwidth communication channels, a *Park transformation* is employed. Especially for zero sequence components, they are mainly variable at fundamental frequency when supplying unbalanced loads. Thus a pair of orthogonal components $V_{\mathrm{SB\_}\alpha\beta}^{0}$ is firstly created by using a second order generalized integrator (SOGI) [12]. Thus negative sequence and zero sequence components can be modulated as DC signals in the secondary level, and demodulated back to AC signals in the primary level. In the secondary level, sensitive bus voltage v_{SB} is measured, while in the primary control DR voltage v_{c} is sensed. When the DC signals are transformed back to AC signals, the same reference angle needs to be used. However, due to the small difference in the fundamental angle between v_{c} and v_{SB}, these two voltages can be respectively used as reference angles in the primary and secondary levels.

As shown in Fig. 4, the sequence components in each synchronous rotating frame are firstly extracted. Afterwards, negative and zero unbalance factors are calculated and compared with reference values. If unbalance factors are already within the required values, then the output will be frozen. Otherwise, proportional integral (PI) controllers will be used to control the negative- and zero-sequence components.

If negative sequence unbalance factor needs to be limited within UF_{ref}^{-}, then the *dq* references for negative sequence voltage $V_{\mathrm{SB\_ref}}^{-}$ at sensitive bus is set as

$$V_{\mathrm{SB\_dref}}^{-} = V_{\mathrm{SB\_qref}}^{-} = \left|V_{\mathrm{SB}}^{+}\right| UF_{\mathrm{ref}}^{-} / \sqrt{2} \tag{10}$$

Based on (9), taking the load currents as disturbances and neglecting them, V_{SB}^{-} is equal to V_{s}^{-}. Therefore, the error of V_{SB}^{-} can be controlled by regulating V_{s}^{-}. In this paper, a simple PI controller is employed and its output is sent to the primary level. The control structure can be simplified as shown in Fig. 5. The secondary control usually has a slow control action. Hence the dynamic response of primary controller can be neglected when analyzing the performance of the secondary controller. Assuming the references can be real-time achieved $G_{\mathrm{P}}^{-}(s)$=1, then we can get

$$V_{\mathrm{SB}}^{-}(s) = V_{\mathrm{SB\_ref}}^{-} \frac{k_{\mathrm{p}}^{-} s + k_{\mathrm{i}}^{-}}{(1+k_{\mathrm{p}}^{-})s + k_{\mathrm{i}}^{-}} - \frac{s}{(1+k_{\mathrm{p}}^{-})s + k_{\mathrm{i}}^{-}} V_{\mathrm{SBL}}^{-} \tag{11}$$

The step response to the reference

$$v_{\mathrm{SB}}^{-}(\mathrm{t}) = v_{\mathrm{SB\_ref}}^{-}\left(1 - \frac{1}{1+k_{\mathrm{p}}^{-}} e^{-\frac{k_{\mathrm{i}}^{-}}{1+k_{\mathrm{p}}^{-}} t}\right) \tag{12}$$

The step response to the load disturbance

$$v_{\mathrm{SB}}^{-}(\mathrm{t}) = -\frac{1}{1+k_{\mathrm{p}}^{-}} e^{-\frac{k_{\mathrm{i}}^{-}}{1+k_{\mathrm{p}}^{-}} t} V_{\mathrm{SBL}}^{-} \tag{13}$$

Then by proper parameter design, unbalanced factors at sensitive bus can be limited within the required values, and dynamic response can be designed.

IV. Real-Time HiL Results

The proposed secondary voltage unbalance compensation strategy is validated through real-time HiL based on dSPACE 1006 platform, with the parameters shown in Table. I. Without loss of generality, two four-leg converters are used in the setup and 5% parameter mismatch is considered. In order to evaluate the performance of the proposed method, two types of loads are applied, where type A simulates three phase balanced load, and type B single phase load is connected between A and N, illustrating performances of the microgrid under the most unbalanced load conditions. The system gradually supplies more loads on the buses as shown in Table II, at last, total single phase loads reach the nominal value (each source 8kW per phase). As aforementioned, the bus which supplies unbalanced loads will impact on the unbalance distribution. Therefore, loads connected to both local and sensitive buses are discussed.

The HiL results are shown in Fig. 6.

At the beginning, the STS is off and microgrid operates in islanded mode. The loads on all the buses are balanced Type A. The voltages on all the buses are balanced.

At T1, an unbalanced load is connected to the sensitive bus, and the negative and zero sequence unbalance factors at all the buses starts to increase as shown in Fig. 6(a) (b).

At T2, the proposed unbalance secondary control is activated. Therefore, the unbalanced factors at sensitive bus

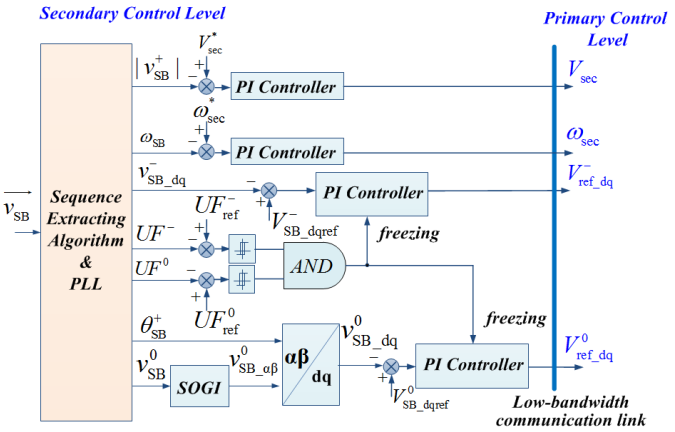

Fig. 4. Control structure of secondary control level

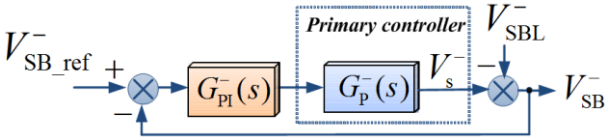

Fig. 5. Simplified control structure of secondary control level

TABLE I. System Parameters

Parameters	Symbol	Value
Power stage parameters		
Nominal output voltage	V_{N}	220V
Nominal output frequency	f_{N}	50Hz
Phase filter inductor	L_{f}	2mH
Neutral filter inductor	L_{n}	1.2mH
Filter Capacitor	C_{f}	30μF
Distribution line parameters		
Distribution line impedance I	Z_{LI}	1.8mH
Distribution line impedance II	Z_{LII}	0.9mH
Secondary control parameters		
Unbalance control	k_{p}^{-}, k_{i}^{-}	10, 10
	k_{p}^{0}, k_{i}^{0}	10, 10
Negative sequence UF reference	UF_{ref}^{-}	0.5%
Zero sequence UF reference	UF_{ref}^{0}	0.5%

TABLE II. System Operating Process: Load Conditions

Time	Local Bus I	Local Bus II	Sensitive Bus
0	Type A: Z_{TYA}=200Ω	Type A: Z_{TYA}=200Ω	Type A: Z_{TYA}=2000Ω
T1	-	-	Type B: Z_{TYB}=16Ω
T2	Activate unbalance control	-	-
T3	Type B: Z_{TYB}=12Ω	Type B: Z_{TYB}=48Ω	-
T4	-	-	Type B: Z_{TYB}=6Ω

are both decreased to the reference value 0.5% as shown in Fig. 6(a)(b).

At T3, different unbalanced loads are respectively connected to Local Bus I and Local Bus II. The unbalanced factors at the sensitive bus can be still fixed at 0.5%, as shown in Fig. 6(a)(b). Furthermore, based on (9), sources still present a good current-sharing, as shown in Fig. 6(c).

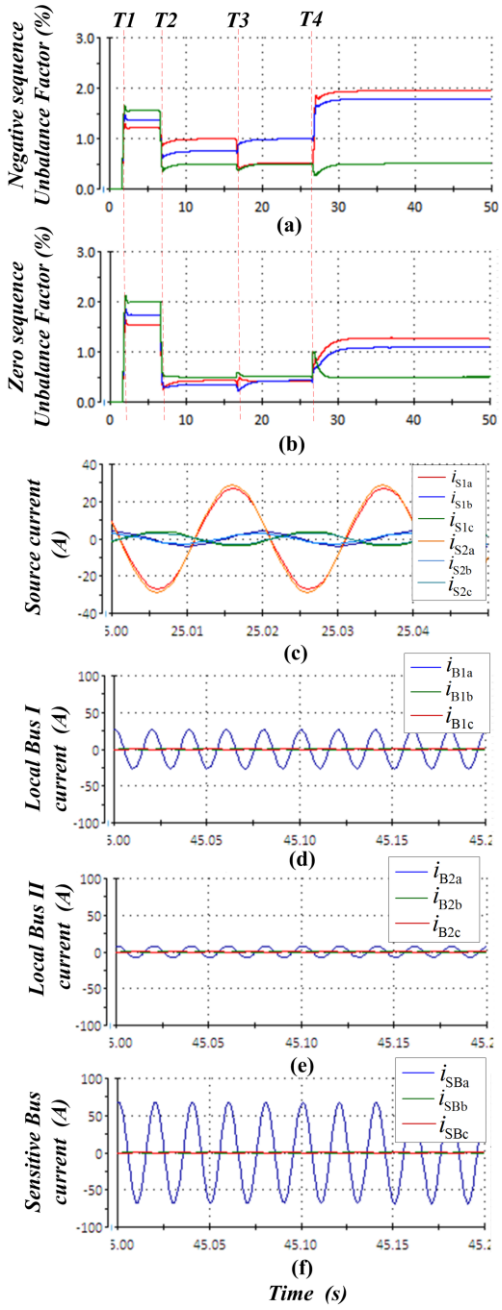

Fig. 6. HiL results

At T4, additional unbalanced loads are connected to the sensitive bus. The total amount of single-phase loads reach the nominal value, i.e. each source 8kW per phase, and load currents are shown in Fig. 6(d)(e)(f). The unbalanced factors at the sensitive bus can still be controlled to 0.5%, as shown in Fig. 6(a)(b). In addition, the unbalanced factors in all the other buses are kept below 2%.

Based on the above analysis, with the proposed unbalance control, the unbalanced factors are kept below the reference values. In addition, DRs can get a good positive, negative and zero sequence current-sharing.

V. Conclusion

Due to the presence of single-phase and/or three-phase unbalanced DRs/loads, unbalanced voltages may appear in the microgrid. In order to achieve unbalance management in three-phase four-wire microgrids, three-phase four-leg converters can be employed. To cope with this, system modeling and unbalanced compensation principle are firstly given. On this basis, a secondary voltage unbalance compensation strategy is proposed. Finally, the proposed method is tested under different load conditions. Real-time HiL results show that by using the proposed method the unbalanced factors are controlled within the specific ranges and at the same time DRs can get good sequence current-sharing.

References

[1] IEEE Guide for Design, Operation, and Integration of Distributed Resource Island Systems with Electric Power Systems, IEEE Std 1547.4-2011, pp.1-54, July 20 2011.

[2] R. C. Dugan, M. F. McGranaghan, S. Santoso, and H. W. Beaty, Electrical Power Systems Quality. 2nd ed., New York: McGrawHill, 2003.

[3] A. Baggini. Handbook of power quality, John Wiley & Sons, 2008.

[4] K. Lee. Power Quality Analysis and New Harmonic and Unbalance Control of Modern Adjustable Speed Drives Or Uninterruptible Power Systems Under Nonideal Operating Conditions. BiblioLife, LLC, 2011.

[5] C. Marnay, "Microgrids and heterogeneous security, quality, reliability, and availability," in Proc PCC 2007, pp. 629–634.

[6] M. Savaghebi, A. Jalilian, J. C. Vasquez, and J. M. Guerrero, "Secondary control for voltage quality enhancement in microgrids," IEEE Trans. Smart Grid, vol. 3, no. 4, pp. 1893–1902, Dec. 2012.

[7] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. Vicuna, and M. Castilla, "Hierarchical control of droop-controlled DC and AC microgrids—a general approach towards standardization," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 158-172, Jan. 2011.

[8] P. Salmeron, J. C. Montano, J. R. Vazquiez, and A. Perez, "Compensation in nonsinusoidal, unbalanced three-phase four-wire systems with active power-line conditioner," IEEE Trans. Power Electron., vol. 19, no. 4, pp. 1968–1974, Oct. 2004.

[9] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," IEEE Trans. Power Electron., vol. 17, no. 3, pp. 314–326, May 2002.

[10] J. M. Guerrero, L. GarciadeVicuna, J. Matas, M. Castilla, and J. Miret, "Output impedance design of parallel-connected UPS inverters with wireless load-sharing control," IEEE Trans. Ind. Electron., vol. 63, no. 5, pp. 1126–1135, Aug. 2005.

[11] V. Moreno, M. Liserre, A. Pigazo, and A. Dell'Aquila, "A comparative analysis of real-time algorithms for power signal decomposition in multiple reference frames," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1280-1289, Jul. 2007.

[12] P. Rodriguez, A. Luna, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Advanced grid synchronization system for power converters under unbalanced and distorted operating conditions," in Proc. 32nd IEEE Annu. Conf. Ind. Electron., Nov. 2006, pp. 5173–5178.