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Improved FRT Control Scheme for DFIG Wind Turbine Connected to a Weak Grid

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***Abstract*— This paper presents an improved coordinated fault ride-through (FRT) control strategy for a doubly fed induction generator (DFIG) based wind turbine, (WT), in a weak grid. A technique for grid synchronization against voltage excursions, i.e., a Dual Second Order Generalized Integrator – Frequency Locked Loop (DSOGI-FLL) is utilized to extract a robust grid voltage synchronization signal irrespective of the mains condition to enhance the overall system performance. Besides, a decoupled double synchronous reference frame (DDSRF) dq current controller is devoted for the grid side converter, (GSC), controller to counteract current ripples and tackle the DC link voltage fluctuations. Also, a reactive power support scheme to manage the DFIG reactive power during contingencies and fulfill the grid codes obligations is presented. Moreover, additional control terms are employed with the DFIG converters controllers to counteract rotor as well as stator currents and regulate the rotor speed. Simulation results which assure the effectiveness of the proposed control scheme is presented.**

Index Terms*— DFIG, DSOGI-FLL, FRT, grid code, weak grid.

I. INTRODUCTION

Wind energy conversion systems (WECS) are typically located in remote zones and connected to the grid via long feeders with lower short circuit ratios (SCRs). In the areas which geographically rich in wind energy, the transmission of huge amount of wind power to the power grid is restricted due to the transmission network weak structure [1]. In a weak grid, a change in active and/or reactive power can pose considerable voltage variation which can be a limiting factor for the integration of more wind power [2]. Besides, the impact of WT output power on the voltage quality can be another limiting factor which necessitates the incorporation of enhanced control systems to address such defects [2], [3].

Owing to the steady growth of decentralized wind power plants, (WPPs) many countries have imposed stringent regulations to the (WPPs) integration which known as grid codes [3]-[5]. Fig. 1.a shows the low voltage ride-through (LVRT) regulation for the German, Scottish and Irish grid code in which the wind turbines (WTs) must stay connected when the terminal voltage lies in or above the shaded area [3]. As illustrated in Fig. 1.a, E.ON LVRT demands fault ride-through (FRT) for voltage levels down to zero with 150 ms duration. Moreover, WTs should release reactive power support as traditional generators to boost and recover the ac voltage. Fig.1.b depicts the German and Spanish reactive power support requirement. Basically, reactive current support is substantial for voltage dips with remnant voltage less than 0.9 p.u., while full reactive current support is necessary for severe voltage dips with remnant voltage lower than 0.5 p.u [3], [4]. DFIG WTs, are extensively preferred due to variable speed operation using partial scale converters rated at 25-30% that allows for independent control of active and reactive power [4]. Nevertheless, DFIG is sensitive to the grid faults and thus prone to various serious issues due to the direct connection of its stator to the grid [2]-[4].

Subsequent to a fault, the rotor side and grid side converters, RSC, GSC respectively are prone to overcurrents and overvoltage unless an additional protection is incorporated. Usually, a crowbar circuit is inserted in the rotor side and activated upon fault detection to mitigate the above-mentioned shortcomings. However, triggering the crowbar results in blocking the RSC, meanwhile the machine absorbs higher reactive power as a conventional induction generator [3]. Using advanced control strategies, DFIG LVRT can be dramatically achieved [2]-[5].

In [5], a stability study for a permanent magnet WT connected to a weak grid is presented. It was shown that the operation of WTs in weak grids with SCRs below 4 is viable by means of advanced ac voltage controllers. The influence of the injected reactive current control to support the ac voltage due to symmetrical faults in a weak grid is investigated in [6]. It has been concluded that, DFIG WT can readily provide reactive power support via fast voltage control for weak grids with SCR of 4. Despite this, further compensation circuits are necessary to support the terminal voltage for SCRs between 2 and 3.

This paper provides an improved coordinated FRT control scheme for DFIG WT connected to a weak grid of SCR of 3 under different contingencies to fulfill the grid code requirements.

Typically, classical synchronous reference frame (SRF) dq current controllers render deficient performance during unbalanced utility conditions. To overcome such shortcoming, a decoupled double synchronous reference frame, (DDSRF) current controller is dedicated to control the GSC to tackle the double-frequency current oscillations and regulate the dc link voltage during disturbances. A reactive power support control scheme is presented to effectively satisfy the grid codes reactive

power boost obligation. Besides, a Dual Second Order Generalized Integrator – Frequency Locked Loop (DSOGI-FLL) is utilized so as to furnish a robust grid voltage synchronization signal against various perturbations.

For better regulation of the transient rotor currents, proportional integral plus resonant, PIR controllers are employed in the RSC controller. Additional proposed blocks are integrated with the DFIG converters controllers, to mitigate the rotor and stator overcurrents during voltage interruptions.

II. DFIG WT Capability Limits

The capability limits of a 2 MW DFIG considering stator and rotor currents heating constraints due to Joule's losses, maximum and minimum active and reactive power is shown in Fig.2 [1]. Identifying the control abilities of the DFIG aims at optimally design the DFIG control system in order to improve the system operation. More details about such capability limits can be found in [2].

III. Grid Synchronization

A. SRF-PLL Synchronization

Among the different aspects for the control of the grid-connected converters, is the exact synchronization with the utility voltage. Phase Locked Loop, PLL based synchronous reference frame, SRF-PLL is the most intensively used technique for detecting the magnitude and position of the positive-sequence grid voltage.

The basic structure of SRF-PLL is shown in Fig.3. Despite its good behaviour under normal conditions, SRF-PLL provides poor dynamic response under unbalanced grid conditions even with reduced bandwidth [7].

B. DSOGI-FLL Synchronization

Fulfilling the grid codes requirements and keeping the WT connected during contingencies entails the usage of alternative synchronization technique. Dual Second Order Generalized Integrator, DSOGI based Frequency Locked Loop, DSOGI-FLL is an insensitive frequency-adaptive synchronization mechanism which benefits the instantaneous symmetrical component analysis considering adaptive filters [7]. Being frequency-based, DSOGI-FLL can efficiently ride-through the grid perturbations, provides a clean synchronization signal and attenuates grid voltage high-frequency components [8]. Fig. 4 illustrates the DSOGI-FLL structure. Further details about DSOGI-FLL can be obtained from [7], [8]. Performance comparison between SRF-PLL and DSOGI-FLL will be presented through the simulation.

IV. Proposed DFIG FRT Control Scheme

This section provides an insight into the coordinated DFIG FRT control strategy used to improve the system performance and meanwhile satisfy the grid codes requirements.

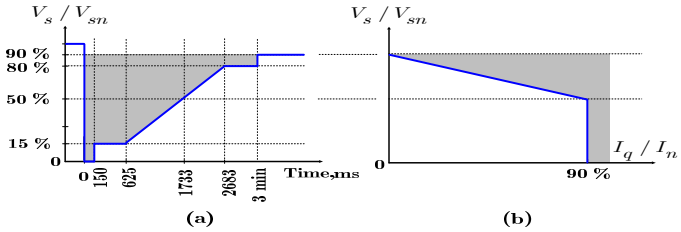

Figure 1. Typical WT Grid code requirements, (a) LVRT (b) Reactive power support

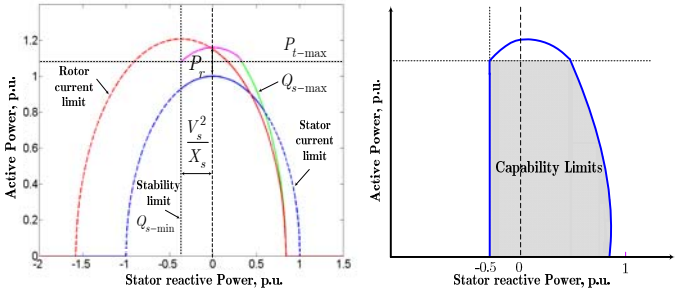

Figure 2. DFIG capability limits (a) Capability limits (b) Final capability area

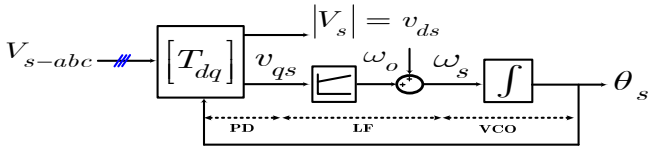

Figure 3. SRF-PLL basic structure

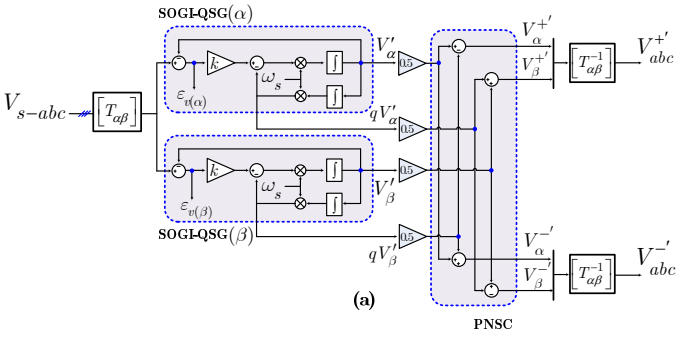

Figure 4. DSOGI-FLL basic structure

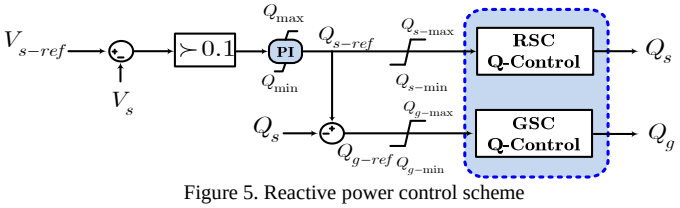

Figure 5. Reactive power control scheme

A. Reactive Power Support Control Scheme

A cascaded reactive power control scheme (see Fig.5) devoted to manage the reactive power sharing via DFIG stator as well GSC sides is adopted here [3]. The priority for the reactive power aid is given to the DFIG stator side -which processed via the RSC control- followed by the GSC side whenever the stator side attains the limit - due to severe faults - which pre-defined through the DFIG capability limit mentioned in section II. The reactive power support is initiated once the rms stator voltage, V_s slips more than 0.1 p.u (see Fig.1) out of the reference value, V_{s-ref}. Typical limiters are incorporated to ensure that the released reactive power does not overtake the respective capability limits of stator and GSC each. Such management scheme is efficient as the GSC reactive power support starts subsequent to the stator side injection which allows for active power transmission at the fault onset and thus mitigating the unwanted transient DC voltage fluctuations.

B. RSC Control Scheme

The stator side active and reactive powers, P_s, Q_s can be regulated via acting on the respective rotor *dq* voltage components. The RSC applied control scheme is demonstrated in Fig.6. The RSC controller is implemented in a reference frame of which *d-axis* is aligned with the stator voltage vector.

For further improvement of the RSC transient response, PIR current regulators are employed in the RSC controller as shown in Fig. 7 [9]. The parallel resonant blocks are tuned at $\omega_s, 2\omega_s$. ω_c is the cut-off frequency and k_{ir} is the proportional gain at the resonant frequency. Hence, the RSC *dq* voltage components are set as:

$$v_{dr} = PIR\left(i_{dr-ref} - i_{dr}\right) - \omega_{slip}\left(L_r i_{qr} + L_m i_{qs}\right) \quad (1.a)$$

$$v_{qr} = PIR\left(i_{qr-ref} - i_{qr}\right) + \omega_{slip}\left(L_r i_{dr} + L_m i_{ds}\right) \quad (1.b)$$

Where, i_{dr}, i_{qr} are the rotor active and reactive current components respectively. i_{ds}, i_{qs} are the stator side active and reactive current components. ω_{slip} is the slip frequency. L_r, L_m refer to rotor and magnetizing inductances.

The stator active and reactive powers, P_s, Q_s can be regulated via the RSC currents, i_{dr}, i_{qr} and subsequently rotor *dq* voltage components, v_{dr}, v_{qr}.

Whenever the stator voltage dips, the DFIG output power decreases as well. Accordingly, to tackle the transient rotor as well as stator currents and maintain the power balance, the MPPT is deactivated and the reference active power is set as [10]:

$$P_{s-ref} = k_p k_{opt}\left(V_s / V_{so}\right)^2 \omega^3_{r-ref} \quad (2)$$

$$k_{opt} = 0.5\rho A_b r_b^3 C_{p-\max} / N_g^3 \lambda_{opt}^3 \quad (3)$$

Where, k_p is a gain factor. V_{s0}, V_s refer to the stator voltage before and during the fault respectively and ω_{r-ref} is the reference rotor speed. With "2", tiny active power supply is sustained during severe faults as recommended by the British and Danish grid codes [3], [10]. With the aid of the reactive power support scheme, the RSC concurrently injects reactive current support with the remnant rotor current to fulfill the grid code commitment and restore the ac voltage.

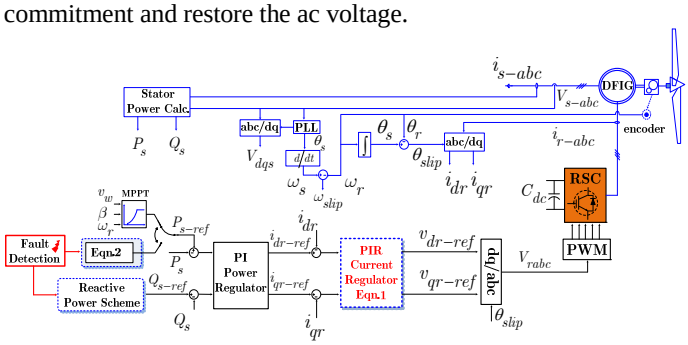

Figure 6. RSC control scheme

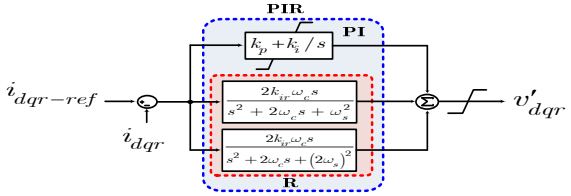

Figure 7. RSC PIR inner current controller

C. Conventional GSC Control Scheme

Likewise, the GSC controller is applied in a reference frame whose d-axis is oriented with the stator voltage$(v_{qs} = 0)$. The dc link voltage, V_{dc} and the reactive power exchanged between the grid and the GSC sides,Q_g can be controlled through acting on the *dq* GSC voltage components which can be expressed as:

$$v_{dg} = v_{ds} + \omega_s L_f i_{qg} - L_f \, di_{dg}/dt - R_f i_{dg} \quad (4)$$

$$v_{qg} = -\omega_s L_f i_{dg} - L_f \, di_{qg}/dt - R_f i_{qg} \quad (5)$$

Where, subscripts, v,i,ω, stand for voltage, current, and angular speed. Subscripts, s,g signify stator and grid sides. Indexes *d,q* stand for direct and quadrature axes of *dq* reference frame. R_f ,L_f refer to GSC interface reactor resistance and inductance.

The active and reactive power flow between the GSC and the grid can be written as:

$$P_g = 1.5 v_{ds} i_{dg} \quad (6)$$

$$Q_g = -1.5 v_{ds} i_{qg} \quad (7)$$

The DC link dynamics is given by:

$$\frac{1}{2} C_{dc} \frac{dV_{dc}^2}{dt} = P_r - P_g \quad (8)$$

In normal conditions, the GSC typically operates with a unity power factor, $Q_g = 0$. Fig. 8 illustrates The GSC traditional control scheme. To mitigate the dc voltage fluctuations during interruptions, a proposed term (P_g/V_{dc}) is activated and added to

the dc link voltage control loop to reflect the transitory variation of the GSC power. The latter can be attributed to the power imbalance between the RSC and GSC resulting from the surplus rotor power followed by the transient voltage dip which adversely impacts the dc voltage transient response [3].

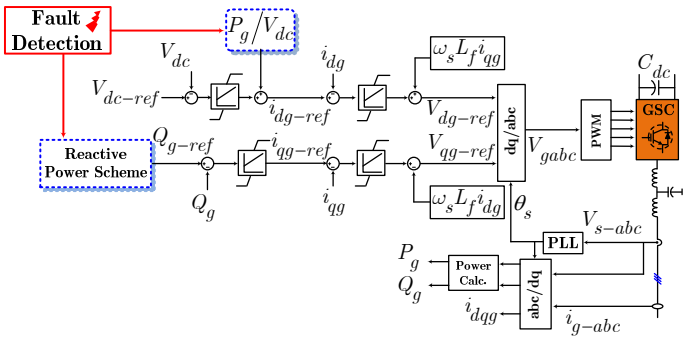

Figure 8. Conventional GSC control scheme

D. *Proposed GSC Controller*

Undoubtedly, LVRT and the associated DFIG WT converters control is a key point to satisfy the grid code requirements. Unbalanced grid voltages emerging from asymmetrical voltage dips can certainly cause sustained oscillations in the DFIG generated active and reactive power. Though this demerit can be overcome via injecting appropriate unbalanced currents by negative sequence controllers, the conventional SRF *dq* current controllers cannot accurately accomplish such objective due to sluggish dynamic performance [11].

Using DDSRF based PI regulators for controlling positive and negative sequences has been intensively implemented and thus can meet the target under such unbalanced grid conditions. Fig.9 shows the DDSRF respective positive and negative reference frames (dq^+, dq^-) rotating with the synchronous speed ($\pm\omega_s$) with angular positions ($\pm\theta'$) respectively. In this regard, decoupling cells to eliminate the reciprocal double-frequency cross-coupled ripples affecting both SRFs are added to enhance the controller performance during unbalanced conditions [10].

Thereby, the resultant DDSRF *dq* current controller can be expressed as [11]:

$$i'^{+}_{g-dq} = i^{+}_{g-dq} + \underbrace{e^{-j(\theta^{+}_{s}-\theta^{-}_{s})}\cdot i^{-}_{g-dq}}_{\text{AC Term}} - \underbrace{e^{-j(\theta^{+}_{s}-\theta^{-}_{s})}\cdot\left(i^{-}_{dqg-ref} - \overline{\Delta i^{-}_{dqg}}\right)}_{\text{Decoupling Term}} \quad (9)$$

$$i'^{-}_{g-dq} = i^{-}_{g-dq} + \underbrace{e^{-j(\theta^{-}_{s}-\theta^{+}_{s})}\cdot i^{+}_{g-dq}}_{\text{AC Term}} - \underbrace{e^{-j(\theta^{-}_{s}-\theta^{+}_{s})}\cdot\left(i^{+}_{dqg-ref} - \overline{\Delta i^{+}_{dqg}}\right)}_{\text{Decoupling Term}} \quad (10)$$

The cut-off frequency of the LPF, ω_f is selected as ($\omega_f = \omega_s/\sqrt{2}$) rad/s. A schematic diagram that abridges (9-10) for the GSC DDSRF dq current controller is shown in Fig.10. The outer controller of the DDSRF current controller is the same as that in [12].

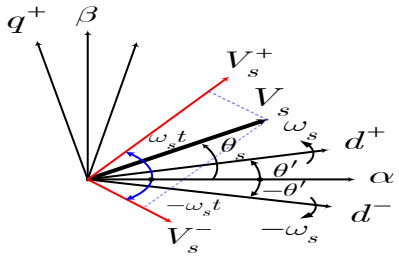

Figure 9. DDSRF respective reference frames phasor diagram

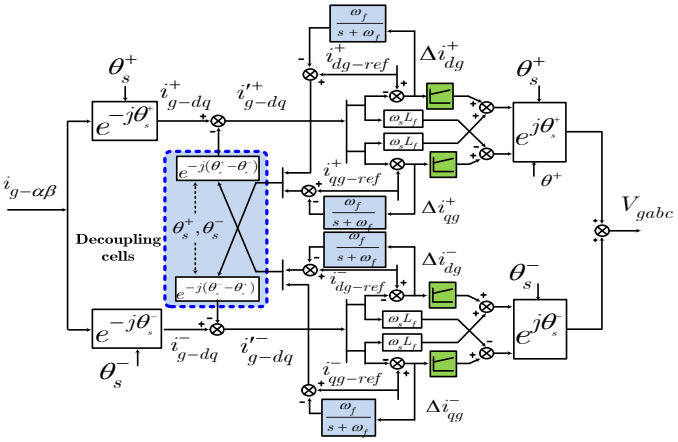

Figure 10. GSC DDSRF dq current controller

V. Simulation Verifications

A 2 MW, 0.69kV DFIG WT system used for the simulation is shown in Fig.11. The system is modeled and simulated in MATLAB/SIMULINK environment to evaluate the effectiveness of the proposed control strategy under various excursions. The simulations tests are performed at the nominal WT wind speed (11.4m/s). Whenever, a voltage dip is detected, the FRT protection strategy is enabled to safeguard the DFIG WT and the associated converters. Throughout the simulations, the maximum allowed dc voltage is set as 1.25 p.u. Stator and rotor currents protection maxima are set to 1.5 p.u. Nonetheless, the DFIG system converters, i.e., RSC and GSC can sustain 2 p.u overcurrent for a transitory time [4]. Furthermore, the pitch controller will be triggered in case of severe voltage dips to handle the rotor speed.

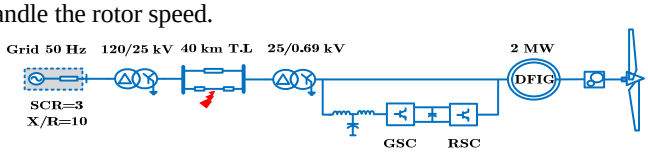

Figure 11. Schematic diagram of the system under study

A. *Symmetrical Fault Response*

Initially, the DFIG WT is supplying the rated output power while the delivered reactive power is set to zero ($Q_s, Q_g = 0$). The corresponding DFIG rotor speed is $\omega_r = 1.1$ p.u. At t=0.7s, the system is subjected to a severe symmetrical 3ϕ fault ($X_f/R_f = 5$) in the transmission line (see Fig. 11). The fault lasts

for 500 ms and cleared at 1.2s while normal operation is retrieved later as depicted in Fig. 12. The stator voltage (Fig. 12.a) drops to 95% during the fault, meanwhile the FRT protection is activated via a fault detection algorithm as that in [4]. Subsequent to the voltage dip, higher stator and rotor transient currents are noticed in Fig. 12.c-f. As a consequence to the transient rotor current growth, the GSC absorbed power -via the RSC side- rises instantaneously, which results in higher dc voltage fluctuations. However, the proposed control strategy is superior to its counterpart in maintaining the dc link voltage within the allowed limits as seen in Figs.12.k,l.

Besides, the adopted RSC fault ride-through, FRT, strategy in in both control schemes (see Figs.12.m,n) proved to regulate the power imbalance via curtailing the DFIG input power based on "2" in response to the reduction of the DFIG active power caused by the voltage dip and accordingly restricting stator as well as rotor overcurrents (Fig.12.c-f). Moreover, the pitch controller is engaged during the fault so as to regulate the rotor speed as seen in Figs. 12.i,j which still below the threshold limit (1.3 p.u.).

As reactive current aid should be released as a consequence to the stator voltage dip as stipulated by the grid codes (see Fig.1.b), the aforementioned reactive power scheme (see Fig.5) is activated to achieve this target in response to the stator voltage dip. The reactive current support led by the WT is shown in Figs.12.o,p. Though adopting the same reactive power scheme, it can be obviously noted from Fig.12.o that the proposed control method holds steadily the maximum reactive current support during the fault whereas, the conventional control method experiences unsuccessful reactive current support as depicted in Fig.12.p. The latter can be assigned to the loss of the accurate PLL synchronization and vector control orientation, VCO, caused by the severe symmetrical fault with 95% dip besides the voltage fluctuation led by the grid lower SCR. Fig.13.a,b show the synchronization signal detected by the DSOGI-FLL and SRF-PLL respectively. Compared with the SRF-PLL detected signal, the DSOGI-FLL extracts unaffected equidistant synchronization signal which correspondingly improves the overall system performance and satisfies the grid code obligations.

B. Asymmetrical Faults Response

Being accompanied with negative sequence currents, asymmetrical faults lead to dc voltage and electromagnetic torque ripples which influence the system converters and the coupling shaft of the WT and might eventually trip the DFIG WT [13]. Under the same pre-fault conditions assumed in the preceding test, the system response to asymmetrical faults is also examined. Figs. 14,15 show the system response to 150 ms, 90% voltage dip $\phi - g$ fault and 50% voltage dip 2ϕ fault respectively. Thanks to the control of the sequence currents via the GSC DDSRF current controller, the dc voltage ripples is well mitigated (Figs.14,15.k) compared with that of the conventional method (Figs.14,15.l) which exceeded the pre-defined limit with 1.32 p.u., voltage overshoot. Also, the transient stator and rotor currents are efficiently regulated below 2 p.u. Moreover, the DFIG delivered active power and injected reactive current (Figs.14,15.n,p) during both faults significantly fluctuate due to the limited RSC control capability [13]. On the other hand, lower oscillations are depicted in Figs.14,15.m,o by means of the proposed control strategy with better response. The superior performance of the proposed controller (Fig.14,15-A) over the conventional one, (Fig.14,15-B) is due to the comparative GSC DDSRF control effort exerted to regulate the sequence currents [13] and concurrently the excellent performance of the DSOGI-FLL of rendering a robust and clean synchronization signal compared with that of the conventional SRF-PLL regardless of the unbalanced mains as seen in Fig.13.c-f.

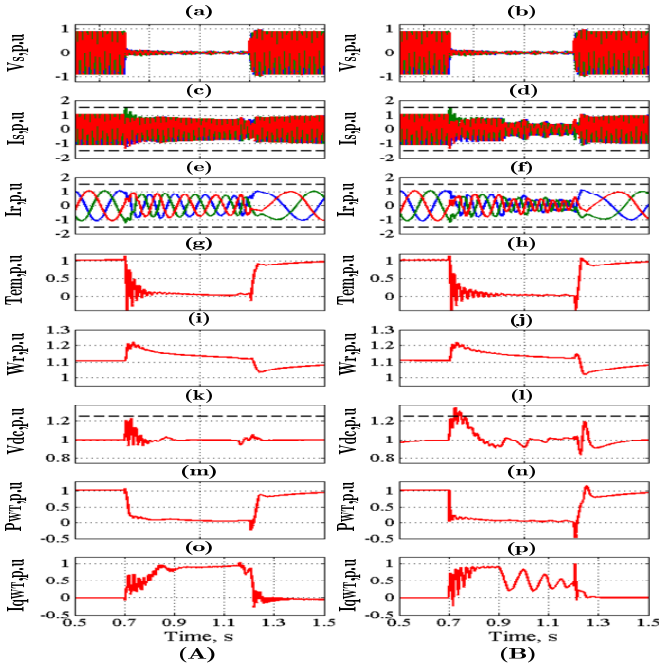

Figure 12. Simulated transient response of the studied system to a symmetrical 3ϕ fault ($X_f/R_f = 5$) (A) proposed control scheme (B) Conventional control scheme.

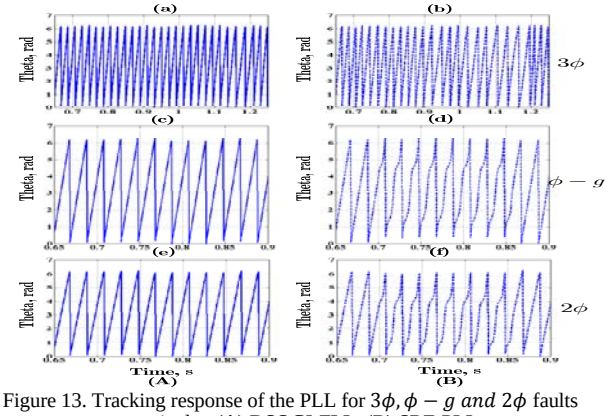

Figure 13. Tracking response of the PLL for $3\phi, \phi - g$ *and* 2ϕ faults respectively. (A) DSOGI-FLL. (B) SRF-PLL

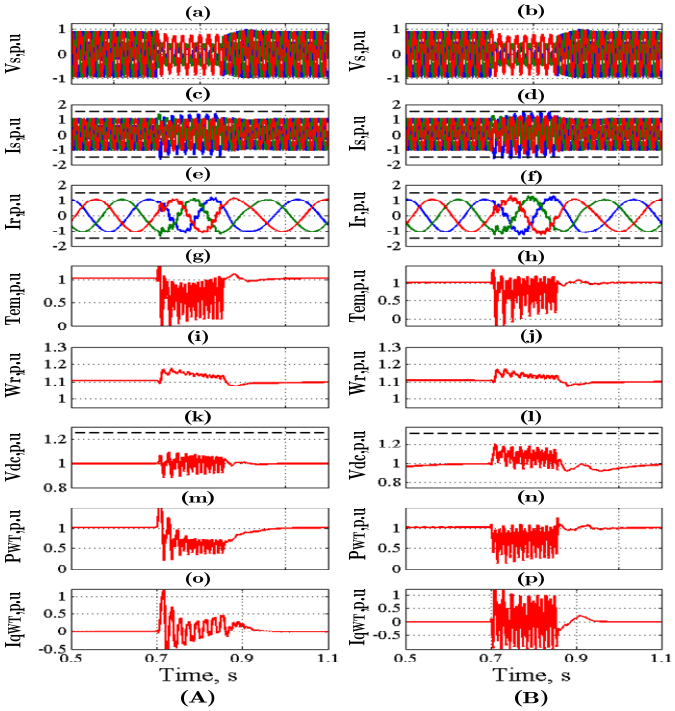

Figure 14. Simulated transient response of the studied system to single $\phi - g$ fault ($X_f/R_f = 5$) (A) proposed control scheme (B) Conventional control scheme.

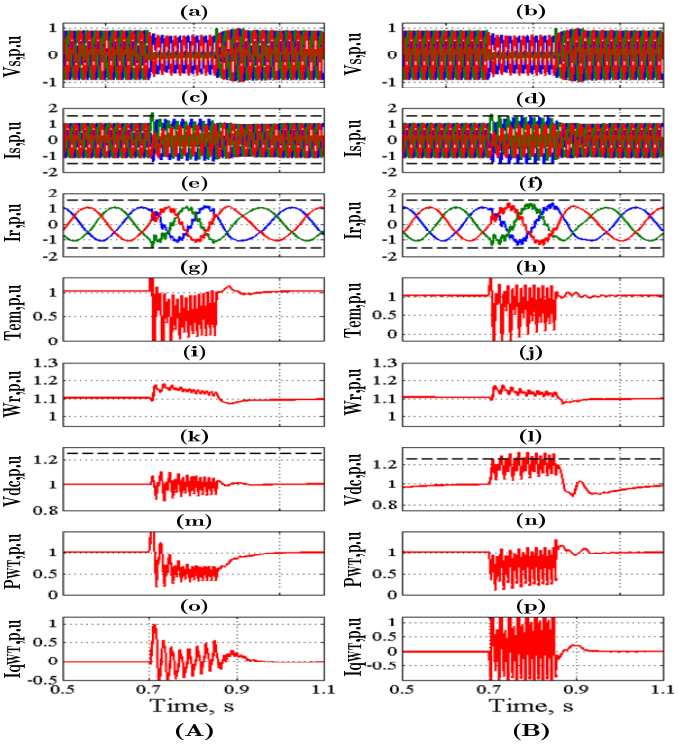

Figure 15. Simulated transient response of the studied system to 2ϕ fault ($X_f/R_f = 5$) (A) proposed control scheme (B) Conventional control scheme.

VI. Conclusions

A proposed coordinated control strategy has been presented to enable a DFIG WT to operate in a weak grid under different contingencies. A DDSRF dq current controller is devoted to control the GSC to mitigate the dc link voltage fluctuations and tackle current ripples.

A DSOGI-FLL is dedicated not only to render robust and clean synchronization signal detection irrespective of the utility condition, but also improve the overall system performance under severe disturbances.

A reactive power control scheme is used to manage reactive power injection during faults to satisfy the grid code obligation. Besides, extra terms are employed with RSC and GSC controllers to suppress the transient stator and rotor currents and regulate the rotor speed. The obtained results revealed the superiority of the proposed strategy that effectively enabled the DFIG WT to satisfy the grid code commitments in a weak grid.

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