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Abstract—This paper proposes an analytical model describing the generation of switching current noise in CMOS substrates. The model eliminates the need for SPICE simulations in existing methods by conducting a transient analysis on a generic CMOS inverter and approximating the switching current waveform using a Modified Raised Cosine (MORAC) equation. The proposed model is scalable, easy to implement and capable of predicting the spectral peak frequency of the substrate noise. The validation has been done via simulations and measurements. Good agreement has been found between the modeled and the measured results.

Index Terms—Analytical model, mixed-signal, raised cosine, substrate noise, spectral peak

I. INTRODUCTION

Substrate noise is one of the most important concerns in mixed-signal IC designs [1]. As illustrated in Fig. 1(a), since digital circuits and analog/RF circuits share the same substrate in mixed-signal ICs, the switching current ($I_s(t)$) generated by digital circuits can be coupled to sensitive analog/RF circuits through the substrate and presents as undesired noise [2]. The noise may cause significant variation of the back-gate voltage or be directly coupled to the inputs of the analog/RF circuits and deteriorate the circuits' performance. To solve this issue, understanding the mechanism of substrate noise is mandatory and a number of efforts have been made for substrate noise characterization [3–6].

Substrate noise characterization mainly involves two steps: modeling the generation of the switching noise, and modeling its coupling through the substrate. While the coupling can be modeled using a simple equivalent circuit network [3, 4], modeling the generation of the switching noise is relatively difficult. This is because the expression of the noise source ($I_s(t)$) is usually complicated and not in a closed form. Thus, simple approximations such as triangular waveforms (Fig. 1(c)) have been used to represent the switching current in order to simplify the noise characterization [3]. However, this type of models need to extract the key parameters of the triangular waveform (t_{pon}, t_{psl}, t_{tw} and I_p in Fig. 1(c)) using SPICE simulation [3], providing only limited insights into the mechanism of the switching noise. Recently, another method has been proposed to characterize substrate noise by modeling the generation and propagation of switching current noise in digital cells using mathematical waveforms and a coupling transfer function, respectively [6]. However, the switching current source is simplified to digital cell level in this method. Thus for each specific digital cell the switching

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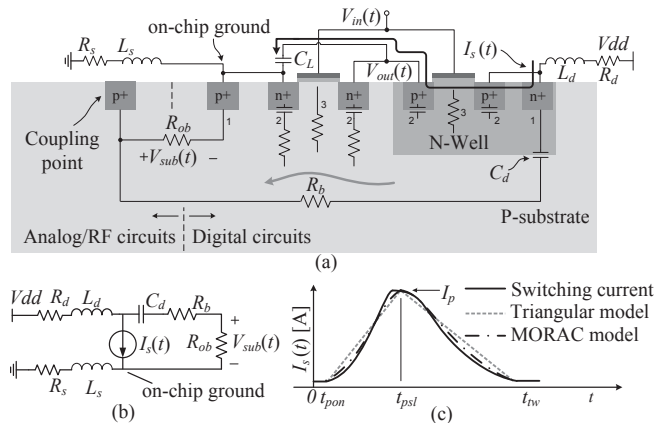
Fig. 1. (a) The generation and propagation of substrate noise in mixed-signal ICs, (b) the proposed model and (c) the switching current source.

current waveform needs to be obtained by SPICE simulation, which degrades its feasibility. To achieve more insights into the noise generation mechanism, an analytical model for the switching current in digital circuits is desired.

This paper proposes an analytical model for the switching noise in individual CMOS inverters, aiming to reveal more insights into the noise generation mechanism and pave the way for analytical modeling of switching noise in large scale digital blocks. The model approximates the switching current waveform using a modified raised cosine (MORAC) equation. And the expressions for the parameters in the equation have been derived by conducting a transient analysis on a generic CMOS inverter, eliminating the SPICE simulations required in existing methods. Based on the analysis, the expressions for t_{pon}, t_{psl}, t_{tw} and I_p needed in the conventional triangular model (Fig. 1(c)) have been provided as well. The transfer function modeling the injection and propagation of the switching current is also discussed. Combining the switching current model and the transfer function, the peak frequency where locates the most severe substrate noise can be predicted.

II. THE PROPOSED MODEL

In this paper, the switching current is modeled as a current source $I_s(t)$ (Fig. 1(b)) and the coupling and propagation of the switching noise is modeled by a circuit network. The model neglects the source/drain to bulk capacitive coupling and impact ionization (coupling 2, 3 in Fig. 1(a)). This is to simplify the analysis as the power/ground contacts coupling (coupling 1 in Fig. 1(a)) dominates the injection effects [2]. R_d, R_s, L_d and L_s are the resistances and inductances to the
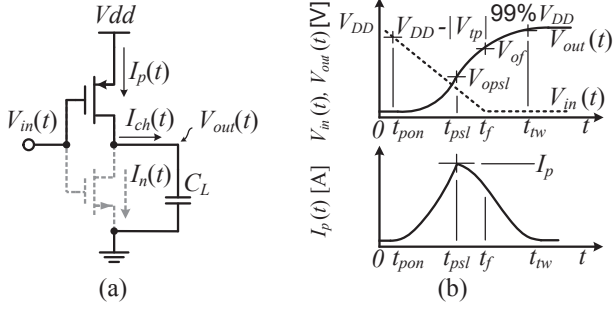
Fig. 2. a) The typical schematic of a capacitively loaded inverter and b) the switching current at the falling edge of the signal driving the inverter

off-chip DC supply and ground respectively. C_d is the junction capacitance of the N-well. R_{ob} is the substrate resistance between the noise coupling point and the on-chip ground. R_b denotes the spreading resistance between the inverter and the the coupling point. Based on Fig. 1(b) the resulting noise voltage observed at the coupling point may be expressed as

$$V_{sub}(j\omega) = H(j\omega) \cdot I_s(j\omega)$$
$$= \frac{-j\omega C_d R_{ob}(R_d + R_s)(1 + j\omega \frac{(L_s+L_d)}{(R_d+R_s)})}{1 + j\omega(R_d + R_s + R_b + R_{ob})C_d - \omega^2(L_s + L_d)C_d} I_s(j\omega). \quad (1)$$

A. *Calculating t_{pon}, t_{psl}, t_{tw} and I_p*

A typical schematic of an inverter with a capacitive load is shown in Fig. 2(a), where $I_p(t)$ is the drain current of the PMOS, $I_n(t)$ is the drain current of the NMOS and $I_{ch}(t)$ is the current charging/discharging the capacitor load. In this study, the short circuit current during switching transients is neglected to simplify analysis. Thus $I_p(t)$ is $I_s(t)$ in Fig. 1(b). One low-to-high switching transient of the inverter is shown in Fig. 2(b), while a high-to-low transient is similar in principle. As V_{in} falls, the PMOS is turned on at time t_{pon}, and start charging C_L. When $V_{out}(t)$ reaches V_{opsl} at t_{psl} and $V_{out}(t_{psl}) - V_{in}(t_{psl}) = |V_{tp}|$, where V_{tp} is the threshold voltage, the PMOS leaves the saturation region and enters the linear region. V_{of} is the output voltage at the falling time t_f. The time when the output reaches $0.99 \cdot V_{DD}$ is defined as t_{tw}.

In the Square-law MOSFET model the transistor drain current is expressed as [7]

$$I_D = \mu C_{ox} \frac{W}{L}[(V_{gs} - V_t)V_{DS} - \frac{V_{DS}^2}{2}], \quad V_{DS} \leq V_{Dsat} \quad (2)$$

$$I_D = \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{gs} - V_t)^2, \quad V_{DS} \geq V_{Dsat}, \quad (3)$$

where $V_{Dsat} = V_{GS} - V_t$, and V_{DS}, V_{GS} are the drain-source, gate-source voltage respectively. V_t denotes the threshold voltage. For generic analysis, corresponding lowercase letters are used to denote voltages normalized by V_{DD} in the following analysis. For example, $v_{out}(t) = V_{out}(t)/V_{DD}$. Considering Fig. 2(b), the input voltage waveform is assumed to have a falling ramp slope of $s_f = -1/t_f$:

$$v_{in}(t) = \begin{cases} s_f(t - t_f) & 0 \leq t \leq t_f \\ 0 & t \geq t_f \end{cases} \quad (4)$$

With this, the parameters of the switching current can be derived based on the expression of v_{out}, which can be found

by solving the differential equation

$$C_L \frac{dV_{out}(t)}{dt} = I_p(t), \quad (5)$$

where $I_p(t)$ can be replaced using Eq. (2) or (3) with corresponding terminal voltages [7, 8]. It should be noted that the falling input transient can be categorized as two cases: $v_{opsl} > v_{of}$ or $v_{opsl} < v_{of}$. For each case, the corresponding t_{psl} and t_{tw} can be found by solving Eq. (5).

Case A: $v_{opsl} \geq v_{of}$

$$t_{psl} = t_f - \frac{2pC_L}{K_p V_{DD}(1 + p)^2} + \frac{1 + p}{3s_f}, \quad (6)$$

$$t_{tw} = t_{psl} + \frac{\ln[(2(1 + p) - 0.01)/0.01] C_L}{K_p V_{DD}(1 + p)}. \quad (7)$$

Case B: $v_{opsl} < v_{of}$

$$t_{psl} = (v_{opsl} + p)/s_f, \quad (8)$$

where $p = V_{tp}/V_{DD}$, and v_{opsl} can be found by solving the equation

$$v_{opsl} = \frac{K_p V_{DD}}{6s_f C_L}(v_{opsl} - 1)^3. \quad (9)$$

Furthermore, t_{tw} can be found by

$$t_{tw} = t_f + [\ln((2(1 + p) - 0.01)/0.01) - $$
$$\ln\left(\frac{2p + 1 + v_{of}}{1 - v_{of}}\right)] C_L/(K_p V_{DD}(1 + p)), \quad (10)$$

where v_{of} can be determined from

$$v_{of}(t) = 1 - \exp\left(\frac{K_p V_{DD}(-1 - p)^2}{2s_f C_L}\right) / \left[\frac{\exp\left(\frac{K_p V_{DD} v_{opsl}^2}{2s_f C_L}\right)}{v_{opsl}} + \sqrt{\frac{K_p V_{DD} \pi}{8s_f C_L}} \mathrm{erf}\left(\sqrt{\frac{K_p V_{DD} v_{opsl}^2}{2s_f C_L}}, \sqrt{\frac{K_p V_{DD}(-1 - p)^2}{2s_f C_L}}\right)\right] \quad (11)$$

In addition, it is easy to derive that $t_{pon} = v_{tp}/s_f$, and $I_p = K_p(s_f t_{psl} + v_t)^2/2$.

B. *Modified Raised Cosine (MORAC) model*

Region 1: $0 < t < t_{pon}$.

$$I_p(t) = 0; \quad (12)$$

Region 2: $t_{pon} < t < t_{psl}$.

$$I_p(t) = I_p \frac{(1 + \cos(a_l(t - t_{psl})))}{2}; \quad (13)$$

where a_l is determined so that

$$(1 + \cos(a_l(t_{pon} - t_{psl})))/2 = 0; \quad (14)$$

Region 3: $t_{psl} < t < t_{tw}$.

$$I_p(t) = I_p \frac{(1 + \cos(a_r(t - t_{psl})))}{2}; \quad (15)$$

where a_r is determined so that

$$(1 + \cos(a_r(t_{tw} - t_{psl})))/2 = 0.01; \quad (16)$$

Region 4: $t_{tw} < t$.

$$I_p(t) = 0; \tag{17}$$

The Fourier transform of the MORAC model waveform is

$$I_p(j\omega) = I_{pml}(j\omega)/2 + I_{pml}(j(\omega - \frac{\pi}{t_{ml}}))/4+$$

$$I_{pml}(j(\omega + \frac{\pi}{t_{ml}}))/4 + I_{pmr}(j\omega)/2+$$

$$I_{pmr}(j(\omega - \frac{\pi}{t_{ml}}))/4 + I_{pmr}(j(\omega + \frac{\pi}{t_{ml}}))/4 \tag{18}$$

where $t_{ml} = t_{psl} - t_{pon}$, $t_{mr} = t_{tw} - t_{psl}$ and

$$I_{pml}(j\omega) = \frac{I_p}{\omega} exp(j\omega t_{ml}/2) sin(\omega t_{ml}/2) \tag{19}$$

$$I_{pmr}(j\omega) = \frac{I_p}{\omega} exp(j\omega t_{mr}/2) sin(\omega t_{mr}/2) \tag{20}$$

The rule of thumb to calculate the -3 dB cut-off frequency is

$$f_{prc} = \frac{min(a_l, a_r)}{2\pi}. \tag{21}$$

III. SIMULATION AND PEAK FREQUENCY PREDICTION

The proposed MORAC mode is validated by HSPICE simulation using a $0.18~\mu m$ CMOS process with $0.34~\mu m$ option. The PMOS and the NMOS have a W/L ratio of $0.68/0.34~\mu m$ and $0.34/0.34~\mu m$ respectively. The parameters of the PMOS are: $K_p = 4.75 \times 10^{-5}$, $V_{tp} = -0.66$ V, $V_{DD} = 3.3$ V and $t_f = 5$ ns. To evaluate the model in both case A and case B, C_L is chosen as 1 and 0.3 pF respectively. It should be noted that Eq. (6) to (11) are functions of the term $K_p V_{DD}/C_L$ and p, which means that the inverters having the same V_t, $V_{in}(t)$ and $K_p V_{DD}/C_L$ generate switching currents with the same t_{pon}, t_{psl} and t_{tw}. Thus the example shown here represents a group of general scenarios. The modeled and simulated switching current for case A and B are shown in Fig. 3 and Fig. 4 respectively. The results using triangular mode and the directly calculated switching current using Eq. (5) (denoted as Calculation) are shown as well. It can be seen that the MORAC model matches the simulated results very well and superior than the triangular model at frequencies lower than 300 MHz. It is also noted that the MORAC model has similar error level at further higher frequencies. But the magnitude of the switching current is significantly low (<-50 dB) at those frequencies and is less of concern. From Fig. 3 (b) and Fig. 4 (b) it can be seen that most energy of the switching current pulse is at low frequencies. Further, $H(j\omega)$ in Eq. (1) can be reformulated as

$$H(j\omega) = \frac{Aj\omega(1 + \frac{j\omega}{z_1})}{(1 + \frac{j\omega}{p_1})(1 + \frac{j\omega}{p_2})}, \tag{22}$$

where A is $-C_d R_{ob}(R_d + R_s)$. $H(j\omega)$ is found to have one zero at 0 rad/s and another at $(R_d + R_s)/(L_s + L_d)$ rad/s. The two poles are given as

$$p_{1,2} = \frac{R_\triangle C_d \pm \sqrt{R_\triangle^2 C_d^2 - 4(L_s + L_d)C_d}}{2(L_s + L_d)C_d}, \tag{23}$$

where $R_\triangle$ is $(R_d + R_s + R_b + R_{ob})$. Since neither the poles nor the second zero is located at 0 Hz, there exists a frequency
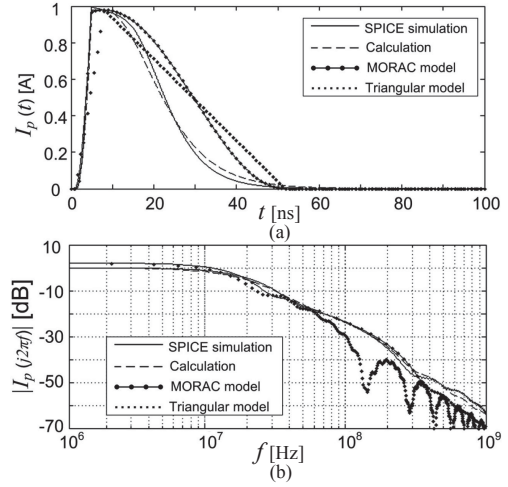

Fig. 3. Simulated and modeled switching current of Case A a) in time domain, and b) in frequency domain.
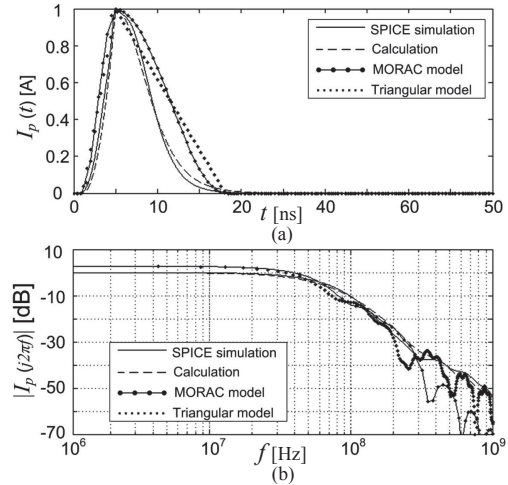

Fig. 4. Simulated and modeled switching current of Case B a) in time domain, and b) in frequency domain.

band from DC to a higher frequency, where $H(j\omega)$ can be simplified as

$$H(j\omega) = Aj\omega. \tag{24}$$

Since the magnitude of $Aj\omega$ is a 20 dB/decade line in frequency domain and the substrate noise has a constant magnitude at lower frequencies, the magnitude peak of the substrate noise is close to, and can be predicted using the -3 dB cut-off frequency (Eq. (21)).

IV. EXPERIMENTAL VERIFICATION

A test chip composed of an inverter and a substrate noise detector has been fabricated using a standard 0.18 μm CMOS process for experimental verification. The microphotograph of the test chip is shown in Fig. 6. The PMOS and NMOS devices are 600 μm and 300 μm wide respectively, and both transistors have the same length of 0.34 μm. In this case, K_p of the PMOS is 0.04. The value of the load capacitor is 20 pF. By comparing v_{opsl} and v_{of} obtained from Eq. (9) and (11) respectively, the MORAC model of case B is applicable in this test. A periodic square wave signal was used as input. The substrate noise was measured using a spectrum analyzer from an ohmic
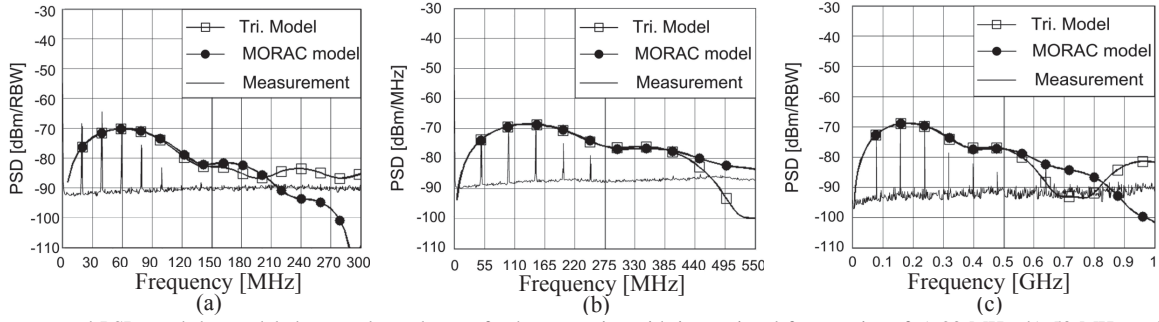
Fig. 5. The measured PSDs and the modeled spectral envelopes of substrate noise with input signal frequencies of a) 20 MHz, b) 50 MHz and c) 80 MHz.
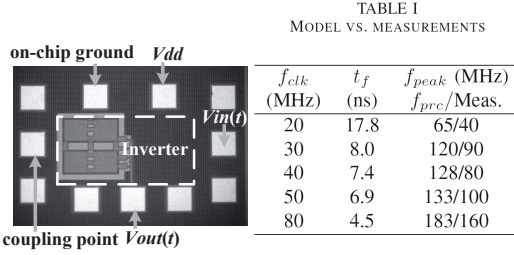

Fig. 6. Microphotograph of the test chip, the modeled cut-off frequency and the measured spectral peak frequency.

TABLE I
MODEL VS. MEASUREMENTS

f_{clk} (MHz)	t_f (ns)	f_{peak} (MHz) f_{prc}/Meas.
20	17.8	65/40
30	8.0	120/90
40	7.4	128/80
50	6.9	133/100
80	4.5	183/160

contact connected to the substrate [8]. Since the input signal is periodic, the substrate noise is periodic as well. Based on Parseval's theorem, the term

$$|H(jk2\pi/T)I_p(jk2\pi/T)/T|^2, \qquad (25)$$

is the average power of the switching noise at its k(th) harmonic. T is the period of the input signal and k is an integer. The magnitude of $V_{sub}(j\omega)$ depends on the layout and the circuit parameters. To have accurate magnitude prediction of the substrate noise, the value of $R_{ob}(R_d + R_s)$ in A needs to be extracted from layout and bonding wires [3, 6]. But A and T affect only the magnitude of the substrate noise but not the spectral envelope, which is given by the term

$$|j\omega I_p(j\omega)|^2. \qquad (26)$$

Therefore the measured PSDs of the substrate noise were compared with the spectral envelopes calculated using Eq. (26) to verify the proposed model. Measurements with different signal frequencies from 20 MHz to 80 MHz and falling times have been conducted. The comparisons between measurement, the MORAC model and conventional triangular model with three frequencies are shown in Fig. 5. The maximal magnitude of the modeled spectral envelopes is normalized to the power level of the measured substrate noise PSD at the same frequency. It can be seen that the modelled spectral envelopes match the measured results very well at lower frequencies in Fig. 5(b) and Fig. 5(c) when the input signal frequency is 50 MHz and 80 MHz respectively. Big deviations are found in lower frequencies in Fig. 5(a) for the case of 20 MHz and the falling time is 17.8 ns. This is because the mode is based on the assumption of no short current and it is less valid for cases with long falling time. In addition, relatively bigger errors are found at higher frequencies in all results. This might be explained

by the simplification of $H(j\omega)$ to $Aj\omega$. At last, the calculated -3 dB cut-off frequencies and the measured frequencies of the spectral peaks of the substrate noise are shown in Table I. The calculated cut-off frequencies provide a good prediction of, yet relatively higher than the measured peak frequencies. Considering that the attenuation of the measurement setup at higher frequencies has been included, the predicted cut-off frequency should be more accurate for on-chip substrate noise.

V. CONCLUSION

This paper proposes an analytical model providing an insight understanding of the generation and propagation of switching noise in CMOS technologies. The model needs no SPICE simulations which are mandatory in existing methods. Based on the model, the spectral peak frequency of the substrate noise can be predicted, which is useful for noise impact evaluation in mixed-signal IC designs. A test chip has been fabricated using a $0.18\ \mu m$ CMOS process for validation and good agreement has been found between the modeled and measured results.

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