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Design of a Window Comparator with Adaptive Error Threshold for Online Testing Applications

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Abstract

This paper presents a novel window comparator circuit whose error threshold can be adaptively adjusted according to its input signal levels. It is ideal for analog online testing applications. Advantages of adaptive comparator error thresholds over constant or relative error thresholds in analog testing applications are discussed. Analytical equations for guiding the design of proposed comparator circuitry are derived. The proposed comparator circuit has been designed and fabricated using a CMOS 0.18μ *technology. Measurement results of the fabricated chip are presented.*

1 Introduction

Online testing has been widely used in mission-critical applications to improve the fidelity of electronic systems. In the past, various techniques have been developed to perform online testing for analog circuits [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. Among those techniques, an effective approach is to duplicate a portion of the circuit under test (CUT) and compare the outputs of the original circuit and its replication [1, 2, 3]. This testing approach, referred to as redundancy-based online testing scheme, is illustrated in Figure 1. Comparators used in this testing scheme are expected to sensitively detect output differences caused by circuit faults and meanwhile ignore small variations due to circuit mismatches and parasitic effects. Typically, window comparators are used in such testing applications. The output of a window comparator switches from one logic value to the other when the difference between its analog inputs exceeds the range of $[-V_\epsilon, V_\epsilon]$, where V_ϵ is referred to as the error threshold of the window comparator.

There are three types of window comparator error thresholds, namely *constant*, *relative*, and *adaptive* error thresholds. As illustrated in Figure 2(a), a constant error threshold does not change its value at different input signal levels. In the figure, we assume input signals are centered at the signal ground level V_{sg} and the maximum peak-to-peak value of the inputs is $2 \cdot V_A$. It is not rare that the difference of the faulty and fault-free circuit responses is proportional to the input levels of the CUT. For this reason, window comparators with constant error thresholds may not be able to detect circuit faults when the CUT input signals are small during online testing operations. To avoid this problem, relative error thresholds, which are proportional to comparator input levels as shown in Figure 2(b), can be implemented. However, the problem associated with relative error thresholds is that they become too small when comparator input levels are close to the signal ground level. Thus, small differences between comparator inputs, caused by device mismatches or other parasitic effects, may be identified as faults by window comparators with relative error thresholds.

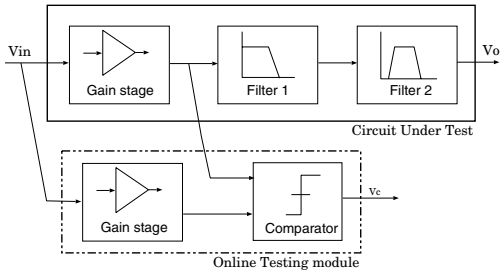

Figure 1. Redundancy based online testing scheme.

To address the above problems, an adaptive error threshold approach, which is shown in Figure 2(c), can be used in window comparator design. In such a circuit, when comparator inputs are large, the relative error threshold scheme is used. While, if the comparator experiences small input signals, it switches to the constant error threshold mode. For the convenience of discussion, we refer to the region that the comparator has a constant error threshold as the *flat band region*. The voltage, V_F, at which the window comparator switches from the constant error threshold mode to the relative error threshold mode, is called *flat band voltage*. The ratio of V_F to V_A is called *flat band ratio* and denoted by symbol $\mathcal{R}$. Also, we define V_{in}^{eff}, comparator effective input, as $V_{in}^{eff} = V_{in} - V_{sg}$. Then, the adaptive error threshold of a window compara-

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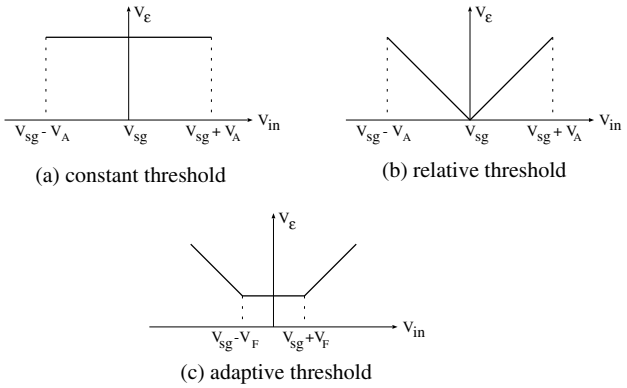

Figure 2. Different window comparator error threshold schemes.

tor can be expressed as:

$$V_\epsilon = \begin{cases} \kappa \cdot |V_{in}^{eff}| & \text{for} \quad V_A > |V_{in}^{eff}| > V_F \\ V_{const} & \text{for} \quad |V_{in}^{eff}| \leq V_F \end{cases} \quad (1)$$

where κ is the coefficient of the error threshold when the comparator circuit operates outside its flat band region. In this work, we present a novel design for implementing window comparators with adaptive error thresholds. We also address design considerations and develop analytical equations to help the selection of component parameters during the design phase.

The rest of the paper is organized as follows. Section 2 reviews previously proposed window comparator circuits. Section 3 describes our proposed comparator design. Implementation and testing results are presented in Section 4, and the paper is concluded in Section 5.

2 Previous Implementations of Window Comparators

Previously, various window comparators have been developed. In literature [11], a switched-capacitor based window comparator is presented. It has the advantage that the error threshold can be programmed by digitally adjusting capacitor ratios. However, if the circuit is not carefully optimized, channel charge injection and clock feedthrough associated with CMOS switches may affect the accuracy of the realized error thresholds. *Zhang et al.* propose a comparator circuit that utilizes two operational amplifiers (op-amps) and a set of resistors that govern the error threshold [12]. This circuit can perform self-testing. However, it requires accurate resistor ratios and may result in large footprint due to the use of multiple op-amps. The window comparator presented in [13] is designed to take two pairs of differential inputs and monitor the difference between their common-mode levels. This implementation employs differential input pairs as pre-amplifiers, and use inverters to digitize the outputs of the pre-amplifiers. Comparator implementations in [14, 15] are based on folded-cascoded op-amp circuits. Asymmetric differential pairs are intentionally used at the input stages of the op-amps to introduce input offset voltage, which is translated into the comparator error threshold. De Venuto et.al, have proposed window comparator design using digital inverters with different inverter thresholds [16, 17, 18, 19]. Such circuits have very simple structures and take small silicon area. More interestingly, they can be self-tested before the normal operations. Due to the use of digital circuits, the realized error threshold is sensitive to process variations. To address this problem, an automatic repositioning technique is proposed in [18]. All the window comparators discussed above belong to the category of constant error threshold comparators.

A window comparator with relative error threshold voltage is described in [15]. It uses switched-capacitor circuit techniques and dynamically adjusts the comparator error thresholds by taking advantage of CMOS switch channel charge injection effects. A large input signal results in a small transistor overdrive voltage and, consequently, leads to less channel charge injection when the switch is turned off. This fact is exploited in the design to vary the comparator error threshold. Window comparators with adaptive error thresholds are presented in [20, 21, 22]. They also rely on a pair of inverters to digitize the amplified (using a fully differential pre-amplifier) input difference. The adaptive error threshold is implemented by dynamically adjusting the impedance of the pull-up paths of the two inverters according to input levels. Improved concurrent error detecting capabilities have been reported using such comparators.

3 Proposed window comparator implementation

In this work, we present a novel design of window comparator with adaptive error thresholds. Compared to previously developed circuits, our proposed circuit can be more easily optimized for different parameters associated with the adaptive error threshold scheme. Closed-form design equations are developed for guiding the design process to achieve the specified flat band ratio, flat band voltage and error threshold slope κ. The proposed circuit consists of two components. The first component is a window comparator circuit whose threshold can be programmed through its biasing current [23]. The second component is an adaptive biasing circuit, whose output current varies according to its input signal level. The design of these two components is described as follows.

3.1 Proposed Window Comparator

The proposed window comparator circuit, as shown in Figure 3, is comprised of a differential input pair and four current mirrors. Transistors N_1 and N_2 constitute the dif-

ferential pair and their tail current is provided by transistor N_3. PMOS devices $P_1 \sim P_6$, which have the same size, implement two sets of PMOS current mirrors. While, transistors N_4 and N_7, N_5 and N_6, realize two NMOS current mirrors with a current gain of m (the size of transistors N_6 and N_7 is m times larger than that of N_4 and N_5). Assume the tail current flowing through N_3 is I_b. When both comparator inputs are at the same level, transistors N_1, N_2, N_4, N_5, and $P_1 \sim P6$ are in their saturation regions, and all the currents flowing through these transistors are $\frac{I_b}{2}$. Devices N_6 and N_7, working in their linear regions, pull voltages at nodes A and B close to ground, driving the comparator output to logic *1*. If comparator input V_{in1} is larger than input V_{in2}, currents flowing through devices N_1 and N_2 become $\frac{I_b}{2}+i$ and $\frac{I_b}{2}-i$, or *vice versa*. When the input difference as well as the resultant current i are large enough, the current supplied by P_5 or P_6 will be larger than the current that can be sunk by N_6 or N_7 if they all operate in their saturation regions. As a result, either node A or B will switch to a high voltage level, forcing the corresponding PMOS device into its linear region to balance the current flow. This triggers the comparator output switching to logic *0*.

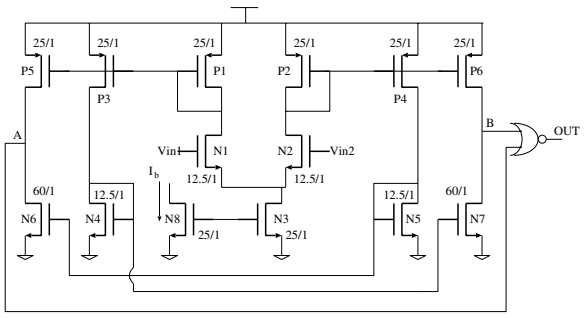

Figure 3. Proposed comparator sub-circuit.

The condition for node A or B switching to the high voltage level is:

$$\frac{I_b}{2} + i > m \cdot (\frac{I_b}{2} - i) \tag{2}$$

Assuming that the relation between I_{DS} and V_{GS} of N_1 and N_2 follows the perfect square-law, the comparator error threshold can be derived as:

$$V_\epsilon = \sqrt{\frac{2I_b}{\mu_n \cdot C_{ox} \cdot (W/L)^c_{1,2}}} \cdot \sqrt{1 - \sqrt{1 - (\frac{m-1}{m+1})^2}} \tag{3}$$

where μ_n is the electron mobility; C_{ox} is the device unit gate capacitance; and $(W/L)^c_{1,2}$ is the size of N_1 and N_2.

To implement the error threshold scheme described in Equation 1, an adaptive biasing current is needed for this comparator circuit. When the comparator inputs are within the flat band region, the biasing current should be a constant. However, when the comparator inputs are out of the flat band region, the biasing current needs to be proportional to the square value of the input signals. The implementation of such a biasing circuit is presented in the next section.

3.2 Adaptive biasing circuit

The proposed adaptive biasing circuit, shown in Figure 4, can be partitioned into four blocks according to their functions. Depending on whether the level of the input signal is right ($V_{in} > V_{sg} + V_F$), left ($V_{in} < V_{sg} - V_F$), or within (($V_{sg} + V_F < V_{in} < V_{sg} + V_F$) the flat band region as shown in Figure 2 blocks labeled by U_1, U_2, and U_3 are selectively activated and, consequently, determine the biasing current. The fourth block, consisting of transistors $M_{6\sim7}$ and $M_{13\sim17}$, sums the outputs of U_1, U_2, and U_3. The operation of U_3 is simple. When the sum of the currents from U_1 and U_2 is greater than I_{min}, node Z is discharged to a low voltage level. M_{15} is off and the biasing circuit output I_b is independent of U_3. However, when the sum of U_1 and U_2 outputs is smaller than I_{min}, node Z will be charged and, consequently, M_{15} is on to increase the biasing circuit output. The circuit will reach a stable point when $I_b = I_{min}$. This constant biasing current will result in a constant comparator error threshold, which is required in the flat band region.

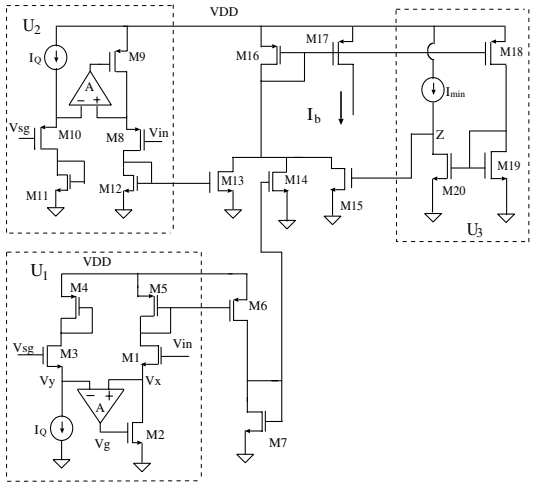

Figure 4. Proposed adaptive biasing circuit.

U_1 and U_2 operate in a similar manner. Thus, only U_1 is discussed here. In the design, current I_Q is selected very small. Thus, $V_y \approx V_{sg} - V_t'$, where V_t' is the threshold voltage of M_4 with considering body effect. With a reasonable amplifier gain A, V_x is close to V_y and, hence, the threshold of M_1 is also approximately equal to V_t'. If the input of the biasing circuit (same as the window comparator input) is smaller than V_{sg}, M_1 is off and U_1 does not affect the biasing circuit output. When the input level is greater than V_{sg}, the currents flowing through M_1 and M_2, denoted by I_{DS1} and I_{DS2}, are the same. Thus, V_x

can be solved as:

$$V_x = \frac{k \cdot A \cdot V_{sg}}{1 + k \cdot A} + \frac{V_{in}}{1 + k \cdot A} + \frac{k \cdot V_t}{1 + k \cdot A} - V_t' \quad (4)$$

where, $k = \sqrt{\frac{(W/L)_2}{(W/L)_1}}$ and V_t is the threshold voltage of M_2. Consequently, I_{DS1} can be derived as:

$$I_{DS1} = \frac{\mu_n \cdot C_{ox}}{2}(\frac{W}{L})_1 \frac{k \cdot A}{1 + k \cdot A} \cdot (V_{in} - V_{sg} - \frac{V_t}{A})^2 \quad (5)$$

If A is not very small, we can practically ignore the term of $\frac{V_t}{A}$ in the above equation. Then, we have:

$$I_{DS1} = \frac{\mu_n \cdot C_{ox}}{2}(\frac{W}{L})_1 \frac{k \cdot A}{1 + k \cdot A} \cdot (V_{in} - V_{sg})^2 \quad (6)$$

I_{DS1} is copied by $M_{5\sim7}$ and added to the biasing circuit output by M_{14}. If $I_{DS1} > I_{min}$, the biasing circuit output I_b is the same as I_{DS1}, which is proportional to the square value of the input signal. From the above relation, flat band voltage V_F can be solved as:

$$V_F = \sqrt{\frac{2 \cdot I_{min} \cdot (1 + k \cdot A)}{\mu_n \cdot C_{ox} \cdot (W/L)_1 \cdot k \cdot A}} \quad (7)$$

Also, substituting Equation 6 into Equation 3 and comparing the resultant V_ϵ expression with Equation 1, we obtain the value of coefficient κ as:

$$\kappa = \sqrt{\frac{1}{2}\frac{(W/L)_1}{(W/L)^c_{1,2}}\frac{k \cdot A}{1 + k \cdot A}} \cdot \sqrt{1 - \sqrt{1 - (\frac{m-1}{m+1})^2}} \quad (8)$$

Note that $(W/L)_1$ is the size of M_1 in the biasing circuit and $(W/L)^c_{1,2}$ represents the size of N_1 and N_2 in the window comparator circuit (shown in Figure 3). The above equations show that various parameters can be adjusted to achieve the desired V_F and κ values.

Note that the amplifiers used in the biasing circuits can be simple low-gain amplifiers. This is explained as follows. If the $\frac{V_t}{A}$ term in Equation 5 is not completely ignored, the expression of I_{DS1} can be re-written as:

$$I_{DS2} \approx \zeta \cdot [(V_{in} - V_{sg})^2 - 2 \cdot (V_{in} - V_{sg}) \cdot \frac{V_t}{A}] \quad (9)$$

where

$$\zeta = \frac{\mu_n \cdot C_{ox}}{2}(\frac{W}{L})_1 \frac{k \cdot A}{1 + k \cdot A} \quad (10)$$

Note that the square term $(\frac{V_t}{A})^2$ is omitted due to its small value. Inside the bracket at the right-hand side of Equation 9, the first term represents the ideal value that will result in a perfect current output; the second term represents a linear error added to the ideal value. Thus, the relative error α[1] of the biasing circuit output can be written as:

$$\alpha \approx \frac{2 \cdot V_t}{A \cdot (V_{in} - V_{sg})} \quad (11)$$

[1] $\alpha = \frac{|I_b(ideal) - I_b(real)|}{|I_b(ideal)|}$

It is easy to see that α has its largest value when the input signal is just beyond the flat band region. Thus, the largest α can be written as:

$$\alpha_{max} = \frac{2 \cdot V_t}{V_A} \cdot \frac{1}{A \cdot \mathcal{R}} \quad (12)$$

We define the relative variation of window comparator error thresholds as:

$$\delta = |\frac{V_\epsilon(ideal) - V_\epsilon(real)}{V_\epsilon(ideal)}| \quad (13)$$

It is shown in Appendix 6.1 that to achieve a given δ value the minimum amplifier gain required is:

$$A_{min} \approx \frac{V_t}{V_A} \cdot \frac{1}{\mathcal{R} \cdot \delta} \quad (14)$$

For a reasonable accuracy requirement, the amplifier gain does not need to be very high. For example, assuming $V_A \approx V_t$, $\mathcal{R} = 1/5$, and $\delta = 10\%$, the required gain is around 50. Therefore, simple single-stage amplifiers can be used in the biasing circuit. In case that a very small δ needs to be achieved, a cascoded circuit topology can be used to boost the amplifier gain. The voltage at the amplifier output can be derived as:

$$V_g = \frac{V_{in} - V_{sg}}{k \cdot A} + \frac{V_t}{A} \quad (15)$$

This indicates that the voltage swing at the amplifier output is very small, which make it easy to design cascoded amplifiers for this application even with low power supply.

4 Experiment results

The proposed window comparator circuit has been designed and fabricated using a 0.18μ CMOS technology. Transistor sizes used in the design are given in Figure 3. The minimum channel length is avoided to reduce channel length modulation effects. The amplifiers used in the adaptive biasing circuit shown in Figure 4 are Single-stage amplifiers [24]. The design is powered by a single 3.3V power supply and the signal ground level is selected at 1.65V. The layout of the design, as shown in Figure 5, is measured by $140\mu \times 220\mu$. As observed from the plot, there are rooms to further compact the layout by carefully placing all the components.

The experiment setup for testing the fabricated chip is shown in Figure 6. To verify its functionality, two synchronized sinusoidal signals with frequency 200KHz and magnitude 500mV are applied to the comparator inputs. The signal applied to comparator input V_{in2} is centered at the signal ground level 1.65V. The other signal is elevated from the signal ground level by 160mV. Thus, the difference between V_{in1} and V_{in2} of the comparator circuit is always 160mV. The captured oscilloscope display is shown in Figure 7. Since the oscilloscope used in our experiment

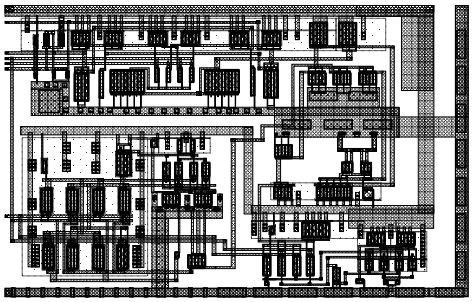

Figure 5. The comparator layout.

has only two channels. One channel of the oscilloscope is used to probe comparator input V_{in1} and the other channel measures the comparator output. When the inputs are close to the signal ground level, the comparator circuit has small error thresholds and the comparator output is logic 0 to indicate the detection of the input difference. However, when the input signals are around their peak values, the comparator error threshold becomes larger and the same input difference is not detected by the comparator circuit.

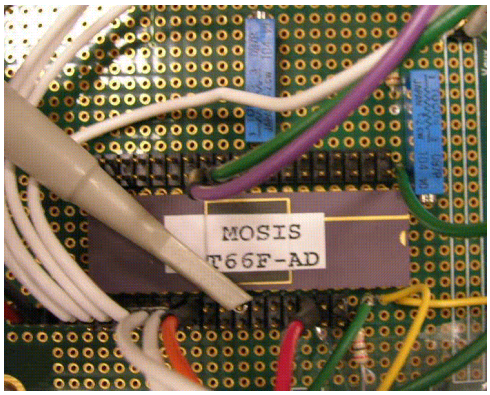

Figure 6. The measurement setup.

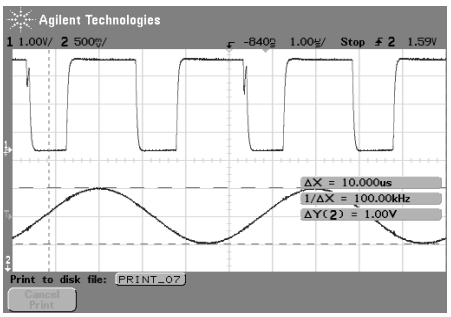

Figure 7. Captured oscilloscope display.

The comparator error thresholds with different input signal levels are also measured. The measurement results are plotted in Figure 8. It clearly indicated that the desired adaptive error threshold is implemented in our design. When the magnitude of the input signal ($|Vin - V_{SG}|$) is smaller than $0.18V$ (V_{in} ranges from $1.47V$ to $1.83V$), the comparator has a constant error threshold of $120mV$ and the realized flat band ratio is 0.36. When the input magnitude is higher than $0.18V$, the comparator has a relative error threshold. The slope of the error threshold is $0.45V/V$. It is observed that the error thresholds in the right side of the relative region are slightly higher than that in the left side of the relative region. This is due to the channel modulation effects of Transistor $N3$ in Figure 3. In the left side of the relative region, the comparator inputs have low voltage and the voltage across the drain and source of $N3$ is also low. Consequently, the drain to source current of $N3$ is reduced, assuming it has finite output resistance due to channel length modulation effects. This can be improved by using a large channel length for $N3$.

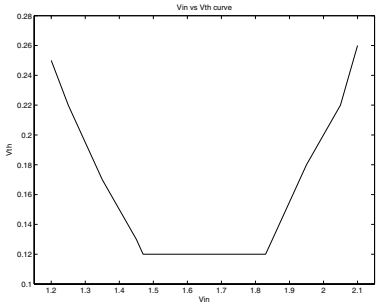

Figure 8. Measured error threshold with different input voltage.

5 Concluding remarks

A window comparator circuit with adaptive error thresholds is presented in this work. Design concerns of the proposed circuits are addressed and analytical equations are developed for helping the selection of component parameters during the design phase. The circuit has been fabricated using a 0.18μ CMOS technology. Measurement results confirmed that the circuit performance meets our design goals. The proposed adaptive error threshold scheme enables window comparators to more effectively distinguish signal differences caused by circuit faults from by tolerable parasitic effects. This feature is very desirable in various analog testing applications.

6 Appendix

6.1 Estimation of the minimum amplifier gain

We use I_{ideal} and I_{real} to represent the ideal and realized biasing currents. Substituting Equations 3 and 11 in the definition of δ, we have:

$$\delta = 1 - \sqrt{\frac{I_{real}}{I_{ideal}}}$$

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$$= \quad 1 - \sqrt{1-\alpha} \tag{16}$$

Move δ to the right-hand side and $\sqrt{1-\alpha}$ to the left-hand side of the equation; perform square operation to both sides of the equation. Then, we have:

$$1 - \alpha = (1-\delta)^2 \tag{17}$$

Substituting Equation 12 into the above equality, we can solve A_{min} as:

$$A_{min} = \frac{2 \cdot V_t}{V_A} \cdot \frac{1}{\mathcal{R} \cdot (2-\delta) \cdot \delta} \tag{18}$$

If δ is small, $2 - \delta \approx 2$. Thus, we have Equation 14.

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