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An Analog Checker with Programmable Adaptive Error Threshold

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Abstract *– This paper presents an analog checker whose error threshold can be adaptively adjusted according to its input signal levels. In addition, the proposed circuit can be programmed to implement different adaptive schemes. Factors that affect the stability and accuracy of the proposed design are investigated. Finally, simulation results are presented.*

Keywords *– adaptive error threshold, analog checker.*

I. INTRODUCTION

Analog checkers are frequently used in analog testing applications. An analog checker has two analog inputs and one digital output. Its output switches from one logic value to the other when the difference between checker inputs exceeds the range of $[-V_\epsilon, V_\epsilon]$, where V_ϵ is referred to as the checker error threshold. Based on the relation between the error threshold and the input signal magnitude, analog checkers can be categorized into three groups, which has *constant*, *relative*, and *adaptive* error thresholds. As illustrated in Figure 1(a), a constant error threshold does not change its value at different input signal levels. In the figure, we assume input signals are centered at the signal ground level V_{sg} and the maximum peak-to-peak value of the inputs is $2 \cdot V_A$, where V_A is the maximum magnitude of the input signal. In the relative error threshold scheme, the error threshold is proportional to the input signal magnitude, as seen in Figure 1(b). Finally, the adaptive error threshold scheme of an analog checker is depicted in Figure 1(c). If the input magnitude is smaller than a pre-selected voltage V_F, the checker has a constant error threshold. However, if the input magnitude is greater than V_F, the checker switches to the relative error threshold mode. For the convenience of discussion, we refer the region that the checker has a constant threshold as the *flat band region*. V_F is called *flat band voltage*, and the ratio of V_F to V_A is defined as *flat band ratio*.

Previously, various analog checkers with constant error threshold have been proposed [1] [2] [3] [4] [5] [7] [8] [6] [9]. Advantages of using relative or adaptive error threshold checker in analog testing and the corresponding circuit implementations are discussed in [5] [11] [12] [13]. In this work, we present a novel design of analog checker with adaptive error threshold scheme. Compared to previous designs, our proposed circuit can be more easily optimized for different parameters associated with the adaptive error threshold scheme. Closed-form design equations are developed for guiding the design process to achieve the specified objectives. In addition, we add programmability to the adaptive error threshold, which makes the design more flexible in analog testing applications.

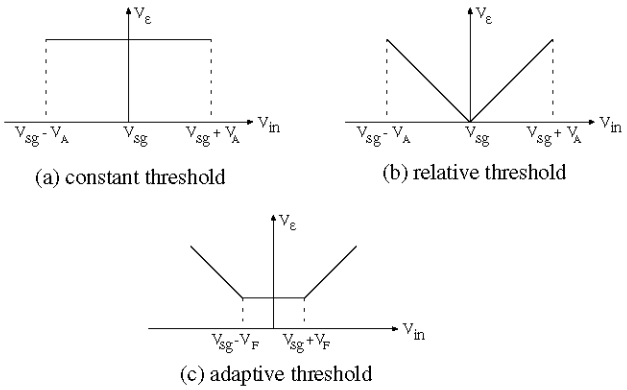

Fig. 1. DIFFERENT ERROR THRESHOLD SCHEMES.

The rest of the paper is organized as follows. Section 2 describes our proposed design. Section 3 discusses design considerations of the circuit. Section 4 presents simulation results and the paper is concluded in Section 5.

II. PROPOSED DESIGN

The proposed circuit consists of two components. The first component is a window comparator circuit whose threshold can be programmed through its biasing current [14]. The second component is an adaptive biasing circuit, whose output current varies according to its input signal level. The design of these two components is described as follows.

A. Comparator circuit

The comparator circuit, as shown in Figure 2, is comprised of a differential input pair and four current mirrors. Transistors N_1 and N_2 constitute the differential pair. PMOS devices $P_1 \sim P_6$, which have the same size, implement two sets of PMOS

current mirrors. Transistors N_4 and N_7, N_5 and N_6, realize two NMOS current mirrors with a current gain of m (the size of N_6 and N_7 is m times larger than that of N_4 and N_5). Assume the current flowing through N_3 is I_b. When both checker inputs are at the same level, N_1, N_2, N_4, N_5, and $P_1 \sim P6$ are in their saturation regions; and all the currents flowing through these transistors are $\frac{I_b}{2}$. N_6 and N_7, working in their linear regions, pull voltages at nodes A and B close to ground, driving the checker output to logic *1*.

When there is a difference at the two inputs, e.g. checker input V_{in1} becomes larger than input V_{in2}. The currents flowing through N_1 and N_2 become $\frac{I_b}{2}+i$ and $\frac{I_b}{2}-i$, where i is the current variation caused by the difference between checker inputs. When $\frac{I_b}{2}+i > m\cdot(\frac{I_b}{2}-i)$, the voltage at node A is pushed close to V_{DD} and node B to ground, hence, the checker output switches to logic *0*.

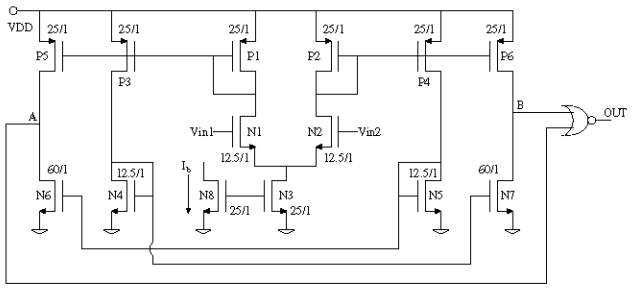

Fig. 2. PROPOSED COMPARATOR SUB-CIRCUIT.

Assuming that I_{DS} and V_{GS} relations of N_1 and N_2 follow the perfect square-law, the checker error threshold can be derived as:

$$V_\epsilon = \sqrt{\frac{I_b}{\mu_n \cdot C_{ox} \cdot (W/L)_{N1,2}}} \cdot \sqrt{1-\sqrt{1-(\frac{m-1}{m+1})^2}} \quad (1)$$

Where μ_n is the carrier mobility; C_{ox} is the transistor unit gate oxide capacitance; and $(W/L)_{N1,2}$ is the size of N_1 and N_2.

The above equation shows that the checker error threshold is proportional to the square root of its biasing current. To achieve the proposed adaptive error threshold scheme, we need a biasing circuit that behaves as follows. When checker inputs are small, (in the *flat-band* region) the biasing circuit has a constant current output. However, when checker inputs are large, the output of the biasing circuit is proportional to the square of the input signal magnitude.

B. Programmable adaptive biasing circuit

The proposed biasing circuit is given in Figure 3. It includes three current generation blocks, labeled as U_1, U_2, and U_3. Transistors M_{16}-M_{30} generate the output biasing current according to the following equation.

$$I_b = \begin{cases} I_{min} & \text{for} \quad V_{sg}-V_f < V_{in} < V_{sg}+V_f \\ w \cdot I_p & \text{for} \quad V_{in} < V_{sg}-V_f \\ w \cdot I_n & \text{for} \quad V_{in} > V_{sg}+V_f \end{cases} \quad (2)$$

Where I_p and I_n are the outputs of U_1 and U_2 respectively. w is the scaling factor that is controlled by programmable inputs a and b. When checker input V_{in} is within *flat band region*, $w \cdot I_p$ (or $w \cdot I_n$) are smaller than I_{min}. In this case, transistor M_{15} will drain current to make sure $I_b = I_{min}$. Hence, the checker has a constant error threshold.

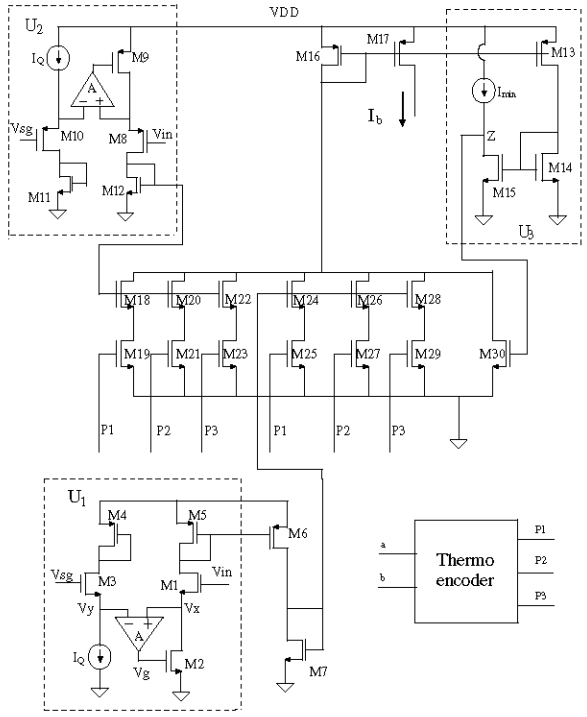

Fig. 3. PROPOSED ADAPTIVE BIASING CIRCUIT.

When V_{in} is greater than signal ground level V_{sg}, M_8 in U_2 is off and M_1 in U_1 conducts current. After V_{in} leaves the flat band region, I_n becomes larger than I_{min}. Subsequently, M_{15} is off and $I_b = I_n$. In the design, I_Q is very small and all the transistors in U_1 are in their saturation regions. Thus, I_b, which is the same as I_{DS1}, can be derived as:

$$I_b = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{(W/L)_{M1}}{1+\frac{1}{A}\cdot\sqrt{\frac{(W/L)_{M1}}{(W/L)_{M2}}}} \cdot (V_{in}-V_{sg}-\frac{V_t}{A})^2 \quad (3)$$

Where V_t is the threshold of MOS devices and A is the gain of the amplifier used in U_1. Ignoring the term of $\frac{V_t}{A}$ in the above equation, the biasing current becomes proportional to the square of the input magnitude $(V_{in}-V_{sg})$. As a result, the

TABLE I
SCALING FACTORS FOR DIFERENT a&b VALUES.

a b	P1 P2 P3	w
0 0	000	0
0 1	001	1
1 0	011	2
1 1	111	3

checker has relative error thresholds. For the same analytical reasoning, the error threshold is proportional to input signal magnitude when V_{in} is smaller than $V_{sg} - V_f$.

The programmability of the biasing circuit is realized by controlling the scaling factor w. A binary to thermometer code encoder circuit converts 2-bit programming inputs a, b to 3-bit control signal P1,P2, and P3, which control the status of M_{19},M_{21},M_{23},M_{25},M_{27} and M_{29}. The weight factor corresponding to different inputs a and b are shown in Table 1. Note that when a=0 and b=0, the biasing current output becomes independent of U_1 and U_2 outputs. Thus the checker circuit has a constant error threshold.

III. DESIGN CONSIDERATIONS

This section investigates how amplifier gain affects the accuracy of the realized error threshold and addresses the stability concern of the proposed biasing circuit.

Amplifier gain requirement: if the $\frac{V_t}{A}$ term in Equation 3 is not completely ignored, the expression of I_{DS1} can be rewritten as:

$$I_{DS2} \approx \zeta \cdot [(V_{in} - V_{sg})^2 - 2 \cdot (V_{in} - V_{sg}) \cdot \frac{V_t}{A}] \quad (4)$$

where

$$\zeta = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{(W/L)_{M1}}{1 + \frac{1}{A} \cdot \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M2}}}} \quad (5)$$

Note that the square term $(\frac{V_t}{A})^2$ is omitted due to its small value. Inside the bracket at the right-hand side of Equation 4, the first term represents the ideal value that will result in a perfect current output; the second term represents a linear error added to the ideal value. Thus, the relative error α of the biasing circuit output can be written as:

$$\alpha \approx \frac{2 \cdot V_t}{A \cdot (V_{in} - V_{sg})} \quad (6)$$

approximated from its definition given by:

$$\alpha = \frac{|I_b(ideal) - I_b(real)|}{|I_b(ideal)|} \quad (7)$$

It is easy to see that α has its largest value when the input signal is just beyond the flat band region. Thus, the largest α can be written as:

$$\alpha_{max} = \frac{2 \cdot V_t}{V_A} \cdot \frac{1}{A \cdot \mathcal{R}} \quad (8)$$

We define the relative variation of analog checker error thresholds as:

$$\delta = |\frac{V_\epsilon(ideal) - V_\epsilon(real)}{V_\epsilon(ideal)}| \quad (9)$$

From Equation 1 and 8, we find that to achieve a given δ value the minimum amplifier gain is:

$$A_{min} \approx \frac{V_t}{V_A} \cdot \frac{1}{\mathcal{R} \cdot \delta} \quad (10)$$

For a reasonable accuracy requirement, the amplifier gain does not need to be very high. For example, assuming $V_A \approx V_t$, $\mathcal{R} = 1/5$, and $\delta = 10\%$, the required gain is around 50. Therefore, simple single-stage amplifiers can be used in the biasing circuit. In case that a very small δ needs to be achieved, a cascoded circuit topology can be used to boost the amplifier gain. The voltage at the amplifier output is very small, which make it easy to design cascoded amplifiers for this application even with low power supply.

Circuit stability concern: unlike the window comparator circuit, the biasing circuit contains closed feedback loops. Thus, circuit stability has to be considered. For the simplicity of discussion, we assume that a single-stage differential pair is used as the amplifier in block U_1 of the biasing circuit. The resultant feedback loop is sketched in Figure 4. This circuit can be treated as a two-stage amplifier configured as a unity-gain buffer. Note that the above analysis ignores the effect of M_3 in the biasing circuit. M_3 can be modeled by an impedance load as drawn by dash lines in Figure 4. The value of the impedance is around $1/g_{m3}$, where g_{m3} is the transconductance of M_3. Adding this impedance load to the circuit decreases the feedback factor of the loop and makes the circuit more stable. Its input devices are M_{a1} and M_{a2}; its output is at node N_3. Note that V_{in} signal is treated as a biasing voltage in this analysis. This circuit has a single dominant pole resulted from the parasitics at node N_2. The two non-dominant poles caused by parasitics at nodes N_1 and N_3 are far away from the dominant pole because of the low impedance at N_1 and N_3 (the impedance at N_1 and N_3 are around $1/g_m$, where g_m is the transconductance of M_{a3} or M_1, respectively). Therefore, the phase margin of the equivalent amplifier is fairly high and the circuit is stable even without adding phase compensation components. This conclusion is confirmed by our simulation results. If a cascoded topology is used, the impedance at N_2 will be even higher and the dominant pole will be further separated from non-dominant poles. Hence, using a cascoded topology will enhance the stability of the biasing circuit.

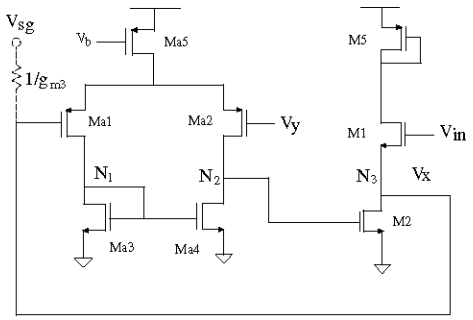

Fig. 4. FEEDBACK LOOP IN THE BIASING CIRCUIT.

IV. SIMULATION RESULTS

The proposed circuits have been implemented using a 0.18μ CMOS technology. Transistor sizes used in the design are given in the schematics. Single-stage differential amplifiers [10] are used in the adaptive biasing circuit. The design requires a single 3.3V power supply and the signal ground level is 1.65V.

Figure 5 shows the realized error thresholds for different a and b values. As the programmable inputs (a and b) vary, the flat band ratios and slopes of the error threshold in the relative regions change correspondingly. When both a and b are zero, the checker has a constant error threshold.

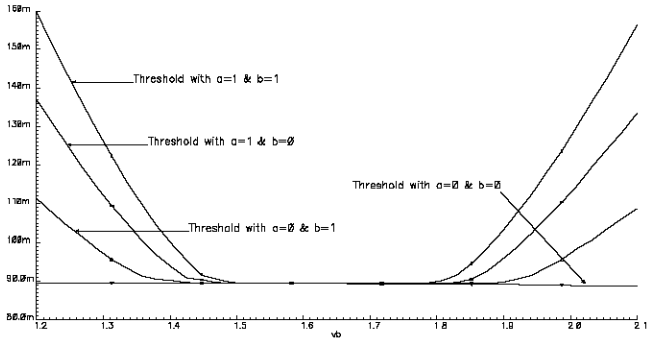

Fig. 5. SIMULATED ERROR THRESHOLDS.

Figure 6 shows a transient simulation result in the configuration of $a = 1$ and $b = 1$. The inputs of the checker are two sinusoidal signals, which are centered at the signal ground level with the same magnitude, frequency, and phase. The offset voltage of V_{in1} is 150 mV higher than that of V_{in2}. Input V_{in1} is also connected to the biasing circuit to control the biasing current. It shows that this difference is detected by the checker (checker output is logic 0) when the signal values are close to the signal ground level. When the inputs are close to their peak values, the same difference is ignored by the checker due to its increased error threshold.

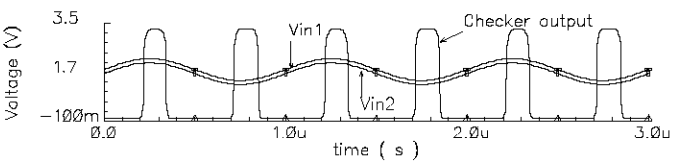

Fig. 6. SIMULATION RESULT OF TRANSIENT ANALYSIS.

V. CONCLUSIONS

An analog checker with adaptive error thresholds is developed. Factors that affect the accuracy of the checker error thresholds are identified and analytical equations are derived. The proposed checker is capable of more effectively detecting circuit faults in analog online testing applications.

[1] J. E. Franca, "Analogue-Digital Window Comparator with Highly Flexible Programmability"*IEE Electronics Letters*, pp. 2063-2064, 1991

[2] Y. Zhang and M. W.T.Wong, "Self-Testable Full Range Window Comparator," Proc *Proc. Region 10 TENCON 2004*, vol. 4, pp. 262-265, 2004

[3] M. Lubaszewski and V. Kolarik and S. Mir and C. Nielsen and B. Courtois, "Mixed-Signal Circuits and Boards for High Safety Applications," *Proc. European Design and Test Conference*, pp. 34-39, 1995.

[4] V. Kolarik and M. Lubaszewski and B. Courtois, "Designing Self-Exercising Analogue Checkers," *Proc. VLSI Test Symposium*, pp. 252-257, 1994.

[5] V. Kolarik and S. Mir and M. Lubaszewski and B. Courtois, " Analog Checkers with Absolute and Relative Tolerances," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 14, issue. 5, pp 607-612, 1995.

[6] D. D. Venuto and M. J. Ohletz and B. Ricco, "Automatic Repositioning Technique for Digital Cell Based Window Comparators and Implementation within Mixed-Signal DfT Schemes," *Proc. Intl. Symp. on Quality Electronic Design*, pp. 431-437, 2003.

[7] D. D. Venuto and M. J. Ohletz and B. Ricco, "Testing of analogue circuits via (standard) digital gates," *Proc. Intl. Symp. on Quality Electronic Design*, pp. 112-119, 2002.

[8] D. D. Venuto and M. J. Ohletz and B. Ricco, "Digital Window Comparator for mixed-signal IC's design for testability," *Journal of Electronic Testing: Theory and Applications*, vol. 18, number. 2, pp. 121-128, 2002.

[9] D. D. Venuto and M. J. Ohletz, "On-Chip Test for Mixed-Signal ASICs using Two-Mode Comparators with Bias-programmable reference voltages," *J. of Electronic Testing: Theory and Applications*, vol. 17, pp. 243-253, 2001.

[10] P. Allen and D. Holberg,"CMOS Analog Circuit Design," *Oxford University Press*, 2002.

[11] H. Stratigopoulos and Y. Makris, " An Analog Checker with Dynamically Adjustable Error Threshold for Fully Differential Circuits," *Proc. VLSI Test Symposium*, pp. 209-214, 2003.

[12] H. Stratigopoulos and Y. Makris, "An Analog Checker with Input-Relative Tolerance for Duplicate signals," *Journal of Electronic Testing: theory and applications*, vol. 20, pp. 479-488, 2003.

[13] H. Stratigopoulos and Y. Makris, "An Adaptive Checker for the Fully Differential Analog Code," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1421-1429, 2006.

[14] A. Laknaur and H. Wang, "Design of window comparators for integrator-based capacitor array testing circuits," *Int. Symposium on Quality Electronic Design*, 2006.