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A Low Power Current Sensing Scheme for CMOS SRAM

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A Low Power Current Sensing Scheme for CMOS SRAM

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Abstract

A low power current sensing scheme for CMOS SRAM is presented in this paper. The proposed scheme includes a modified current conveyor as the column selector, and a new designed low power current sense amplifier to sense the small differential current signals in data lines. The output of the sense amplifier is fed to a clock control RS latch both for power reduction and longer output valid time. This current sensing scheme is clocked asynchronously and the timing control circuits are also discussed. Simulation results show that a sensing speed with 3ns less is achieved by this scheme and the sensing speed is insensitive to both bit line and data line capacitances.

1: Introduction

As the density of memory devices increase, inevitably the associated parasitic capacitances also increase. The larger bit line and data line capacitances constitute a major bottleneck in achieving higher sensing speed in high capacity memory chips. A promising solution to this problem is employing current-mode rather than conventional voltage-mode signal transporting technique in memory design [1]. The key to this approach is the using of current-mode circuits, current-mode column selector and current-mode sense amplifier, at the ends of bit line and data line, respectively. In previous works, two-input, two-output MOS current conveyor (Fig. 1) has been proven to be suitable for implementing the required current-transporting function as a current-mode column selector [1], and this circuit was adopted in some later works [2-3]. In these works, the correct function of column selector was based on an assumption which can not be satisfied in practice. In this paper, this defect is debugged and a solution is proposed.

The cross-coupled latch sense amplifier (Fig. 2) has been successfully used in current-mode sensing scheme with high sensing speed [2, 4, 5]. This type of amplifier operates in two phases: equalization period and sensing period. Unfortunately, in the previous designs the high speed operation always means bigger size for load transistors, M6 and M7 in Fig. 2, and consequently large DC current sinks to ground through M1-M7 during equalization period. Moreover, because the inputs of inverter INV1 and INV2 are not typical CMOS level voltage during equalization, the inverters also contribute to more power consumption. In the proposed scheme, a new current-mode sense amplifier is employed. It has a lower equalization current and the output inverters are replaced by a clock control RS latch both for power consumption reduction and longer data valid time. The sense amplifier and RS latch are clocked asynchronously, the timing control scheme is also discussed in this paper.

Section 2 describes the new sensing scheme and indicates the inherent low power advantage. Section 3 illustrates the operation of the circuits with simulation results. The paper is concluded in section 4.

2: Circuit description

2.1: Column selector

A previous current sensing scheme is shown in Fig. 3 [2]. The current conveyor consisting of M1-M4 is used as the column selector in Fig. 3. When a cell is accessed and the column select signal CS is low to turn on M3 and M4, the differential current signals will flow from bit lines to data lines. Meanwhile, the current difference will cause a voltage difference between nodes A and B as shown in Fig. 3. From voltage-mode circuit viewpoint, M1, M3 and M2, M4 constitute two MOS amplifiers (as shown in Fig. 4) and their gains are proportional to the equivalent resistance of M3 and M4. The two amplifiers are connected in positive feedback in the current conveyor circuit. At the end of read operation, column select signal CS switches from low to high and results in the increase of equivalent resistance of M3 and M4 as well as the gains of the MOS amplifiers consisting of

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M1-M4. The voltage difference between nodes A and B will be enlarged by the high efficient amplifiers after read operation, instead of being eliminated automatically. Simulation with varied transistor sizes of M1-M4 shows that this unbalancing state is mostly locked by the cross-coupled transistors M1 and M2, even when the column select signal CS becoming low again. Hence, the following correct read operation is prohibited by this locked unbalancing state. In the previous analysis, a voltage balance between nodes A and B is assumed before a read operation. This case may be true in the first read operation, but mostly is not true in the following operation. In order to eliminate the unbalancing state, an equalization device M5 is added to the current conveyor as shown in Fig. 5. M5 is off during the read operation. When the sensing operation is complete, M5 is on to equalize the voltage of nodes A and B.

2.2: Sense amplifier

The current sense amplifier (shown in Fig. 6) used in the proposed scheme has a lower power consumption and a higher sensing speed than those of recently proposed [2, 4, 5]. The new circuit also operates in two periods: equalization period and sensing period. In equalization period, M6 and M9 turn off, small size transistor M7 and M8 are the load transistors of sense amplifier. Because of the high load resistance caused by the small size transistors, the DC current flowing through the sense amplifier is reduced. Since the sense amplifier dissipates little power in its sensing period, the whole power consumption of sense amplifier decreases apparently with the equalization current reducing. In sensing period, large size transistors M6 and M9 turn on so that the amplifier has a high current draining capability to enhance the sensing speed. In addition, the higher load resistance in equalization period conduces to constitute a bigger voltage difference between nodes C and D, which is caused by the differential current signals I1 and I2, at the beginning of sense operation. This is another speed enhancing factor for the proposed sense amplifier. With the same input current signals and same transistor sizes, except the size of load transistors, the new designed sense amplifier is compared with the previous one (shown in Fig. 2) in the aspects of power consumption and sensing delay by HSPICE simulation. The results are shown in Fig. 7. For the previous amplifier, the size of load device means the size of M5 and M6 in Fig. 2. For the new one, the size of load device is the sum of M6 and M7, or the sum of M8 and M9. In the simulation, the sizes of M7 and M8 are fixed at 2.4/2.4 and the sizes of M6 and M9 change from 2.4/2.4 to 21.6/2.4.

2.3: Clock control RS latch

A clock control RS latch which is shown in Fig. 8 is connected to the outputs of sense amplifier in this current sensing scheme. After sensing operation is complete, the clock control signal EN is high, M5 and M6 are on, the amplifier output is loaded into the RS latch. In sense amplifier equalization period, EN is low, the previously loaded data is kept by the cross-coupled transistors M1 and M2. Although the amplifier outputs are not typical CMOS level voltage in this time, there is no static current dissipation by the RS latch because M5 and M6 are switched off. Compared with the previous scheme in which inverters are used as the following stage of sense amplifier [2,3], the new scheme avoids the static power consumption caused by the untypical CMOS level amplifier outputs in equalization period, it also has a longer data valid time.

2.4: Timing control scheme

The proposed current sensing scheme is shown in Fig. 9, the sensing operation is clocked by address transition detection signal ATD [6] and a sense clock signal CLOCK. Before the sensing operation there is no new address transition, both ATD and CLOCK are low, consequently, EQ is low and EN is high to enable the column selector equalization device and RS latch, respectively. When a new address arrives, address transition detection circuit delivers a positive pulse to set the negative edge triggered toggle-flip-flop, EQ becomes high and turns off column selector equalization device before column select signal CS switching to low. Meanwhile, CLOCK switches to high to equalize the sense amplifier and later it becomes low again to start the sense operation. During the sense amplifier equalization, transistors M1 and M2 in sense complete detection circuit (SCDC) [7] both are on so that the sense complete detection signal SCDS is high. The high level SCDS keeps RS latch clock signal EN to low. In the mean time, the latched data is the previous amplifier output. After the new sense operation is complete, either M1 or M2, in SCDC, turns off and SCDS becomes to low, which switches EN to high and thus the RS latch is enabled to load the output of sense amplifier. The negative SCDS edge also overturns the toggle-flip-flop with the result of EQ becoming low. Hence the voltage difference between the internal nodes of column selector is eliminated and the whole circuit is ready for the next read operation.

3: Simulation results

The proposed current sensing scheme has been implemented based on 1.2μ CMOS technology and verified by HSPICE simulation. Shown in Fig. 10 are the waveforms of simulation. The first illustration shows the ATD signal, column selector equalization signal EQ and the voltage changing of the internal nodes of the current-mode column selector. The CLOCK signal and the output of sense amplifier are presented in the second picture. The switching of RS clock signal EN, SCDS and the output of RS latch are described in the third picture. With 4 pf capacitive loads in both bit line and data line, the average current consumption of this current sensing scheme is 0.68mA. Under the same condition, the power consumption of the previous scheme [2] is 0.87mA. Because the current sensing technique is employed in this scheme, the sensing delay is insensitive to both bit line and data line capacitances. The sensing delay (from CLOCK signal to the output of RS latch) with different bit line and data line capacitances are shown in Fig. 11.

4: Conclusion

In this work, efforts have been done to reduce the equalization current of cross-coupled latch sense amplifier. Because this equalization current is the main cause of static power consumption for this type of sense amplifier, this power saving step is effective. Some speed enhancement is also obtained by this measure. A clock control RS latch is introduced to screen out the untypical CMOS level output voltage of the sense amplifier, which usually causes the static power consumption in its following stage. A modification to the current-mode column selector is proposed to eliminate the unbalancing state between the internal nodes of MOS current conveyor after read operation. Employing above circuits, a low power current sensing scheme is developed. Its sensing speed is less than 3ns and insensitive to both bit line and data line capacitances.

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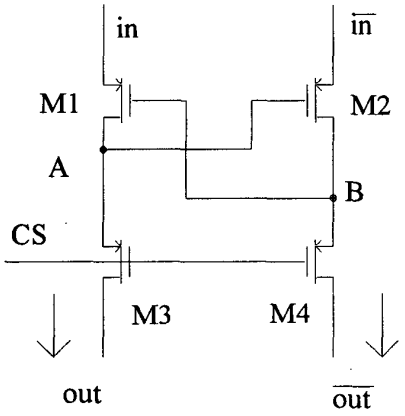

Fig. 1 Current conveyor.

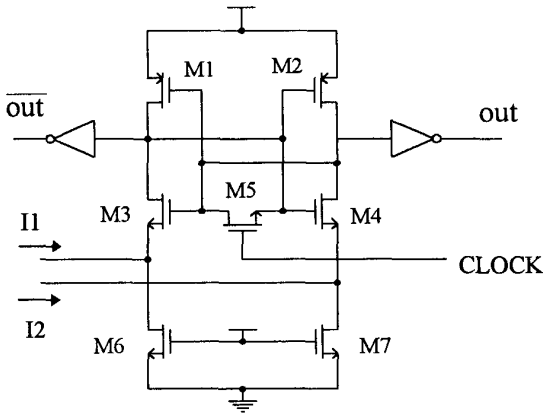

Fig. 2 Cross-coupled latch sense amplifier.

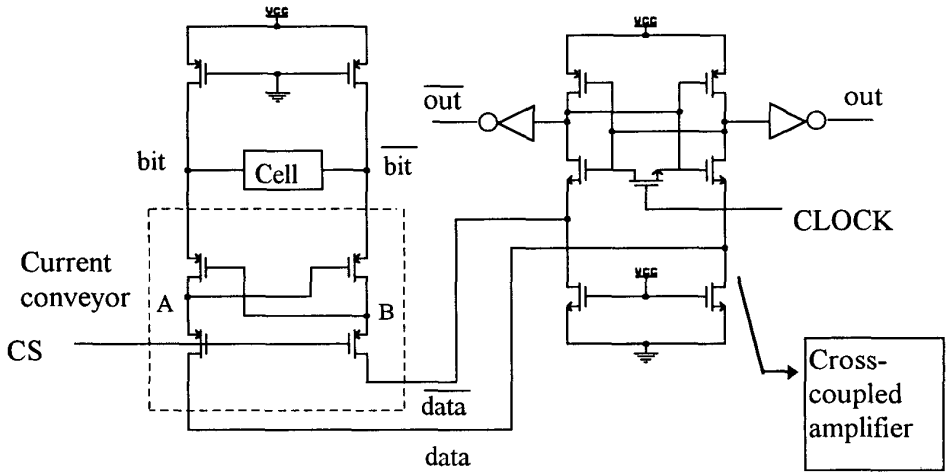

Fig. 3 Previous proposed current sensing scheme.

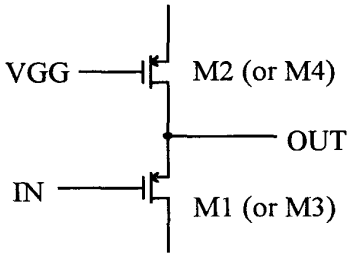

Fig. 4 MOS amplifier.

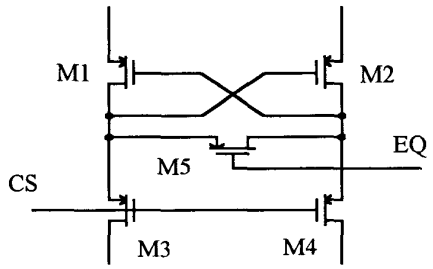

Fig.5 Modified column selector.

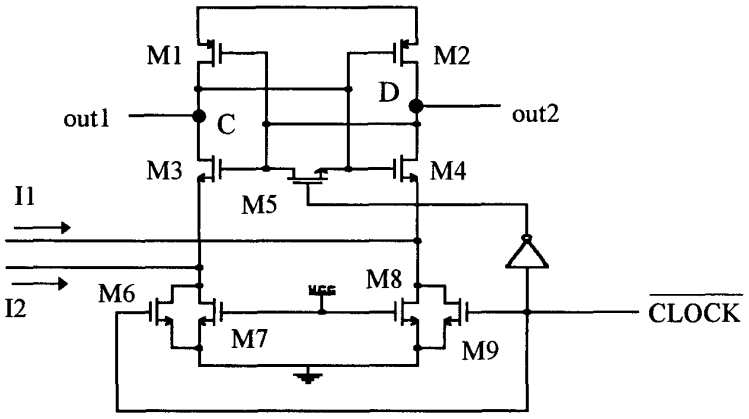

Fig. 6 Proposed current sense amplifier.

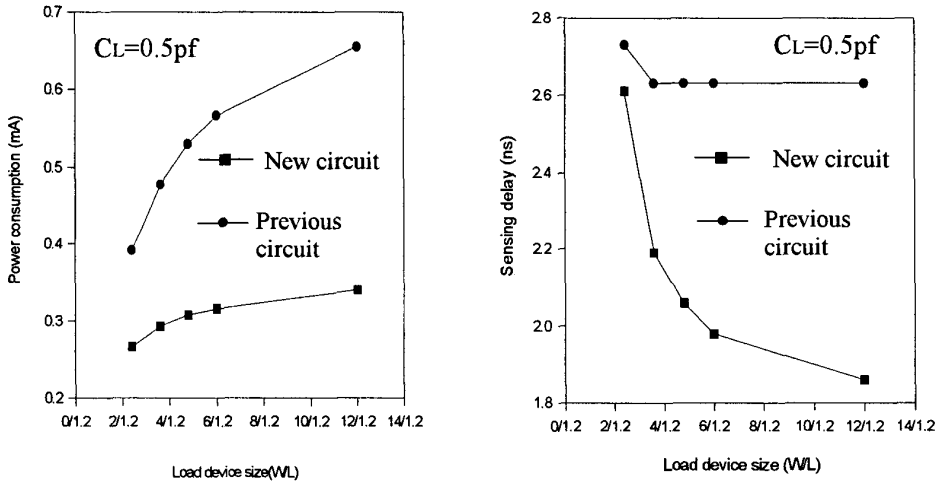

Fig. 7 Power consumption and sensing delay of the two current sense amplifiers.

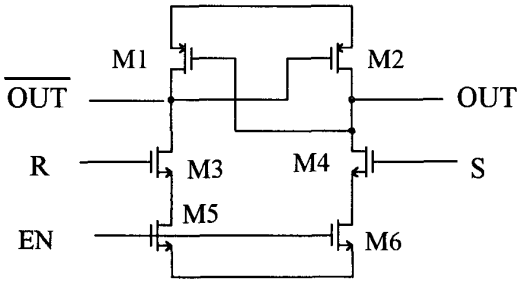

Fig. 8 Clock control RS latch.

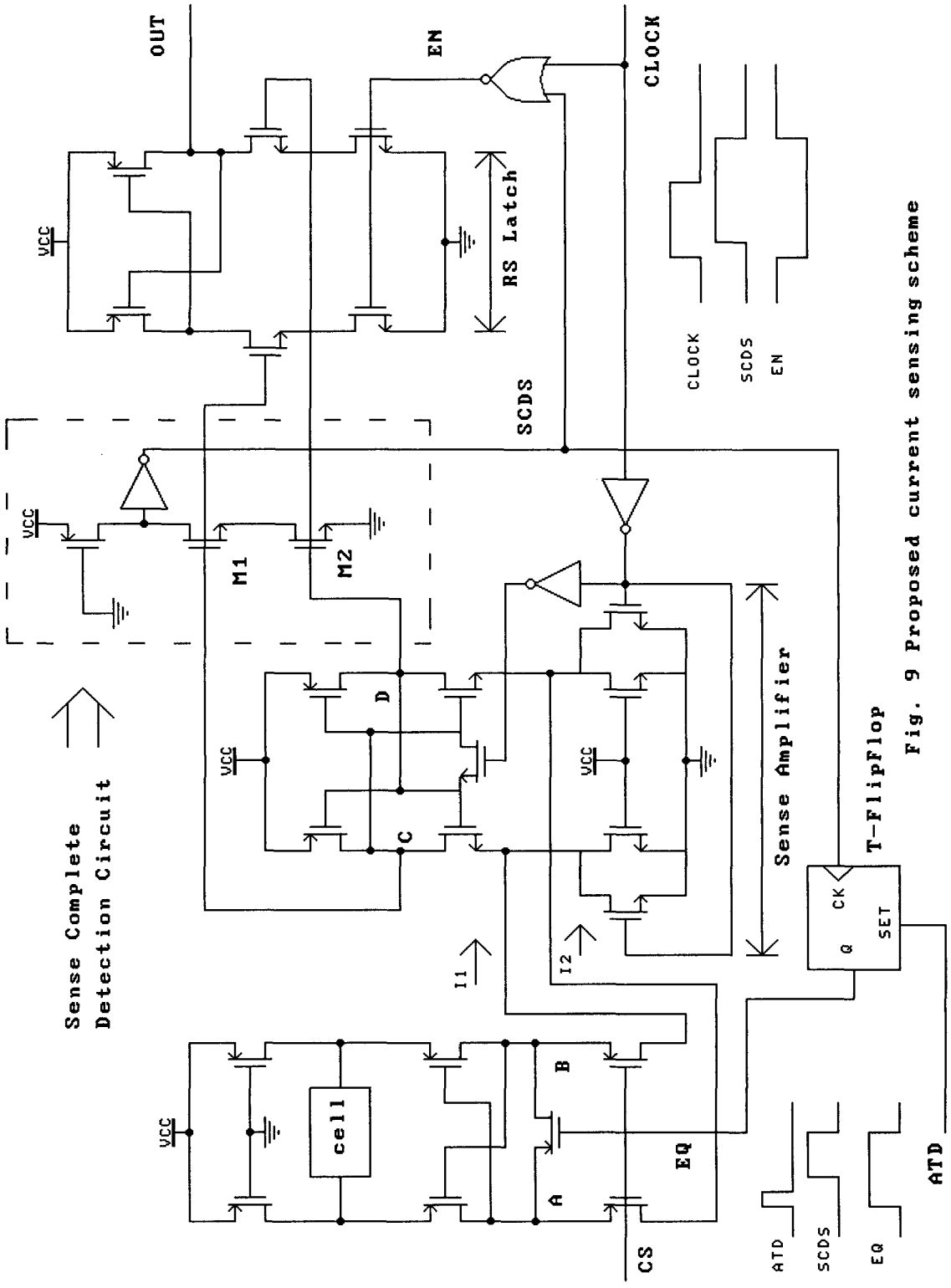

Fig. 9 Proposed current sensing scheme

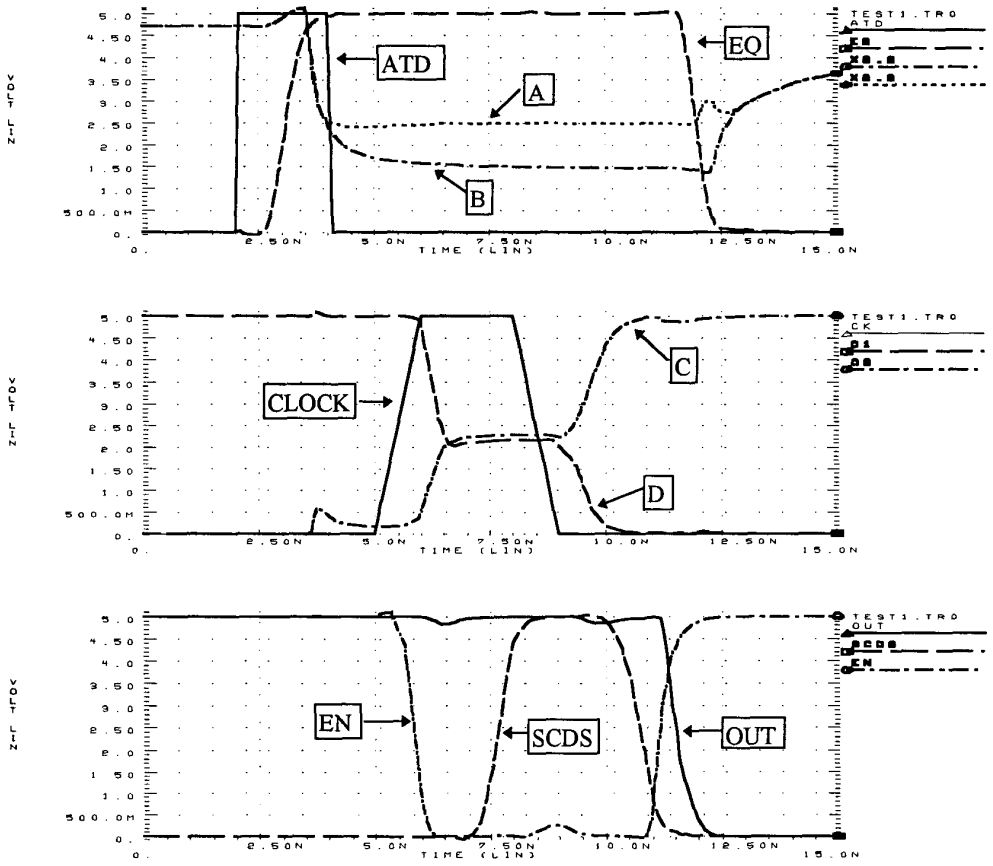

Fig. 10 Waveforms of simulation result.

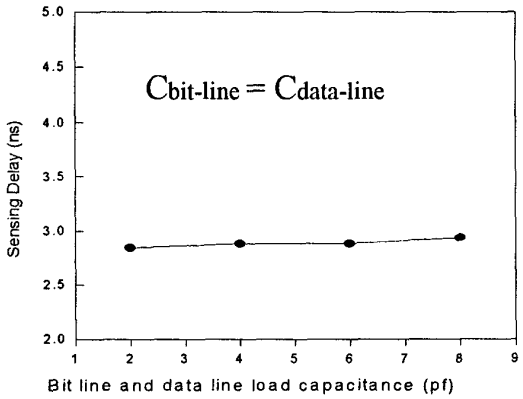

Fig. 11 Sensing delay with different bit line and data line capacitance.

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