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Single-carrier Modulation for Neutral-Point-Clamped Inverters in Three-Phase Transformerless Photovoltaic Systems

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***Abstract*—Modulation strategy is one of the most important issues for three-level neutral-point-clamped inverters in three-phase transformerless photovoltaic systems. A challenge for modulation is how to keep the common-mode voltages constant to reduce the leakage currents. A single-carrier modulation strategy is proposed. It has a very simple structure, and the common-mode voltages can be kept constant with no need of complex space vector modulation or multicarrier pulsewidth modulation. Experimental results verify the theoretical analysis and the effectiveness of the presented method.**

***Index Terms* —Modulation, neutral-point-clamped inverter, common-mode voltage, transformerless photovoltaic system**

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I. INTRODUCTION

Transformerless photovoltaic (PV) inverters have been received more and more attention due to cost and size reduction, as well as efficiency improvement, compared with the conventional transformer ones [1-11]. A number of technical challenges may arise with increased grid-connected transformerless PV systems. One of the most important issues is how to reduce or eliminate the leakage currents through the parasitic capacitor between the PV array and the ground. For three-phase neutral-point-clamped (NPC) transformerless PV systems, the modulation strategy should be carefully designed to retain the constant common mode voltages (CMV) to eliminate the leakage currents [3]. In general, there are two typical modulation strategies for three-phase NPC inverters. One is space vector modulation (SVM), and the other is the multicarrier pulsewidth modulation (PWM). SVM is more favorable from the viewpoint of the switching pulse pattern study, but it requires complex implementation such as switching vector selection, duty cycles calculation and vector sequence arrangement [12]. On the other hand, the multicarrier PWM is more attractive for implementation because it only needs to compare the reference and carrier signal to generate the switching gating signals. Cavalcanti, et al [3] has presented an interesting SVM method to keep CMV constant by using only the medium vectors and the zero vector to comprise the reference vector. In practice, however, its implementation is not an easy task as discussed before. For the multicarrier PWM solution, the common voltage problems can be mitigated by rearranging the multicarrier according to the vector region [13], which increases the computational burden. In order to overcome the abovementioned limitation, a single-carrier modulation strategy is proposed. It has a very simple structure, and the constant CMV can be achieved, with no need of complex SVM or multicarrier PWM.

II. PROPOSED METHOD

The schematic diagram of the three-phase NPC inverter is shown in Fig.1, where the system common mode voltage V_{CM} is defined as [3]

$$V_{\mathrm{CM}} = \frac{V_{\mathrm{AN}} + V_{\mathrm{BN}} + V_{\mathrm{CN}}}{3} \tag{1}$$

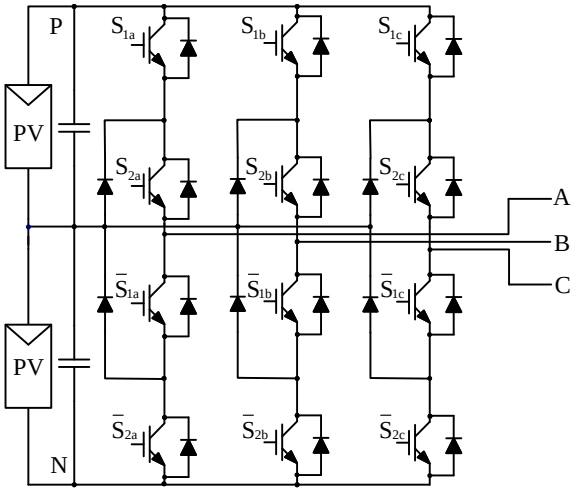


Fig. 1. Diode-clamped three-level inverter.

According to [3], V_{CM} should be kept constant as $V_{PN}/2$ to eliminate the leakage current. Considering that V_{iN} (i=A, B, C) has three possible values (V_{PN}, $V_{PN}/2$, 0), there are two ways to achieve the constant CMV, as listed in Table I.

Case I: Switching strategy A

When the outer switches of S_{1a}, $\bar{S}_{2a}$, S_{1b}, $\bar{S}_{2b}$, S_{1c}, $\bar{S}_{2c}$ are off, and other inner switches are on, $V_{AN}=V_{BN}=V_{CN}=V_{PN}/2$. Therefore, the CMV defined by (1) is constant as $V_{PN}/2$ [3].

Case II: Switching strategy B

For the constant CMV of $(V_{AN}+V_{BN}+V_{CN})/3=V_{PN}/2$ [3], another switching strategy is presented. Considering that three possible values of (V_{PN}, $V_{PN}/2$, 0) of V_{iN} (i=A, B, C), the switch states should be configured to ensure that three possible values are evenly distributed among V_{AN}, V_{BN}, and V_{CN}, as listed in Table I. For example, When the switches of $\bar{S}_{1a}$, $\bar{S}_{2a}$, S_{1b}, $\bar{S}_{2b}$, S_{1c}, S_{2c} are off, and other switches are on, $V_{AN}=V_{PN}$, $V_{BN}=V_{PN}/2$ and $V_{CN}=0$, as shown in line 3 of Table I. Therefore, the constant CMV of (1) can be achieved. In the same way, the other five switching states listed in Table I can achieve the constant CMV as well.

In order to achieve the abovementioned switching strategy A and B, a new single-carrier modulation strategy is presented in Fig.2, where the zero sequence signal is added to the reference signals to increase the voltage utilization.

Detailed information about zero sequence signal calculator can be found in [14] (See Part D of Section IV). The modulation signals of v_a, v_a and v_c are compared with the carrier to generate the logic (0 or 1) signals of SA, SB and SC. The simple logic circuits behind three comparators are used to generate the specified gating signals to keep the constant CMV, regardless of output logic (0 or 1) of three comparators.

Note that there are eight possible states for SA, SB and SC, as listed in Table I. Take the line 2 for example, when SA= SB=SC=0, the switching states after the simple logic circuits in Fig.2 will be determined as follows: S_{1a}, $\bar{S}_{2a}$, S_{1b}, $\bar{S}_{2b}$, S_{1c}, $\bar{S}_{2c}$ are off, and other inner switches are on. This switching state is in good agreement with Case I (Switching strategy A). Therefore, the CMV is kept constant as $V_{PN}/2$. In the similar manner, the CMV can be achieved by other seven switching states, as listed in Table I.

In summary, it is clear that the constant common mode voltage can be achieved with the proposed single-carrier modulation strategy.

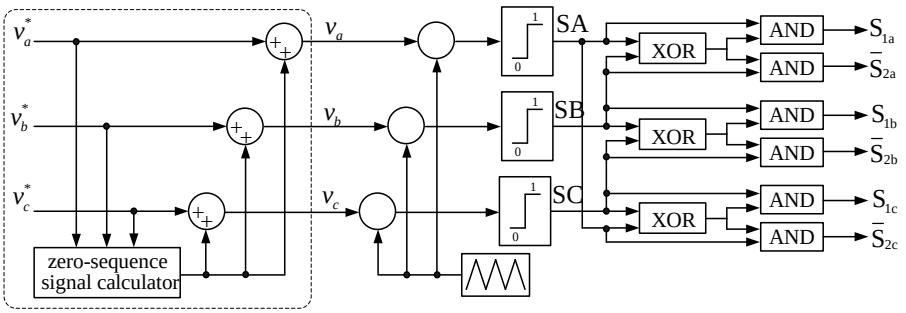


Fig. 2. Proposed single-carrier modulation strategy.

TABLE I

DEVELOPMENT OF SINGLE-CARRIER MODULATION FOR CONSTANT COMMON VOLTAGE

SA	SB	SC	S_{1a}	$\bar{S}_{2a}$	S_{1b}	$\bar{S}_{2b}$	S_{1c}	$\bar{S}_{2c}$	V_{AN}	V_{BN}	V_{CN}	V_{CM}
0	0	0	0	0	0	0	0	0	$V_{PN}/2$	$V_{PN}/2$	$V_{PN}/2$	$V_{PN}/2$
1	0	0	1	0	0	0	0	1	V_{PN}	$V_{PN}/2$	0	$V_{PN}/2$
1	1	0	0	0	1	0	0	1	$V_{PN}/2$	V_{PN}	0	$V_{PN}/2$
0	1	0	0	1	1	0	0	0	0	V_{PN}	$V_{PN}/2$	$V_{PN}/2$
0	1	1	0	1	0	0	1	0	0	$V_{PN}/2$	V_{PN}	$V_{PN}/2$
0	0	1	0	0	0	1	1	0	$V_{PN}/2$	0	V_{PN}	$V_{PN}/2$
1	0	1	1	0	0	1	0	0	V_{PN}	0	$V_{PN}/2$	$V_{PN}/2$
1	1	1	0	0	0	0	0	0	$V_{PN}/2$	$V_{PN}/2$	$V_{PN}/2$	$V_{PN}/2$

Note that the switching signals of each phase, e.g. S_{1i} and $\bar{S}_{2i}$ (i=a, b, c), have the relationship with the other phase due to the logic circuits in Fig.2. This will lead to 30-degree phase shift from the modulation signal. A simple solution is to replace the previous modulation signals with the line-to-line reference signals, as shown in Fig.3, where the coefficient 'K' is used to avoid overmodulation (e.g. $K=1/\sqrt{3}$).

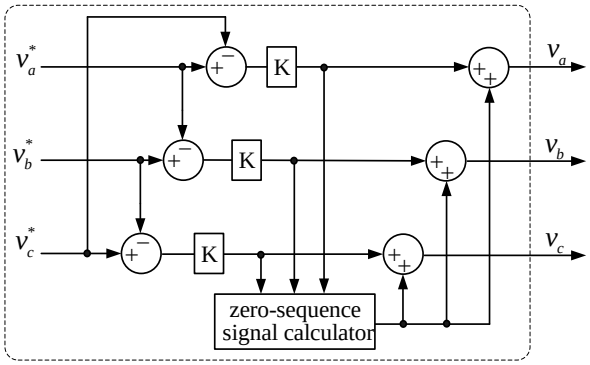
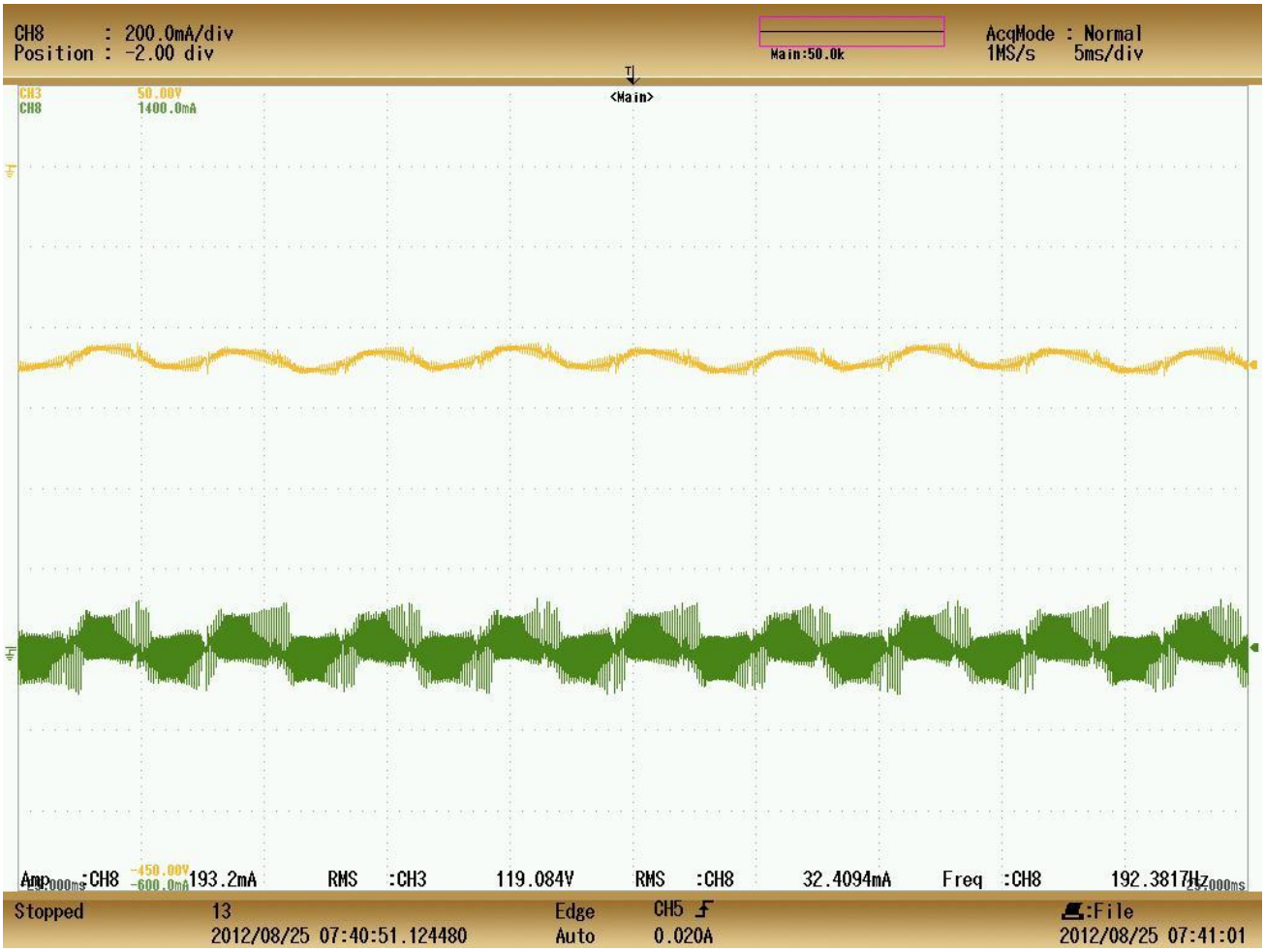


Fig. 3. 30-degree phase shift compensation strategy.

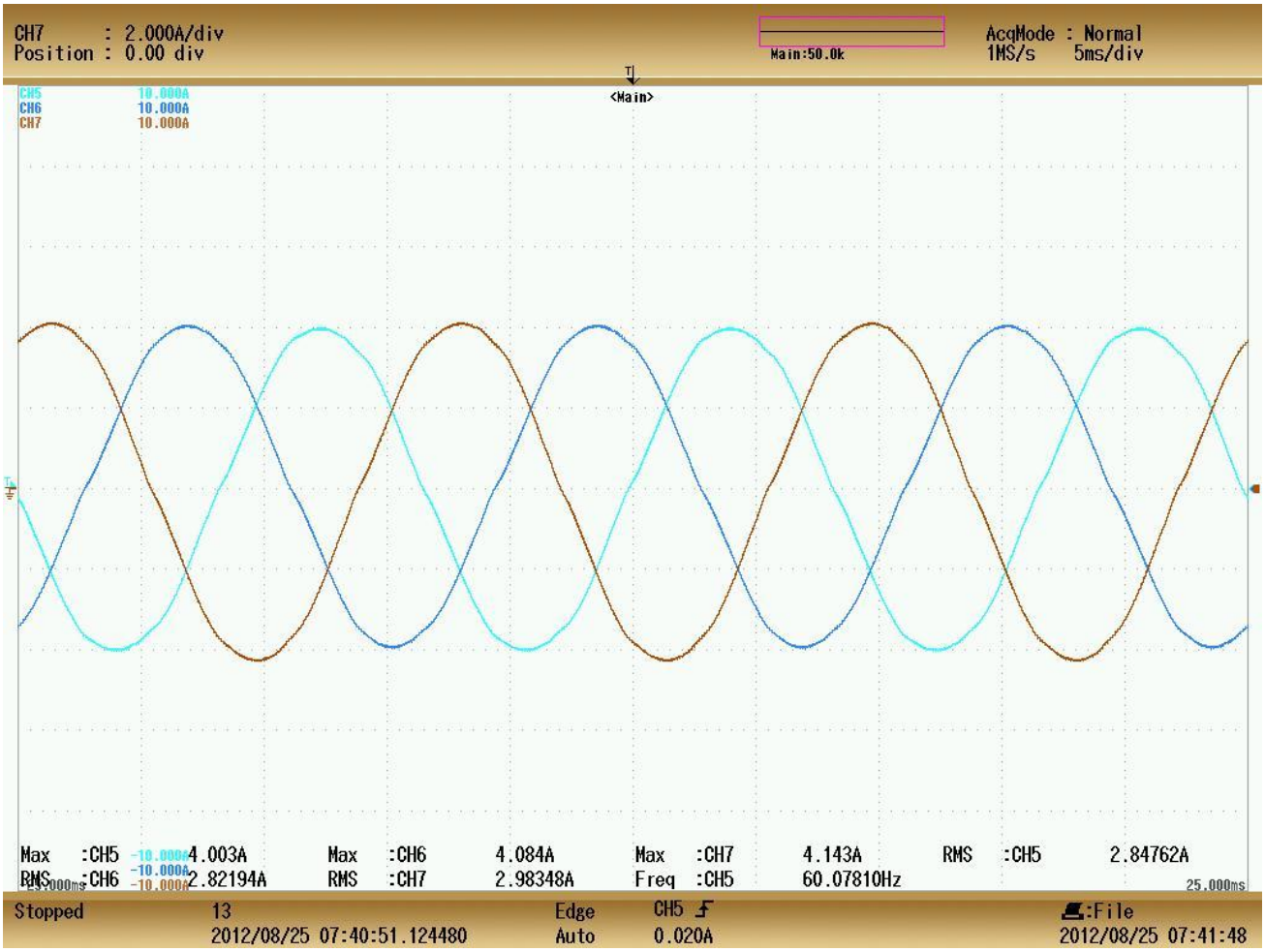
To evaluate the performance of the proposed modulation method, the experimental tests are carried out. The system parameters are switching period is 200us, dead time is 3.54us, load inductance is 5mH, load resistance is 17Ω, dc link voltage is 240V, modulation index is 0.9, parasitic capacitance is 220 nF, and ground resistance is15Ω. The simple logic circuits in Fig.2 are implemented with analogy circuits (SN7486 for XOR and SN7408 for AND).Note that this letter focused on the switching strategy. Other issues such as the grid synchronization [15] and anti-islanding protection [16]

are beyond the scope of this paper.

The experimental results are shown in Fig.4. From Fig.4 (a), it can be observed that the common mode voltage is kept almost constant with the value (119.084V) approximate equal to V_{PN} /2, which is in good agreement with the above theoretical analysis. The rms value of the leakage current is about 32.41mA, which is well below the VDE 0126-01-01 standard requirement of 300 mA. Fig. 4(b) shows the inverter output current waveform. In summary, the proposed modulation strategy will be very attractive for both sinusoidal output current and leakage current mitigation



(a)



(b)

Fig. 4. Experimental Results, (a) Common mode voltage and leakage current; (b) Inverter output currents

IV. CONCULSION

A single-carrier modulation strategy has been presented for three-level neutral-point-clamped inverters in three-phase transformerless PV systems. It has the interesting feature that, with no need of complex space vector modulation or multicarrier pulsewidth modulation, the system common mode voltage can be kept constant, which is beneficial to the leakage current elimination. It also has a very simple structure, which is easy to implement by digital signal processors or analog circuits.

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