The Use of Active Elements to Reduce the Size and Weight of Passive Components in Adjustable Speed Drives

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Publication date:
2012

Document Version
Publisher's PDF, also known as Version of record

The Use of Active Elements to Reduce the Size and Weight of Passive Components in Adjustable Speed Drives

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2011

Acknowledgement

It had been an honor for me to work as a PhD student in the Department of Energy Technology, Aalborg University, Denmark. I would like to thank the department to give me the opportunity to work on this project.

I am grateful to my supervisor Dr. Stig Munk-Nielsen from Aalborg University for his support and patience during the project. It was always a great pleasure to discuss different technical issues with him and gain knowledge from his experience. I am truly indebted and thankful to my supervisor Dr. Henrik Kragh from Grundfos A/S for his assistance and advice.

I owe sincere and earnest thankfulness to Dr. Sergio Busquets-Monge of Technical University of Catalonia, Spain for his help during development of the controller for the three-level inverter. His positive attitude and energy towards solving a problem are always source of inspiration for me.

I want to thank Dr. Kaiyuan Lu from Aalborg University for his constructive criticism, which improved my work on the active damping technique.

This dissertation would not have been possible without the support of the Electronics Hardware Team, Grundfos A/S, Bjerringbro, Denmark. I would like to thank Mr. Thorkild Kvisgaard, Hardware Technology Manager, Grundfos A/S for his endless support, technical as well as non-technical, during the project. Special thanks to Mr. Palle M. Obel, Mr. Bjarne Henriksen, and Mr. Niels H. Petersen for their help, feedback, and discussions concerning the development of hardware. I would like to acknowledge Mr. Klaus Bak for his fine PCB design, which helped me develop the three-level inverter without any difficulty.

It was of great joy to work with my friends Sanjay Kumar Chaudhary, Lajos Torok, Szymon Beczkowski, Ionut Trintis, Laszlo Mathe, Benoit Bidoggia, Pukar Mahat, and Jayakrishnan Pillai. It was exciting to have discussions with them, both academic as well as non-academic.

I also thank Mr. Walter Neumayr for helping in the purchase of the components. I would like to thank Mr. Jan Christiansen and Mr. Flemming Bo Larsen for their help in the lab on various occasions.

I would like to express my deepest gratitude to my parents and sisters for their unconditional love and support. This dissertation would have simply been impossible without them.

Abstract

Adjustable speed drives are considered as workhorse of industry due to various applications in different kind of industries. According to a market survey, low voltage drives are most profitable in the drive industries. The drive consists of a machine and a converter, which processes grid power and converts into usable power for the machine. The converter consists of active and passive components. The size, weight, and volume of the drive are decided by the passive components since they typically contribute to 75% of the weight and volume of the drive. Most popular topology for the low voltage drive is a six-pulse diode bridge rectifier followed by a two-level inverter. For these drives, the DC-link capacitor is the major contributor among the passive components.

The DC-link capacitance value can be reduced in the drive systems known as small DC-link capacitor based drives. However, small DC-link capacitor based drive system shows instability while it is operated with high input line inductance at the operating points with high power. This thesis presents a simple, new active damping technique that can stabilize effectively the drive system at the unstable operating points offering greatly reduced input line current THD. The active damping terms introduced are linked directly to the DC-link voltage ripple, and damping voltage components are added to the input voltage of the drive machine. The stabilizing effect of the active damping terms is demonstrated for an induction machine drive system. To facilitate the design and analysis of the active damping terms, the effects of the active damping terms on the machine current and the DC-link voltage of the drive system are discussed. A design recommendation for the proposed active damping terms is given. Simulation and experimental results verifying the effectiveness of the new active damping method are presented.

A Neutral-Point-Clamped (NPC) three-level inverter with small DC-link capacitors is selected as viable option for a two-level inverter in this thesis for low voltage applications. This inverter requires zero average neutral-point current for stable neutral-point potential. The small DC-link capacitors may not maintain the capacitor voltage balance even with zero neutral-point current due to nonlinearities present in the circuit. This requires a fast control of the neutral-point voltage. A simple carrier-based modulation strategy is proposed which allows modeling the neutral-point voltage dynamics as a continuous function of the power drawn from the converter. This model shows that the neutral-point current is proportional to the power drawn from the converter, and it enables the use of well established classical control theory for the neutral-point voltage controller design. A simple PI controller is designed for the neutral-point voltage balance based on this model. The design method for optimum performance is discussed. The implementation of the proposed modulation strategy and controller is very simple. The controller is implemented in a 7.5 kW induction machine based drive with only 14 μF DC-link capacitors. A fast and stable performance of the neutral-point voltage controller is achieved and verified by experiments.

The performances of the two-level and three-level inverter based drive systems with small DC-link capacitors are compared. The shaft voltage, the common mode

voltage, the conducted emissions, and the efficiency of the two systems are compared since they are major factors which affect the size of the passive components in the drives. Although the three-level inverter requires higher number of active components as compared to the two-level inverter, it has been found that the three-level inverter is better solution than the two-level inverter even with small DC-link capacitors if the passive components size is concerned.

Chapter 1

Introduction

1.1 Background and Motivation

Adjustable Speed Drives (ASD) are extensively used in various industries like traction; process industry; and heating, ventilation, and air-conditioning (HVAC) etc. They require controlled frequency and voltage magnitude of AC supply for easy control. However, the available power is the grid power, which has AC supply of constant amplitude and frequency. Grid power is converted to controlled AC power using AC to AC converter for electric drive applications. An typical AC to AC converter can have following parts as shown in Figure 1-1.

1. Input Filters
2. Power Processing Section (AC-AC conversion)
    a. AC to DC Rectification Stage
    b. Energy Storage Elements after Rectification Stage
    c. DC to AC Inversion Stage
3. Output Filter

Each part can consist of active or passive components. Input filter, energy storage elements after rectification stage, and output filter consist of only passive components such as inductors, capacitors etc. The DC to AC inversion stage is made of active components such as insulated gate bipolar transistors (IGBT), microcontrollers, etc. The AC to DC rectification stage may consist of active or passive components and it depends on the topology. If AC to DC rectifier is based on diode bridge rectification, it consists of diodes and transformers (for medium and high power applications). On the other hand, if the rectifier is realized by a power electronics converter, it consists of active components.

According to a market research on AC drives, low power drives (5 to 40 kW) segment was the most profitable segment in 2010 [87]. The most common topology for this power level is a six-pulse diode bridge rectifier stage followed by a two-level inverter. This topology has passive components, which typically contribute to 75% of the size and weight of a power inverter [99]. The passive components;

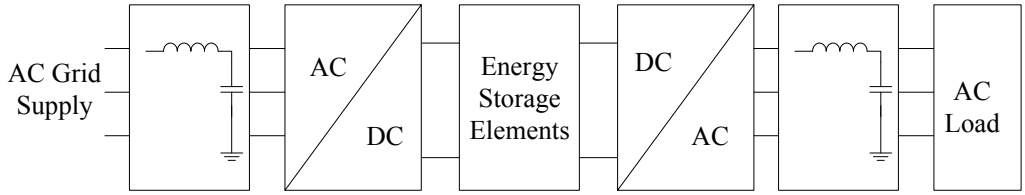


Figure 1-1 Different Parts of an ASD.

capacitors, magnetics, and thermal management components; are the major parts of the drive system [99].

The evolution of power semiconductor devices, which are used as active components, is rapid. Thyristors are the first generation of power semiconductor devices and they were introduced in market in 1958 for high power applications [41]. They are dominating high power low frequency applications even nowadays. Some 35 years ago, Power MOSFETs were introduced by International Rectifiers. They made linear power supplies, which used bipolar junction transistors, obsolete and replaced them with switched mode power supplies [91]. Few years later, IGBT was introduced, which had revolutionized the power electronics industry. It has been estimated that a cumulative cost saving of $15.8 trillion for over the last 20 years has been achieved by this technology [92]. During past years, from the 1st generation to the 5th generation of IGBT, overall losses are reduced to one third [18]. Recent developments show that the wide band gap material such as GaN and SiC can help increase in efficiency of the converters [86], [97]. However, the passive components evolution is slow. It can be seen from Fig. 13 in [99] that the highest contribution to the weight and volume of the drive is from capacitors. In voltage fed inverters such as two-level and three-level inverters, which are most common converter for drive applications, research has been focused on reducing the size of capacitors [9], [14], [26], [67], [75], [82]. However, small DC-link capacitor based drive system exhibits unstable operating point while it is operated with high input line inductance at operating points with high power. The instability of the operating point can be explained if the load connected to the drive system is considered as constant power load. Constant power load acts as negative impedance and can cause unstable operating point at high power [75].

1.2 Objectives and Scope of the Project

1.2.1 Objectives

The main objectives of this project were:

1. To provide active damping for Small DC-link capacitor based ASD

   The small DC link capacitor based drive may show unstable operating point at high power level. This unstable operating point may cause poor THD at the input line current and high voltage oscillation at the DC-link. A stabilization technique is required.

2. To reduced passive components size and volume in a three-level inverter based drive

   The three-level inverter generates less electromagnetic interference. This reduces the requirement of EMI filter in the three-level inverter. However, the requirement for DC-link capacitor size is higher as compared to the two-level inverter. This depends on the modulation strategies. A modulation strategy is required to minimize the size of DC-link capacitor in the three-level inverter.

1.2.2 Project Scope

This project focuses on the reduction of passive components in an adjustable speed drive. The induction machine based drive is considered for experiments. However, the developed methods or techniques in the project should be in such a way that it can also be used for a permanent magnet synchronous machine.

The low voltage drives are considered in this project and the power range is 5 kW -40 kW.

1.2.3 Tools used

Following softwares are used during this project

1. MATLAB® ver. 7.10.0.499 (R2010a): MATLAB is used for various numerical calculations in this project.
2. Simulink ver. 7.5 (R2010a): This is a dynamic system simulation tool for MATLAB®. In this project, Simulink is used for simulation of various controllers and dynamics systems.
3. Plecs ver. 3.1.1: This simulation tool is used for simulation of the electrical components.
4. Code composer studio ver. 3.3.59.4: This is a tool for programming the Texas Instrument's processors. In this project TMS320F28335 digital signal controller is used for implementing various control algorithms for the inverters. Code composer studio is used as a development platform for this digital signal controller.
5. Altium Designer 6: This software is used to design different printed circuit boards (PCB) during this project.

1.3 Major Contributions

The main contributions of this project are listed below:

1. A detailed model of the drive system is presented. This detailed model is linearized about an operating point for stability analysis of the operating point since the system is nonlinear.

2. It has been shown that the small DC-link capacitor based drive exhibits stable limit cycle at unstable operating point. This limit cycle causes high DC-link voltage oscillation and poor input line current THD.
3. A simple active damping technique is proposed in this thesis to stabilize the unstable operating point. This helps improving the input line current THD. The active damping terms add harmonic component of the DC-link voltage to the stator voltage of machine.
4. The effect of active damping terms on the machine current is analyzed and a design recommendation is derived based on the analysis.
5. In a drive with vector control, the damping term can be added to a current reference command of the machine. Using simple block diagram reduction techniques, a relationship between damping terms added to the machine voltage and damping terms added to the machine current reference is established.
6. A three-phase neutral-point clamped three-level inverter requires high DC-link capacitance value due to nonzero neutral-point current. A new modulation strategy, which adds a scaled common mode offset to the three-phase voltage reference command, is developed.
7. A simple, first-order continuous model, which defines the dynamics of the neutral-point voltage, is derived for the proposed modulation strategy. Using this model, linear control theories can be applied to design a fast and robust neutral-point voltage controller.

1.4 Outline of the Thesis

The organization of the thesis is given as follows:

Chapter 2 deals with small DC-link capacitor based two-level inverter. It presents a detailed model of the drive system. Since small DC-link capacitor based system may have unstable operating point, an active damping technique is proposed in this chapter to stabilize the operating point. The active damping terms add harmonic components of the DC-link voltage to the machine stator voltage. This affects the harmonic components of the machine current. Analysis of the harmonic components of the machine current is also presented in the chapter and this analysis leads to design recommendations for selecting active damping terms. Simulation and experimental results are also presented for open loop V/f controlled drive to support the analysis.

Chapter 3 presents with the closed loop control of the small DC-link capacitor based two-level inverter. The active damped technique can be implemented in a closed loop system. A stator flux oriented closed loop control drive is considered. It has been discussed that the active damping term can be added to either the stator voltage command or the stator current reference. A relationship between these two methods is presented in this chapter.

A neutral-point clamped (NPC) three-level inverter can be a viable option for the DC-AC inverter. This topology helps in reducing size of the passive components in the drive. Chapter 4 presents an overview of the NPC three-level inverter. In this chapter, different modulation strategies and neutral-point voltage controllers, which are proposed in the literature, are discussed in brief. It has been found that the design of the neutral-point voltage controller for small DC-link capacitor based NPC three-level inverter is complicated due to discontinuous model of the system.

Chapter 5 discusses a new modulation strategy for the NPC three-level inverter. This modulation strategy is based on the scaled common mode offset approach. With this modulation strategy, a simple first-order continuous equation is derived for neutral-point voltage dynamics. This continuous equation enables the use of classical control theory for the neutral-point voltage controller. In this chapter, a proportional-integral (PI) controller design is presented and it is verified by the experimental results.

Chapter 6 shows performance comparison for the two- level and the three-level inverter based on small DC-link capacitors. The common mode voltage, shaft voltage, conducted emission, and efficiency are compared since they are main factors for passive components in an inverter. It has been shown that the three-level inverter with small DC-link capacitors can reduce the size of passive components by increasing the efficiency and reducing the conducted emission.

Chapter 7 concludes the thesis with mention of future work related to the work presented in the thesis.

1.5 List of Publications

Conference Publications

1. Maheshwari, R.; Munk-Nielsen, S.; Henriksen, B.; Obel, P.M.; Kragh, H.; , "Active damping technique for small DC-link capacitor based drive system," *Industrial Electronics (ISIE), 2010 IEEE International Symposium on* , vol., no., pp.1205-1209, 4-7 July 2010.
2. Maheshwari, R.; Munk-Nielsen, S.; , "Closed loop control of active damped small DC-link capacitor based drive," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.4187-4191, 12-16 Sept. 2010.
3. Maheshwari, R.; Munk-Nielsen, S.; , "Performance analysis of active damped small DC-link capacitor based drive for unbalanced input voltage supply," *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on* , vol., no., pp.1-10, Aug. 30 2011-Sept. 1 2011.
4. Maheshwari, RamKrishan; Munk-Nielsen, Stig; Busquets-Monge, Sergio; , "Neutral-point current modeling and control for Neutral-Point Clamped three-level converter drive with small DC-link capacitors," *Energy*

Conversion Congress and Exposition (ECCE), 2011 IEEE , vol., no., pp.2087-2094, 17-22 Sept. 2011.

5. Maheshwari, R.; Munk-Nielsen, S.; Busquets-Monge, S.; , "EMI performance comparison of two-level and three-level inverters in small dc-link capacitors based motor drives," Industrial Electronics (ISIE), 2012 IEEE International Symposium on , vol., no., pp.652-657, 28-31 May 2012.

Transaction Publications

6. Maheshwari, R.; Munk-Nielsen, S.; Busquets-Monge, S.; , "Design of Neutral-Point Voltage Controller of a Three-level NPC Inverter with Small DC-Link Capacitors," Industrial Electronics, IEEE Transactions on , vol.PP, no.99, pp.1, 0. doi: 10.1109/TIE.2012.2202352

Transaction Publications (under review)

7. Maheshwari, R.; Munk-Nielsen, S.; Kaiyuan Lu; , "An Active Damping Technique for Small DC-Link Capacitor Based Drive System," under review in *Transaction of Industrial Informatics*.

8. Maheshwari, R.; Munk-Nielsen, S.; , "Performance Analysis of Active Damped Small DC-link Capacitor Based Drive for Unbalanced Input Voltage Supply," under review in *EPE journal*.

Chapter 2

Small DC-Link Capacitor Based Two-Level Converter

A typical adjustable speed drive consists of a six-pulse diode bridge rectifier followed by a two-level inverter with a DC-link filter as an in-between stage as shown in Figure 2-1. The DC-link filter consists of a DC-link capacitor and an optional DC-link inductor. The DC-link capacitor (generally an electrolytic capacitor) and the DC-link inductor contribute to passive components in a drive besides high frequency EMI filters. The poor reliability and cost of the electrolytic capacitor has been a major driving force to reduce the value of capacitance and use film capacitors [9]. These kinds of drives are referred as slim DC-link or small DC-link drives.

The six-pulse diode bridge rectifier output voltage consists of harmonic components of sixth multiple of line frequency. These frequency components are filtered by DC-link filter if a high value of DC-link capacitor is used and the DC-link voltage has constant value. Since small DC-link capacitor based drive has small value of DC-link capacitor, the DC-link voltage has harmonic components of sixth multiple of line frequency. In other words, the DC-link voltage in the small DC-link capacitor based drive has oscillations. These oscillations may cause unstable operating point of the drive for constant power load. If the load is assumed as constant power load, the current drawn by the DC-AC inverter decreases with increase in the DC-link voltage and vice versa. The load then can be considered as a load with negative impedance and can be the cause of unstable operating point.

Section 2.1 describes the instability of the operating point using a small-signal model. An overview of the methods to stabilize the operating point available in the literature is given in Section 2.2. An improved stabilization technique, which is based on the detailed model of the drive system, is presented in this chapter. The detailed model is presented in Section 2.3 followed by the proposed stabilization technique which is described in Section 2.4. The stabilization technique affects the input and output currents of the drive which is explained in Section 2.5. The stabilization technique is verified by simulation and experiments for an induction machine based drive with open loop *V*/*f* control, and the results are presented in Section 2.6.

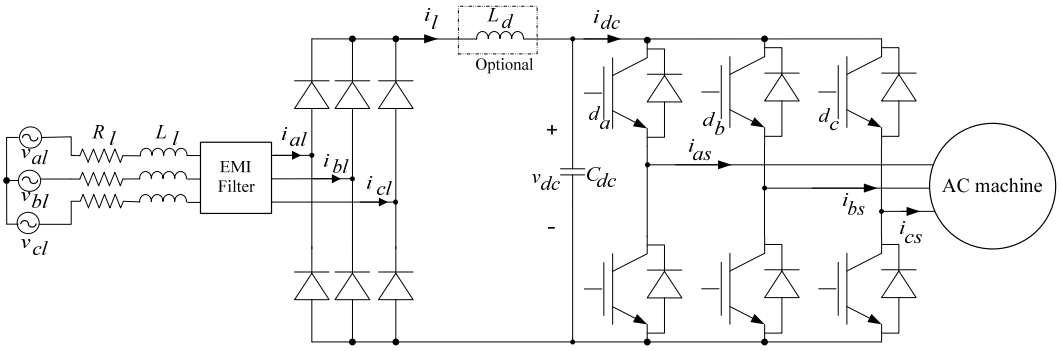


Figure 2-1 Adjustable speed drive topology.

2.1 Stability of Small DC-Link Capacitor Based Drive

A typical adjustable speed drive (ASD) consists of an AC to DC converter followed by a DC-link capacitor and a DC to AC inverter which drives an AC machine. The AC to DC converter is realized by the six-pulse diode bridge rectifier, and a two-level inverter is used as the DC to AC inverter as shown in Figure 2-1. To analyze the stability of the system, a simple model is used where the two-level inverter and the AC machine is modeled as a current source as shown in Figure 2-2. The equivalent resistance (R) and the equivalent DC-link inductance (L_{dc}), as shown in Figure 2-2, are related to the DC-link inductance (L_d), the source resistance (R_l), and the source inductance (L_l), which include the resistance and inductance offered by the grid supply together with the impedance offered by any series choke between grid and rectifier (Figure 2-1), as given by

$$R = 2R_l + {}^{3\omega_g L_l}\!/_{\pi}, \qquad L_{dc} = L_d + 2L_l \tag{2.1}$$

where ${}^{3\omega_g L_l}\!/_{\pi}$ corresponds to the nonohmic voltage drop due to commutation in the diodes. ω_g is the frequency of the supply voltage.

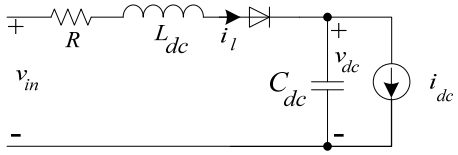


Figure 2-2 Equivalent model of the drive.

The input voltage v_{in} in Figure 2-2 can be approximated by

$$v_{in} = \frac{3\sqrt{3}V_{ph}}{\pi}\left(1 - \sum_{n=1}^{\infty}\frac{2}{(6n)^2 - 1}\cos(6n\omega_g t)\right) \tag{2.2}$$

where V_{ph} represents the amplitude of the three phase input voltages v_{al}, v_{bl}, and v_{cl} to the rectifier as shown in Figure 2-1.

The equivalent circuit shown in Figure 2-2 has two state variables (the inductor current (i_l) and the DC-link voltage (v_{dc})) and two inputs (the input voltage (v_{in}) and equivalent DC-link current (i_{dc})). The equations defining the dynamics of the state variables i_l and v_{dc} are given as

$$\begin{aligned} L_{dc}\frac{di_l}{dt} + Ri_l &= v_{in} - v_{dc} \\ C_{dc}\frac{dv_{dc}}{dt} &= i_l - i_{dc} \\ i_l &\geq 0 \end{aligned} \tag{2.3}$$

It can be seen from (2.3) that the system dynamics depends on the DC-link current (i_{dc}), which in turn depends on the duty cycle of the IGBTs in the inverter and machine current. An equation for i_{dc}, as a function of the machine currents, is derived in the next subsection.

2.1.1 The DC-link Current (i_{dc})

It can be seen from Figure 2-1 that the DC-link current is equal to the sum of the machine phase currents if those particular phases are connected to the top DC-link terminal. The time for which a particular phase is connected to the top DC-link terminal is decided by the duty cycles of the top IGBTs of the two-level converter. An expression of the DC-link current averaged over a switching period is given as

$$i_{dc} = d_a i_{as} + d_b i_{bs} + d_c i_{cs} \tag{2.4}$$

where d_a, d_b, and d_c are the duty cycles of the top IGBTs, and i_{as}, i_{bs}, and i_{cs} are the machine phase currents as shown in Figure 2-1.

Typically, carrier-based modulation is used for generating the duty cycles for the IGBT in the ASDs. The duty cycle is generated by comparing the triangular carrier wave by the control signals as shown in Figure 2-3 [5]. Inputs to the modulator are the control voltages ($v_{as,c}$, $v_{bs,c}$, and $v_{cs,c}$) of different phases. Using symmetry of triangles in Figure 2-3, the duty cycles for the corresponding phases can be expressed as

$$d_a = \frac{V_{tri} + v_{as,c}}{2V_{tri}}; d_b = \frac{V_{tri} + v_{bs,c}}{2V_{tri}}; d_c = \frac{V_{tri} + v_{cs,c}}{2V_{tri}} \tag{2.5}$$

where V_{tri} is the peak value of the carrier wave signal of the modulator.

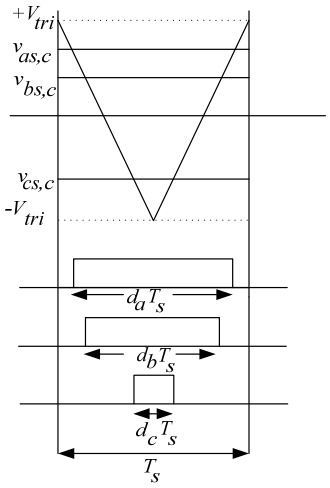


Figure 2-3 PWM duty cycle generation.

Replacing (2.5) in (2.4) and assuming $i_{as}+i_{bs}+i_{cs}=0$, the DC-link current can be expressed as

$$i_{dc} = \frac{1}{2V_{tri}}\left(v_{as,c}i_{as} + v_{bs,c}i_{bs} + v_{cs,c}i_{cs}\right) \tag{2.6}$$

The control voltages supplied to the modulator are proportional to the ratio of the required inverter pole voltages of their respective phases and the DC-link voltage as given by

$$v_{ks,c} = v_{ks}\frac{2V_{tri}}{v_{dcs}} \quad ;k = 1,2,3 \tag{2.7}$$

where v_{ks} is the fundamental component of the inverter pole voltage to be applied and v_{dcs} is the sensed DC-link voltage.

By using (2.6) and (2.7), i_{dc} can be expressed as

$$i_{dc} = \frac{1}{v_{dcs}}\left(v_{as}i_{as} + v_{bs}i_{bs} + v_{cs}i_{cs}\right) \tag{2.8}$$

The machine variables v_{as}, v_{bs}, v_{cs}, i_{as}, i_{bs}, and i_{cs} can be transformed from the stationary reference frame to an arbitrary rotating reference frame using the transformation as described in Appendix A. The equation for i_{dc} in terms of the variables referred to an arbitrary rotating dq-reference frame can be given by

$$i_{dc} = \frac{1}{v_{dcs}}\left[\begin{bmatrix} v_{as} & v_{bs} & v_{cs}\end{bmatrix}\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs}\end{bmatrix}\right]$$

$$i_{dc} = \frac{1}{v_{dcs}}\begin{bmatrix} v_{ds} & v_{qs}\end{bmatrix}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & 0.866 & -0.866\end{bmatrix}\begin{bmatrix} 1 & 0 \\ -0.5 & 0.866 \\ -0.5 & -0.866\end{bmatrix}\begin{bmatrix} i_{ds} \\ i_{qs}\end{bmatrix}$$

$$i_{dc} = \frac{1}{v_{dcs}}\begin{bmatrix} v_{ds} & v_{qs}\end{bmatrix}\begin{bmatrix} 1.5 & 0 \\ 0 & 1.5\end{bmatrix}\begin{bmatrix} i_{ds} \\ i_{qs}\end{bmatrix}$$

$$i_{dc} = \frac{1}{v_{dcs}} \frac{3}{2} \left(v_{ds} i_{ds} + v_{qs} i_{qs} \right) = \frac{p_e}{v_{dcs}} \tag{2.9}$$

where v_{ds} and v_{qs} are the stator *d*- and *q*-axis voltages, and i_{ds} and i_{qs} are the stator *d*- and *q*-axis currents. It can be noted from (2.9) that the term $\frac{3}{2}\left(v_{ds} i_{ds} + v_{qs} i_{qs} \right)$ is the electrical power drawn by the machine expressed in terms of the *dq*-axes machine voltages and currents and is denoted as p_e.

2.1.2 Stability Analysis

The DC-link current is an input to the equivalent system shown in Figure 2-2. By substituting the DC-link current (2.9) into (2.3), the system dynamics can be expressed as

$$\begin{aligned} & L_{dc} \frac{di_l}{dt} + R i_l = v_{in} - v_{dc} \\ & C_{dc} \frac{dv_{dc}}{dt} = i_l - \frac{p_e}{v_{dcs}} \\ & i_l \geq 0 \end{aligned} \tag{2.10}$$

The dynamic equations given in (2.10) require the sensed DC-link voltage (v_{dcs}) which can be equal to the instantaneous DC-link voltage (v_{dc}) or the average DC-link voltage (V_{dc}). If the instantaneous DC-link voltage is used, the load to the rectifier acts as a negative impedance, on the other hand, if the average DC-link voltage is used, it does not cause negative impedance for the rectifier, and the system is always stable. For both cases, the system stability analyses are shown in the following.

2.1.2.1 Case 1: (v_{dcs}=v_{dc})

The system dynamic equations for v_{dcs}=v_{dc} are given as

$$\begin{aligned} & L_{dc} \frac{di_l}{dt} + R i_l = v_{in} - v_{dc} \\ & C_{dc} \frac{dv_{dc}}{dt} = i_l - \frac{p_e}{v_{dc}} \\ & i_l \geq 0 \end{aligned} \tag{2.11}$$

The system dynamic equations are nonlinear. To analyze the stability of the system, the linearized equations are required about an operating point. Considering only the first-order terms of the Taylor series expansion of (2.11), the linearized equations for the system are given by

$$L_{dc}\frac{d\tilde{i}_l}{dt}+R\tilde{i}_l=\tilde{v}_{in}-\tilde{v}_{dc}$$
$$C_{dc}\frac{d\tilde{v}_{dc}}{dt}=\tilde{i}_l-\frac{\tilde{p}_e}{V_{dc}}+\frac{P_e}{V_{dc}^2}\tilde{v}_{dc} \tag{2.12}$$

where "~" indicates the small-signal value, and capital letter denotes the quiescent value of that particular variable or input. Using (2.12), the transfer function from the inductor current ($\tilde{i}_l$) to the input voltage ($\tilde{v}_{in}$) may be given as

$$\frac{\tilde{i}_l(s)}{\tilde{v}_{in}(s)}=\frac{C_{dc}s-\frac{P_e}{V_{dc}^2}}{L_{dc}C_{dc}s^2+\left(RC_{dc}-\frac{L_{dc}P_e}{V_{dc}^2}\right)s+1-\frac{RP_e}{V_{dc}^2}} \tag{2.13}$$

and the characteristic equation for the system becomes

$$L_{dc}C_{dc}s^2+\left(RC_{dc}-\frac{L_{dc}P_e}{V_{dc}^2}\right)s+\left(1-\frac{RP_e}{V_{dc}^2}\right)=0 \tag{2.14}$$

The poles related to the system may be found by solving (2.14). Equation (2.14) is a quadratic equation, and the coefficient of '*s*' in the equation should be positive for stable poles with negative real part for the stable operating point of the system which gives a criterion

$$RC_{dc}-\frac{L_{dc}P_e}{V_{dc}^2}>0$$
$$\frac{R}{L_{dc}}>\frac{P_e}{C_{dc}V_{dc}^2} \tag{2.15}$$

If the criterion (2.15) is not satisfied, the system operating point about which the equations are linearized will be unstable. At high power with small DC-link capacitance, the term $\frac{P_e}{C_{dc}V_{dc}^2}$ may become more than $\frac{R}{L_{dc}}$ and results in an unstable operating point. Generally an unstable operating points exhibit limit cycles. This can be analyzed using the phase plane analysis. In the following, the phase plane analysis [3] is presented for the unstable operating point of the system.

Let us consider a system with parameters given in Table 2-1. The operating point of the system is given in Table 2-2. Using (2.14), the poles for the linearized system about this operating point can be calculated as 230 ± *j*4063.2, which correspond to an unstable operating point. The phase portraits of the system for two different initial conditions ((565 V, 3.6 A) & (666.6 V, 3 A)) are plotted as shown in Figure 2-4. It can be seen form Figure 2-4 that the trajectory of the states is approaching towards the limit cycle in steady state. Figure 2-4 shows that the operating points, which are used as the initial conditions for the system, are not stable since the trajectory of the states are moving away from those initial conditions. The trajectory will tend to infinity if negative inductor current (i_l) is allowed. The diodes are preventing negative inductor current, and it results in a stable limit cycle.

Table 2-1 System Parameters

L_{dc}	6 mH
C_{dc}	10 μF
R	1 Ω

Table 2-2 System Operating Point

P_e	2 kW
V_{dc}	565 V

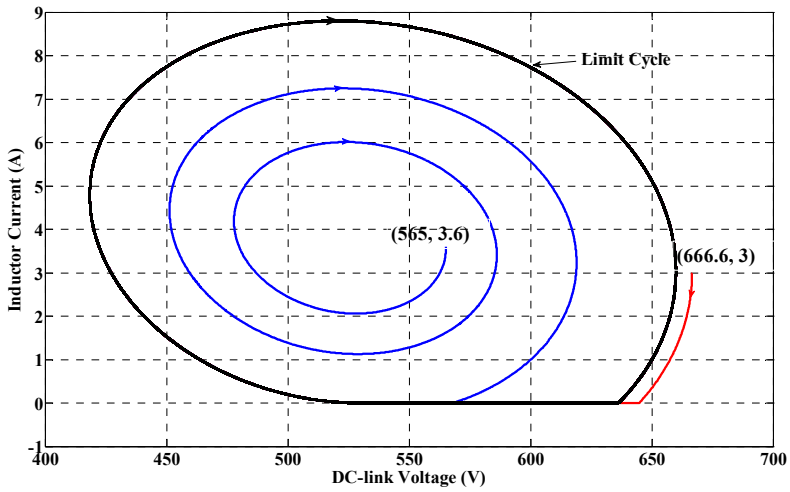


Figure 2-4 Phase portrait of the sytem.

2.1.2.2 Case 2: (v_{dcs}=V_{dc})

Using (2.10), the system dynamic equations for v_{dcs}=V_{dc} are given as

$$L_{dc}\frac{di_l}{dt}+Ri_l=v_{in}-v_{dc}$$
$$C_{dc}\frac{dv_{dc}}{dt}=i_l-\frac{p_e}{V_{dc}} \qquad (2.16)$$

By comparing (2.16) to (2.11), it can be seen that (2.16) is a linear equation since V_{dc}, which is not varying, is the average value of the DC-link voltage. Using (2.16), the transfer function from the inductor current (i_l) to the input voltage (v_{in}) may be given as

$$\frac{i_l(s)}{v_{in}(s)}=\frac{C_{dc}s}{L_{dc}C_{dc}s^2+RC_{dc}s+1} \qquad (2.17)$$

and the characteristic equation for the system is given by

$$L_{dc}C_{dc}s^2+RC_{dc}s+1=0 \qquad (2.18)$$

which is a characteristic equation for a second-order RLC filter. The system is

always stable in this case since all the coefficients of the characteristic equation are positive, and the poles will never be in the right half s-plane.

2.2 Overview of Stabilization Techniques for the Small DC-Link Capacitor Based Drive

The system stability is analyzed in the previous section. It is shown that the system operating point may become unstable if the instantaneous value of the DC-link voltage is used for calculating the duty cycles. Different stabilization techniques are presented in the literature. The main idea behind the stabilizing techniques discussed in literature is to vary the power drawn from the rectifier in proportional to the DC-link voltage variation [14], [26], [67], [75]. However, they differ in implementation of this idea.

The stabilization technique presented in [75] suggests to vary the torque produced by the machine in proportional to the DC-link voltage variation, which in turn will vary the power drawn by the machine in proportional to the DC-link voltage variation. In other words, the power drawn from the rectifier will be proportional to the DC-link voltage variation. The torque is controlled by controlling the machine current in this method. This implementation demands a fast control of the machine current since the torque reference command vary in proportional to the DC-link voltage variation having frequency equal to six times the grid frequency. The performance of this method depends on the current controller bandwidth.

A similar approach of stabilizing the operating point is presented in [67]. The torque producing current component of the machine is added to a current command, which is proportional to the DC-link voltage variation. It is shown that the characteristic equation of (2.18) for the system can be achieved by this method, where the poles of the linearized system are decided by the system parameters only, independent of the system operating point. However, same performance can be achieved by simply using the average DC-link voltage for duty cycle calculations as proposed in the previous section. In this case, the damping of the system is decided by the resistance present in the system. It is also shown in [67] that the damping of the system can be increased further, but it requires the knowledge of parameters (R, L_{dc}, and C_{dc}) of the system. However, the performance of this method also depends on the current controller bandwidth.

The stabilizing techniques presented in [67] and [75] require the current controller, which can response to the 300 Hz variation present in DC-link voltage. If a current controller with a low bandwidth is used in the drive system, a stabilizing technique where the torque producing voltage reference command is modified, can be used as proposed in [14] and [26]. In this technique, the voltage reference is added to a voltage component proportional to the DC-link voltage variation. Since this component is added to the output of the current controller, current controller bandwidth should be low enough not to respond to components of 300 Hz. The generation of the stabilizing voltage component added to the torque producing voltage reference command requires a high-pass filter. The bandwidth of the high-

pass filter depends on the operating point and the parameters of the system. Thus it requires online tuning for the optimal performance if the system parameters are changed. This situation can occur very often if the drive system is used for different kinds of grids.

A new technique for the stabilizing the operating point is proposed in this chapter. This technique adds voltage components, which is proportional to the high frequency variation in the DC-link voltage, to the machine terminal voltages. The voltage components are referred to as active damping terms, since they stabilize the unstable operating point while actively damping the system. The implementation of the damping terms is independent of the system parameter change. These terms are derived using a detailed linearized model of the machine and (2.10). The detailed linearized model of the drive system is presented in the next section followed by the discussion of the active damping terms in Section 2.4.

2.3 Detailed Drive Model

It can be seen from (2.9) that the DC-link current depends on the machine voltages and the machine currents, which are governed by the induction machine model. The detailed model of an induction machine [8], which is used as the AC machine in the drive, is presented in the following.

2.3.1 Linearized Induction Machine Equation

The three-phase induction machine has constant magnitude field flux, but it is revolving in the space in steady state. So the dynamic model of induction machine is somewhat complicated. A model presented in [8] is used in this section. The assumptions made for the induction machine model are

- The distribution of magneto motive force in air gap is sinusoidal.
- The effect of iron losses and saturation are neglected.
- The zero sequence components do not exist.

Based on the equivalent circuit shown in Figure 2-5, the stator voltage equation in the stationary stator reference frame is given as

$$r_s \underline{\boldsymbol{i}}_{\boldsymbol{s}} + L_s \frac{d}{dt}\underline{\boldsymbol{i}}_{\boldsymbol{s}} + L_o \frac{d}{dt}(\underline{\boldsymbol{i}}_{\boldsymbol{r}} e^{j\varepsilon}) = \underline{\boldsymbol{v}}_{\boldsymbol{s}}(t) \tag{2.19}$$

and rotor voltage equation in rotor reference frame is given as

$$r_r \underline{\boldsymbol{i}}_{\boldsymbol{r}} + L_r \frac{d}{dt}\underline{\boldsymbol{i}}_{\boldsymbol{r}} + L_o \frac{d}{dt}(\underline{\boldsymbol{i}}_{\boldsymbol{s}} e^{-j\varepsilon}) = \underline{\boldsymbol{v}}_{\boldsymbol{r}}(t) \tag{2.20}$$

where L_s is the stator inductance and equals to the sum of the stator leakage inductance (L_{ls}) and the mutual inductance (L_o) ($L_s = L_{ls} + L_o$), and L_r is the rotor inductance and equals to the sum of the rotor leakage inductance (L_{lr}) and the mutual inductance (L_o) ($L_s = L_{lr} + L_o$) [8]. The space phasor quantities are set by bar under

letter ('_'), e.g., $\underline{\boldsymbol{v}}_s$, $\underline{\boldsymbol{i}}_s$, $\underline{\boldsymbol{v}}_r$ etc. *s* and *r* subscripts are used for the stator and rotor variables, respectively. ε is the angle between the stator and rotor axis. r_s and r_r are the stator and rotor resistances. μ is the angle between the stator axis and the *d*- axis as shown in Figure 2-6.

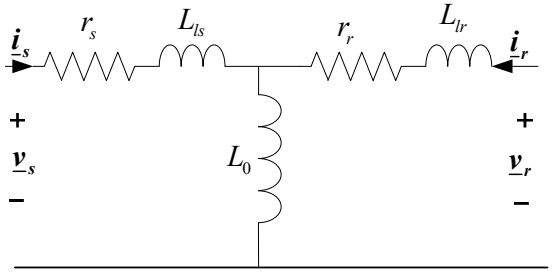


Figure 2-5 Induction machine equivalent circuit

The dynamic equations of the three-phase AC machine are expressed in a synchronously rotating *dq* reference frame because of easy control. The details will be discussed in the next chapter.

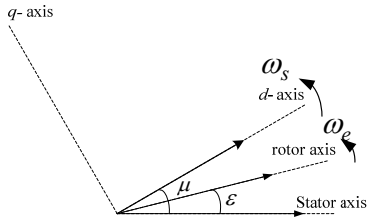


Figure 2-6 Synchronously rotating reference frame

The stator voltage and current phasors in the synchronously rotating reference frame can be expressed in terms of the stator voltage and current phasors in the stator reference frame and the angle between them as

$$v_{ds} + j\,v_{qs} = \underline{\boldsymbol{v}}_s e^{-j\mu} \tag{2.21}$$

$$i_{ds} + j\,i_{qs} = \underline{\boldsymbol{i}}_s e^{-j\mu} \tag{2.22}$$

Similarly, the rotor voltage and current phasors in the synchronously rotating reference frame can be expressed in terms of the rotor voltage and current phasors in the rotor reference frame and the angle between them as

$$v_{dr} + j\,v_{qr} = \underline{\boldsymbol{v}}_r e^{-j(\mu-\varepsilon)} \tag{2.23}$$

$$i_{dr} + j\,i_{qr} = \underline{\boldsymbol{i}}_r e^{-j(\mu-\varepsilon)} \tag{2.24}$$

Substituting $\underline{\boldsymbol{v}}_s$, $\underline{\boldsymbol{i}}_s$, $\underline{\boldsymbol{v}}_r$, and $\underline{\boldsymbol{i}}_r$ from (2.21), (2.22), (2.23), and (2.24) into (2.19) and (2.20), the voltage equations of the induction machine (2.19) and (2.20) may be transformed to equations in an arbitrary *dq*- reference frame rotating with the synchronous speed (ω_s) [8] and expressed as

$$r_s\left(i_{ds}+j\,i_{qs}\right)e^{j\mu}+L_s\frac{d}{dt}\left(\left(i_{ds}+j\,i_{qs}\right)e^{j\mu}\right)+L_o\frac{d}{dt}\left(\left(i_{dr}+j\,i_{qr}\right)e^{j\mu}\right)=\left(\left(v_{ds}+j\,v_{qs}\right)e^{j\mu}\right) \quad (2.25)$$

and

$$r_r\left(i_{dr}+j\,i_{qr}\right)e^{j(\mu-\varepsilon)}+L_r\frac{d}{dt}\left(\left(i_{dr}+j\,i_{qr}\right)e^{j(\mu-\varepsilon)}\right)+L_o\frac{d}{dt}\left(\left(i_{dr}+j\,i_{qr}\right)e^{j(\mu-\varepsilon)}\right)=\left(v_{dr}+j\,v_{qr}\right)e^{j(\mu-\varepsilon)} \quad (2.26)$$

By comparing the real and imaginary parts of both sides of (2.25) and (2.26), the dynamic model of the induction machine in the arbitrary *dq*- reference frame rotating with the synchronous speed can be obtained as

$$\begin{aligned}
v_{ds} &= r_s i_{ds}+L_s\frac{di_{ds}}{dt}-\omega_s L_s i_{qs}+L_o\frac{di_{dr}}{dt}-\omega_s L_o i_{qr}\\
v_{qs} &= r_s i_{qs}+L_s\frac{di_{qs}}{dt}+\omega_s L_s i_{ds}+L_o\frac{di_{qr}}{dt}+\omega_s L_o i_{dr}\\
v_{dr} &= r_r i_{dr}+L_r\frac{di_{dr}}{dt}-\left(\omega_s-\omega_e\right)L_r i_{qr}+L_o\frac{di_{ds}}{dt}-\left(\omega_s-\omega_e\right)L_o i_{qs}\\
v_{qr} &= r_r i_{qr}+L_r\frac{di_{qr}}{dt}+\left(\omega_s-\omega_e\right)L_r i_{dr}+L_o\frac{di_{qs}}{dt}+\left(\omega_s-\omega_e\right)L_o i_{ds}
\end{aligned} \quad (2.27)$$

where $\omega_s=\dfrac{d\mu}{dt}$ (2.28)

and $\omega_e=\dfrac{d\varepsilon}{dt}$ (2.29)

and *d* and *q* subscript describe the *d*- and *q*- axes variables, and ω_e is the speed of the machine in electrical rad/s. The equation defining the dynamics of the machine speed is given by

$$J\frac{d\left(\frac{2}{P}\omega_e\right)}{dt}=\frac{3}{2}\frac{P}{2}L_o\left(i_{dr}i_{qs}-i_{ds}i_{qr}\right)-m_L \quad (2.30)$$

where J is the moment of inertia of the machine, P is the number of poles in the machine and m_L is the load torque applied to the machine.

Since the system under consideration is nonlinear, the linearized induction machine equations about an operating point can be given as [6]

$$\tilde{v}_{ds} = r_s\tilde{i}_{ds} + L_s\frac{d\tilde{i}_{ds}}{dt} - \omega_s L_s\tilde{i}_{qs} + L_o\frac{d\tilde{i}_{dr}}{dt} - \omega_s L_o\tilde{i}_{qr}$$

$$\tilde{v}_{qs} = r_s\tilde{i}_{qs} + L_s\frac{d\tilde{i}_{qs}}{dt} + \omega_s L_s\tilde{i}_{ds} + L_o\frac{d\tilde{i}_{qr}}{dt} + \omega_s L_o\tilde{i}_{dr}$$

$$\tilde{v}_{dr} = r_r\tilde{i}_{dr} + L_r\frac{d\tilde{i}_{dr}}{dt} - (\omega_s - \omega_e)L_r\tilde{i}_{qr} + L_o\frac{d\tilde{i}_{ds}}{dt} - (\omega_s - \omega_e)L_o\tilde{i}_{qs} + (L_r I_{qr} + L_o I_{qs})\tilde{\omega}_e \quad (2.31)$$

$$\tilde{v}_{qr} = r_r\tilde{i}_{qr} + L_r\frac{d\tilde{i}_{qr}}{dt} + (\omega_s - \omega_e)L_r\tilde{i}_{dr} + L_o\frac{d\tilde{i}_{qs}}{dt} + (\omega_s - \omega_e)L_o\tilde{i}_{ds} - (L_r I_{dr} + L_o I_{ds})\tilde{\omega}_e$$

$$J\frac{d\left(\frac{2}{P}\tilde{\omega}_e\right)}{dt} = \frac{3}{2}\frac{P}{2}L_o\left(\tilde{i}_{dr}I_{qs} - \tilde{i}_{ds}I_{qr} + I_{dr}\tilde{i}_{qs} - I_{ds}\tilde{i}_{qr}\right) - \tilde{m}_L$$

where "~" indicates the small-signal value, and the capital letter denotes the DC value of that particular variable or input. Equation (2.31)can be written in state-space form as

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{ds}\\ \tilde{i}_{qs}\\ \tilde{i}_{dr}\\ \tilde{i}_{qr}\\ \tilde{\omega}_e\end{bmatrix} = \boldsymbol{A}\begin{bmatrix}\tilde{i}_{ds}\\ \tilde{i}_{qs}\\ \tilde{i}_{dr}\\ \tilde{i}_{qr}\\ \tilde{\omega}_e\end{bmatrix} + \boldsymbol{B}\begin{bmatrix}\tilde{v}_{ds}\\ \tilde{v}_{qs}\\ \tilde{v}_{dr}\\ \tilde{v}_{qr}\\ \tilde{m}_L\end{bmatrix} \quad (2.32)$$

where

$$\boldsymbol{A} = \begin{bmatrix}
\frac{-r_s}{\sigma L_s} & \omega_s + \frac{\omega_e L_o^2}{\sigma L_s L_r} & \frac{r_r L_0}{\sigma L_s L_r} & \frac{\omega_e L_0}{\sigma L_s} & \frac{L_0(L_r I_{qr} + L_o I_{qs})}{\sigma L_s L_r}\\
-\left(\omega_s + \frac{\omega_e L_o^2}{\sigma L_s L_r}\right) & \frac{-r_s}{\sigma L_s} & -\frac{\omega_e L_0}{\sigma L_s} & \frac{r_r L_0}{\sigma L_s L_r} & -\frac{L_0(L_r I_{dr} + L_o I_{ds})}{\sigma L_s L_r}\\
\frac{r_s L_0}{\sigma L_s L_r} & -\frac{\omega_e L_0}{\sigma L_r} & -\frac{r_r}{\sigma L_r} & \omega_s - \frac{\omega_e}{\sigma} & -\frac{(L_r I_{qr} + L_o I_{qs})}{\sigma L_r}\\
\frac{\omega_e L_0}{\sigma L_r} & \frac{r_s L_0}{\sigma L_s L_r} & -\left(\omega_s - \frac{\omega_e}{\sigma}\right) & -\frac{r_r}{\sigma L_r} & \frac{(L_r I_{dr} + L_o I_{ds})}{\sigma L_r}\\
-\left(\frac{P}{2}\right)^2\frac{3}{2}\frac{L_o I_{qr}}{J} & \left(\frac{P}{2}\right)^2\frac{3}{2}\frac{L_o I_{dr}}{J} & \left(\frac{P}{2}\right)^2\frac{3}{2}\frac{L_o I_{qs}}{J} & -\left(\frac{P}{2}\right)^2\frac{3}{2}\frac{L_o I_{ds}}{J} & 0
\end{bmatrix}$$

and

$$\boldsymbol{B}=\begin{bmatrix} \frac{1}{\sigma L_s} & 0 & \frac{-L_0}{\sigma L_s L_r} & 0 & 0 \\ 0 & \frac{1}{\sigma L_s} & 0 & \frac{-L_0}{\sigma L_s L_r} & 0 \\ \frac{-L_0}{\sigma L_s L_r} & 0 & \frac{1}{\sigma L_r} & 0 & 0 \\ 0 & \frac{-L_0}{\sigma L_s L_r} & 0 & \frac{1}{\sigma L_r} & 0 \\ 0 & 0 & 0 & 0 & -\frac{P}{2J} \end{bmatrix}$$

where σ is the total leakage factor defined as

$$\sigma = 1-\frac{L_o^2}{L_s L_r} \tag{2.33}$$

2.3.2 Detailed Drive Model

Using (2.11), the linearized equations of the system, which describe the dynamic behavior of i_l and v_{dc}, in terms of the machine voltages and currents, can be given as

$$\begin{aligned} L_{dc}\frac{d\tilde{i}_l}{dt}+R\tilde{i}_l &= \tilde{v}_{in}-\tilde{v}_{dc} \\ C_{dc}\frac{d\tilde{v}_{dc}}{dt} &= \tilde{i}_l-\frac{1}{V_{dc}}\frac{3}{2}\left(\tilde{v}_{ds}I_{ds}+\tilde{v}_{qs}I_{qs}+V_{ds}\tilde{i}_{ds}+V_{qs}\tilde{i}_{qs}\right)+\frac{1}{V_{dc}^2}\frac{3}{2}\left(V_{ds}I_{ds}+V_{qs}I_{qs}\right)\tilde{v}_{dc} \end{aligned} \tag{2.34}$$

By combining (2.34) and (2.32) for a squirrel cage induction machine ($\tilde{v}_{dr}$=0, $\tilde{v}_{qr}$=0), the linearized state-space equation of the complete drive system is given by

$$\frac{d}{dt}\begin{bmatrix} \tilde{i}_{ds} \\ \tilde{i}_{qs} \\ \tilde{i}_{dr} \\ \tilde{i}_{qr} \\ \tilde{\omega}_e \\ \hline \tilde{v}_{dc} \\ \tilde{i}_l \end{bmatrix} = \boldsymbol{A}'\begin{bmatrix} \tilde{i}_{ds} \\ \tilde{i}_{qs} \\ \tilde{i}_{dr} \\ \tilde{i}_{qr} \\ \tilde{\omega}_e \\ \hline \tilde{v}_{dc} \\ \tilde{i}_l \end{bmatrix} + \left[\begin{array}{ccc:c} \multicolumn{3}{c:}{\boldsymbol{B}_{5X3}} & \boldsymbol{0}_{5X1} \\ \hline -\frac{3}{2}\frac{I_{ds}}{V_{dc}C_{dc}} & -\frac{3}{2}\frac{I_{qs}}{V_{dc}C_{dc}} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{dc}} \end{array}\right]\begin{bmatrix} \tilde{v}_{ds} \\ \tilde{v}_{qs} \\ \tilde{m}_L \\ \hline \tilde{v}_{in} \end{bmatrix}$$

where

$$\boldsymbol{A}'=\left[\begin{array}{ccccc:cc} \multicolumn{5}{c:}{\boldsymbol{A}_{5X5}} & \multicolumn{2}{c}{\boldsymbol{0}_{5X2}} \\ \hline -\frac{3}{2}\frac{V_{ds}}{V_{dc}C_{dc}} & -\frac{3}{2}\frac{V_{qs}}{V_{dc}C_{dc}} & 0 & 0 & 0 & \frac{3}{2}\frac{\left(V_{ds}I_{ds}+V_{qs}I_{qs}\right)}{C_{dc}V_{dc}^2} & \frac{1}{C_{dc}} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{dc}} & -\frac{R}{L_{dc}} \end{array}\right] \tag{2.35}$$

It can be seen from (2.35) that the matrix ***A'*** has a null block matrix. Using block matrices in ***A'***, it can be written as

$$\boldsymbol{A'} = \begin{bmatrix} \boldsymbol{A}_{5x5} & \boldsymbol{0}_{5x2} \\ \boldsymbol{C'}_{2x5} & \boldsymbol{B'}_{2x2} \end{bmatrix} \tag{2.36}$$

where $\boldsymbol{C'} = \begin{bmatrix} -\frac{3}{2}\frac{V_{ds}}{V_{dc}C_{dc}} & -\frac{3}{2}\frac{V_{qs}}{V_{dc}C_{dc}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ and $\boldsymbol{B'} = \begin{bmatrix} \frac{3}{2}\frac{\left(V_{ds}I_{ds}+V_{qs}I_{qs}\right)}{C_{dc}V_{dc}^2} & \frac{1}{C_{dc}} \\ -\frac{1}{L_{dc}} & -\frac{R}{L_{dc}} \end{bmatrix}$

The poles of the detailed system described by (2.35) are given by the eigenvalues of ***A'***, and the eigenvalues of ***A'*** are equal to the eigenvalues of ***A*** and ***B'***. It can be proven as follows

$$\left|\boldsymbol{A'} - s\boldsymbol{I}\right| = \left|\begin{bmatrix} \boldsymbol{A} - s\boldsymbol{I} & \boldsymbol{0} \\ \boldsymbol{C'} & \boldsymbol{B'} - s\boldsymbol{I} \end{bmatrix}\right|$$

$$\left|\boldsymbol{A'} - s\boldsymbol{I}\right| = \left|\begin{bmatrix} \boldsymbol{A} - s\boldsymbol{I} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{I} \end{bmatrix}\right|\left|\begin{bmatrix} \boldsymbol{I} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{B'} - s\boldsymbol{I} \end{bmatrix}\right|\left|\begin{bmatrix} \boldsymbol{I} & \boldsymbol{0} \\ \left(\boldsymbol{B'} - s\boldsymbol{I}\right)^{-1}\boldsymbol{C'} & \boldsymbol{I} \end{bmatrix}\right|$$

or,

$$\left|\left(\boldsymbol{A'} - s\boldsymbol{I}\right)\right| = \left|\left(\boldsymbol{A} - s\boldsymbol{I}\right)\right|\left|\left(\boldsymbol{B'} - s\boldsymbol{I}\right)\right| \tag{2.37}$$

Typically, the eigenvalues of ***A*** are in the left half s-plane if the machine is operating in the negative slope region of the torque-speed characteristics [6]. The eigenvalues of ***B'*** can be given by

$$L_{dc}C_{dc}s^2 + \left(RC_{dc} - \frac{3}{2}\frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{C_{dc}V_{dc}^{\ 2}}\right)s + \left(1 - \frac{3}{2}\frac{\left(V_{ds}I_{ds}+V_{qs}I_{qs}\right)R}{V_{dc}^{\ 2}}\right) = 0 \tag{2.38}$$

which is same as (2.14) since $P_e = \frac{3}{2}\left(V_{ds}I_{ds}+V_{qs}I_{qs}\right)$ and supports criterion (2.15), described in the subsection 2.1.2.1. It gives an important indication that for a small DC-link capacitor value (C_{dc}) and/or the high power load on the machine, term $3(V_{ds}I_{ds}+V_{qs}I_{qs})/(2\cdot C_{dc}V_{dc}^{\ 2})$ may eventually be greater than R/L_{dc}. As a consequence, the coefficient of *'s'* of the quadratic equation (2.38) will become negative. This results in positive real part of the roots of (2.38), which are related to the input L_{dc} – C_{dc} filter and the operating point becomes unstable. These roots can be forced to move into the left half s-plane by introducing the active damping terms.

2.4 Active Damping Terms

As discussed in the previous section, small DC-link capacitor based drive has the unstable operating point at high power load. To stabilize the operating point, active damping terms are defined as

$$\tilde{v}_{ds} = K1 \cdot \tilde{v}_{dc}$$
$$\tilde{v}_{qs} = K2 \cdot \tilde{v}_{dc} \tag{2.39}$$

where $K1$ and $K2$ are constants. The idea here is to add the DC-link voltage dependant voltage components to the *dq*-axes stator voltages of the machine. By introducing these active damping terms, the unstable poles in the original state-space matrix of the drive system may be effectively modified, and the stability of the drive system is greatly improved. The modified state-space matrix involving the active damping terms (2.39) is given by

$$\boldsymbol{A''} = \left[\begin{array}{ccccc:cc} & & \boldsymbol{A}_{5\text{x}5} & & & \frac{K1}{\sigma L_s} & 0 \\ & & & & & \frac{K2}{\sigma L_s} & 0 \\ & & & & & -\frac{K1 \cdot L_o}{\sigma L_s L_r} & 0 \\ & & & & & -\frac{K2 \cdot L_o}{\sigma L_s L_r} & 0 \\ & & & & & 0 & 0 \\ \hdashline -\frac{3}{2}\frac{V_{ds}}{V_{dc}C_{dc}} & -\frac{3}{2}\frac{V_{qs}}{V_{dc}C_{dc}} & 0 & 0 & 0 & \frac{3}{2}\left(\frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{V_{dc}^2 C_{dc}} - \frac{K1 \cdot I_{ds} + K2 \cdot I_{qs}}{V_{dc}C_{dc}}\right) & \frac{1}{C_{dc}} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{dc}} & -\frac{R}{L_{dc}} \end{array}\right] \tag{2.40}$$

This is derived by substituting (2.39) in (2.35) and rearranging the state-space matrix. It can be seen from (2.35) and (2.40) that the term $\frac{3\left(V_{ds}I_{ds}+V_{qs}I_{qs}\right)}{2V_{dc}^2 C_{dc}}$ is now changed to $\frac{3}{2}\left(\frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{V_{dc}^2 C_{dc}} - \frac{K1 \cdot I_{ds} + K2 \cdot I_{qs}}{V_{dc}C_{dc}}\right)$ in the state-space matrix. The effect of these active damping terms may be easily observed. For example, by choosing proper values of

$$K1 = \frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{V_{dc}I_{ds}} \quad K2 = 0 \tag{2.41}$$

or

$$K1 = 0 \quad K2 = \frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{V_{dc}I_{qs}} \tag{2.42},$$

the term $\frac{3}{2}\left(\frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{V_{dc}^2 C_{dc}} - \frac{K1 \cdot I_{ds} + K2 \cdot I_{qs}}{V_{dc}C_{dc}}\right)$ can be forced to be zero and the stability of the drive system becomes independent of the working power range and the DC-link capacitor value. It can be seen form (2.41) and (2.42) that the values of $K1$ and $K2$ are independent of the system parameters.

The signs of $K1$ and $K2$ depend on the signs of I_{ds} and I_{qs}, which in turn depend on the choice of the synchronously rotating reference frame. In this chapter, the *d*-

axis of the synchronously rotating reference frame is aligned with the stator voltage space vector as shown in Figure 2-7. v_{as}, v_{bs}, and v_{cs} are the machine phase voltages. For this reference frame choice, I_{ds} is positive and I_{qs} is negative as shown in Figure 2-7. From (2.41) and (2.42), it can be seen that a positive value of $K1$ and/or a negative value of $K2$ are required for achieving active damping effects.

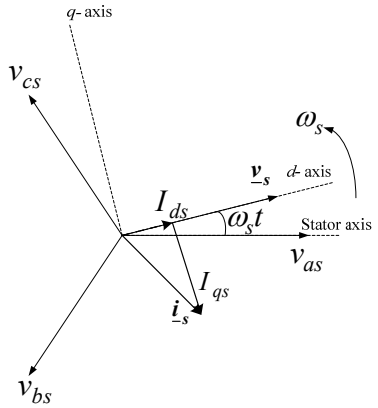


Figure 2-7 Synchronously rotating reference frame.

The values of parameters $K1$ and $K2$ depend on the drive system operating point. The effect of the damping technique will be demonstrated by using an induction machine drive system. The parameters of the drive system to be studied are summarized in Appendix B. The model of the drive system is linearized about a selected working point given in Table 2-3, which exhibits an unstable operating point. The poles of the system are calculated using $\boldsymbol{A'}$ given in (2.35). It can be seen from Table 2-4 that the poles relating to the input L_{dc} –C_{dc} filter have positive real parts for this particular operating point. This shows that the selected operating point of the drive system is unstable. The operating point can be stabilized using the active damping terms given by (2.39). By substituting this operating point values in (2.41), $K1$ is calculated as 0.4. The root locus plot of the system is shown in Figure 2-8, which shows the change in the poles of the drive system as $K1$ is varied. It is important to note that by changing $K1$, the poles related to the induction machine also change. When $K1$ is increased from 0 to 0.4, the induction machine poles still remain in the left half s-plane and will not cause any stability problems.

Table 2-3 Operating Point of the Drive

V_{ds}=225 V	I_{ds}=5.95 A	I_{dr}= − 6.1 A
V_{qs}=0 V	I_{qs}= − 3.8 A	I_{qr}=0.5 A
V_{dc} =565 V	ω_e=305 rad/s	ω_s=314.2 rad/s

Table 2-4 Poles of the System

232 ± 4063j	− 145 ± 286j	− 27.5 ±87.40j	− 66

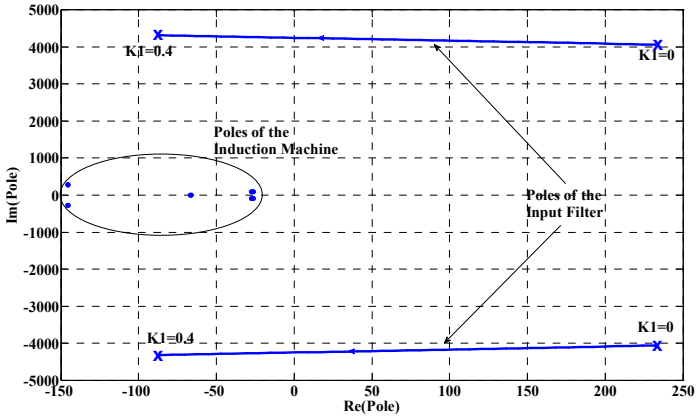


Figure 2-8 Root locus plot of the system as $K1$ varies 0 to 0.4 with $K2$=0.

The effect of the active damping terms on the poles of the induction machine at a particular operating point needs to be evaluated to secure the stability of the operating point. Application of the active damping terms may move the poles of the induction machine towards the right half s-plane. The change in a particular pole ($\delta\lambda$) due to the change in the state-space matrix introduced by adding the active damping terms can be calculated using first-order perturbation theory [2], which gives

$$\delta\lambda = \frac{\boldsymbol{w}^T \cdot \boldsymbol{\delta A} \cdot \boldsymbol{v}}{\boldsymbol{w}^T \cdot \boldsymbol{v}} \tag{2.43}$$

where $\boldsymbol{v}$ and $\boldsymbol{w}$ are the right and left eigenvector of matrix $\boldsymbol{A'}$, and

$$\boldsymbol{\delta A} = \boldsymbol{A''} - \boldsymbol{A'} = \left[\begin{array}{c:c} \boldsymbol{O}_{7\text{x}5} & \begin{matrix} \frac{K1}{\sigma L_s} & 0 \\ \frac{K2}{\sigma L_s} & 0 \\ -\frac{K1L_o}{\sigma L_s L_r} & 0 \\ -\frac{K2L_o}{\sigma L_s L_r} & 0 \\ 0 & 0 \\ -\frac{3}{2}\left(\frac{K1I_{ds} + K2I_{qs}}{V_{dc}C_{dc}}\right) & 0 \\ 0 & 0 \end{matrix} \end{array}\right] \tag{2.44}$$

By solving (2.43), the expression for $\delta\lambda$ can be given as

$$\delta\lambda = \frac{v_6}{\boldsymbol{w}^T \cdot \boldsymbol{v}} \boldsymbol{w}^T \left[\frac{K1}{\sigma L_s} \quad \frac{K2}{\sigma L_s} \quad -\frac{K1 L_o}{\sigma L_s L_r} \quad -\frac{K2 L_o}{\sigma L_s L_r} \quad 0 \quad -\frac{3}{2}\frac{K1 I_{ds} + K2 I_{qs}}{C_{dc} V_{dc}} \quad 0 \right]^T \tag{2.45}$$

where v_6 is the sixth element of the right eigenvector $\boldsymbol{v}$ of matrix $\boldsymbol{A'}$. Equation (2.45) may be used to calculate the change in the poles of the linearized system for different values of $K1$ and $K2$.

The change in the poles of the system for $K1$=0.4 are shown in Table 2-5. These values are calculated using (2.45) and are in agreement with the root locus plot shown in Figure 2-8. It can be seen from the Table 2-5 that the poles of the induction machine are moving towards the right half s-plane, while the poles affected by the input L_{dc}-C_{dc} filter are moving towards the left half s-plane. But the effect of $K1$=0.4 on the induction machine poles is not significant, and all the poles remain in the left half s-plane, giving a stable drive operating point.

Table 2-5 Poles of the Linearized Drive System

***K*1=0, *K*2=0**	***K*1=0.4, *K*2=0**
232 ± *j* 4063	-87.1± *j* 4338
-145 ± *j* 286	-145± *j* 265
-27.5 ± *j* 87.40	-26± *j* 88
-66	-67

2.5 Effect of Damping Terms on the DC-Link Voltage and the Machine Currents in Steady State

It is shown in the previous section that the unstable operating point of the drive system can be stabilized by using active damping terms. These terms add a voltage proportional to the small-signal variation of the DC-link voltage ($\tilde{v}_{dc}$) in the *d*- or *q*-axes voltages of the induction machine. The small-signal variation of the DC-link voltage consists of high frequency signal of the DC-link voltage. Since the equivalent circuit of the rectifier and the grid (Figure 2-2) is excited by the input voltage v_{in} having spectral components only at sixth multiples of the line frequency given by (2.2), the high frequency signal of the DC-link voltage have the same frequency components. From (2.39), the small-signal variation in the *d*- and *q*- axis machine voltage in steady state may be approximated as

$$\begin{aligned} \tilde{v}_{ds} &= K1 \cdot \tilde{v}_{dc} = K1 \sum_{n=1}^{\infty} v_{dcn} = K1 \sum_{n=1}^{\infty} V_{dcn} \cos\left(6n\omega_g t + \phi_n\right) \\ \tilde{v}_{qs} &= K2 \cdot \tilde{v}_{dc} = K2 \sum_{n=1}^{\infty} v_{dcn} = K2 \sum_{n=1}^{\infty} V_{dcn} \cos\left(6n\omega_g t + \phi_n\right) \end{aligned} \tag{2.46}$$

where v_{dcn} is the 6*n*th harmonics of the DC-link voltage having amplitude V_{dcn} and phase Φ_n. The effect of PWM on the machine harmonics voltages is neglected for simplicity. These high frequency components of the machine voltage will induce the high frequency components in the machine currents, which in turn introduce the

high frequency components in the DC-link current which are governed by (2.9). An expression for the high frequency component of the machine current and the DC-link current will be derived in this section. This DC-link current is also an input of the equivalent circuit of the rectifier and the grid as shown in Figure 2-2 and affects the DC-link voltage. A simplified closed form solution for the DC-link voltage harmonics components is derived in this section using only first-order terms. Using this solution, it is shown that the same amplitude of DC-link voltage harmonics can be achieved by applying the active damping terms to either the *d*-axis or the *q*- axis.

2.5.1 The Machine Current

The active damping terms introduce the harmonic components of sixth multiples of line frequency in the machine *d*- and *q*- axes voltages. They produce harmonic components in the machine currents, which are governed by the leakage inductances of the induction machine only. This is because the impedance offered by induction machine at that frequency may be approximated as the impedance due to the sum of the stator leakage inductance (L_{ls}) and the rotor leakage inductance (L_{lr}) in the stationary reference frame as shown in Figure 2-9 [70].

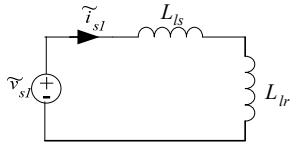


Figure 2-9 Equivalent circuit of the induction machine for a harmonic component.

Using (2.46), the machine phase voltage in the stationary reference frame, because of the 6*n*th harmonic component of the DC-link voltage, can be given by

$$\begin{aligned} v_{a,n} &= K1\,V_{dcn}\cos\left(6n\omega_g t+\phi_n\right)\cos\left(\omega_s t\right)-K2\,V_{dcn}\cos\left(6n\omega_g t+\phi_n\right)\sin\left(\omega_s t\right) \\ v_{a,n} &= \frac{K\,V_{dcn}}{2}\left(\cos\left(\left(6n\omega_g-\omega_s\right)t+\phi_n-\phi_k\right)+\cos\left(\left(6n\omega_g+\omega_s\right)t+\phi_n+\phi_k\right)\right) \end{aligned} \tag{2.47}$$

where $K=\sqrt{K1^2+K2^2}$, $\phi_k=\tan^{-1}\left(\frac{K2}{K1}\right)$, and $v_{a,n}$ denotes the voltage of phase *a* of the machine caused by the 6*n*th harmonic component of the DC-link voltage added as the active damping terms. Since the machine acts as an inductance for high frequencies, the machine current for phase *a* ($i_{a,n}$) due to $v_{a,n}$ may be given as

$$\begin{aligned} i_{a,n} &= \frac{K\,V_{dcn}}{2\left(6n\omega_g-\omega_s\right)\left(L_{ls}+L_{lr}\right)}\cos\left(\left(6n\omega_g-\omega_s\right)t+\phi_n-\phi_k-\frac{\pi}{2}\right) \\ &+\frac{K\,V_{dcn}}{2\left(6n\omega_g+\omega_s\right)\left(L_{ls}+L_{lr}\right)}\cos\left(\left(6n\omega_g+\omega_s\right)t+\phi_n+\phi_k-\frac{\pi}{2}\right) \end{aligned} \tag{2.48}$$

Using phase symmetry of the three-phase machine and park's transformation, the *d*- and *q*- axis machine currents, due to the 6*n*th harmonic component of the DC-link

voltage added as the active damping terms, denoted as i_{dsn} and i_{qsn}, are expressed as given by

$$\begin{aligned} i_{dsn} &= \frac{K\,V_{dcn}}{2\left(L_{ls}+L_{lr}\right)}\left(\frac{\cos\left(6n\omega_g\,t+\phi_n-\phi_k-\frac{\pi}{2}\right)}{\left(6n\omega_g-\omega_s\right)}+\frac{\cos\left(6n\omega_g\,t+\phi_n+\phi_k-\frac{\pi}{2}\right)}{\left(6n\omega_g+\omega_s\right)}\right) \\ i_{qsn} &= \frac{K\,V_{dcn}}{2\left(L_{ls}+L_{lr}\right)}\left(-\frac{\sin\left(6n\omega_g\,t+\phi_n-\phi_k-\frac{\pi}{2}\right)}{\left(6n\omega_g-\omega_s\right)}+\frac{\sin\left(6n\omega_g\,t+\phi_n+\phi_k-\frac{\pi}{2}\right)}{\left(6n\omega_g+\omega_s\right)}\right) \end{aligned} \tag{2.49}$$

Using $K=\sqrt{K1^2+K2^2}$, $\sin\phi_k=\frac{K2}{K}$, and $\cos\phi_k=\frac{K1}{K}$; this can be simplified as

$$\begin{aligned} i_{dsn} &= \frac{V_{dcn}}{2\left(L_{ls}+L_{lr}\right)}\left(\frac{K1\cdot\sin\left(6n\omega_g\,t+\phi_n\right)12n\omega_g}{\left(6n\omega_g-\omega_s\right)\left(6n\omega_g+\omega_s\right)}-\frac{K2\cdot\cos\left(6n\omega_g\,t+\phi_n\right)2\omega_s}{\left(6n\omega_g-\omega_s\right)\left(6n\omega_g+\omega_s\right)}\right) \\ i_{qsn} &= \frac{V_{dcn}}{2\left(L_{ls}+L_{lr}\right)}\left(\frac{K1\cdot\cos\left(6n\omega_g\,t+\phi_n\right)2\omega_s}{\left(6n\omega_g-\omega_s\right)\left(6n\omega_g+\omega_s\right)}+\frac{K2\cdot\sin\left(6n\omega_g\,t+\phi_n\right)12n\omega_g}{\left(6n\omega_g-\omega_s\right)\left(6n\omega_g+\omega_s\right)}\right) \end{aligned} \tag{2.50}$$

The *d*- axis machine current contains two components. The first component, which is proportional to $K1$ and $12n$ times the grid frequency, is the current induced by the *d*-axis voltage. The second component, which is proportional $K2$ and twice the synchronous frequency, is the current induced due to the *q*-axis voltage. Similar components are present in the *q*-axis machine harmonic current. If $\omega_s=\omega_g$, in the *d*-axis current, the harmonics current induced by the *d*-axis active damping term will be $6n$ times the harmonics current induced by the *q*-axis active damping term with same gain ($K1=K2$).

2.5.2 The DC-link Current

It can be seen from (2.50) that the *d*- and *q*- axes currents have frequency equal to $6n\omega_g$ due to the applied machine voltage of same frequency. The machine currents and voltages decide the DC-link current (i_{dc}) as given by (2.9). Using only first-order terms of Taylor series expansion of (2.9), for $v_{dcs}=v_{dc}$, the small-signal variation of the DC-link current may be given by

$$\tilde{i}_{dc}=\frac{3}{2}\frac{1}{V_{dc}}\left(\tilde{v}_{ds}I_{ds}+\tilde{v}_{qs}I_{qs}+V_{ds}\tilde{i}_{ds}+V_{qs}\tilde{i}_{qs}\right)-\frac{3}{2}\frac{1}{V_{dc}^2}\left(V_{ds}I_{ds}+V_{qs}I_{qs}\right)\tilde{v}_{dc} \tag{2.51}$$

If the small-signal variation is approximated as the high frequency component, the $6n$th harmonic component of the DC-link current (i_{dcn}) may be given by

$$i_{dcn} = \frac{3}{2}\frac{1}{V_{dc}}\left(K1\cdot v_{dcn}I_{ds} + K2\cdot v_{dcn}I_{qs} + V_{ds}i_{dsn} + V_{qs}i_{qsn}\right) - \frac{3}{2}\frac{1}{V_{dc}^2}\left(V_{ds}I_{ds} + V_{qs}I_{qs}\right)v_{dcn}$$

Since $V_{qs} = 0$;

$$i_{dcn} = \frac{3}{2}\frac{1}{V_{dc}}\left(K1\cdot v_{dcn}I_{ds} + K2\cdot v_{dcn}I_{qs} + V_{ds}i_{dsn}\right) - \frac{3}{2}\frac{1}{V_{dc}^2}\left(V_{ds}I_{ds}\right)v_{dcn} \tag{2.52}$$

In steady state, the machine is operated with the synchronous speed of 50 Hz, which is equal to grid supply frequency (ω_s=ω_g). In this case, the *d*-axis and the *q*-axis active damping terms have different effect on the harmonics components of the DC-link current which are governed by (2.52). If the *d*-axis active damping term is only applied (*K*2=0), using (2.46), (2.50), and (2.52), the 6*n*th harmonic component of the DC-link current (i_{dcn}) is given by

$$i_{dcn}\big|_{K2=0} = \frac{3}{2}\frac{1}{V_{dc}}\left(K1\cdot V_{dcn}\cos(6n\omega_g t + \phi_n)I_{ds} + V_{ds}\frac{K1\cdot V_{dcn}}{2(L_{ls}+L_{lr})}\left(\sin\left(6n\omega_g t + \phi_n\right)\frac{12n}{(6n-1)(6n+1)\omega_g}\right)\right)$$
$$-\frac{3}{2}\frac{1}{V_{dc}^2}\left(V_{ds}I_{ds}\right)V_{dcn}\cos(6n\omega_g t + \phi_n)$$

or,

$$i_{dcn}\big|_{K2=0} = \frac{3}{2}\frac{1}{V_{dc}}\left(\left(K1 - \frac{V_{ds}}{V_{dc}}\right)\cdot V_{dcn}\cos(6n\omega_g t + \phi_n)I_{ds} + V_{ds}\frac{K1\cdot V_{dcn}}{2(L_{ls}+L_{lr})}\left(\sin\left(6n\omega_g t + \phi_n\right)\frac{12n}{(6n-1)(6n+1)\omega_g}\right)\right) \tag{2.53}$$

Similarly, from (2.52), the 6*n*th harmonic component of the DC-link current (i_{dcn}), for *K*1=0, is given by

$$i_{dcn}\big|_{K1=0} = \frac{3}{2}\frac{1}{V_{dc}}\left(K2\cdot v_{dcn}I_{qs} + V_{ds}i_{dsn}\right) - \frac{3}{2}\frac{1}{V_{dc}^2}\left(V_{ds}I_{ds}\right)v_{dcn} \tag{2.54}$$

Using (2.46) and (2.50), v_{dcn} and i_{dsn} is replaced in (2.54) for ω_s=ω_g.

$$i_{dcn}\big|_{K1=0} = \frac{3}{2}\frac{1}{V_{dc}}\left(K2\cdot V_{dcn}\cos(6n\omega_g t + \phi_n)I_{qs} + V_{ds}\frac{K2\cdot V_{dcn}}{2(L_{ls}+L_{lr})}\left(\cos\left(6n\omega_g t + \phi_n\right)\frac{-2}{(6n-1)(6n+1)\omega_g}\right)\right)$$
$$-\frac{3}{2}\frac{1}{V_{dc}^2}V_{ds}I_{ds}V_{dcn}\cos(6n\omega_g t + \phi_n)$$

or,

$$i_{dcn}\big|_{K1=0} = \frac{3}{2}\frac{V_{dcn}}{V_{dc}}\left(K2\cdot I_{qs} - \frac{K2\cdot V_{ds}}{2(L_{ls}+L_{lr})}\frac{2}{(6n-1)(6n+1)\omega_g} - \frac{V_{ds}I_{ds}}{V_{dc}}\right)\cos(6n\omega_g t + \phi_n) \tag{2.55}$$

It can be seen from (2.53) and (2.55) that the DC-link current also consists of the high frequency components with frequency $6n\omega_g$ introduced by the active damping terms for the condition of ω_s=ω_g. In addition, the amplitude of the harmonic component of the DC-link current is a function of the amplitude of the harmonic component of DC-link voltage as shown in (2.53) and (2.55).

2.5.3 The DC-link Voltage

The inputs to the equivalent circuit of the rectifier and the grid are the input voltage (v_{in}) and the DC-link current (i_{dc}) as shown in Figure 2-2 and they have the spectral components of sixth multiples of the line frequency ((2.2), (2.53), and (2.55)). For the steady state analysis of the DC-link voltage, for a 6nth frequency component, the equivalent circuit of input L_{dc}-C_{dc} filter is given in Figure 2-10.

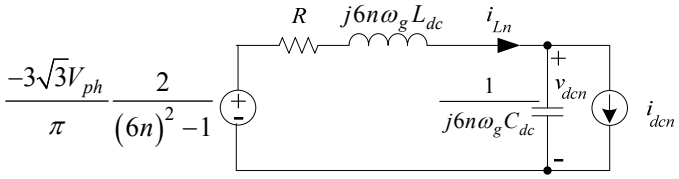


Figure 2-10 Equivalent circuit of the input L_{dc}-C_{dc} filter for a harmonic component.

Using superposition theorem, a particular frequency component of the v_{dc} is given as

$$\underline{\boldsymbol{v}}_{\boldsymbol{dcn}} = \frac{1}{1-L_{dc}C_{dc}\left(6n\omega_g\right)^2+j\left(RC_{dc}6n\omega_g\right)}\left(-\frac{3\sqrt{3}V_{ph}}{\pi}\frac{2}{(6n)^2-1}-\underline{\boldsymbol{i}}_{\boldsymbol{dcn}}\left(R+j6n\omega_g L_{dc}\right)\right) \tag{2.56}$$

'_' shows the phasor representation of a particular variable.

To calculate the harmonic component of v_{dc}, the harmonic component of the DC-link current, which is dependent on the active damping terms as described in the previous subsection, is required. Substituting $K1 = \frac{V_{ds}}{V_{dc}} = 0.4$ in (2.53), the 6nth harmonic component of the DC-link current can be expressed in phasor form as given by

$$\underline{\boldsymbol{i}}_{\boldsymbol{dcn}}\big|_{K2=0,K1=0.4} = \frac{3}{2}\frac{-j\underline{\boldsymbol{v}}_{\boldsymbol{dcn}}}{V_{dc}}\left(\frac{0.4V_{ds}}{2(L_{ls}+L_{lr})}\frac{12n}{(6n-1)(6n+1)\omega_g}\right) \tag{2.57}$$

By substituting (2.57) in (2.56) and rearranging the terms, the 6nth harmonic component of DC-link voltage is given by

$$\underline{\boldsymbol{v}}_{\boldsymbol{dcn}}\big|_{K2=0,K1=0.4} = \frac{-\frac{3\sqrt{3}V_{ph}}{\pi}\frac{2}{(6n)^2-1}-\frac{3}{2}\frac{\left(-j\,\underline{\boldsymbol{v}}_{\boldsymbol{dcn}}\big|_{K2=0,K1=0.4}\right)}{V_{dc}}\left(\frac{0.4V_{ds}}{2(L_{ls}+L_{lr})}\frac{12n}{(6n-1)(6n+1)\omega_g}\right)\left(R+j6n\omega_g L_{dc}\right)}{1-L_{dc}C_{dc}\left(6n\omega_g\right)^2+j\left(RC_{dc}6n\omega_g\right)}$$

or, $$\underline{\boldsymbol{v}}_{\boldsymbol{dcn}}\big|_{K2=0,K1=0.4} = \frac{-\frac{3\sqrt{3}V_{ph}}{\pi}\frac{2}{(6n)^2-1}}{\underline{\boldsymbol{Z1}}} \tag{2.58}$$

where $$\underline{\boldsymbol{Z1}} = 1-L_{dc}C_{dc}\left(6n\omega_g\right)^2+j\left(RC_{dc}6n\omega_g\right)-\frac{3}{2}\frac{j\left(R+j6n\omega_g L_{dc}\right)}{V_{dc}}\left(\frac{0.4V_{ds}}{2(L_{ls}+L_{lr})}\frac{12n}{(6n-1)(6n+1)\omega_g}\right)$$

The DC-link voltage amplitude for a particular harmonic component is given by (2.58) when the active damping term is added to the *d*-axis machine voltage. The effect of the active damping term in the *q*-axis machine voltage can also be analyzed in the same way. From (2.55), the DC-link current can be expressed in phasor form as given by

$$\underline{\boldsymbol{i}}_{\boldsymbol{dcn}}\big|_{K1=0} = \frac{3}{2}\frac{\underline{v}_{dcn}}{V_{dc}}\left(K2\cdot I_{qs} - \frac{K2\cdot V_{ds}}{2(L_{ls}+L_{lr})}\frac{2}{(6n-1)(6n+1)\omega_g} - \frac{V_{ds}I_{ds}}{V_{dc}} \right) \tag{2.59}$$

By substituting (2.59) in (2.56) and rearranging the terms, the 6*n*th harmonic component of the DC-link voltage is given by

$$\underline{\boldsymbol{v}}_{\boldsymbol{dcn}}\big|_{K1=0} = \frac{\left(-\frac{3\sqrt{3}V_{ph}}{\pi}\frac{2}{(6n)^2-1} - \frac{3}{2}\frac{\underline{\boldsymbol{v}}_{\boldsymbol{dcn}}\big|_{K1=0}}{V_{dc}}\left(K2I_{qs} - \frac{K2V_{ds}}{2(L_{ls}+L_{lr})}\frac{2}{(6n-1)(6n+1)\omega_g} - \frac{V_{ds}I_{ds}}{V_{dc}} \right)\left(R + j6n\omega_g L_{dc}\right) \right)}{1 - L_{dc}C_{dc}\left(6n\omega_g\right)^2 + j\left(RC_{dc}6n\omega_g\right)}$$

$$\underline{\boldsymbol{v}}_{\boldsymbol{dcn}}\big|_{K1=0} = \frac{\left(-\frac{3\sqrt{3}V_{ph}}{\pi}\frac{2}{(6n)^2-1} \right)}{\underline{\boldsymbol{Z2}}} \tag{2.60}$$

where,

$$\underline{\boldsymbol{Z2}} = 1 - L_{dc}C_{dc}\left(6n\omega_g\right)^2 + j\left(RC_{dc}6n\omega_g\right) + \frac{3}{2}\frac{\left(R + j6n\omega_g L_{dc}\right)}{V_{dc}}\left(K2I_{qs} - \frac{K2V_{ds}}{2(L_{ls}+L_{lr})}\frac{2}{(6n-1)(6n+1)\omega_g} - \frac{V_{ds}I_{ds}}{V_{dc}} \right)$$

From (2.58) and(2.60), same amplitude of v_{dcn} can be achieved by applying the damping terms either in the *d*-axis or in the *q*-axis for a particular value of *n* if $|\underline{\boldsymbol{Z1}}|=|\underline{\boldsymbol{Z2}}|$. The resonance frequency of the input L_{dc}-C_{dc} filter is 650 Hz in this case, which causes low impedance of the input L_{dc}-C_{dc} filter for 600 Hz (*n*=2). *K*1=0.4 and *K*2=−1.3 result in $|\underline{\boldsymbol{Z1}}|=|\underline{\boldsymbol{Z2}}|$ for *n*=2. The key factor, which affects the amplitude of v_{dcn}, is the current drawn by the inverter (i_{dcn}). It can be seen from (2.52) that the DC-link current is affected by the *d*-axis machine current (i_{dsn}), which in turn is proportional to 12*n* times the *d*-axis voltage plus 2 times the *q*-axis voltage (2.50). So a higher value of *K*2 is required to achieve the same damping since the current induced in the *d*-axis by the *q*-axis voltage is low.

2.6 Experimental and Simulation Results

The active damping technique is simulated and implemented in an open loop *V/f* controlled induction machine drive. The block diagram of the drive with controller is shown in Figure 2-11. The ASD parameters are given in Table 2-3. Since the choice of the synchronously rotating reference frame does not have any impact on the system model, the *d*-axis is aligned to the stator voltage vector in this case. The equations for the voltage reference in the synchronously rotating *dq*- reference frame are given by

$$\begin{aligned} v_{sd} &= V_m + K1 \cdot \tilde{v}_{dc} \\ v_{sq} &= K2 \cdot \tilde{v}_{dc} \end{aligned} \tag{2.61}$$

The active damping terms, which are proportional to the small-signal variation of the DC-link voltage, are added to the *d*- and *q*- axis voltage as given in (2.61). The small-signal variation is approximated as the high frequency signal in simulation and experiments, which is generated by applying the signal to a high-pass filter. A first-order high-pass filter with cutoff frequency less than the sixth multiples of the line frequency is used in this chapter for generating the small-signal variation of the DC-link voltage, which does not block any high frequency component of the DC-link voltage. The cut off frequency of the high-pass filter is chosen as 10 Hz. From (2.61), the equations for the PWM voltage reference in stationary reference frame are given as

$$\begin{aligned} v_1 &= \frac{1}{v_{dc}}\left(\left(V_m + K1 \cdot \tilde{v}_{dc}\right)\cos\left(\omega_s t\right) - \left(K2 \cdot \tilde{v}_{dc}\right)\sin\left(\omega_s t\right)\right) \\ v_2 &= \frac{1}{v_{dc}}\left(\left(V_m + K1 \cdot \tilde{v}_{dc}\right)\cos\left(\omega_s t - \frac{2\pi}{3}\right) - \left(K2 \cdot \tilde{v}_{dc}\right)\sin\left(\omega_s t - \frac{2\pi}{3}\right)\right) \\ v_3 &= \frac{1}{v_{dc}}\left(\left(V_m + K1 \cdot \tilde{v}_{dc}\right)\cos\left(\omega_s t + \frac{2\pi}{3}\right) - \left(K2 \cdot \tilde{v}_{dc}\right)\sin\left(\omega_s t + \frac{2\pi}{3}\right)\right) \end{aligned} \tag{2.62}$$

Since the PWM voltage reference should be scaled to DC-link voltage, the reference voltage equations have division of the DC-link voltage (v_{dc}).

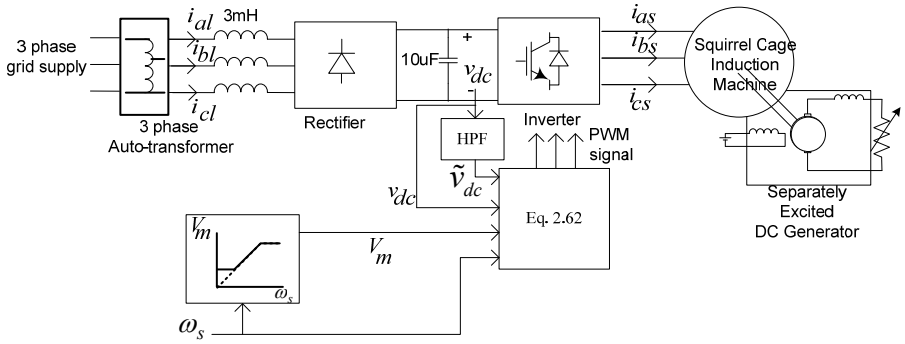


Figure 2-11 Block diagram of ASD.

The simulation results for the DC-link voltage (v_{dc}), the input line current (i_{s1}), and the machine current (i_1) are shown Figure 2-12 (a), (b), (c), and (d) for *K1*=0,

K2=0; *K1*=0.4, *K2*=0; *K1*=0, *K2*= −1.3; and *K1*=0, *K2*= −1.2, respectively. Figure 2-12 (e) shows the FFT plot of the DC-link voltage (v_{dc}) for the three cases. It can be seen that the DC-link voltage has very high voltage amplitude of 95 V at 600 Hz without any active damping terms. The damping of the DC-link voltage is achieved by adding the damping terms to either the *d*- or *q*- axis machine voltage. It was shown in the previous section that with *K*1=0.4, *K*2=0 and *K*1=0 and *K*2= −1.3 have the same effect on the DC-link voltage at 600 Hz, but it is not the same for the two cases since only first-order terms are considered for analysis and the effect of PWM on the machine harmonics voltage was also neglected. It is shown in Figure 2-12 (e) that the 600 Hz harmonics of the DC-link voltage has the same amplitude of 39 V for *K*1=0.4, *K*2=0 and *K*1=0 and *K*2= −1.2, and it is verified by the experiments as well.

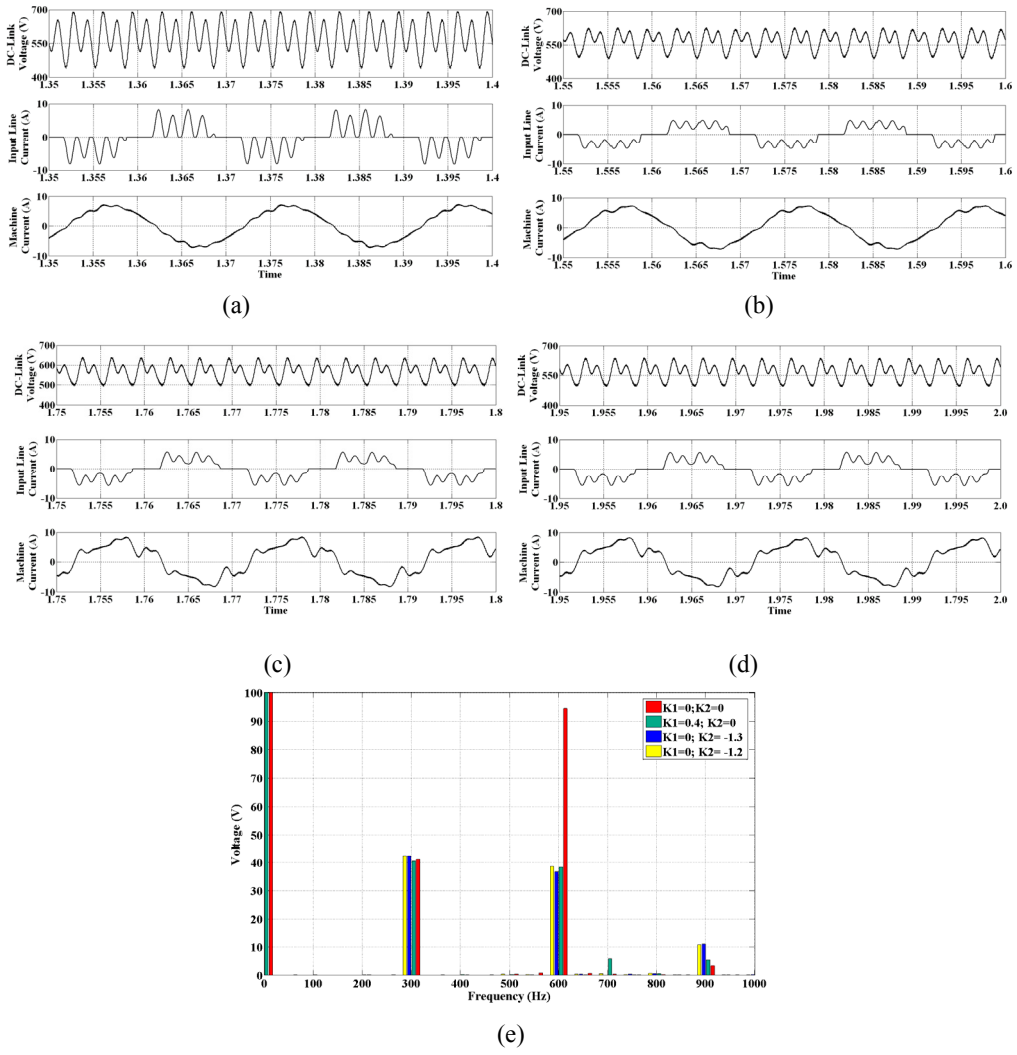


Figure 2-12 Simulation results for the ASD. (a) *K*1=0, *K*2=0. (b) *K*1=0.4, *K*2=0. (c) *K*1=0, *K*2= −1.3. (d) *K*1=0, *K*2= −1.2. (e) FFT plot of the DC-link voltage v_{dc}.

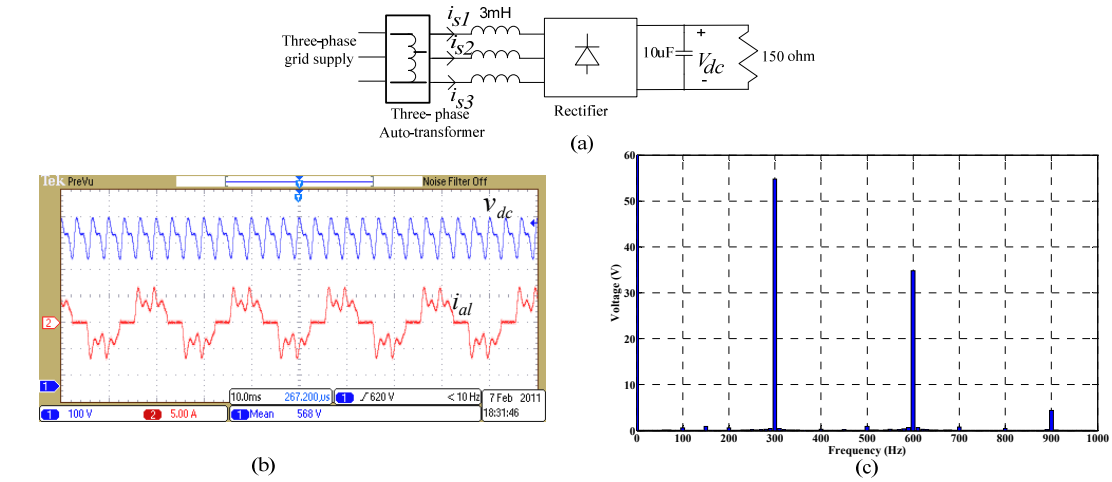


Figure 2-13 (a) Block diagram of the circuit with resistive load. (b) DC-link voltage and line current for resistive load on diode bridge. (c) FFT plot of the DC-link voltage.

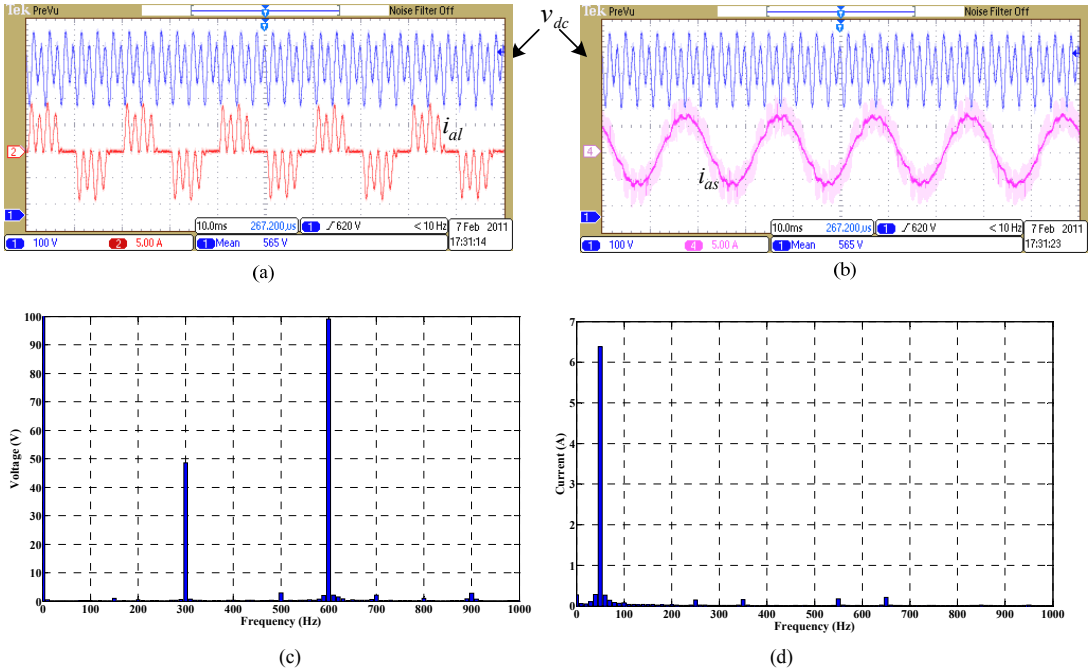


Figure 2-14 (a) DC-link voltage and line current. (b) DC-link voltage and machine current. (c) FFT plot of the DC-link voltage. (d) FFT plot of the machine current with induction machine as load with $K1$=$K2$=0.

The ASD (a constant power load) acts as negative impedance to the input L_{dc}-C_{dc} filter, which may cause an unstable operating point at high power. To show the effect of the unstable operating point of the drive, the diode bridge rectifier is loaded with a resistive load of 150 Ω as shown in Figure 2-13, and the results are compared when the rectifier is loaded with the induction machine drive. Figure 2-13(a) shows the block diagram of the circuit used when the rectifier is loaded with resistive load. Figure 2-13(b) shows the DC-link voltage and the input line current in that case.

Figure 2-13(c) shows the FFT plot of the DC-link voltage at this condition. Figure 2-14(a) shows the DC-link voltage and the input line current with the induction machine as a load to the inverter. Figure 2-14(b) shows the DC-link voltage and the machine phase current. Figure 2-14(c) and (d) show the FFT plot of the DC-link voltage and the machine current, respectively. It can be seen from Figure 2-14(c) that the 600 Hz component of the DC-link voltage has increased to 100 V when the resistive load is replaced with the two-level converter followed by the induction machine.

Figure 2-14 shows the condition of unstable operating point for the drive. This operating point can be stabilized by changing the values of $K1$ and/or $K2$ as described in Section 2.4. Figure 2-15 shows the system response for $K1$=0.4 and $K2$=0. The DC-link voltage waveform and the input line current are shown in Figure 2-15(a). Figure 2-15(b) shows the DC-link voltage and the machine phase current. The FFT plot of the DC-link voltage and the FFT plot for the machine current are shown in Figure 2-15(c) and (d), respectively. It can be seen from Figure 2-15(c) that the amplitude of 600 Hz harmonics component of the DC-link voltage is reduced to 40 V in this case as compared to 100 V as shown in Figure 2-14(c), while the machine current WTHD is increased to 1.66%.

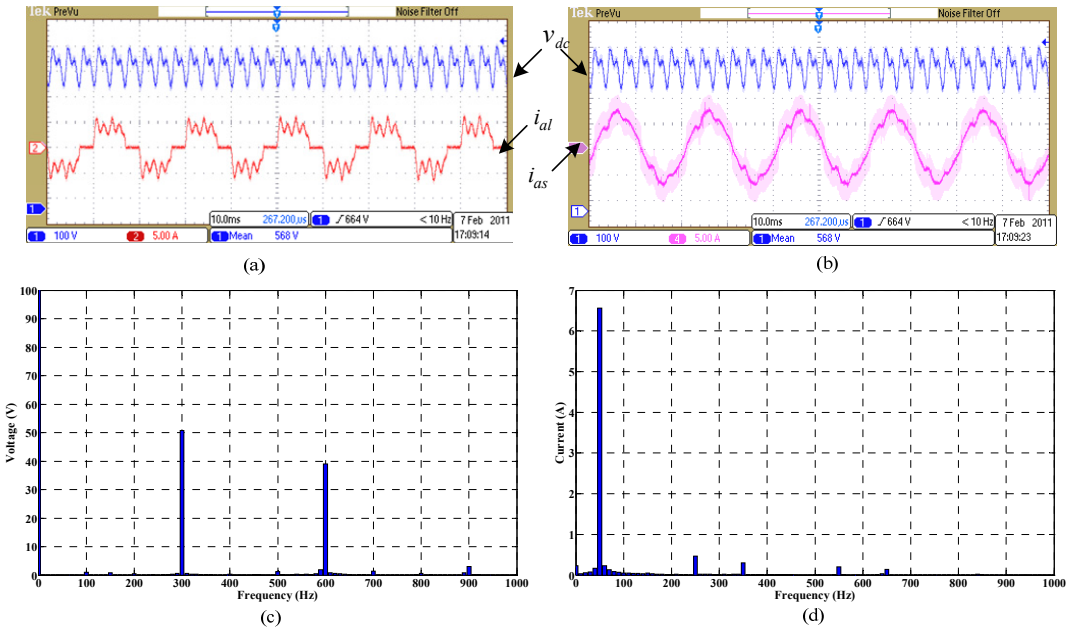


Figure 2-15 (a) DC-link voltage and input line current. (b) DC-link voltage and machine current. (c) FFT plot of the DC-link voltage. (d) FFT plot of the machine current for $K1$=0.4 & $K2$=0.

It was shown in the previous section that the same amplitude of the 600 Hz component of the DC-link voltage can be achieved by either $K1$=0.4 or $K2 = -1.3$. Since only first-order term was considered in analysis, it has been seen that $K2 = -1.2$ is required to achieve that performance. Figure 2-16 shows the response of the system with $K1$=0 & $K2 = -1.2$. Figure 2-16(a) shows the DC-link voltage and the input line current. The machine phase current and the DC-link voltage waveform are shown in Figure 2-16(b). The FFT plot of the DC-link voltage and the FFT plot of

the machine current are shown in Figure 2-16(c) and (d), respectively for this case. With $K1$=0 & $K2$= −1.2, the machine current WTHD is 5.14%.

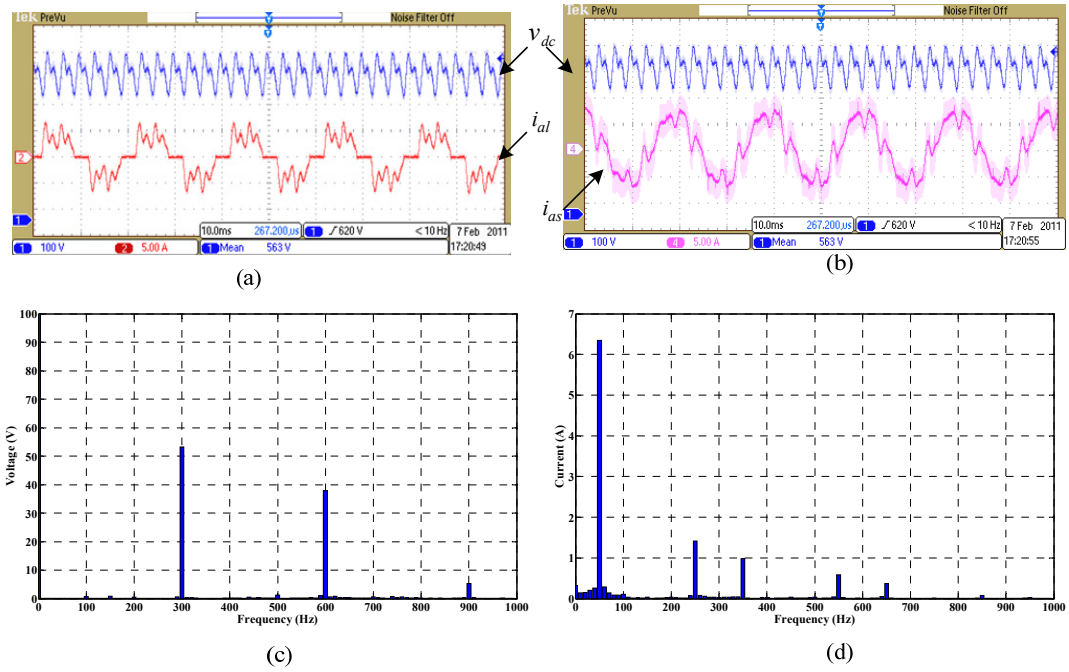


Figure 2-16 (a) DC-link voltage and input line current. (b) DC-link voltage and machine stator current. (c) FFT plot of the DC-link voltage. (d) FFT plot for the machine current for $K1$=0 & $K2$= −1.2.

The input current THD and the machine current WTHD are compared in all four cases in Table 2-6. In case of the induction machine as a load, the minimum input line current THD is obtained by $K1$=0.4 & $K2$=0. It is seen that same DC-link harmonics voltage can be obtained by different values of $K1$ and $K2$. But the effect of these parameters on the input line current and the machine current are not the same because of the phase angle of the damping term $\tilde{v}_{dc}$ with respect to the voltage vector (d-axis) is different. It is seen that the best performance is achieved in terms of the machine current and the input line current if the damping term is added to the d-axis stator voltage of the induction machine only ($K2$=0).

Table 2-6 Line Current and Machine Current Harmonics Distortion

Conditions		Line Current THD	Machine Current WTHD
Resistive Load		43%	NA
Induction Machine as Load	K1=0 & K2=0	78%	0.92%
	K1=0.4 & K2= 0	41.2%	1.66%
	K1=0 & K2= −1.2	45.3%	5.14%

2.7 Summary and Conclusion

A detailed model of a drive system linearized about an operating point is presented in this chapter. The model suggests that the operating point may become

unstable for high power load for a small DC-link capacitor based adjustable speed drive. A new method of stabilizing the operating point is presented using a detailed model of the drive system. To stabilize the operating point, a simple active damping terms are used, which are not dependent on the system parameters. The effects of damping terms on the DC-link voltage, the input line current, and the machine current are also analyzed using first-order approximation. It is shown analytically and experimentally that the active damping term added to the in-phase fundamental component of the voltage space phasor results in the minimum machine current distortion while stabilizing the operating point. The proposed method is implemented in an induction machine based drive system, but the approach is general and it can be used for other kinds of machine as well.

Chapter 3

Active Damping Technique in Vector-Controlled Drive

The most common machine used in adjustable speed drives is the induction machine because of the robustness of this machine. It has been focus of research since last century. With the advent of the voltage source inverter, the induction machine fed by the voltage source inverter has become the most popular drive topology. There are different control strategies developed for the induction machine based drive system. The control strategies can be classified into the scalar and vector control.

The scalar control methods are based on the steady state model of the induction machine. Therefore, they have low dynamic performance, which makes it suitable for low performance applications, such as pumps or fans. A common scalar control method is the constant *V*/*f* control. In this method, the machine is operated with constant stator flux with an assumption of negligible voltage drop across stator resistance [8].

A high dynamic performance, similar to a DC machine, can be obtained by using the vector control. In the DC machine, the torque is produced by the interaction of the flux and the machine armature current. Since they are decoupled from each other, an excellent dynamic performance can be achieved in a DC machine [8]. To get high dynamic performance in the induction machine, a linear relationship between the torque and the control variable is required provided that the amplitude of the flux is constant. This relationship can be obtained if the *d*-axis of the synchronous reference frame is aligned with the stator flux vector, the rotor flux vector, or the air-gap flux vector. Based on this, the vector control of the induction machine can be classified as the stator flux orientation, the rotor flux orientation, and the air-gap flux orientation control.

The rotor flux orientation control of the induction machine can achieve an excellent dynamic performance if the speed sensor is used [56]. To improve the system reliability and reduce cost (especially for low cost drives), it is recommended to avoid the mechanical speed sensor. It can be done if the flux is estimated using electrical measurements. In a squirrel cage induction machine, rotor electrical variables are not available for measurements. In this case, the rotor flux estimation depends on the machine parameters such as the leakage inductance. On the other

hand, the stator flux estimation depends on the stator resistance only. It is shown in [28] that the estimation of the stator flux is more accurate than the estimation of the rotor flux from the stator variable measurements.

A stator flux oriented vector control of the induction machine is considered in this chapter. The model of the induction machine in the stator flux oriented reference frame, which was presented in [8], is described in Section 3.1 for sake of completeness. The design of the current controller, the speed estimator, and the flux observer based on this model are presented in Section 3.2. The active damping technique, presented in the previous chapter, is used for the vector controlled induction machine drive. The effect of the current controller bandwidth on the active damping terms in the stator flux oriented vector control is presented in Section 3.3.

3.1 Induction Machine Model in Stator Flux Oriented Reference Frame

The stator flux vector, which is aligned with the *d*- axis of the reference frame as shown in Figure 3-1, can be defined as

$$\underline{\boldsymbol{\psi}}_{\boldsymbol{s}} = L_o \underline{\boldsymbol{i}}_{\boldsymbol{ms}} \tag{3.1}$$

where

$$\underline{\boldsymbol{i}}_{\boldsymbol{ms}} = i_{ms} e^{j\mu} = (1+\sigma_s)\underline{\boldsymbol{i}}_{\boldsymbol{s}} + \underline{\boldsymbol{i}}_{\boldsymbol{r}} e^{j\varepsilon} \tag{3.2}$$

represents a stator based magnetizing current, where

$$\sigma_s = \frac{L_{ls}}{L_o}, \tag{3.3}$$

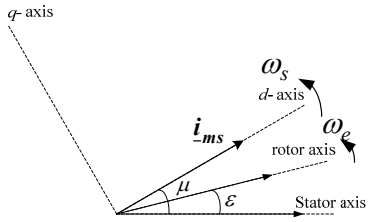


Figure 3-1 Stator flux oriented reference frame.

the angle between the stator axis and the stator flux vector (*d*-axis) is μ, and the angle between the stator axis and rotor axis is ε.

The stator and rotor variables are defined in (2.21) - (2.24) and are repeated here for sake of readability. The stator voltage and current phasors in the stator flux oriented reference frame can be expressed in terms of the stator voltage and current phasors in the stator reference frame and the angle between the reference frames as

$$v_{ds} + j v_{qs} = \underline{\boldsymbol{v}}_{\boldsymbol{s}} e^{-j\mu} \tag{3.4}$$

$$i_{ds} + j i_{qs} = \underline{\boldsymbol{i}}_{\boldsymbol{s}} e^{-j\mu} \tag{3.5}$$

Similarly, the rotor voltage and current phasors in the stator flux oriented reference frame can be expressed in terms of the rotor voltage and current phasors in the rotor reference frame and the angle between the reference frames as

$$v_{dr} + j\,v_{qr} = \underline{\boldsymbol{v}}_{\boldsymbol{r}} e^{-j(\mu-\varepsilon)} \tag{3.6}$$

$$i_{dr} + j\,i_{qr} = \underline{\boldsymbol{i}}_{\boldsymbol{r}} e^{-j(\mu-\varepsilon)} \tag{3.7}$$

After expressing the stator and rotor voltages and currents in the stator flux oriented reference frame, the machine voltage equations need to be transformed into that frame. The stator voltage equation given by (2.19) can be written as

$$r_s \underline{\boldsymbol{i}}_{\boldsymbol{s}} + L_o \frac{d}{dt}\left(\frac{L_s}{L_o} \underline{\boldsymbol{i}}_{\boldsymbol{s}} + \underline{\boldsymbol{i}}_{\boldsymbol{r}} e^{j\varepsilon} \right) = \underline{\boldsymbol{v}}_{\boldsymbol{s}}$$

or,

$$r_s \underline{\boldsymbol{i}}_{\boldsymbol{s}} + L_o \frac{d}{dt}\left(\left(1 + \frac{L_{ls}}{L_o} \right) \underline{\boldsymbol{i}}_{\boldsymbol{s}} + \underline{\boldsymbol{i}}_{\boldsymbol{r}} e^{j\varepsilon} \right) = \underline{\boldsymbol{v}}_{\boldsymbol{s}} \tag{3.8}$$

Using (3.2) and (3.3), equation (3.8) can be simplified as

$$r_s \underline{\boldsymbol{i}}_{\boldsymbol{s}} + L_o \frac{d}{dt}\left(\underline{\boldsymbol{i}}_{\boldsymbol{ms}} \right) = \underline{\boldsymbol{v}}_{\boldsymbol{s}} \tag{3.9}$$

Sunstituting (3.2), (3.4), and (3.5) into (3.9), the stator voltage equation can be expressed as

$$r_s \left(i_{ds} + j\,i_{qs} \right) e^{j\mu} + L_o \frac{d}{dt}\left(i_{ms} e^{j\mu} \right) = \left(v_{ds} + j\,v_{qs} \right) e^{j\mu} \tag{3.10}$$

This can be simplified as

$$r_s \left(i_{ds} + j\,i_{qs} \right) e^{j\mu} + L_o \frac{di_{ms}}{dt} e^{j\mu} + j\,L_o i_{ms} \frac{d\mu}{dt} e^{j\mu} = \left(v_{ds} + j\,v_{qs} \right) e^{j\mu} \tag{3.11}$$

or, using $\omega_s = \dfrac{d\mu}{dt}$, (3.11) can be written as

$$r_s \left(i_{ds} + j\,i_{qs} \right) + L_o \frac{di_{ms}}{dt} + j\,\omega_s L_o i_{ms} = \left(v_{ds} + j\,v_{qs} \right) \tag{3.12}$$

It can be seen from (3.12) that both sides of the equation have variables in the *dq*-reference frame. Similarly the rotor voltage equation can be expressed in the *dq*-reference frame. Since the rotor current is inaccessible, the rotor current is eliminated from the rotor voltage equation (2.20) using (3.2) as given below

$$r_r \left(\underline{\boldsymbol{i}}_{\boldsymbol{ms}} - \left(1 + \sigma_s \right) \underline{\boldsymbol{i}}_{\boldsymbol{s}} \right) e^{-j\varepsilon} + L_r \frac{d}{dt}\left(\left(\underline{\boldsymbol{i}}_{\boldsymbol{ms}} - \left(1 + \sigma_s \right) \underline{\boldsymbol{i}}_{\boldsymbol{s}} \right) e^{-j\varepsilon} \right) + L_o \frac{d}{dt}\left(\underline{\boldsymbol{i}}_{\boldsymbol{s}} e^{-j\varepsilon} \right) = 0 \tag{3.13}$$

Since the rotor input voltage is zero in case of the squirrel cage induction machine, the right hand term in (3.13) is zero. To separate the stator flux terms and the stator current terms, (3.13) can be rearranged as

$$L_r \frac{d\underline{\boldsymbol{i}}_{\boldsymbol{ms}}}{dt} - j\,\omega_e L_r \underline{\boldsymbol{i}}_{\boldsymbol{ms}} + r_r \underline{\boldsymbol{i}}_{\boldsymbol{ms}} = r_r\left(\left(1+\sigma_s\right)\underline{\boldsymbol{i}}_{\boldsymbol{s}}\right) + \left(\left(1+\sigma_s\right)L_r - L_o\right)\frac{d\underline{\boldsymbol{i}}_{\boldsymbol{s}}}{dt} - j\,\omega_e\left(\left(1+\sigma_s\right)L_r - L_o\right)\underline{\boldsymbol{i}}_{\boldsymbol{s}} \tag{3.14}$$

If (3.14) is multiplied by $\frac{L_o}{L_r}$ and subtracted from (3.9), term $\frac{d\underline{\boldsymbol{i}}_{\boldsymbol{ms}}}{dt}$ can be removed, and an equation defining the dynamics of the stator currents can be obtained. This is given as below

$$r_s \underline{\boldsymbol{i}}_{\boldsymbol{s}} + j\,\omega_e L_o \underline{\boldsymbol{i}}_{\boldsymbol{ms}} - \frac{L_o}{T_r}\underline{\boldsymbol{i}}_{\boldsymbol{ms}} = \underline{\boldsymbol{v}}_{\boldsymbol{s}} - \frac{L_s}{T_r}\underline{\boldsymbol{i}}_{\boldsymbol{s}} - \sigma L_s \frac{d\underline{\boldsymbol{i}}_{\boldsymbol{s}}}{dt} + j\,\omega_e \sigma L_s \underline{\boldsymbol{i}}_{\boldsymbol{s}} \tag{3.15}$$

where $T_r = \frac{L_r}{r_r}$ (3.16)

Equation (3.15) can be rearranged as

$$\sigma L_s \frac{d\underline{\boldsymbol{i}}_{\boldsymbol{s}}}{dt} + \left(r_s + \frac{L_s}{L_r} r_r\right)\underline{\boldsymbol{i}}_{\boldsymbol{s}} = \underline{\boldsymbol{v}}_{\boldsymbol{s}} + L_o\left(\frac{1}{T_r} - j\,\omega_e\right)\underline{\boldsymbol{i}}_{\boldsymbol{ms}} + j\,\omega_e \sigma L_s \underline{\boldsymbol{i}}_{\boldsymbol{s}} \tag{3.17}$$

Using (3.2), (3.4), and (3.5), (3.17) can be expressed in *dq*-axes variables, and it is derived as

$$\begin{aligned} &\sigma L_s \frac{d\left(i_{ds} + j\,i_{qs}\right)e^{j\mu}}{dt} + \left(r_s + \frac{L_s}{L_r} r_r\right)\left(i_{ds} + j\,i_{qs}\right)e^{j\mu} \\ &= \left(v_{ds} + j\,v_{qs}\right)e^{j\mu} + L_o\left(\frac{1}{T_r} - j\,\omega_e\right) i_{ms} e^{j\mu} + j\,\omega_e \sigma L_s \left(i_{ds} + j\,i_{qs}\right)e^{j\mu} \end{aligned} \tag{3.18}$$

or,

$$\begin{aligned} &\sigma L_s \frac{d\left(i_{ds} + j\,i_{qs}\right)}{dt} + \left(r_s + \frac{L_s}{L_r} r_r\right)\left(i_{ds} + j\,i_{qs}\right) \\ &= \left(v_{ds} + j\,v_{qs}\right) + L_o\left(\frac{1}{T_r} - j\,\omega_e\right) i_{ms} - j\left(\omega_s - \omega_e\right)\sigma L_s \left(i_{ds} + j\,i_{qs}\right) \end{aligned} \tag{3.19}$$

Equations (3.12) and (3.19) describe the dynamics of the electrical state variables i_{ms}, i_{ds}, and i_{qs}. To complete the model of the induction machine, the dynamics of the induction machine speed should also be expressed in the stator flux oriented reference frame. This requires an expression of i_{dr} and i_{qr} in terms of i_{ms}, i_{ds}, and i_{qs} to get rid of rotor the current terms in (2.30). Substituting $\underline{\boldsymbol{i}}_{\boldsymbol{s}}$ and $\underline{\boldsymbol{i}}_{r}$ from (3.5) and (3.7) into (3.2) and comparing the real and imaginary terms on both sides of the equation, it can be shown that

$$i_{dr} = i_{ms} - \left(1+\sigma_s\right) i_{ds} \tag{3.20}$$

$$i_{qr} = -\left(1+\sigma_s\right) i_{qs} \tag{3.21}$$

Substituting i_{dr} and i_{qr} from (3.20) and (3.21) into (2.30), the equation defining the dynamics of the mechanical speed of the machine can be obtained as

$$J\frac{d\left(\frac{2}{P}\omega_e\right)}{dt}=\frac{3}{2}\frac{P}{2}L_o i_{ms}i_{qs}-m_L \tag{3.22}$$

It can be seen from (3.22) that the term $\frac{3}{2}\frac{P}{2}L_o i_{ms}i_{qs}$ is the torque developed by the machine. The torque developed is equal to the load torque in steady state and it is proportional to the *q*-axis component of the machine current if the stator flux i_{ms} is maintained constant. This is similar to the DC machine, where the torque produced by the machine is proportional to the armature current if the flux is constant.

By comparing the real and imaginary parts of the both sides of (3.12) and (3.19), the dynamic behavior of the electrical variables of the induction machine can be given in the stator flux oriented reference frame. From this and (3.22), the equations defining the complete model of the induction machine in the stator flux oriented reference frame are given below

$$\begin{aligned}
&L_o\frac{di_{ms}}{dt}+r_s i_{ds}=v_{ds}\\
&\omega_s L_o i_{ms}+r_s i_{qs}=v_{qs}\\
&\sigma L_s\frac{di_{ds}}{dt}+\left(r_s+\frac{L_s}{L_r}r_r\right)i_{ds}=v_{ds}+\frac{L_o}{T_r}i_{ms}+\left(\omega_s-\omega_e\right)\sigma L_s i_{qs}\\
&\sigma L_s\frac{di_{qs}}{dt}+\left(r_s+\frac{L_s}{L_r}r_r\right)i_{qs}=v_{qs}-\omega_e L_o i_{ms}-\left(\omega_s-\omega_e\right)\sigma L_s i_{ds}\\
&J\frac{2}{P}\frac{d\omega_e}{dt}=\frac{3}{2}\frac{P}{2}L_o i_{ms}i_{qs}-m_L
\end{aligned} \tag{3.23}$$

Knowing the system model, the controller can be designed. The design of the controller and the estimators are presented in the next section.

3.2 Controller and Estimator for Induction Machine in Stator Flux Oriented Reference Frame

3.2.1 Current Controller Design

It can be seen from the third and fourth equation of (3.23) that the terms $\frac{L_o}{T_r}i_{ms}+\left(\omega_s-\omega_e\right)\sigma L_s i_{qs}$ and $-\omega_e L_o i_{ms}-\left(\omega_s-\omega_e\right)\sigma L_s i_{ds}$ are the coupling terms in the *d*-axis and *q*-axis voltage equations. If these terms can be eliminated using feedforward terms, the voltage equation can be given as

$$\sigma L_s \frac{di_{ds}}{dt} + \left(r_s + \frac{L_s}{L_r} r_r \right) i_{ds} = v_{ds}$$
$$\sigma L_s \frac{di_{qs}}{dt} + \left(r_s + \frac{L_s}{L_r} r_r \right) i_{qs} = v_{qs} \tag{3.24}$$

and they are the linear first-order equations. These equations can be used to design the stator current PI controller. Since the equations given in (3.24) are similar with same coefficients, the design of the current controller will be same for them. Let us consider the *d*-axis equation in (3.24); the transfer function of the *d*-axis stator current to the *d*-axis stator voltage can be given by

$$\frac{i_{ds}(s)}{v_{ds}(s)} = \frac{1}{\sigma L_s s + \left(r_s + \frac{L_s}{L_r} r_r \right)} \tag{3.25}$$

This transfer function can be used as a transfer function of a plant to be controlled. Using this, the block diagram of the equivalent *d*-axis system with current controller can be given by Figure 3-2. The gain of the PI controller is given by K_c and the corner frequency is given by $1/T_c$.

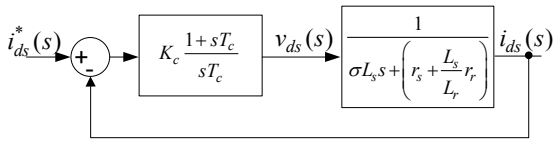


Figure 3-2 Block diagram of the current controller.

The open loop transfer function of the system shown in Figure 3-2 can be given as

$$G_{sys}(s) = K_c \frac{1+sT_c}{sT_c} \frac{1}{\sigma L_s s + \left(r_s + \frac{L_s}{L_r} r_r \right)} \tag{3.26}$$

Using (3.26), the characteristic equation of the closed loop control system can be given as

$$1 + G_{sys}(s) = 0$$
$$1 + K_c \frac{1+sT_c}{sT_c} \frac{1}{\sigma L_s s + \left(r_s + \frac{L_s}{L_r} r_r \right)} = 0 \tag{3.27}$$

which can be simplified as

$$s^2 + \frac{1}{\sigma L_s} \left(\left(r_s + \frac{L_s}{L_r} r_r \right) + K_c \right) s + \frac{K_c}{\sigma L_s T_c} = 0 \tag{3.28}$$

Equation (3.28) has the form of the characteristic equation of a simple second-order system given by

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \tag{3.29}$$

where ξ is the damping ratio and ω_n is the undamped natural frequency of the system. By comparing the coefficients of (3.28) and (3.29),

$$\begin{aligned} 2\xi\omega_n &= \frac{1}{\sigma L_s}\left(\left(r_s + \frac{L_s}{L_r}r_r\right) + K_c\right) \\ \omega_n^2 &= \frac{K_c}{\sigma L_s T_c} \end{aligned} \tag{3.30}$$

Using (3.30), the parameters of the PI controller can be chosen to obtain a desired performance specified by the second-order system parameters ξ and ω_n, and they are given as [11].

$$\begin{aligned} K_c &= 2\xi\omega_n\sigma L_s - \left(r_s + \frac{L_s}{L_r}r_r\right) \\ T_c &= \frac{2\xi\omega_n\sigma L_s - \left(r_s + \frac{L_s}{L_r}r_r\right)}{\sigma L_s \omega_n^2} \end{aligned} \tag{3.31}$$

The current controllers are used for the machine stator currents, and they require the current reference commands. It can be seen from the last equation of (3.23) that the *q*-axis machine stator current (i_{qs}) controls the torque produced by the machine, which in turn can control the mechanical speed of the machine. Therefore, the reference signal for the *q*-axis machine stator current controller can be generated by the speed controller output.

It is shown in [8] that the *d*-axis stator current should be increased with load to maintain the stator flux in steady state. Therefore, a flux controller is employed whose output provides the reference for the *d*-axis stator current. This controller is also a slow controller and it requires the stator magnetizing current as a feedback. The estimation of the stator magnetizing current can be done using the stator voltages and currents as described in the next subsection.

3.2.2 Speed and Flux Estimation

The speed controller requires the feedback signal of the speed, which can be estimated using measured electrical variables. The mechanical speed is the difference between the synchronous speed and the slip speed. By subtracting second equation in (3.23) from fourth equation in (3.23), it can be shown that

$$\sigma L_s \frac{di_{qs}}{dt} + \frac{L_s}{L_r} r_r i_{qs} = \left(\omega_s - \omega_e\right) L_o i_{ms} - \left(\omega_s - \omega_e\right)\sigma L_s i_{ds} \tag{3.32}$$

which can be simplified as

$$\omega_{sl} = \omega_s - \omega_e = \frac{\sigma L_s \frac{di_{qs}}{dt} + \frac{L_s}{L_r} r_r i_{qs}}{L_o i_{ms} - \sigma L_s i_{ds}} \tag{3.33}$$

where ω_{sl} is the slip speed of the machine. It can be seen from (3.33) that the slip speed depends on the derivative of i_{qs}, which can be a source of noise in the estimated signal. However, the speed loop is a relatively slow loop, which enables the use of the low-pass filter to remove the noise. In practice, the derivative term can be neglected for the estimation of the slip speed.

The speed estimation requires the knowledge of the equivalent stator based magnetizing current (i_{ms}) and the synchronous speed (ω_s). The synchronous speed of the machine is the rotational speed of all the space vectors and can be estimated by the rotational speed of the stator based magnetizing current vector $\left(\underline{\boldsymbol{i}}_{\boldsymbol{ms}}\right)$. Using (3.9) , the expression of the stator based magnetizing current phasor in terms of the stator voltage and current can be given by

$$\underline{\boldsymbol{i}}_{\boldsymbol{ms}} = \frac{1}{L_o}\int\left(\underline{\boldsymbol{v}}_{\boldsymbol{s}} - r_s\underline{\boldsymbol{i}}_{\boldsymbol{s}}\right)dt \tag{3.34}$$

The phasor equation (3.34) can be converted to two real equations by comparing the real and imaginary part of both sides of (3.34) and given as

$$i_{ms\alpha} = \frac{1}{L_o}\int\left(v_{s\alpha} - r_s i_{s\alpha}\right)dt \tag{3.35}$$

$$i_{ms\beta} = \frac{1}{L_o}\int\left(v_{s\beta} - r_s i_{s\beta}\right)dt \tag{3.36}$$

where α and β represent the variables related to real and imaginary axis of the stationary reference frame, respectively (Appendix A). The implementation of (3.35) and (3.36) requires an integration. A pure integration has problems of DC components and initial conditions. The DC component, caused by measured variable, can drive the output of the integrator into saturation. The other issue is the initial conditions of the input, which results in the DC offset at the estimated output. However, it can't happen in a practical AC machine during normal operation. These problems can be solved by using a low-pass filter instead of the integrator, but the low-pass filter introduces errors in the magnitude and the phase of the output. The error will be significant if the machine runs with frequency lower than the filter corner frequency. Different algorithms for integration were presented in [60] to solve the above mentioned problems. Algorithm 2 presented in [60] is used for stator based magnetizing current vector estimation, which is suitable for constant flux operation of the machine [60]. The block diagram of the estimation algorithm is given in Figure 3-3. This estimator also gives the angle μ of the stator flux for transforming the variables to the rotating reference frame. The cutoff frequency of the low-pass filter is given by ω_f.

Knowing the real and imaginary value of the vector $\left(\underline{\boldsymbol{i}}_{\boldsymbol{ms}}\right)$, the rotational speed of the vector $\left(\underline{\boldsymbol{i}}_{\boldsymbol{ms}}\right)$ can be expressed as

$$\omega_s = \frac{d\mu}{dt} = \frac{d}{dt}\left(\tan^{-1}\left(\frac{i_{ms\beta}}{i_{ms\alpha}}\right)\right) = \frac{i_{ms\alpha}^2}{i_{ms\alpha}^2 + i_{ms\beta}^2}\frac{i_{ms\alpha}\dfrac{di_{ms\beta}}{dt} - \dfrac{di_{ms\alpha}}{dt}i_{ms\beta}}{i_{ms\alpha}^2}$$

or,

$$\omega_s = \frac{1}{L_o}\frac{i_{ms\alpha}\left(v_{s\beta} - r_s i_{s\beta}\right) - \left(v_{s\alpha} - r_s i_{s\alpha}\right)i_{ms\beta}}{i_{ms\alpha}^2 + i_{ms\beta}^2} \tag{3.37}$$

and the magnitude of the stator based magnetizing current vector can be expressed as

$$i_{ms} = \sqrt{i_{ms\alpha}^2 + i_{ms\beta}^2} \tag{3.38}$$

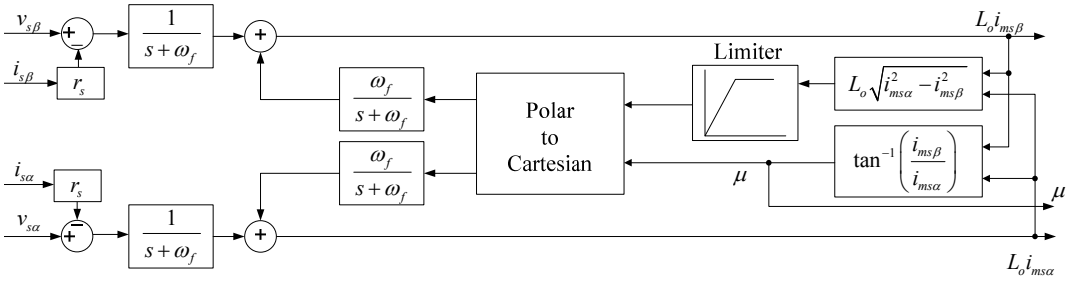


Figure 3-3 Block diagram of the estimation of stator based magnetizing current

The speed and stator flux of the machine can be estimated using (3.33), (3.37), and (3.38) from the stator voltages and currents of the machine. The stator currents are measured from the current sensors.

3.3 Active Damping Technique in Closed Loop Controlled Drive

The active damping technique proposed in the previous chapter was implemented in an open loop constant *V/f* controlled induction machine drive. The active damping terms add the voltage signal in proportional to the DC-link voltage variation to the *d*- or *q*- axes stator voltages of the machine to stabilize the operating point. Same effects of stabilization can be obtained by using active damping terms in a closed loop controlled induction machine drive system. The block diagram of the closed loop control system for induction machine drive with the active damping terms is shown in Figure 3-4. The decoupling terms are neglected for simplicity.

The stabilization techniques [14], [26], [67], and [75] add the stabilization terms to either the stator voltages or the stator currents. However, the technique proposed in Section 2.4 adds the active damping terms, which act as stabilization terms, to the stator voltages only. In the closed loop drive, the active damping terms are added to the output of the current PI controller. To get the stabilizing effect of the active damping terms, the current controller parameters should be chosen in a way that the controller does not respond to the active damping terms. So the natural frequency

(ω_n) of the closed loop current control system should be less than 300 Hz since the active damping terms have the spectral components at sixth multiples of the line frequency as given by (2.46).

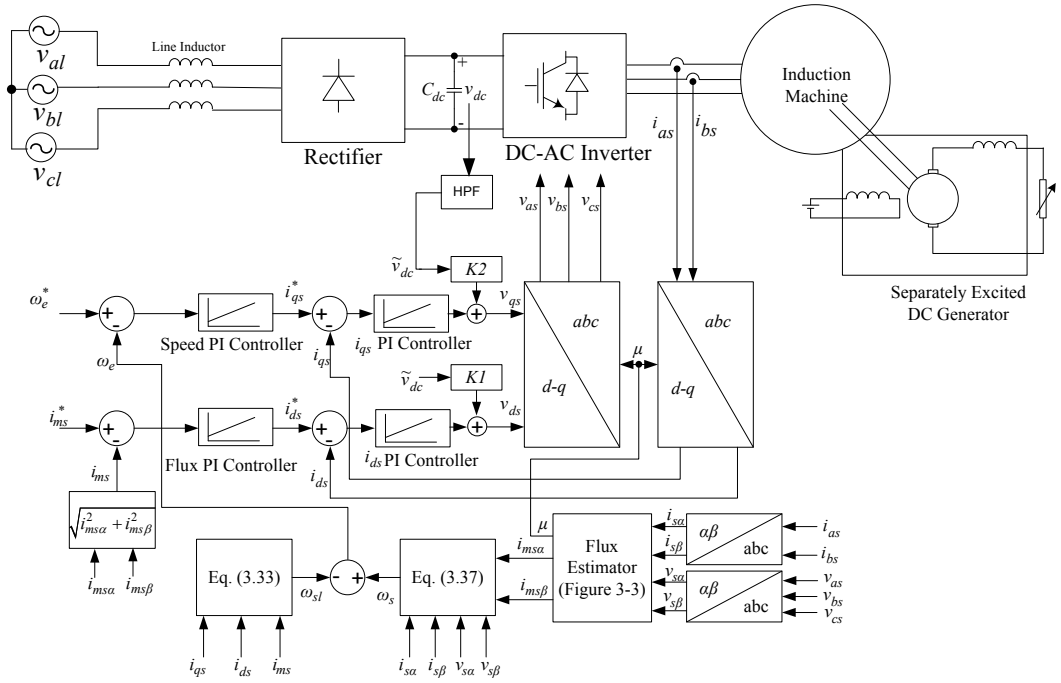


Figure 3-4 Block diagram of a stator flux oriented control of an induction machine drive with active damping

It can be seen from Figure 3-4 that the outputs of the current controllers provide the voltage references needed for the machine. If the current references are modified in such a way that the outputs of the current controllers consist the active damping term, the stability of the unstable operating point can be achieved. The modification in the current reference command should be in proportional to the DC-link voltage variations. A simple relationship between the current reference modification and the voltage reference modification can be seen by the block diagram reduction technique as shown in Figure 3-5. The relationship between the gain of the active damping term ($K2$) for the voltage and the gain of the active damping term ($K2'$) for the current can be derived using the block diagram reduction technique and can be given as

$$K2' = \frac{K2}{C(s)} \tag{3.39}$$

where $C(s)$ is the transfer function of the PI controller, which is given as

$$C(s) = K_c \frac{1 + sT_c}{sT_c}. \tag{3.40}$$

The experimental verification of the relationship between the current reference modification and the voltage reference modification based on above discussion is presented in [17].

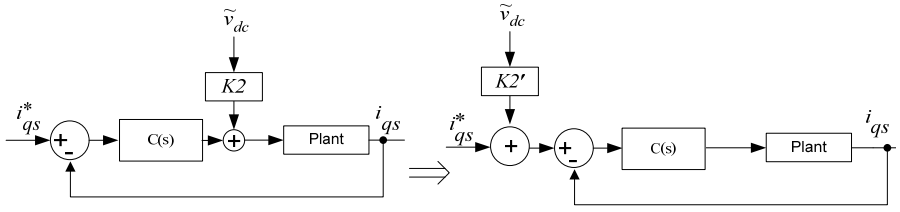


Figure 3-5 Relationship between current and voltage command modification to achieve active damping

As discussed in the previous chapter that the effects on the stator currents and the DC-link voltage due to addition of the active damping term to the *d*-axis stator voltage are different than those of due to the active damping terms added to the *q*-axis stator voltage. It was shown in the previous chapter that it is advantageous to add the active damping term to the in-phase component of the voltage vector to have the minimum machine current harmonics distortion. In case of the stator flux oriented control of the induction machine, *d*-axis is aligned to the stator flux. Since the stator voltage vector lags the stator flux vector by 90° in steady state if the stator resistive voltage drop is neglected, so the active damping term should be added to the *q*-axis current controller output to get least total harmonics distortion in the machine current.

3.4 Summary and Conclusion

This chapter has given a contribution to simplified analysis and implementation of the new active damping in the closed loop controlled drive system. This chapter considers the methods of active damping by modifying the i^*_{qs} and v_{qs} and describes how to select gain parameter of the active damping *K2´*. The recommendation for selecting the current loop bandwidth is also discussed for effective use of the active damping term.

Chapter 4

Three-Level Neutral-Point Clamped Inverter

The two-level inverter fed adjustable speed drives are well established in the low-voltage drives' market. However, the medium and high voltage drive systems are served by multilevel power inverters successfully. Different multilevel inverter topologies have been discussed in [33], [37], [62], [63], [65], [71]-[73] for medium- and high-voltage drives. The multilevel inverters have the advantage of lower device stress, lower output voltage harmonics distortion, and high efficiency compared to the two-level inverter. A neutral-point-clamped (NPC) three-level inverter, as shown in Figure 4-1, is one of them, and it was proposed in [65] for high efficiency drive systems. There has been a great deal of research activities in the neutral-point-clamped three-level inverter since last three decades. A comparison study of this topology vs. the two-level converter topology has shown that it is a viable solution for the low voltage drives [77]. Now this topology has become popular for low-voltage and low power drive application [77], [81], and [88].

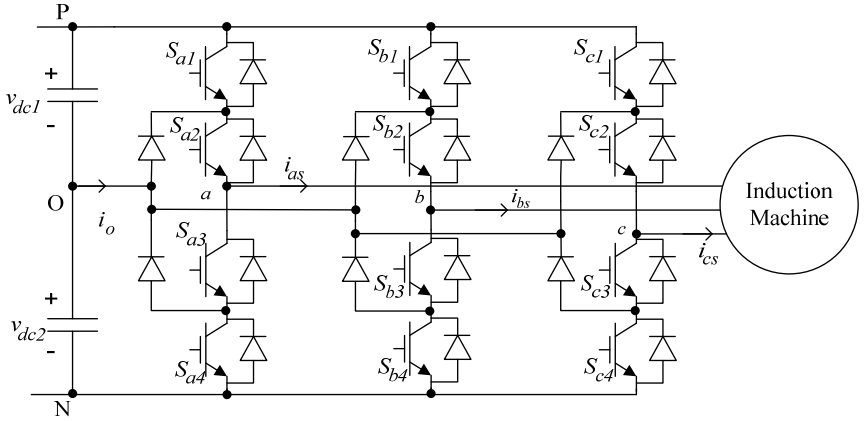


Figure 4-1 A NPC three-level inverter.

The NPC three-level inverter requires 12 IGBTs, which increase complexity in the hardware implementation and layout of the components. However, the hardware implementation of this inverter for low-voltage applications has become simple due to availability of modules realizing a leg of the inverter [88], [90], [93], and [94].

The three-level inverter has three voltage levels at the DC-link. The additional level, which is not available at the two-level inverter output, is realized by the midpoint of two series connected DC-link capacitors. This midpoint is known as the neutral-point in a three level inverter, and the potential of the neutral-point should be balanced. In other words, the voltage across the two series connected capacitors should be equal. Since any disturbance in this potential reflects in the output voltages of the inverter and can cause additional harmonic distortion.

The higher numbers of active switches provide higher degree of freedom, which helps reducing the common mode voltage and maintaining the neutral-point voltage balance, but on the other hand, they increase the complexity in the controller for the inverter. Different modulation and control strategies were proposed in the literature for the NPC three-level inverter.

This chapter provides an overview of different modulation and control strategies used for the NPC three-level inverter. The operation of the inverter is explained in Section 4.1. Section 4.2 presents different modulation strategies commonly used for the NPC three-level inverter. These modulation strategies affect the neutral-point current and the common mode voltage. Section 4.3 shows the effect of modulation on the neutral-point current of the NPC inverter and discusses different controller for neutral-point voltage. Different modulation strategies, which produce zero average the neutral-point current in a switching period, were proposed. They are discussed in Section 4.4

4.1 Principles of the NPC Three-Level Inverter

The circuit diagram of the NPC three-level inverter is shown in Figure 4-1. The positive and negative terminals of the DC-bus are denoted by P and N, respectively. The neutral-point of the inverter is denoted by O, and it is realized by the midpoint of two series connected capacitors. The output of the three-level inverter can be connected to P, N, or O terminals of the DC-bus creating the three levels at the output. This can be seen in Figure 4-2, which is representing a switching model of the inverter.

If the total DC-link voltage is considered as v_{dc}, the voltages of the terminal P, the terminal O, and the terminal N can be considered as $+½v_{dc}$, 0, and $-½v_{dc}$. If an output phase of the inverter is connected to terminal P, the output phase voltage will be $+½v_{dc}$. As an example, to achieve this for phase a, switches S_{a1} and S_{a2} should be turned on, and switches S_{a3} and S_{a4} should be turned off. The voltage level of an output phase and the state of the switches to achieve that particular voltage level is summarized in Table 4-1, where 1 represents that the switch is turned on, and 0 represents that the switch is turned off. When the switch S_{x1} is on, the switch S_{x3} is off and vice versa. The same is true for the switch S_{x2} and the switch S_{x4}. It shows that a phase needs only two independent gate signal for its switches. If S_{x1} and S_{x2} are known, the inverted signals of them can be used for S_{x3} and S_{x4}, respectively.

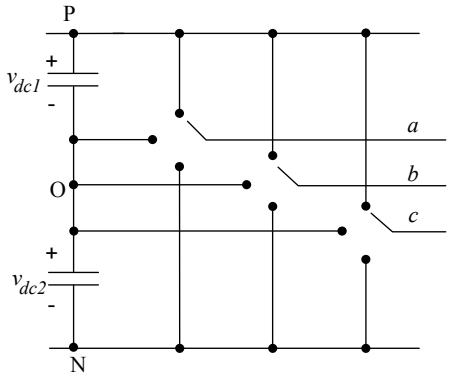


Figure 4-2 Switching model of a three-level inverter.

Table 4-1 Output phase voltage level and state of the switches

Phase x* Output Voltage	S_{x1}	S_{x2}	S_{x3}	S_{x4}
$+½V_{dc}$	1	1	0	0
0	0	1	1	0
$-½V_{dc}$	0	0	1	1

*x represents a phase in general.

The requirements for the switches in a three-level converter for connection to the P and N terminals are to conduct current in both directions during ON state and block only positive voltage during OFF state. This requires current-bidirectional two-quadrant switch. However, the switch, required for connection to O terminal, should block positive and negative voltages during OFF state and conduct current in both directions during ON state. So a four-quadrant switch should be used for connection to O terminal. These combinations of switches are realized by using 4 IGBTs and 6 diodes in a phase as shown in Figure 4-1 for the NPC three-level inverter. The current paths for positive and negative current through the switches during ON state and the voltages across the switches during OFF state are shown in Figure 4-3, when a phase output is connected to the P, O, and N terminals.

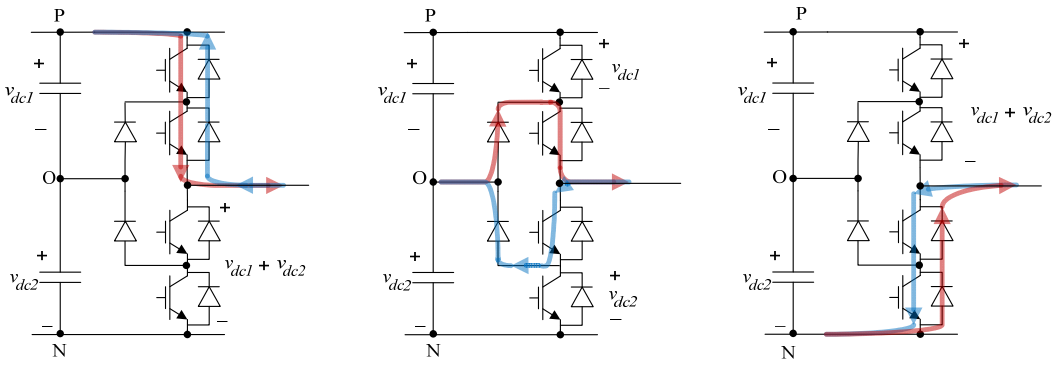


Figure 4-3 Current paths during ON state and voltage across devices during OFF state

After discussing the output phase voltage levels and the switch realization for a NPC three-level inverter, another important feature, which needs attention, is three phase space vectors that can be generated by the three-level converter. Since each phase can have three different voltage levels, total number of switch states generated by the NPC three-level inverter are given by

$$n_{ss} = N^p = 3^3 = 27, \tag{3.41}$$

where N represents the number of voltage level at one phase, and p denotes the number of phases. If a space vector is defined by

$$\underline{\boldsymbol{v}}_{\boldsymbol{s}} = \frac{2}{3}\left[v_{aO} + e^{j(2\pi/3)}v_{bO} + e^{j(4\pi/3)}v_{cO}\right], \tag{3.42}$$

the inverter can generate 27 different voltage vector. The different voltage vectors generated by the three-level inverter are shown in Figure 4-4. Symbols +, 0, and – denote that a phase is connected to the terminal P, O, and N, respectively. As an example (+ 0 –) denote that phase *a* is connected to the P terminal, phase *b* is connected to the O terminal, and phase *c* is connected to the N terminal of the NPC three-level converter. It can be seen from Figure 4-4 that some vectors have redundant switching states. In other words, they can be generated by more than one switching state of the inverter. This important feature is used for the neutral-point balancing and/or common mode voltage reduction techniques.

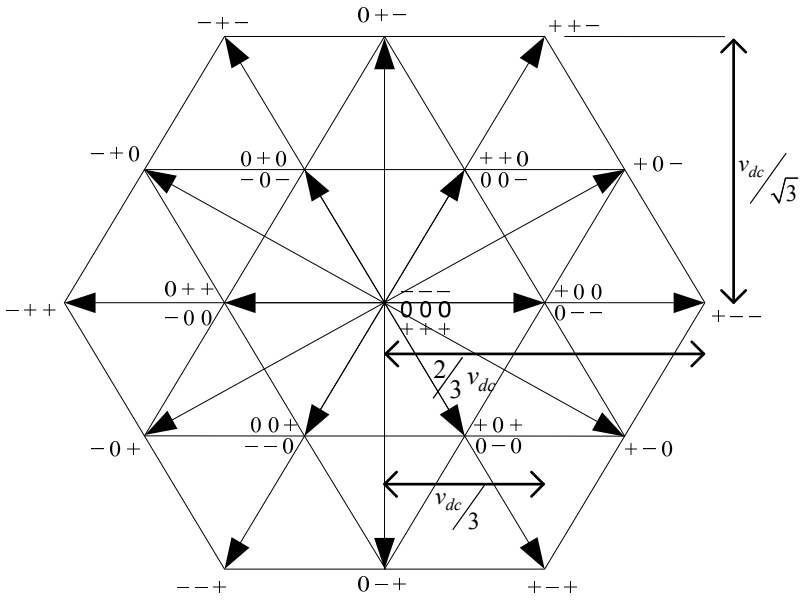


Figure 4-4 Space vector diagram of a three-level inverter.

By using (3.42), the length and angle of a vector can be calculated. It can be shown that the length of the vectors creating six vertices of the outer hexagon of the space vector diagram is $(2/3)\cdot v_{dc}$. The length of the vectors with redundancy of two switching states is $(1/3)\cdot v_{dc}$. The length of vectors, which lies in the middle of edges of outer hexagonal, can be calculated as $v_{dc}/\sqrt{3}$. The length of the vector with three

redundant switching states is zero, and it is known as zero vector. These vectors are used to approximate a desired voltage vector.

4.2 Modulation Strategies for NPC Three-Level Inverter

The NPC three-level converter can produce only fixed voltage vectors as shown in Figure 4-4. However, these vectors can be used to approximate a desired voltage vector. This can be achieved by using different pulse width modulation (PWM) techniques [1], [32], and [57]. In PWM modulation techniques, the output voltage of an inverter leg is controlled by varying the duty cycles of the switches. By changing the duty cycles of different phase switches, the output phase connections to different DC-link terminals are changed generating different voltage vectors, which in turn can approximate the desired voltage vector.

The PWM techniques can be divided into two categories based on their implementation methods: carrier-based PWM techniques and space vector based PWM techniques. In carrier-based techniques, a reference modulating waveform is compared with high frequency carrier waveform (the frequency of the carrier waveform is kept equal to the switching frequency of the inverter) to generate the duty cycles. In this way, the average output phase voltage in a switching time period is proportional to the modulating waveform. While in a space vector based modulation technique, different voltage vector are applied for some time in a switching period. The time for which different vectors need to be applied are calculated in such a way that the time-average in a switching period is equal to the desired voltage vector [57]. Although the carrier-based and space vector based PWM seem different from their implementation point of view, the results obtained as the output voltage of the inverter are equivalent.

4.2.1 Carrier-Based Sinusoidal PWM

Generally in a three-phase inverter, desired output voltages are the three-phase balanced sinusoidal voltages. Since the output can have only discrete values equal to the voltages of the dc-link terminals, the output voltage of a phase is time-averaged over one switching period. To obtain time-averaged sinusoidal output voltages, three sinusoidal modulating waveforms are compared with the carrier waveform using carrier-based PWM technique. Carrier-based PWM for a NPC three-level inverter is shown in Figure 4-5. It can be seen from Figure 4-5 that it requires two carrier waveforms. If the modulating waveform is positive, it is compared with carrier 1 and if the modulating waveform is negative, it is compared with carrier 2. Since the frequency of carrier waveform is higher than that of the modulating signal, the modulating signal can be assumed constant in a time period of the carrier waveform as shown in an expanded view during time period of the carrier signal in Figure 4-5. It is discussed in the previous section that a leg of the NPC three-level converter requires two independent gate signals for switches S_{x1} and S_{x2}. The gate signal of first switch S_{x1} in a leg can be obtained by comparing the phase modulating signal

with carrier 1. If the modulating signal is higher than carrier 1 signal, the gate signal for S_{x1} should be high to turn the switch on. Similarly the gate signal for S_{x2} can be obtained by the modulating signal with carrier 2. If the modulating signal is higher than carrier 2 signal, the gate signal for S_{x2} should be high. As an example, if we consider phase *a* modulating signal in a carrier wave time period (it is also switching time period T_s) as shown in Figure 4-5, the modulating signal is positive. It is greater than carrier 2 so the switch S_{x2} should be ON during whole switching time period and the switch S_{x1} should be ON only during the time when it is greater than carrier 1 waveform. This yields an output phase *a* terminal voltage as shown in Figure 4-5. Similarly the terminal voltage for another phase can be derived. This modulation strategy is known as sinusoidal PWM for the NPC three-phase inverter [45]. Different implementations using single carrier waveform are presented in [24], [74].

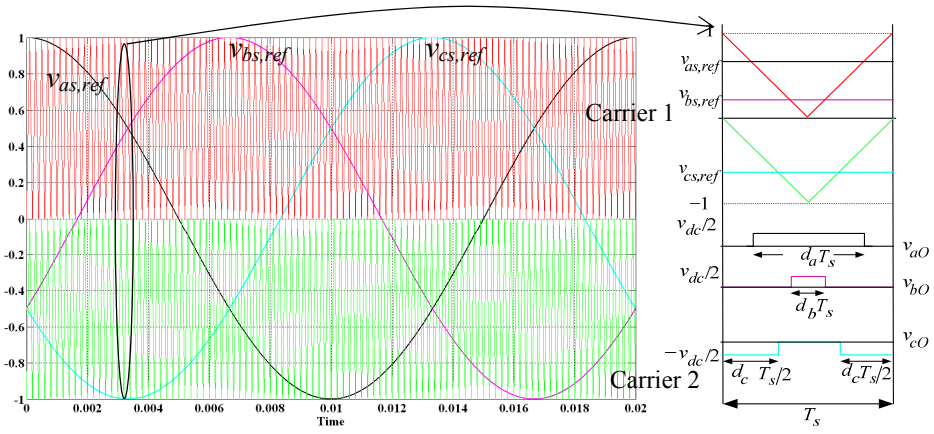


Figure 4-5 Carrier-based implementation of sinusoidal PWM for NPC three-level inverter.

Let us consider that the modulating signal for generating the three-phase balanced sinusoidal voltages are given by

$$\begin{aligned} v_{as,ref} &= m\cos(\omega t) \\ v_{bs,ref} &= m\cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_{cs,ref} &= m\cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{3.43}$$

where $v_{as,ref}$, $v_{bs,ref}$, and $v_{cs,ref}$ are the reference modulating signals for phase *a*, *b*, and *c*, respectively. The time-averaged phase terminal voltage over one switching time period can be given as

$$\begin{aligned} \langle v_{aO} \rangle_{T_s} &= m\frac{v_{dc}}{2}\cos(\omega t) \\ \langle v_{bO} \rangle_{T_s} &= m\frac{v_{dc}}{2}\cos\left(\omega t - \frac{2\pi}{3}\right) \\ \langle v_{cO} \rangle_{T_s} &= m\frac{v_{dc}}{2}\cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{3.44}$$

where *m* represents modulation index and can be defined as

$$m = \frac{V_{des}}{v_{dc}/2} \tag{3.45}$$

where V_{des} is the amplitude of the desired voltage vector, and it is equal to the amplitude of a phase voltage. It can be seen from Figure 4-5, that the maximum amplitude of the output voltage, which can be obtained from sinusoidal PWM is equal to half of the DC-link voltage in linear modulation range ($m \leq 1$) [5].

4.2.2 Space Vector Modulation

Space vector modulation is based on the space vector diagram shown in Figure 4-4. In this method, a desired voltage vector is synthesized by applying three nearest voltage vectors. Different methods have been proposed for the determination of the switching sequence and the calculation of time duration of different states [16], [30], [46], and [59]. The method proposed in [59] simplifies the space vector diagram of a three-level inverter to that of a two-level inverter. The space vector diagram of the three-level inverter can be visualized as it has six small hexagons with center at the vectors with redundancy of two switching states as shown in Figure 4-6. The center vectors are marked with arrow to highlight them. It can be seen from Figure 4-6 that if these small hexagons are moved towards the origin by $v_{dc}/3$, the space vector diagram of three-level inverter can be visualized as that of a two-level inverter, and the space vector modulation methods for the two-level inverter can be applied. To calculate the time for which a switching state needs to applied, first, one of the six small hexagonal is identified, where the desired vector is located. After that, the center vector of that small hexagon is subtracted from the desired vector. The resultant vector then can be used to calculate the time for which a switching state needs to be applied using conventional two-level converter method [59]. An important point to be noted in this method is that the six small hexagons have some overlapping area. To avoid any discrepancy in identifying the small hexagons, the space vector diagram of three-level converter can be divided into six parts as shown in Figure 4-6(b), and each part can be assigned to one hexagon. If the desired vector lies in a particular part of the space vector diagram, that particular small hexagon can be selected to calculate the time for which a switching state needs to be applied.

The three-phase sinusoidal balanced voltages have a circular trajectory in a space vector diagram. The radius of this circular trajectory is equal to the amplitude of a phase voltage. A maximum radius that can be achieved inside the hexagon of the space vector diagram is $v_{dc}/\sqrt{3}$. This means that the maximum phase voltage that can be achieved by space vecor PWM is $v_{dc}/\sqrt{3}$, and it corresponds to the modulation index of 1.1547 if $V_{des}= v_{dc}/\sqrt{3}$ is substituted in (3.45).

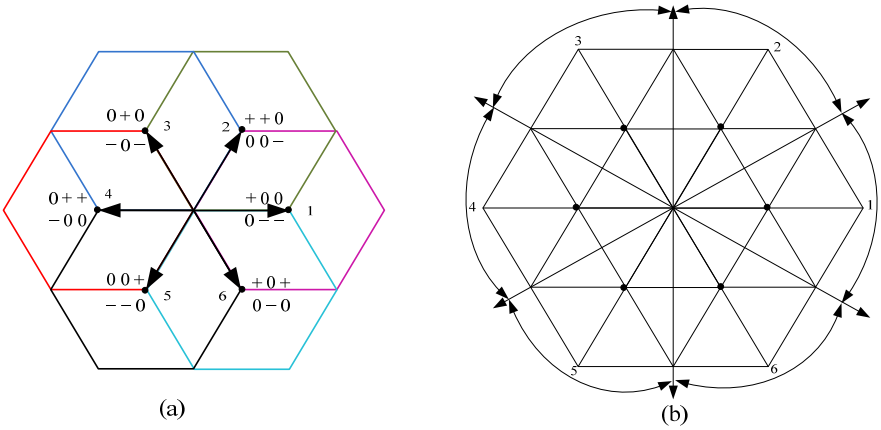


Figure 4-6 (a) Six hexagons inside a space vector diagram of the three-level inverter. (b) Divisions of the space vector diagram without redundancy.

4.2.3 Carrier-Based PWM vs. Space Vector Based PWM

Space vector based PWM has capability to produce output voltages with higher modulation index as compared to sinusoidal PWM. On the other hand, the implementation of space vector PWM is more complex as shown in the previous sections. However, the linear range of the output phase voltage for carrier-based PWM can be extended by 15% if one-sixth of third harmonic is subtracted from the modulating reference phase voltages waveforms as shown in Figure 4-7(a) [52], [58]. In this case, a common mode offset added to the voltage references, which are given by (3.43), is

$$v_{off} = -\frac{m}{6}\cos(3\omega t) \tag{3.46}$$

The linear range of carrier-based modulation can also be increased if the three-phase voltage references in a switching period are sorted as the maximum, the middle, and the minimum voltage values given as

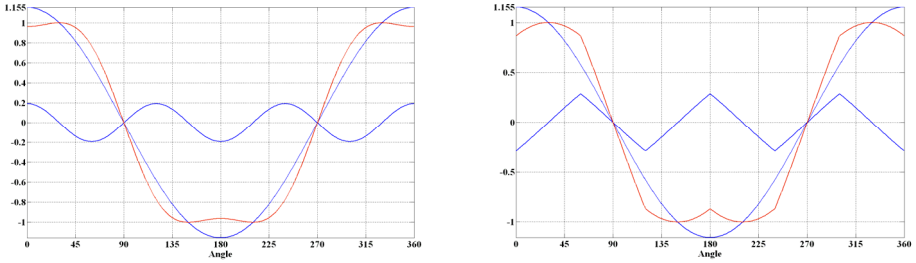
$$\begin{aligned} v_{\max} &= \max\left(v_{as,ref}, v_{bs,ref}, v_{cs,ref}\right) \\ v_{\text{mid}} &= \text{mid}\left(v_{as,ref}, v_{bs,ref}, v_{cs,ref}\right) \\ v_{\min} &= \min\left(v_{as,ref}, v_{bs,ref}, v_{cs,ref}\right), \end{aligned} \tag{3.47}$$

and the half of the middle voltage value is added to the reference three-phase voltage waveforms as a common mode offset in a switching period as shown in Figure 4-7(b) [40]. In this case, the common mode offset is given by

$$v_{off} = \frac{1}{2}v_{\text{mid}} \tag{3.48}$$

The switching states and the duty cycles of different IGBTs achieved by adding (3.48) to the reference voltages are the same as that of space vector modulation in a two-level inverter [40]. The maximum modulation index that can be achieved by both methods is 1.154, which is the same as space vector modulation. In space vector PWM, for the two-level inverter, time for which zero vectors (+++ and − − −)

are applied are equal, and it can be achieved either by adding (3.48) to the reference voltages or by standard space vector algorithm as described in [78].



(a) (b)

Figure 4-7 (a) Third harmonic addition. (b) Addition of half of the middle voltage value for extending the linear range.

The modulating waveform given in Figure 4-7(b) can be used in the three-level inverter to achieve high modulation index. However, it is shown in [64] that it is not equivalent to space vector modulation for the three-level inverter. In case of the three-level inverter, the space vector PWM applies the two redundant switching states, which have the length of $v_{dc}/3$, for the equal amount of time in a switching period, but the modulating voltage references given by(3.43) added to (3.48) do not distribute equal amount of time between the two redundant switching states. The carrier-based implementation of space vector PWM for the three-level inverter can be achieved if the common mode offset give in Table 4-2 is added to the modulating references [80].

Table 4-2 Common mode offset for three-level inverter

Condition		Common mode Offset (v_{off})
$(v_{max}-v_{min}) < ½$	$v_{mid} < 0$	$v_{min}/2$
	$v_{mid} > 0$	$v_{max}/2$
$(v_{max}-v_{min}) > ½$	$v_{mid} < 0$ & $(v_{max}-v_{mid}) < ½$	$-(1-v_{max})/2$
	$v_{mid} > 0$ & $(v_{mid}-v_{min}) < ½$	$(1+v_{min})/2$
Others		$-(v_{max}+v_{min})/2$

The common mode offset shown in Table 4-2 can also be calculated in another approach described in the following [29], [42], and [64]. First, the common mode offset given by (3.48) is added to the voltage references given by (3.43), and the results of that are shifted in such a way that they lie within the carrier band of [+1/2, – 1/2]. The modified voltage references can be represented by

$$v'_{k,ref} = \left(v_{k,ref} + v_{off} + 1\right) \bmod (1) - \frac{1}{2}, \qquad k = as, bs, cs \tag{3.49}$$

where (x mod y) results the remainder of division (x/y). An additional common mode offset is calculated from (3.49) as given by

$$v'_{off} = -\frac{v'_{max} + v'_{min}}{2} \tag{3.50}$$

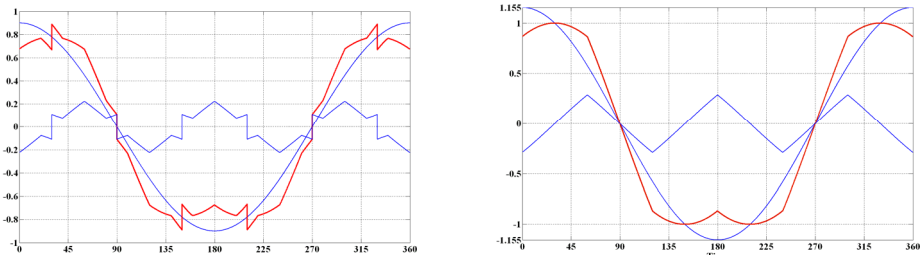
where

$$v'_{\max} = \max\left(v'_{as,ref}, v'_{bs,ref}, v'_{cs,ref}\right)$$
$$v'_{\min} = \min\left(v'_{as,ref}, v'_{bs,ref}, v'_{cs,ref}\right), \tag{3.51}$$

Finally, the modified three-phase reference voltage waveforms are given by

$$v''_k = v_k + \frac{v_{\text{mid}}}{2} + v'_{off}, \qquad k = as, bs, cs \tag{3.52}$$

The reference voltage waveforms for the carrier-based implementation of three-level inverter space vector PWM are given in Figure 4-8 for m =0.9 and 1.155. It can be seen from Figure 4-7(b) and Figure 4-8(b) that the common mode offsets added in case of the two-level inverter and the three-level inverter are same for m=1.155.



(a) (b)

Figure 4-8 Carrier-based implementation for three-level inverter space vector PWM for (a) m=0.9 and (b) m=1.155.

4.2.4 Discontinuous PWM Techniques

Sinusoidal PWM and carrier-based space vector PWM are very popular PWM methods due to easy implementation. In carrier-based space vector PWM, the common mode offset is added to the voltage references in such a way that the resultant reference waves are within the range of peak of the carrier waves. This results in switching of each phase in every switching period. These kinds of PWM techniques are referred to as continuous PWM (CPWM). It has been shown in [54] and [66] that PWM strategies, where a phase discontinues modulation for at most a total of 120°, can also achieve same line-line voltage in a two-level inverter as that can be achieved by sinusoidal or space vector PWM. These kinds of PWM techniques are referred to as discontinuous PWM (DPWM). Since the phase with discontinuous modulation does not switch during that period, these PWM strategies have advantages of reduced switching losses and reduced harmonic distortion at high modulation index for the two-level inverter [54]. Different types of DPWM strategies are proposed in literature where the discontinuity of the phase for 120° is applied at once, twice with 60° duration, or 4 times with 30° duration. The detailed analysis of different types of DPWM for the two-level inverter and their carrier-based implementation are discussed in [7], [54], [66]. Similar types of DPWM can be implemented in the three-level inverter.

4.2.4.1 The 120° DPWM

In this DPWM, a phase in the inverter stops modulating for 120°. In the two-level inverter, it can be divided into groups [54]:

- DPWMMAX where a phase having the maximum value is connected to the positive DC-bus for 120°.
- DPWMMIN where a phase having the minimum value is connected to the negative DC-bus for 120°.

To achieve the carrier-based implementation of these PWM techniques, common mode offsets need to be added to the voltage references (3.43) for the two-level inverter are given by

$$v_{off\_\mathrm{DPWMMAX}} = 1 - v_{\max} \quad \text{for DPWMMAX} \tag{3.53}$$

and

$$v_{off\_\mathrm{DPWMMIN}} = -1 - v_{\min} \quad \text{for DPWMMIN} \tag{3.54}$$

An equivalent to 120° DPWM in the two-level inverter for the three-level inverter can be obtained adding a common mode offset for the carrier-based implementation. In case of the three-level inverter, the three-phase voltage references are scaled to [+1/2, – 1/2] using (3.49), and the common mode offset for the equivalent 120° DPWM can be calculated by

$$v'_{off\_\mathrm{DPWMMAX}} = \frac{1}{2} - v'_{\max} \quad \text{for DPWMMAX} \tag{3.55}$$

and

$$v'_{off\_\mathrm{DPWMMIN}} = -\frac{1}{2} - v'_{\min} \quad \text{for DPWMMIN} \tag{3.56}$$

where $v'_{\max}$ and $v'_{\min}$ are given by (3.51).

For DPWMMAX in the three-level inverter, the modified three-phase reference voltage waveforms are given by

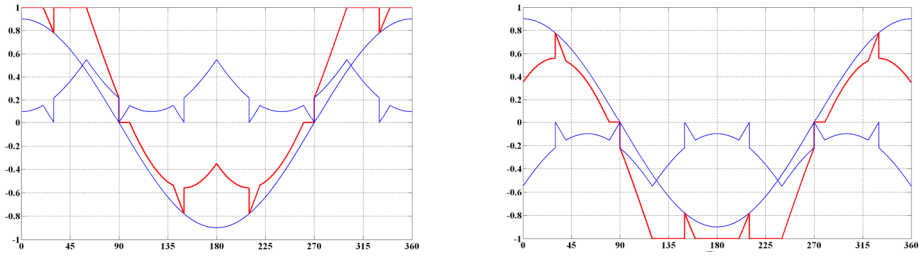
$$v''_k = v_k + \frac{v_{\mathrm{mid}}}{2} + v'_{off\_\mathrm{DPWMMAX}}, \qquad k = as, bs, cs \tag{3.57}$$

For DPWMMIN in the three-level inverter, the modified three-phase reference voltage waveforms are given by

$$v''_k = v_k + \frac{v_{\mathrm{mid}}}{2} + v'_{off\_\mathrm{DPWMMIN}}, \qquad k = as, bs, cs \tag{3.58}$$

The voltage references for equivalent DPWMMAX and DPWMIN are shown in Figure 4-9 for m=0.9. It can be seen from Figure 4-9 that the voltage reference has six discontinuities in a fundamental cycle and discontinuities occur near the zero crossing of the three-phase voltage references. The reason for this behavior is that the reference near to zero is clamped to the neutral-point. In case of DPWMMAX, the reference, which is slightly smaller to zero, is clamped to the neutral-point, and

in case of DPWMMIN, the reference, which is slightly greater than zero, is clamped to the neutral-point [7]. A detailed analysis for this behavior based on space vector diagram for the three-level inverter can be found in [7].



(a) (b)

Figure 4-9 Modulating wave for m=0.9 for three-level inverter for (a) 120° DPWMMAX and (b) 120°DPWMMIN.

4.2.4.2 The 60° DPWM

In the DPWM techniques, either a phase having the maximum value or a phase having the minimum value stop modulating for 120°. If this 120° period is divided into two 60° periods, and during one 60°, a phase having the maximum value and during rest of 60° when the same phase has the minimum value stops modulating, this modulation is known as 60° DPWM. This approach clamps the phase with the maximum absolute value to the nearest DC-bus, either the positive or negative DC-bus. Since the duration of a phase having the maximum or minimum value in a three-phase balanced phase voltages is 120°, the 60° clamping interval can be centered during the 120° interval where the phase has the maximum value (DPWM1 in [54]) or it can be moved ±30°(DPWM0 and DPWM2 in [54]). In the two-level inverter, DPWM1 can be achieved by adding a common mode offset to the three-phase voltage references as given by

$$v_{off\_\mathrm{DPWM60}} = sign\left(|v|_{\max}\right) - |v|_{\max} \tag{3.59}$$

where

$$|v|_{\max} = \begin{cases} v_{as,ref} & if \quad |v_{as,ref}| > |v_{bs,ref}|, |v_{cs,ref}| \\ v_{bs,ref} & if \quad |v_{bs,ref}| > |v_{as,ref}|, |v_{cs,ref}| \\ v_{cs,ref} & if \quad |v_{cs,ref}| > |v_{bs,ref}|, |v_{as,ref}| \end{cases} \tag{3.60}$$

Similarly for the three-level inverter, a common mode offset can be calculated to implement 60° DPWM. For 60° DPWM, first the voltage references are scaled as given by

$$v^s_{k,ref} = \left(v_{k,ref} + 1\right) \bmod (1) - \frac{1}{2}, \qquad k = as, bs, cs \tag{3.61}$$

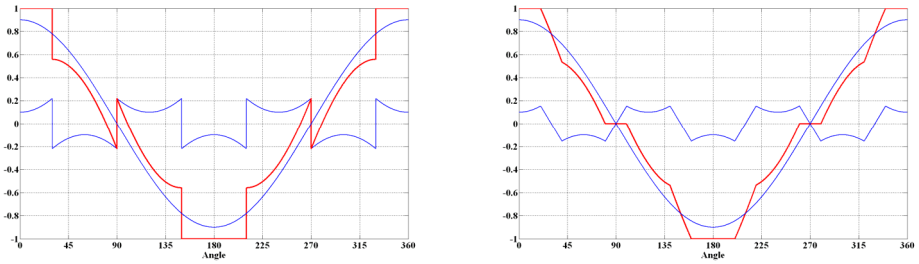
and then the common mode offset is given by [42]

$$v^s_{off\_DPWM60} = sign\left(\left|v^s\right|_{\max}\right)\frac{1}{2} - \left|v^s\right|_{\max} \tag{3.62}$$

where

$$\left|v^s\right|_{\max} = \begin{cases} v^s_{as,ref} & if \quad \left|v^s_{as,ref}\right| > \left|v^s_{bs,ref}\right|, \left|v^s_{cs,ref}\right| \\ v^s_{bs,ref} & if \quad \left|v^s_{bs,ref}\right| > \left|v^s_{as,ref}\right|, \left|v^s_{cs,ref}\right| \\ v^s_{cs,ref} & if \quad \left|v^s_{cs,ref}\right| > \left|v^s_{bs,ref}\right|, \left|v^s_{as,ref}\right| \end{cases} \tag{3.63}$$

A phase voltage reference for the two-level inverter DPWM1 and for the three-level inverter 60° DPWM are shown in Figure 4-10. It can be seen from Figure 4-10(b) that the resulting reference waveform for the three-level inverter clamps to the neutral-point near zero crossing. At low modulation index, the interval for which a phase is clamped to the neutral-point can be made 60°. This is termed as zero clamped PWM [42]. However, at low modulation index, other 60° DPWM also exist where the phase is clamped to the positive DC-bus and the negative DC-bus for 60° interval. A detailed analysis of different kinds of 60° DPWM for the three-level inverter can be found in [42].



(a) (b)

Figure 4-10 Modulating wave for m=0.9 for 60° DPWM for
(a) Two-level inverter and (b) Three-level inverter.

4.2.4.3 The 30° DPWM

For 30° DPWM, a common mode offset for the two-level inverter is given by

$$v_{off\_\text{DPWM30}} = sign\left(\left|v\right|_{\text{mid}}\right) \cdot 1 - \left|v\right|_{\text{mid}} \tag{3.64}$$

where

$$\left|v\right|_{\text{mid}} = \begin{cases} v_{as,ref}, & if \quad \left|v_{bs,ref}\right| \geq \left|v_{as,ref}\right| \geq \left|v_{cs,ref}\right| \\ v_{bs,ref}, & if \quad \left|v_{as,ref}\right| \geq \left|v_{bs,ref}\right| \geq \left|v_{cs,ref}\right| \\ v_{cs,ref}, & if \quad \left|v_{as,ref}\right| \geq \left|v_{cs,ref}\right| \geq \left|v_{bs,ref}\right| \end{cases} \tag{3.65}$$

The reference waveform for a phase is shown in Figure 4-11. It can be seen that the modulating waveform is clamped to 1 and −1 for 60° interval each, and the interval is divided into two 30° intervals. It is shown in [7] that the common mode offset given by (3.64) cannot be transformed for the three-level inverter with scaled reference waveforms since it violates certain boundary for certain intervals. However, 30° DPWM can be implemented in the three-level inverter by calculating the duty cycle of individual vector from space vector technique described in

subsection 4.2.2 and manipulating the duty cycle for the switching states to realize the vector in such a way that a phase is clamped for 4x30° interval in a fundamental cycle [7].

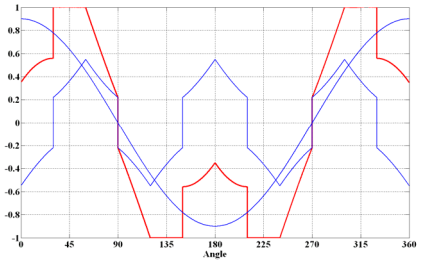


Figure 4-11 Modulating wave for m=0.9 for 30° DPWM for two-level inverter.

4.3 Control of the Neutral-Point Voltage

The three-level inverter has three voltage level at its DC-link; positive (P), negative (N), and neutral-point (O); as shown in Figure 4-1. The voltage differences among these levels in the DC-bus should be maintained constant for generating proper output voltages using the modulation strategies discussed in the previous section. Generally, the three-level inverter is supplied by a two-terminal voltage supply, which maintains the constant voltage difference between the positive and negative terminals of the inverter. However, the voltage of the neutral-point can vary during transients, due to non-idealities in the devices, or by tolerances of the DC-link capacitance values etc. This requires an additional control for the neutral-point voltage. There are two ways to control the neutral-point voltage:

- Additional circuit for maintaining the constant voltage [25], [38], [49], and [51].
- Controllers to modify the modulating signals to accomplish the neutral-point voltage control.

4.3.1 Circuits for Neutral-Point Voltage Control

Generally, high resistances are connected across the DC-link capacitors for balancing the voltage. It is shown in [51] that they can contribute to significant loss under certain conditions. An active voltage balancing circuit consisting of high impedance voltage divider and a complementary emitter-follower circuit was proposed in [51] as shown in Figure 4-12. High-voltage bipolar transistors are required for this configuration, but they have low current gain (typically 40) due to wide effective base region. So it is realized by a series of general-purpose low-voltage small-signal transistors with high current gain (typically 600-800). But high number of components is a disadvantage since it affects the reliability and requires bigger PCB area.

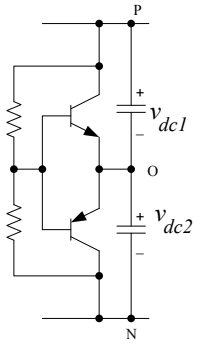


Figure 4-12 Voltage balancing circuit for DC-link electrolytic capacitor.

The disadvantage of higher number of components can be overcome by using a switch mode power converter as a voltage balancing circuit. A bidirectional buck-boost converter can be used as a voltage balancing circuit for the DC-link capacitors [25] as shown in Figure 4-13. Switches required to realize should be current-bidirectional two-quadrant switch. An IGBT with antiparallel diode can be used for this purpose. This circuit works on the principle of the buck-boost converter. If $v_{dc1}>v_{dc2}$, the duty cycle of top switch should be greater 0.5, and the energy will be transferred from the top capacitor to charge the bottom capacitor and vice versa.

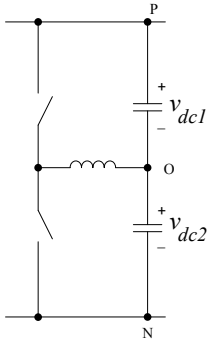


Figure 4-13 Bidirectional buck-boost converter for active voltage balancing

The size of the DC-link voltage balancing converter depends on many factors. One of them is energy that can be stored in the inductor used in the converter. If the energy is high, the balance can be achieved very fast but it requires a big inductor. A high power prototype of this topology with five-level inverter was presented in [49], [38]. In [38], a 1 MVA five-level inverter was conceptualized for high voltage application with the voltage balancing circuit rated at 6 kVA.

The active voltage balancing circuits provide an independent control of the neutral-point voltage for the multilevel inverter. However, they require extra hardware, which makes these solutions unattractive for low cost applications.

4.3.2 Neutral-Point Voltage Control by PWM Techniques

The neutral-point voltage is decided by the neutral-point current, and the neutral-point current is a function of the duty cycles of the three-phases and the output phase

currents. The time for which a phase is connected to different points in the DC bus can be modified without changing the line-line output voltage. In other words, the duty cycle of different phases can be changed by adding the common mode offset to the reference voltages for PWM without affecting the average line-line voltage. This common mode offset can be used as a control variable for the neutral-point voltage controller. An advantage of controlling the neutral-point voltage by PWM techniques is that it does not require an extra hardware circuit and a controller for the hardware. It requires only a neutral-point voltage controller whose output can be used as a common mode offset or duty cycle for different phases depending on the method.

Different neutral-point voltage controllers require models for the neutral-point voltage dynamics. Since the neutral-point voltage depends on neutral-point current, it is necessary to analyze the neutral-point current. The modulation methods affect the duty cycles of the phases to the neutral-point. Since the modulation methods can be divided into two groups; carrier-based PWM and space vector based PWM; the neutral-point current can be analyzed from two different point-of-views:

- Carrier-based PWM approach.
- Space vector based PWM approach.

4.3.2.1 Carrier-Based PWM Approach for Neutral-Point Current Analysis

In a carrier-based PWM for the three-level inverter, the three-phase voltage reference waveforms (modulating waveforms) are compared with two triangular carrier waveforms as shown in Figure 4-5. If a reference waveform is greater than zero, it is compared with carrier 1, and if it is less than zero, it is compared with carrier 2. From Figure 4-5, the duty cycle for which a phase is connected to the positive or negative bus in a switching period can be derived using symmetry of triangles. It is dependent on the reference voltage of a phase (see eq. (3.43)), and it is given by [21]

$$d_k = \begin{cases} v_{k,ref} + v_{off}, & \text{if} \quad \left(v_{k,ref} + v_{off}\right) > 0 \\ 0, & \text{if} \quad \left(v_{k,ref} + v_{off}\right) = 0 \\ -\left(v_{k,ref} + v_{off}\right), & \text{if} \quad \left(v_{k,ref} + v_{off}\right) < 0 \end{cases}$$

or

$$d_k = \left|v_{k,ref} + v_{off}\right| \qquad \text{where} \quad k = \{as, bs, cs\} \tag{3.66}$$

If a phase is not connected to the positive or negative DC bus, it will be connected to the neutral-point, and during that period, the phase current will contribute to the neutral-point current. Using this statement, it can be said that the average neutral-point current over a switching period is equal to the sum of the duty periods times the phase currents. So, the average neutral-point current over a switching period is given by

$$\langle i_o \rangle_{T_s} = \sum_k (1 - d_k) \cdot i_k \tag{3.67}$$

where $\langle\ \rangle_{Ts}$ denotes the average value of a particular variable over a switching period (T_s). i_o represents the neutral-point current, and i_k represents the output phase current of phase k. For a three-phase three wire system, the sum of the output currents is zero.

$$\sum_k i_k = i_{as} + i_{bs} + i_{cs} = 0 \tag{3.68}$$

Substituting (3.66) and (3.68) into (3.67), the average neutral-point current can be simplified as

$$\begin{aligned} \langle i_o \rangle_{T_s} &= \sum_k \left(1 - \left|v_{k,ref} + v_{off}\right|\right) \cdot i_k \\ \langle i_o \rangle_{T_s} &= \sum_k \left(-\left|v_{k,ref} + v_{off}\right|\right) \cdot i_k \end{aligned} \tag{3.69}$$

If the output currents of the inverter are given by

$$\begin{aligned} i_{as} &= I_m \cdot \cos(\omega t - \theta) \\ i_{bs} &= I_m \cdot \cos\left(\omega t - \frac{2\pi}{3} - \theta\right) \\ i_{cs} &= I_m \cdot \cos\left(\omega t + \frac{2\pi}{3} - \theta\right), \end{aligned} \tag{3.70}$$

the average neutral-point current can be plotted as a function of ωt. The power factor angle of the load is denoted by θ. The amplitude of the load current is represented by I_m. The average neutral-point current is shown in Figure 4-14 for sinusoidal PWM with m=0.9, I_m=15 A, and θ=30°. The average neutral-point current can be plotted for other modulation strategies using (3.69) since the reference waveforms for different modulation strategies can be obtained by changing the common mode offset.

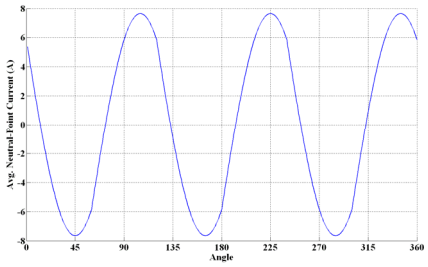


Figure 4-14 Average neutral-point current for sinusoidal PWM.

It can be seen from Figure 4-14 that the average neutral-point current is oscillating with a frequency which is three times the fundamental output frequency. It is shown in [19] that the average neutral-point current over the fundamental output period is zero for sinusoidal PWM. However, any DC component in the common mode offset results in nonzero neutral-point current averaged over one fundamental output period [21]. The neutral-point current averaged over one output fundamental

period as a function of DC common mode offset was derived in [19], [39] and can be given as

$$\langle i_o \rangle_{Tf} = \frac{3}{\pi}\cos(\theta) I_m \left[m\delta - \left(2v_{off} + m\sin\delta\right)\cos\delta \right] \tag{3.71}$$

where

$$\delta = \frac{\pi}{2} - \cos^{-1}\left(\frac{v_{off}}{m}\right) \tag{3.72}$$

and T_f is the fundamental time period of the inverter output voltage. It can be seen from (3.72) that δ= 0° for v_{off}=0 and using this, (3.71) yield zero average neutral-point average current over one output fundament cycle. A nonzero value of average neutral-point current can be obtained by using a nonzero value of v_{off}, which can be used for controlling the neutral-point voltage.

4.3.2.2 Space Vector PWM Based Approach for Neutral-Point Current Analysis

Carrier-based PWM methods are more popular due to their easy implementation capability, but space vector PWM gives a deeper insight on the inverter as a whole. The inverter is treated as a three-phase unit in a space vector approach instead of three single phase unit. The same approach of space vectors can be used for the neutral-point current analysis.

Different space vectors are realized by different switching states. It can be seen from Figure 4-4 that few space vectors can be realized by one or more than one switching states. However, they contribute to different neutral-point current. As an example, if we consider a space vector which can be realized either by (+ 0 0) or by (0 – –), the neutral-point current produced by the two switching states are different. For (+ 0 0), phase *b* and *c* are connected to the neutral-point so the neutral-point current is equal to the sum of phase *b* and *c* currents

$$(i_o)_{+00} = i_{bs} + i_{cs} = -i_{as} \tag{3.73}$$

On the other hand, for (0 – –), phase *a* is connected to the neutral-point which gives the neutral-point current as

$$(i_o)_{0--} = i_{as} \tag{3.74}$$

Similarly, the neutral-point current can be found for different switching , and it is shown in Figure 4-15. The neutral-point currents are indicated in a bracket beside corresponding switching states.

The neutral-point current averaged over a switching period can be calculated by adding the dwell times of switching states times the neutral-point currents which are generated by applying those switching states. The dwell times of the switching states depend on the reference vector position in the space vector diagram and its magnitude. If one sextant of the space vector diagram is considered, it can be divided into six subsectors as shown in Figure 4-16. Different vectors in the sextant are also marked in Figure 4-16. $\underline{\boldsymbol{V}}_{S0}$ and $\underline{\boldsymbol{V}}_{S1}$ represent the small vectors with two redundant switching states. $\underline{\boldsymbol{V}}_{L1}$ and $\underline{\boldsymbol{V}}_{L0}$ represent the long vectors which makes the

boundary of a sextant. $\underline{\boldsymbol{V_M}}$ represents the middle vector. The neutral-point current needs to be calculated for different subsectors separately since the switching states, which are applied, are different.

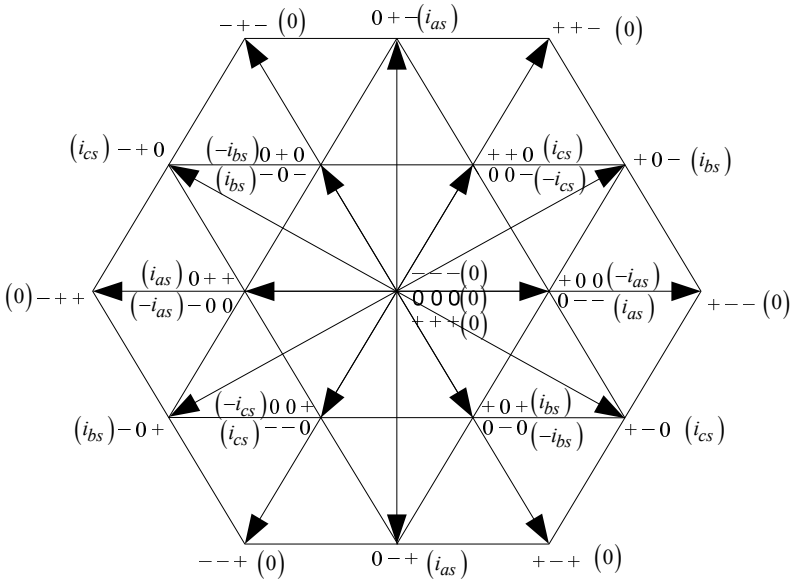


Figure 4-15 Neutral-point current due to different switching states.

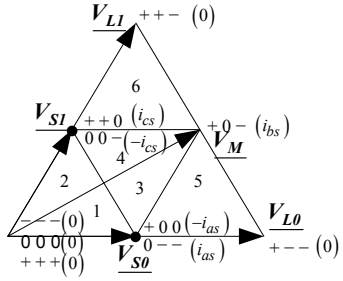


Figure 4-16 Subsectors in a sextant of space vector diagram.

If a reference vector lies in the subsector 1, 3, or 5, vector $\underline{\boldsymbol{V_{S0}}}$ is considered as center, and the duty cycles of (+ 0 0) and (0 – –) will be equal. It means that the neutral-point current because of $\underline{\boldsymbol{V_{S0}}}$ will be zero, and the neutral-point current can be given by

$$\begin{aligned}
\langle i_o \rangle_{T_s} &= -d_{S1} i_{cs} && \text{for subsector 1} \\
\langle i_o \rangle_{T_s} &= -d_{S1} i_{cs} + d_M i_{bs} && \text{for subsector 3} \\
\langle i_o \rangle_{T_s} &= d_M i_{bs} && \text{for subsector 5}
\end{aligned} \tag{3.75}$$

where d_{S1} and d_M are the duty cycle for $\underline{\boldsymbol{V_{S1}}}$ and $\underline{\boldsymbol{V_M}}$ vectors. On the other hand, if the reference vector lies in the subsector 2, 4, or 6, vector $\underline{\boldsymbol{V_{S1}}}$ is considered as a center and the duty cycles of (+ + 0) and (0 0 –) will be equal. In this case, the contribution of the vector $\underline{\boldsymbol{V_{S1}}}$ for the neutral-point current is zero. The neutral-point current will be due to $\underline{\boldsymbol{V_{S0}}}$ and $\underline{\boldsymbol{V_M}}$ vectors, and it is given by

$$\begin{aligned}
\langle i_o \rangle_{T_s} &= -d_{S0} i_{as} && \text{for subsector 2} \\
\langle i_o \rangle_{T_s} &= -d_{S0} i_{as} + d_M i_{bs} && \text{for subsector 4} \\
\langle i_o \rangle_{T_s} &= d_M i_{bs} && \text{for subsector 6.}
\end{aligned} \tag{3.76}$$

Similarly the neutral-point current can be calculated for other sextants also. The neutral-point current is shown in Figure 4-17 for space vector PWM with m=0.9, I_m=15 A, and θ=30°. It can be seen from Figure 4-17 that the average neutral-point current over a switching time period has a frequency, which is equal to thrice of the output fundamental frequency.

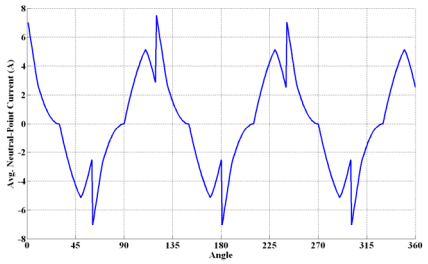


Figure 4-17 Average neutral-point current for Space Vector PWM.

Different PWM methods redistribute the duty cycles of the different switching states without changing line-line voltage. In this way, the neutral-point current can be changed. A general analysis for calculating the neutral-point current based on the space vector diagram was presented in [47].

4.3.2.3 Neutral-Point Voltage Control

Different methods of the neutral-point current analysis are used to determine the dynamics of the neutral-point voltage, and these methods can be used for the neutral-point voltage controller tuning. For a carrier-based modulation technique, it has been shown that the neutral-point current can be controlled by changing the common mode offset. Different PWM methods for reduced neutral-point voltage variation and controllers, which add the common mode offset to the three-phase reference voltages, are proposed in [19], [21], [22], [39], [48], and [76].

A common mode offset, which yield zero average neutral-point current in a switching period, is calculated in [21]. The calculation of the common mode offset requires the knowledge of the power factor angle, the phase angle of the reference voltages, and the amplitude of the reference voltage. However, the calculated common mode offset can be more than the maximum limit of the common mode offset that could be added under certain condition. This results nonzero neutral-point current which may cause oscillation in the neutral-point voltage, and the DC-link capacitor should be designed to limit that oscillation. Similar approach for adding a common mode offset to reduce the neutral-point current can be found in [22].

A closed loop controller design procedure was discussed in [19], [39] for the neutral-point voltage controller. In this controller, a DC common mode offset was used as a control variable. However, an equation, which describes dynamic behavior

of the neutral-point current as a function of the control variable for small variations, should be derived. The small-signal equation is required because of the nonlinear relationship between the neutral-point current and the common mode offset, which is given by (3.71). The small-signal equation can be derived by taking the partial derivative of (3.71) with respect to v_{off} and it is given by [39]

$$\frac{\partial\left(\langle i_o\rangle_{Tf}\right)}{\partial v_{off}} = \frac{\partial}{\partial v_{off}}\left(\frac{3}{\pi}\cos(\theta) I_m\left[m\delta - \left(2v_{off} + m\sin\delta\right)\cos\delta\right]\right)$$

$$\frac{\partial\left(\langle i_o\rangle_{Tf}\right)}{\partial v_{off}} = -6\cos(\theta) I_m\left[\frac{m^2 - 3v_{off}^2}{m^2\pi\sqrt{1-\frac{v_{off}^2}{m^2}}}\right] \tag{3.77}$$

Using (3.77), a simple proportional controller can be designed for the neutral-point voltage balance. A control system block diagram is shown in Figure 4-18.

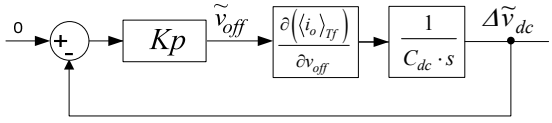


Figure 4-18 Neutral-point voltage closed loop control system.

The method discussed in [19] requires the power factor of the load currents, and the calculation of the power factor can be difficult to implement during transients. On the other hand, the method discussed in [39] requires change in the controller parameters if the direction of power flow is changed. An improved control algorithm was presented in [76], which does not require the power factor and the direction of power flow. It requires knowledge of the three-phase currents and the DC-link voltages. In this method, a common mode offset, which is added to the three-phase voltage references, is calculated depending on the phase currents and the controller output.

The methods discussed above use sinusoidal PWM which has a limitation of maximum modulation index of 1. However, space vector PWM has the capability to allow maximum modulation index of 1.1547 within the linear range. For space vector PWM, the neutral-point current can be controlled by changing the duty cycles of the redundant switching states which realize the space vector having length $v_{dc}/3$.

In the space vector PWM, one vector is realized by using two redundant switching states. As an example, if the reference vector is in subsector 1, only $\underline{\boldsymbol{V}}_{\boldsymbol{S0}}$ is realized by using redundant switching states (+ 0 0) and (0 – –). The space vector $\underline{\boldsymbol{V}}_{\boldsymbol{S1}}$ is realized by applying (0 0 –) even though the space vector $\underline{\boldsymbol{V}}_{\boldsymbol{S1}}$ can be realized by using the switching state (+ + 0) and (0 0 –), and the neutral-point current is decided by the state (0 0 –). A method proposed in [83] utilizes all the redundant switching states within a switching period to vary the neutral-point current and controls the neutral-point voltage. The duty cycles of the switching states are varied

using a controller. A detailed description of the controller can be found in [83]. In this method, it should be noted that if the reference vector lies in subsector 1,2,3, or 4, all switching states, which are required to realize $\underline{V}_{S0}$ and $\underline{V}_{S1}$, are used. On the other hand, if the reference vector lies in subsector 5 or 6, only the switching states, which are required to realize $\underline{V}_{S0}$ or $\underline{V}_{S1}$, is used, respectively. If all the switching states, which are required to realize $\underline{V}_{S0}$ and $\underline{V}_{S1}$, are used, a phase having middle value has to switch 4 times instead of 2 in a switching period. If subsector 1 or 2 is considered, the switching sequences will be (+ + +) (+ + 0) (+ 0 0) (0 0 0) (0 0 –) (0 – –) (– – –) and reverse. It can be seen from this sequence that the phase *b* is switching four times in a switching period, i.e., + →0→ – → 0 → +, while phase *a* is switching from + to 0 and phase *c* is switching between – and 0.

The approach discussed in [83] utilizes all the switching states and thus increases switching losses. However, it was shown in [13] that a discontinuous PWM can be used for neutral-point voltage control. In this method, vector $\underline{V}_{S0}$ and $\underline{V}_{S1}$ are realized by using only one of the redundant switching states. The switching states are chosen in such a way that a phase is not switching in a switching period. The choice of the phase, which will have no switching, depends on the power factor angle. The neutral-point voltage balance can not be obtained by adjusting the duty cycle of the redundant switching states in this method because this method uses only one of the redundant switching states, but the load to the DC-link capacitors can be controlled by choosing proper sequence. The current drawn from the DC-link capacitors depends on the power factor angle also. Same switching sequence can load top DC-link capacitor more than the bottom DC-link capacitor or vice versa depending on the power factor angle. This property is used to balance the DC-link capacitor voltages and control the neutral-point voltage.

The controllers discussed above have different limitations depending on their implementation techniques. The method discussed in [21] produces zero neutral-point current under certain conditions only and this method fails to produce zero neutral-point current at high modulation index. The methods discussed in [19], [39] also can't control the neutral-point voltage at high modulation index, since they add a DC common mode offset to the voltage reference and at high modulation index, the controller may demand a common mode offset, which corresponds to the reference voltage of greater than 1. The advanced control discussed in [13], [22], [48], and [76] require the knowledge of phase currents or power factor angle and controller output depends on that. The implementation of such controller is more complicated because of that.

Most of the PWM techniques discussed above works with sinusoidal PWM and space vector PWM. However, the average neutral-point current averaged over one switching period is not zero and it can be seen from Figure 4-14 and Figure 4-17 that the peak value of that can be as high as 8 A for 15 A peak load current value and it is a function of load power factor angle, peak load current, and modulation index. This peak current decides the size of the DC-link capacitor, since the neutral-point current creates a third harmonic voltage oscillation in the neutral-point and the peak-peak value of voltage oscillation is decided by the DC-link capacitors. It has been shown in [15] that the size of DC-link capacitors for the three-level NPC inverter

can be 50% more than that of a two-level inverter for a fixed output frequency operation. Different modulation strategies were developed to reduce the size of DC-link capacitors. Those PWM techniques and the neutral-point voltage controller for them will be discussed in the next section.

4.4 PWM Techniques and Controllers with Zero Neutral-Point Current

The neutral-point current is one of the major deciding factors while selecting the DC-link capacitors for the three-level NPC inverter as discussed in the previous section. If the average neutral-point current over a switching period can be made zero, the DC-link capacitor size can be reduced. Some modulation strategies that guarantee zero average neutral-point current were proposed in literature [43], [68]. These modulation strategies utilize the redundant switching states in the NPC three-level inverter.

4.4.1 PWM Techniques with Zero Neutral-Point Current

It was shown in Figure 4-15 that different switching states cause neutral-point current. The redundant switching states of the vector with length $v_{dc}/3$ cause same neutral-point current but in opposite direction. This property was utilized to control neutral-point current. However, if the redundant switching vectors are applied for equal amount of time in a switching period, the average neutral-point current caused by them will be zero. Using this approach, the neutral-point current can be maintained only for low modulation index. For high modulation index, if the reference voltage vector lies in subsector 2-6 of Figure 4-16, it will be required to apply vector $\underline{\boldsymbol{V}}_{\boldsymbol{M}}$, which contributes to the neutral-point current. The neutral-point current due to $\underline{\boldsymbol{V}}_{\boldsymbol{M}}$ can't be made zero since this vector does not have redundant switching states. A PWM strategy was proposed in [43], which overcomes this problem and allows the control of the neutral-point voltage over the full range of modulation index and for any three-phase three-wire load.

In the method, which was proposed in [43], virtual vectors are defined as combination of switching states in such a way that each virtual vector produces zero average neutral-point current. Using these virtual vectors, any reference voltage vector was synthesized. Since the average neutral-point current produced by each vector is zero, the average neutral-point current will become zero in a switching period. The virtual vectors for one sector of the space vector diagram are shown in Figure 4-19. It can be seen from Figure 4-19, that the virtual vectors $\underline{\boldsymbol{V}}_{\boldsymbol{Z0}}$, $\underline{\boldsymbol{V}}_{\boldsymbol{ZL0}}$ and $\underline{\boldsymbol{V}}_{\boldsymbol{ZL1}}$ are generated by switching states (000), (+ – –) and (+ + –), respectively and these switching states do not generate any neutral-point current. $\underline{\boldsymbol{V}}_{\boldsymbol{ZS0}}$ and $\underline{\boldsymbol{V}}_{\boldsymbol{ZS1}}$ are generated by all the redundant switching states as described above. It should be noted in this modulation strategy that a virtual vector is defined as a combination of three switching states (0 – –), (+ 0 –), and (+ + 0). These three states are applied for equal amount of time to synthesize the virtual vector. This virtual vector is denoted by $\underline{\boldsymbol{V}}_{\boldsymbol{ZM}}$. The three switching states, which are used to synthesize the virtual vector,

are chosen in such a way that the neutral-point current generated is equal to the sum of output phase currents. In the first sextant of the space vector diagram, (0 – –), (+ 0 –) and (+ + 0) are chosen because the neutral-point current generated by them are equal to i_{as}, i_{bs}, and i_{cs}, respectively. Since the sum of these currents is zero for a three-phase three-wire system, the average neutral-point current produced by this virtual vector is also zero.

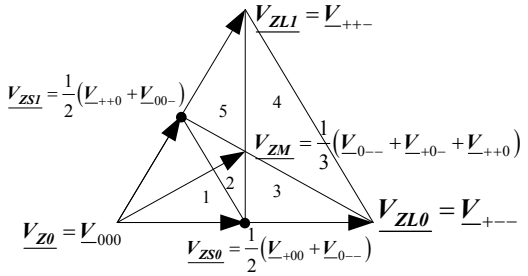


Figure 4-19 Virtual space vectors for first sextant of the space vector diagram.

These virtual vectors redefine the subsectors in a sextant of the space vector diagram. It can be seen from Figure 4-19 that there are 5 subsectors in a sextant in this case. The reference voltage vector lying in a subsector is realized by three virtual vectors, which are the three vertices of the subsector triangle. Another important point about this PWM strategy is that a phase, which has middle voltage value in a switching period, switches 4 times instead of 2 in a switching period. In the first sextant of the space vector diagram, phase *b* has the middle voltage value and it switches 4 times in a switching period. It is shown in Table 4-3, which describes the switching sequence in each subsector, that phase *b* switches from terminal N to terminal O and terminal O to terminal P and vice versa in each subsector. This results in increased switching in the inverter.

Table 4-3 Switching sequence for PWM with virtual vectors

Subsector	Virtual Vectors	Switch Sequence
1	$\underline{V}_{ZS0}$, $\underline{V}_{ZS1}$, $\underline{V}_{Z0}$	(0 – –)(0 0 –)(0 0 0)(+ 0 0)(+ + 0) and reverse
2	$\underline{V}_{ZS0}$, $\underline{V}_{ZS1}$, $\underline{V}_{ZM}$	(0 – –)(0 0 –)(+ 0 –)(+ 0 0)(+ + 0) and reverse
3	$\underline{V}_{ZS0}$, $\underline{V}_{ZL0}$, $\underline{V}_{ZM}$	(0 – –)(+ – –)(+ 0 –)(+ 0 0)(+ + 0) and reverse
4	$\underline{V}_{ZL0}$, $\underline{V}_{ZL1}$, $\underline{V}_{ZM}$	(0 – –)(+ – –)(+ 0 –)(+ + –)(+ + 0) and reverse
5	$\underline{V}_{ZS1}$, $\underline{V}_{ZL1}$, $\underline{V}_{ZM}$	(0 – –)(0 0 –)(+ 0 –)(+ + –)(+ + 0) and reverse

The details of the modulation strategy with virtual vectors can be found in [43]. from space vector point of view. A simple carrier-based implementation of this PWM strategy was discussed in [68]. According to [68], each phase has two modulating signals (one modulating signal for carrier 1 and another for carrier 2) and the modulating signals for a phase were derived as

$$\begin{cases} v_{kp,ref} = \dfrac{v_{k,ref} - v_{\min}}{2} \\ v_{kn,ref} = \dfrac{v_{k,ref} - v_{\max}}{2} \end{cases} \quad \text{for } k = \{as, bs, cs\} \tag{3.78}$$

where $v_{kp,ref}$ and $v_{kn,ref}$ represent the phase k modulating signal for carrier waveform 1 and 2, respectively. It can be seen from (3.78) that the modulating signal, which will be compared with carrier 2 ($v_{kn,ref}$), will be zero for the phase having maximum value since it is equal to the half of difference of the reference signal and maximum value among the reference signals. Similarly, the modulating signal, which will be compared with carrier 1 ($v_{kp,ref}$), for the phase having minimum value will be zero. However, the phase having middle value will have nonzero values for both modulating signals and it corresponds to four transitions instead of two transitions in this output phase voltage.

A different approach to make average neutral-point current zero was proposed in [10] and it was termed as radial state space vector modulation. In this PWM technique, the switching states, which have vector length of $v_{dc}/\sqrt{3}$, are not applied. They are approximated by the large vectors of length $2{\cdot}v_{dc}/3$ because they do not cause any neutral-point current. If first sextant of the space vector diagram is considered, the switching state (+ 0 –) is not applied. Instead of this, the switching states (+ + –) and (+ – –) are applied. The neutral-point current caused by the small vectors of length $v_{dc}/3$ is zero since both redundant switching states are applied for equal amount of time to generate each small vector with equal and opposite neutral-point current. The switching sequence for first sextant of the space vector is given in Table 4-4. The subsectors mentioned in Table 4-4 is as per Figure 4-16. It can be seen for Table 4-4 that the switching state (+ + –) is applied after (+ – –) in the switching sequence for subsector 3-6. This requires switching of phase b from terminal N to terminal P of the DC-link without connecting to terminal O. This switch sequence creates additional switching losses in the three-level inverter as compare to the modulation strategy with virtual vectors and it is not preferable.

Table 4-4 Switching sequence for radial state space vector modulation

Subsector	Switch Sequence
1 & 2	(0 – –)(0 0 –)(0 0 0)(+ 0 0)(+ + 0) and reverse
3-6	(0 0 –)(0 – –)(+ – –)(+ + –)(+ + 0)(+ 0 0) and reverse

4.4.2 Neutral-Point Voltage Controller based on Zero Neutral-Point Current PWM Techniques

The neutral-point voltage controllers presented in [44], [68], and [84] are based on modulation strategies producing zero average neutral-point current in a switching period. The neutral-point current carries only switching-frequency components in this case. Thus the required DC-link capacitance is minimal. The controllers presented in [44], [68], and [84] add offset to the duty ratios of the inverter switches. The controller presented in [44] uses the optimized virtual-vector-based modulation strategy for low output voltage distortion and it is a generalized version of PWM method proposed in [43]. The controller presented in [44] calculates a DC common mode offset which acts as a control variable. The common mode offset is added to the reference voltages in such a way that the switching frequency remains unchanged. This requires addition of the offset to the modulating signal for carrier 1

in case of the phase having maximum value, addition of the offset to the modulating signal for carrier 2 in case of the phase having minimum value, and addition a part of the offset to the modulating signal for carrier 1 and rest to the modulating signal for carrier 2 in case of the phase having middle value. However, the relationship between the control variable (DC common mode offset) and the neutral-point voltage is discontinuous and criterion to design the controller was not presented.

The carrier-based implementation of the PWM strategy, which insures zero neutral-point current presented in [68], does not require the knowledge of the reference voltage vector angle. This makes the implementation very simple. The controller for neutral-point voltage proposed in [68] also adds an offset to the duty ratios. The offset added to the duty cycle of a phase depends on the sign of the neutral-point voltage variation times the phase current. This makes the controller discontinuous and nonlinear. The design criterion for the determination of the controller parameters is also not discussed. An optimal controller based on the modulation strategy presented in [68] was developed in [84] but it requires the information of the output currents, the modulation index, the carrier frequency, the DC-link capacitor values, and the DC-link voltages. This controller guarantees stability under all operating conditions, but this requires high computational effort for the controller.

4.5 Summary and Conclusion

The operation of three-level NPC converter is discussed in this chapter. Different conventional modulation strategies cause neutral-point voltage oscillation and the peak-peak voltage variation is dependent on the size of DC-link capacitors. For a fixed frequency operation, if conventional modulation strategies, e.g. sinusoidal PWM or space vector PWM, are used, the required DC-link capacitor size will be 50% higher than that of the two-level inverter. The size of DC-link capacitor can be more for variable frequency operation of the three-level inverter for adjustable speed drives and it depends on the lowest frequency at which the system is supposed to operate. However, different modulation strategies, which produce zero average neutral-point current in a switching period, exist in the literature. If these modulation strategies are used, the neutral-point current contains only high frequency harmonic components caused by switching frequency. In this case, the size of the DC-link capacitor can be reduced to minimal. If the DC-link capacitor size is reduced, the neutral-point voltage can vary for very small disturbances in the system. This requires a fast and stable neutral-point voltage controller. Different controllers, which are applied with these modulation strategies, were proposed in the literature. However, the controllers are based on the nonlinear and discontinuous system model. The controller design becomes very complicated due to this. A continuous model describing the dynamics of the neutral-point voltage is proposed in the next chapter. Using this model, a controller is designed and tested for small DC-link capacitor based three-level inverter.

Chapter 5

Three-level Inverter with Small DC-link Capacitor

A Neutral-Point-Clamped (NPC) three-level inverter can be a viable alternative for low voltage drive applications as mentioned in the previous chapter. The NPC three-level inverter, with conventional modulation, was seen to require 50% higher capacitance at the DC-link compared to a two-level inverter for a fixed grid frequency operation [15]. A high capacitance value requires the use of electrolytic capacitors. The higher reliability of film capacitors has been a major driving force to reduce the value of capacitance and be able to use them [9]. A small DC-link capacitor based NPC three-level converter is presented in this chapter.

A small DC-link capacitor based NPC three-level converter requires zero average neutral-point current in a switching period. A suitable modulation strategy, similar to the PWM presented in [43] and [68], is selected for meeting this condition. This strategy is derived using different approach for carrier-based implementation in Section 5.1. Since a small disturbance in the neutral-point current can drift the neutral-point voltage in a few switching periods because of the low energy stored in the DC-link capacitors, a fast and stable controller for the neutral-point voltage balance is required. In Section 5.2, a new first-order model of the neutral-point voltage dynamics is presented, and this model is based on a continuous equation. With this new model, classical control theories can be applied to design the controller for the neutral-point voltage balance. The controller design is presented in Section 5.3. A simple Proportional-Integral (PI) controller is used to control the neutral-point voltage. The considerations required to implement the PWM for a small DC-link capacitor based converter are discussed in Section 5.4. The implementation of the proposed controller with modulation strategy only requires the information of the sensed DC-link voltages and the PI controller. It does not require output phase current information and the reference voltage vector angle. The controller is tested with an induction machine drive of 7.5 kW output power. The neutral-point is realized by the mid point of two series-connected 14 μF capacitors. The experimental results, which verify the fast dynamics of the controller, are presented for this drive in Section 5.5.

5.1 Carrier-Based PWM for Zero Neutral-Point Current

It has been shown in previous chapter that zero average neutral-point current can be achieved if a phase having the middle voltage value can be connected to the positive (P), the negative (N), and the neutral-point (O) of the DC-link. This requires four switching transitions instead of two for the phase in a switching time period as shown in Figure 5-1. In addition to this, a common mode offset needs to be added to the sinusoidal PWM reference voltages.

Since the phases require four switching transition in the interval when they have middle voltage value, each phase will have two modulating waveforms, one modulating for each carrier waveform. If a phase has a maximum value, the value of modulating reference signal for carrier 2 will be zero. If a phase has a minimum value, the value of modulating reference signal for carrier 1 will be zero. The value of reference voltages for carrier 1 and carrier 2 is marked by *p* and *n* subscript. *d* denotes the duty cycle for a particular phase; max, mid, and min subscripts represent the phase having the maximum, the middle, and the minimum fundamental voltage values, respectively; e.g., $d_{\max p}$ represents the duty cycle of the phase having the maximum voltage value and connected to the positive terminal (P) of the DC-bus.

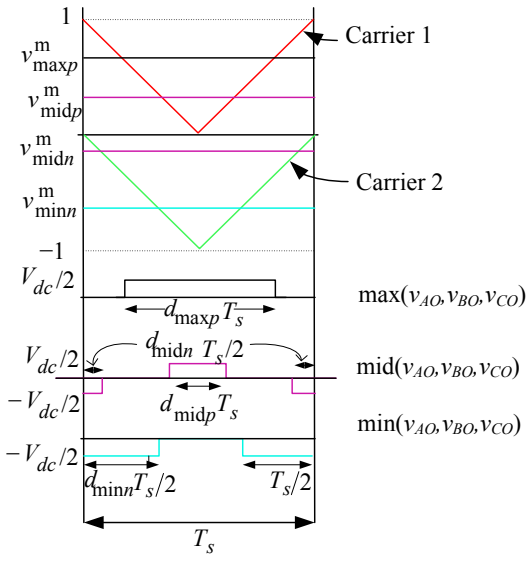


Figure 5-1 Three phase reference voltages for zero neutral-point current.

Let us consider, the modified reference voltages for a carrier-based implementation of the PWM with zero average neutral-point current are given by

$$
\begin{aligned}
v_{\max p}^{\mathrm{m}} &= v_{\max} + v_{off} \\
v_{\max n}^{\mathrm{m}} &= 0 \\
v_{\mathrm{mid}p}^{\mathrm{m}} &= \frac{v_{\mathrm{mid}}}{2} + v_{off1} \\
v_{\mathrm{mid}n}^{\mathrm{m}} &= \frac{v_{\mathrm{mid}}}{2} + v_{off2} \\
v_{\min p}^{\mathrm{m}} &= 0 \\
v_{\min n}^{\mathrm{m}} &= v_{\min} + v_{off}
\end{aligned}
\tag{4.1}
$$

where $v_{off1} + v_{off2} = v_{off}$ (to add the same common mode offset to all three-phases). Superscript 'm' denotes the modified variable. v_{off1} and v_{off2} are the common mode offsets added to the two reference voltages of the phase having the middle voltage value. Using (4.1), the modified duty cycles are given by

$$
\begin{aligned}
d_{\max p}^{\mathrm{m}} &= v_{\max} + v_{off} \\
d_{\max n}^{\mathrm{m}} &= 0 \\
d_{\mathrm{mid}p}^{\mathrm{m}} &= v_{\mathrm{mid}}/2 + v_{off1} \\
d_{\mathrm{mid}n}^{\mathrm{m}} &= -\left(v_{\mathrm{mid}}/2 + v_{off2} \right) \\
d_{\min p}^{\mathrm{m}} &= 0 \\
d_{\min n}^{\mathrm{m}} &= -\left(v_{\min} + v_{off} \right)
\end{aligned}
\tag{4.2}
$$

The common mode offsets v_{off1} and v_{off2} should be calculated in such a way that the average neutral-point current over one switching period will be zero. The neutral-point current averaged over one switching period can be given by

$$
\begin{aligned}
\langle i_o \rangle_{T_s} &= \left(1 - d_{\max p} - d_{\max n}\right) \cdot i_{\mathrm{vmax}} + \left(1 - d_{\mathrm{mid}p} - d_{\mathrm{mid}n}\right) \cdot i_{\mathrm{vmid}} + \left(1 - d_{\min p} - d_{\min n}\right) \cdot i_{\mathrm{vmin}} \\
\langle i_o \rangle_{T_s} &= -\left(d_{\max p} + d_{\max n}\right) \cdot i_{\mathrm{vmax}} - \left(d_{\mathrm{mid}p} + d_{\mathrm{mid}n}\right) \cdot i_{\mathrm{vmid}} - \left(d_{\min p} + d_{\min n}\right) \cdot i_{\mathrm{vmin}}
\end{aligned}
\tag{4.3}
$$

where i_{vmax}, i_{vmid}, and i_{vmin} are the currents of the phases which have the maximum, the middle, and the minimum fundamental voltage values, respectively. Substituting (4.2) into (4.3), the average neutral-point current can be given as

$$
\begin{aligned}
\langle i_o \rangle_{T_s} &= -\left(v_{\max} + v_{off}\right) \cdot i_{\mathrm{vmax}} - \left(v_{\mathrm{mid}}/2 + v_{off1} - v_{\mathrm{mid}}/2 - v_{off2} \right) \cdot i_{\mathrm{vmid}} + \left(v_{\min} + v_{off}\right) \cdot i_{\mathrm{vmin}} \\
\langle i_o \rangle_{T_s} &= -\left(v_{\max} + v_{off}\right) \cdot i_{\mathrm{vmax}} - \left(v_{off1} - v_{off2}\right) \cdot i_{\mathrm{vmid}} + \left(v_{\min} + v_{off}\right) \cdot i_{\mathrm{vmin}}
\end{aligned}
\tag{4.4}
$$

It can be seen from (4.4) that there is no neutral-point current term because of v_{mid}, since v_{off1} and v_{off2} are added to half of v_{mid} to obtain the duty cycles $d_{\mathrm{mid}p}^{\mathrm{m}}$ and $d_{\mathrm{mid}n}^{\mathrm{m}}$ as given in (4.2). For a three-phase three-wire system, $i_{\mathrm{vmax}} + i_{\mathrm{vmid}} + i_{\mathrm{vmin}} = 0$. Using this relationship, equation (4.4) can be simplified as

$$
\begin{aligned}
\langle i_o \rangle_{T_s} &= -\left(v_{\max} + v_{off}\right) \cdot i_{\mathrm{vmax}} + \left(v_{off1} - v_{off2}\right) \cdot \left(i_{\mathrm{vmax}} + i_{\mathrm{vmin}}\right) + \left(v_{\min} + v_{off}\right) \cdot i_{\mathrm{vmin}} \\
\langle i_o \rangle_{T_s} &= \left(-v_{\max} - 2v_{off2}\right) \cdot i_{\mathrm{vmax}} + \left(v_{\min} + 2v_{off1}\right) \cdot i_{\mathrm{vmin}}
\end{aligned}
\tag{4.5}
$$

The zero average neutral-point current condition ($\langle i_o \rangle_{T_s}$=0) can be achieved by different values of v_{off1} and v_{off2}. One set of possible and simple choice of v_{off1} and v_{off2} is given by

$$\begin{aligned} v_{off\,1} &= -v_{\min}/2 \\ v_{off\,2} &= -v_{\max}/2 \\ \Rightarrow v_{off} &= v_{\mathrm{mid}}/2 \end{aligned} \tag{4.6}$$

and the modified phase reference voltages are given by

$$\begin{aligned} v^{\mathrm{m}}_{\max\,p} &= (v_{\max} - v_{\min})/2 \\ v^{\mathrm{m}}_{\max\,n} &= 0 \\ v^{\mathrm{m}}_{\mathrm{mid}p} &= (v_{\mathrm{mid}} - v_{\min})/2 \\ v^{\mathrm{m}}_{\mathrm{mid}n} &= -(v_{\max} - v_{\mathrm{mid}})/2 \\ v^{\mathrm{m}}_{\min\,p} &= 0 \\ v^{\mathrm{m}}_{\min\,n} &= -(v_{\max} - v_{\min})/2 \end{aligned} \tag{4.7}$$

The modified reference voltages for phase *a* are shown in Figure 5-2 for modulation index 1.1547. The reference phase voltages for other phases will be shifted in phase by 2π/3 and 4π/3 radians. It can be seen from Figure 5-2 that the maximum modulation index achieved in the linear range is 1.1547, which is equal to the maximum modulation index achieved by space vector PWM [80]. The reference voltage waveform for this modulation strategy is the same as of Nearest Three Virtual Space Vector PWM proposed in [43]. A fast carrier-based implementation of this modulation strategy was proposed in [68]. This implementation is similar to the carrier-based implementation of PWM given by (4.7). The main advantage of this implementation is its simplicity and maximum utilization of the modulation index linear range to achieve $\langle i_o \rangle_{Ts}$=0.

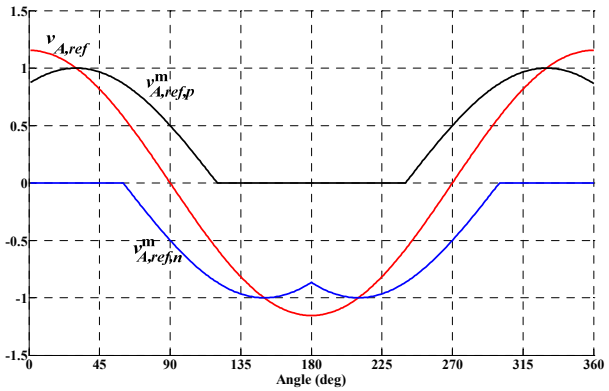


Figure 5-2 Reference voltage waveform of phase A for carrier-based implementation to achieve $\langle i_o \rangle_{Ts}$=0 (m=1.1547).

5.2 Model of Neutral-Point Voltage Dynamics

The modified reference voltage waveforms given by (4.7) ensure zero average neutral-point current in a switching time period for ideal conditions of high inductive load, ideal switching devices, etc. The non-idealities of the components, transients, etc., may cause the unbalance of the neutral-point voltage. A closed loop controller is required to maintain the neutral-point voltage balance. To design a neutral-point voltage controller, a model describing the dynamic behavior of the neutral-point voltage is required.

It is shown in the previous section that zero average neutral-point current can be achieved if the common mode offsets, given by (4.6), are added to the reference voltages for sinusoidal PWM, and the phase having the middle voltage value have four transitions in the switching period. The carrier-based implementation of the PWM with zero neutral-point current is extended in this section to gain the control over the neutral-point voltage. A new factor k is introduced which will be used as a control variable for the neutral-point voltage controller. The reference voltages for carrier 1 are made proportional to k, and the reference voltages for carrier 2 are proportional to (1-k). Using this, the modified phase reference voltages are given as

$$\begin{aligned}
&v_{\max p}^{\mathrm{m}} = k\cdot\left(v_{\max}-v_{\min}\right)\\
&v_{\max n}^{\mathrm{m}} = 0\\
&v_{\mathrm{mid}p}^{\mathrm{m}} = k\cdot\left(v_{\mathrm{mid}}-v_{\min}\right)\\
&v_{\mathrm{mid}n}^{\mathrm{m}} = -\left(1-k\right)\cdot\left(v_{\max}-v_{\mathrm{mid}}\right)\\
&v_{\min p}^{\mathrm{m}} = 0\\
&v_{\min n}^{\mathrm{m}} = -\left(1-k\right)\cdot\left(v_{\max}-v_{\min}\right)
\end{aligned} \tag{4.8}$$

and the duty cycles are given as

$$\begin{aligned}
&d_{\max p}^{\mathrm{m}} = k\left(v_{\max}-v_{\min}\right)\\
&d_{\max n}^{\mathrm{m}} = 0\\
&d_{\mathrm{mid}\,p}^{\mathrm{m}} = k\left(v_{\mathrm{mid}}-v_{\min}\right)\\
&d_{\mathrm{mid}\,n}^{\mathrm{m}} = \left(1-k\right)\left(v_{\max}-v_{\mathrm{mid}}\right)\\
&d_{\min p}^{\mathrm{m}} = 0\\
&d_{\min n}^{\mathrm{m}} = \left(1-k\right)\left(v_{\max}-v_{\min}\right)
\end{aligned} \tag{4.9}$$

It can be seen from (4.8) that the factor k is applied in such a way that the line-line voltages are not changed. As a check, the line-line voltage between the phase having the maximum voltage value and the phase having the middle voltage value can be derived as

$$\begin{aligned}
&\left(v_{\max p}^{\mathrm{m}}+v_{\max n}^{\mathrm{m}}\right)-\left(v_{\mathrm{mid}p}^{\mathrm{m}}+v_{\mathrm{mid}n}^{\mathrm{m}}\right)\\
&= k\left(v_{\max}-v_{\min}\right)-k\left(v_{\mathrm{mid}}-v_{\min}\right)+\left(1-k\right)\left(v_{\max}-v_{\mathrm{mid}}\right)\\
&= v_{\max}-v_{\mathrm{mid}}\,.
\end{aligned} \tag{4.10}$$

In this case, the common mode offsets added to the voltage reference signals for sinusoidal PWM are functions of k as given by

$$\begin{aligned} v_{off1} &= -k \cdot v_{\min} \\ v_{off2} &= -(1-k) \cdot v_{\max} \\ \Rightarrow v_{off} &= v_{off1} + v_{off2} = -k \cdot v_{\min} - (1-k) \cdot v_{\max}. \end{aligned} \tag{4.11}$$

The modified reference voltages for phase a are shown in Figure 5-3 for modulation index 0.9 with different values of k. The reference phase voltages for other phases will be shifted in phase by $2\pi/3$ and $4\pi/3$ radians. Since the reference voltages for the PWM are a function of the factor k as given by (4.8), the average neutral-point current of the inverter will also be a function of factor k. From (4.3) and (4.9), an expression for the neutral-point current is derived as

$$\begin{aligned} \langle i_o \rangle_{T_s} &= -k(v_{\max} - v_{\min}) \cdot i_{v\max} - (1-k)(v_{\max} - v_{\min}) \cdot i_{v\min} - \left(k.(v_{\mid} - v_{\min}) + (1-k)(v_{\max} - v_{\mid})\right) \cdot i_{v\mid} \\ \langle i_o \rangle_{T_s} &= -k \cdot (v_{\max} - v_{\min}) \cdot i_{v\max} + (1-2k) \cdot v_{\mid} \cdot i_{v\mid} + (-k \cdot v_{\min} + (1-k) \cdot v_{\max}) \cdot (i_{v\max} + i_{v\min}) \\ &\quad -(1-k) \cdot (v_{\max} - v_{\min}) \cdot i_{v\min} \\ \langle i_o \rangle_{T_s} &= (1-2k)(v_{\max} \cdot i_{v\max} + v_{\min} \cdot i_{v\min} + v_{\mid} \cdot i_{v\mid}) \end{aligned}$$

$$\langle i_o \rangle_{T_s} = \frac{1-2k}{v_{dc}} \langle p_e \rangle_{T_s} \tag{4.12}$$

where p_e is the output power of the inverter. Equation (4.12) is the expression for the neutral-point current as a function of k, and it shows that the neutral-point current is proportional to the output power drawn from the converter. If k =0.5, the reference voltages given by (4.8) will be equal to the reference voltages given by (4.7), and the average neutral-point current will be zero.

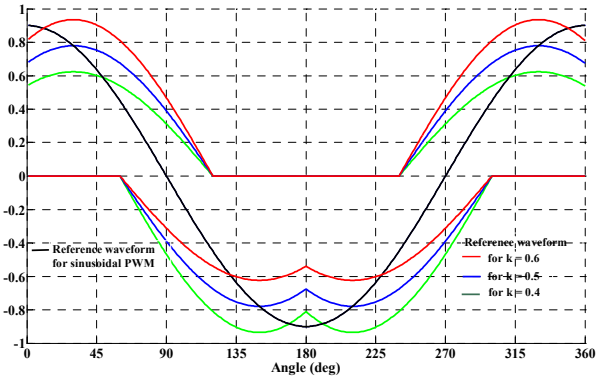


Figure 5-3 Reference voltage waveforms for different values of k (m=0.9)

Since the neutral-point voltage variation depends on the neutral-point current, a model for the neutral-point voltage dynamics can be obtained as a function of factor k. This requires an equivalent circuit diagram, which is shown in Figure 5-4, of the average neutral-point voltage. The top and bottom DC-link capacitor voltages are shown by v_{dc1} and v_{dc2}. The current through the capacitors are given by i_{dc1} and i_{dc2}. By applying the Kirchoff's Current Law at node O, the average DC-link capacitor voltage variation in T_s ($\langle \Delta v_{dc} \rangle_{T_s}$) can be derived as

$$\langle i_{dc1}\rangle_{T_s} - \langle i_{dc2}\rangle_{T_s} = \langle i_o\rangle_{T_s}$$

$$C_{dc}\cdot\frac{d}{dt}\left(\langle v_{dc1}\rangle_{T_s} - \langle v_{dc2}\rangle_{T_s}\right) = \frac{1-2k}{v_{dc}}\langle p_e\rangle_{T_s}$$

$$C_{dc}\cdot\frac{d}{dt}\left(\langle \Delta v_{dc}\rangle_{T_s}\right) = \frac{1-2k}{v_{dc}}\langle p_e\rangle_{T_s} \tag{4.13}$$

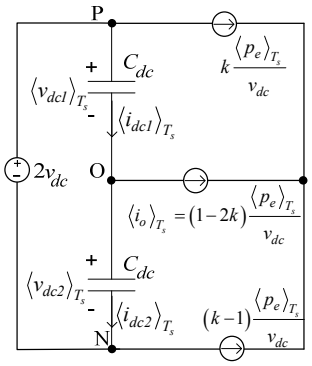


Figure 5-4 Equivalent circuit diagram of the DC-link in the NPC three-level converter.

It can be seen from (4.13) that the DC-link capacitor voltage variation is a continuous function of the output power of the inverter, the factor *k*, and the DC-link voltage, but it is a nonlinear function. So a linearized model describing the behavior of the neutral-point voltage dynamics for small AC perturbations about a DC operating point should be derived. The model can then be treated as a linear system, and linear control theories can be applied. To derive the linearized model, small AC perturbations, represented by "~", are introduced in DC operating point values. The DC operating point values are represented by capital letters. Therefore,

$$\begin{aligned}
&\langle p_e\rangle_{T_s} = P_e + \tilde{p}_e \\
&v_{dc} = \frac{V_{dc}}{2} + \tilde{v}_{dc} \\
&\langle \Delta v_{dc}\rangle_{T_s} = \Delta V_{dc} + \Delta\tilde{v}_{dc} \\
&k = K + \tilde{k}
\end{aligned} \tag{4.14}$$

The steady state solution of (4.13) can be given by

$$\begin{aligned}
&C_{dc}\cdot\frac{d}{dt}\left(\Delta V_{dc}\right) = \frac{1-2K}{V_{dc}}P_e = 0 \\
&K = 0.5
\end{aligned} \tag{4.15}$$

which corresponds to the DC operating point values. Using (4.13), (4.14), and (4.15)

$$C_{dc}\cdot\frac{d}{dt}\left(\Delta V_{dc} + \Delta\tilde{v}_{dc}\right) = \frac{1-2\left(K+\tilde{k}\right)}{V_{dc}+\tilde{v}_{dc}}\cdot\left(P_e + \tilde{p}_e\right)$$

$$\text{or, } C_{dc}\cdot\frac{d}{dt}\left(\Delta\tilde{v}_{dc}\right) = \frac{1-2K}{V_{dc}}\tilde{p}_e - \frac{2P_e}{V_{dc}}\tilde{k} - \frac{1-2K}{V_{dc}^2}P_e\cdot\tilde{v}_{dc}$$

or, $C_{dc} \cdot \frac{d}{dt}\left(\Delta\tilde{v}_{dc}\right) = -\frac{2P_e}{V_{dc}}\tilde{k}$ (4.16)

Equation (4.16) is the linearized model, and it is an equation of a first-order system. It shows that the dynamics of the neutral-point voltage depends on the factor *k*. Equation (4.16) can be used as a plant model to design the neutral-point voltage controller based on classical control theories, which require the transfer function of the plant. Using Laplace transformation of (4.16); the transfer function of the plant, i.e. the transfer function of the control variable $\tilde{k}$ to the output $\Delta\tilde{v}_{dc}$, is given by

$$G_{vk}(s) = \frac{\Delta\tilde{v}_{dc}(s)}{\tilde{k}(s)} = -\left(\frac{2P_e}{V_{dc} \cdot C_{dc}}\right)\frac{1}{s} \quad (4.17)$$

It can be seen from (4.17) that the transfer function is proportional to the average power. If the average power changes, the plant transfer function will change. V_{dc} can be assumed constant since it is determined by the grid supply voltage.

5.3 Controller for Neutral-Point Voltage Balance

A high performance neutral-point voltage controller is required for the small DC-link capacitor based NPC three-level converter. The average neutral-point current can be controlled by changing factor *k*, which in turn controls the neutral-point voltage. The factor *k* will be used as a control variable for the neutral-point voltage controller. The new first-order model of the average neutral-point voltage variation is given by (4.16). Classical linear control theories can be used to design a fast and stable controller using this model. A simple PI controller is used. The block diagram of the controller is given in Figure 5-5. The transfer function given by (4.17) can be used to choose the parameters of the PI controller.

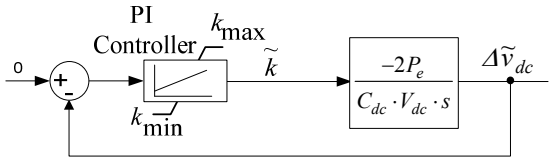


Figure 5-5 Neutral-point voltage controller block diagram.

The transfer function of the PI controller is given by

$$G_c(s) = K_p \frac{1 + s \cdot T}{s \cdot T} \quad (4.18)$$

where K_p is the proportional gain and *T* is the integral time of the controller.

Using (4.17) and (4.18), the open loop transfer function of the neutral-point voltage control system is given by

$$G_{OL}(s) = G_c(s).G_{vk}(s) = -K_p \frac{1 + s \cdot T}{s \cdot T} \frac{2P_e}{V_{dc} \cdot C_{dc} \cdot s} \quad (4.19)$$

The open loop transfer function given by (4.19) can be interpreted as a multiplication of two terms; $\frac{1+s\cdot T}{s\cdot T}$ and $\frac{-2K_pP_e}{V_{dc}\cdot C_{dc}\cdot s}$. The gain crossover frequency of the open loop transfer function is decided by the term $\frac{-2K_pP_e}{V_{dc}\cdot C_{dc}\cdot s}$ if T is chosen such that it will not affect the gain crossover frequency. Assuming this, the gain crossover frequency of the open loop transfer function is given by

$$\omega_c = -\frac{2K_pP_e}{V_{dc}\cdot C_{dc}} \tag{4.20}$$

From (4.20), K_p can be given by

$$K_p = -\omega_c \frac{V_{dc}\cdot C_{dc}}{2P_e}. \tag{4.21}$$

The PI controller is designed for the maximum power condition. The bode plots of plant $(G_{vk}(s))$, controller $(G_c(s))$, and the open loop $(G_{OL}(s))$ transfer functions are shown in Figure 5-6. The value of K_p is chosen in such a way that the gain crossover frequency (ω_c) of the open loop transfer function is 1 kHz. The gain crossover frequency is chosen as one tenth of the switching frequency (10 kHz). The maximum power corresponds to the maximum value of ω_c. If the power is reduced, ω_c will be reduced for a given K_p. If the PI controller was designed for the induction machine no-load condition, ω_c could then become higher than the switching frequency at full load condition which is not recommended.

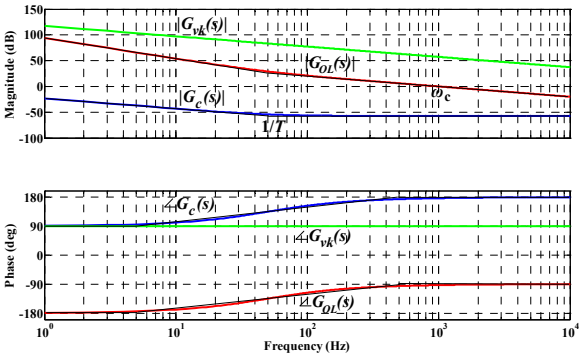


Figure 5-6 Bode plot of plant, controller, and open loop transfer function.

The integral time (T) of the PI controller is the inverse of the corner frequency of the PI controller. This corner frequency should be lower than ω_c to have high phase margin for the whole operating range. The corner frequency of the PI controller is chosen as 50 Hz. This will ensure that even if the power is reduced to 10% of the maximum, i.e., ω_c is reduced to 10% of the maximum, the corner frequency of PI controller will be lower than the gain crossover frequency (ω_c) of the open loop transfer function $(G_{OL}(s))$.

The factor k is the control variable and it is equal to the output of the PI controller. The output of the PI controller should be limited since the control

variable k decides the duty cycle of the switches in the converter. The maximum and minimum limits of the PI controller output are given by $k_{\max}$ and $k_{\min}$. The control variable k should be limited in such a way that the reference phase voltages for carrier 1 be between 0 and 1, and the reference phase voltage for carrier 2 be between 0 and −1 to ensure the PWM operation in the linear range. Using (4.9), the limits for the controller output are given by

$$k_{\max} = \min\left(\frac{1}{v_{\max} - v_{\min}}, 1\right)$$
$$k_{\min} = \max\left(1 - \frac{1}{v_{\max} - v_{\min}}, 0\right) \tag{4.22}$$

5.4 Small DC-Link Capacitors Based Converter

The drive system under consideration is shown in Figure 5-7, where a six-pulse rectifier is used as a front end converter. The six-pulse diode bridge rectifier generates 300 Hz ripple at its output voltage. The DC-link capacitor is used to maintain a constant voltage at DC-link. This requires large value of the DC-link capacitors. Typically the DC-link capacitor is sized in such a way that the DC-link LC filter cutoff frequency will be less than 300 Hz. In that case, the capacitance has a value in the order of a few mF and electrolytic capacitors are required. However, the input supply current has high THD if the rectifier is loaded with a big capacitor. To improve the input supply current THD, the DC-link capacitance value is reduced [82]. Film capacitors are used as the DC-link capacitor which improves the reliability of the drive system as well. In this case, the DC-link voltage features of 300 Hz ripple, and the minimum and maximum values of the DC-link voltage are given by

$$\min\left(v_{dc1}(t) + v_{dc2}(t)\right) \approx v_{l,peak} \cos\left(\frac{\pi}{6}\right) = \frac{3}{2}\sqrt{2} \cdot v_g$$
$$\max\left(v_{dc1}(t) + v_{dc2}(t)\right) \approx v_{l,peak} = \sqrt{6} \cdot v_g \tag{4.23}$$

where $v_{l,peak}$ is the peak line -line voltage supplied by the grid, and v_g is the rms value of the grid phase voltage. The voltage drop across the DC-link inductor is neglected for simplicity.

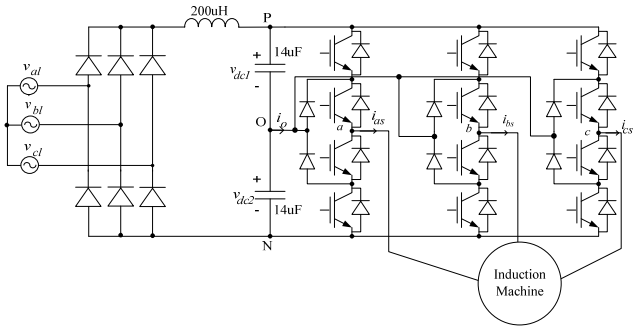


Figure 5-7 Circuit diagram of the NPC converter based drive with small DC-link capacitors.

A space vector modulation strategy for the small DC-link capacitor based two-level converter is proposed in [82], where the modulation index is time-varying and determined by the DC-link voltage in every switching cycle in order to get a sinusoidal output voltage. It is shown in [82] that the maximum modulation index corresponds to the minimum DC-link voltage avoiding the overmodulation region in the space vector modulation strategy. This limits the output voltage of the inverter. As an example, for 230 V grid phase rms voltage, the maximum output phase rms voltage for the modulation index of 1.1547 can be given as

$$v_{o,\max} = \frac{\min\left(v_{dc1} + v_{dc2}\right)}{2}\frac{1.1547}{\sqrt{2}} = \frac{\sqrt{3}\cdot v_g}{2} = 200\,\text{V} \tag{4.24}$$

The maximum output fundamental rms voltage can be increased if the modulation index is constant. If the resistive drop of the DC-link choke is neglected, the average value of the DC-link voltage can be given by

$$V_{dc} = \frac{3\sqrt{6}}{\pi} v_g \tag{4.25}$$

If the DC-link voltage ripple is denoted by v_{dch}, the DC-link voltage can be given as

$$v_{dc} = V_{dc} + v_{dch} \tag{4.26}$$

Substituting (4.26) in (3.44)

$$\begin{aligned}
\left\langle v_{AO} \right\rangle_{T_s} &= m \cdot \frac{\left(V_{dc} + v_{dch}\right)}{2} \cdot \cos\left(\omega_s t\right) \\
\left\langle v_{BO} \right\rangle_{T_s} &= m \cdot \frac{\left(V_{dc} + v_{dch}\right)}{2} \cdot \cos\left(\omega_s t - 2\pi/3\right) \\
\left\langle v_{CO} \right\rangle_{T_s} &= m \cdot \frac{\left(V_{dc} + v_{dch}\right)}{2} \cdot \cos\left(\omega_s t - 4\pi/3\right)
\end{aligned} \tag{4.27}$$

Since $m \cdot v_{dch}$ has an average value equal to zero, the rms value of the inverter output voltage is

$$v_o = m\frac{V_{dc}}{2\sqrt{2}} \tag{4.28}$$

Substituting (4.25) and the maximum modulation index m=1.1547 in (4.28)

$$v_{o,\max} = 1.1547\frac{3\sqrt{6}}{2\sqrt{2}\pi} v_g = \frac{3}{\pi} v_g = 220\ \text{V} \tag{4.29}$$

The maximum output voltage is increased to 220 V in the linear range. The small DC-link capacitor based converter improves the input line THD, but this modulation strategy causes harmonics at the inverter output voltage, which in turn causes low-order harmonics in the machine phase currents. The three level inverter with stiff DC-link voltage is compared to a small DC-link capacitor based converter in terms of the machine current harmonics and the input supply current THD in the next section. The small DC-link capacitor based converter has small amount of energy stored in the DC-link capacitor, and a high performance controller is required for the

neutral-point voltage balance. The performance of the controller is also verified experimentally in the next section.

5.5 Experimental Results

The block diagram of the drive system is shown in Figure 5-8.The drive system utilizes the NPC three-level converter with the small DC-link capacitors fed from a six-pulse diode bridge rectifier. The diode bridge rectifier is directly connected to grid. The grid has 230 V line-neutral rms voltage which corresponds to V_{dc} = 538 V. The induction machine is rated for 7.5 kW power as the shaft output power. This requires an output power of the three-level inverter of 8.7 kW approximately (P_e=8.7 kW). The rating of the induction machine is given in Table 5-1. The three-level inverter is realized using SEMIKRON IGBT module SK30MLI066. Each module has 4 IGBTs and 6 diodes required for one leg of the NPC three-level converter.

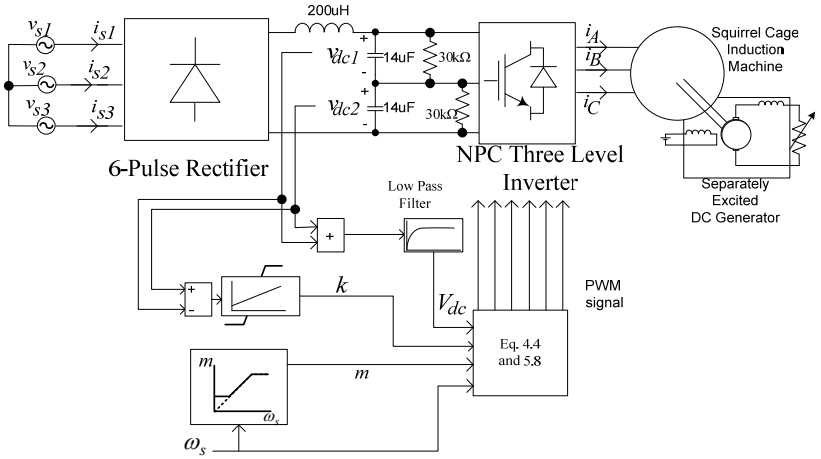


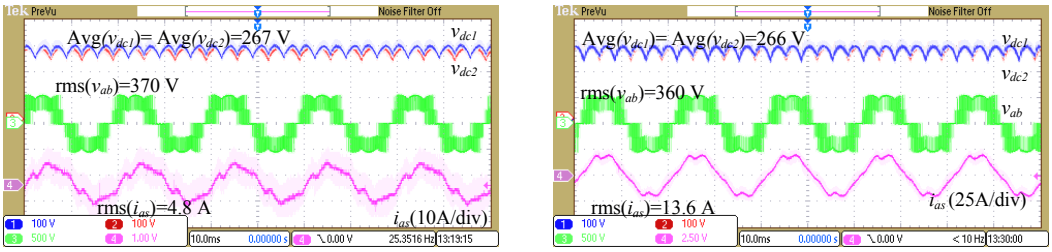
Figure 5-8 Block diagram of the drive system with controller.

Table 5-1 Induction machine ratings

Rotor Mechanical Power	7500 W
Input Phase Voltage (rms)	220 V
Input Phase Current (rms)	14.8 A
Output Speed	2920 rpm
Rated Output Torque	24.6 N·m

The DC-link capacitors used in the converter are 14 μF each, as shown in Figure 5-8. The drive is controlled using the open loop *V*/*f* control. The maximum modulation ratio of 1.1547 is used at 50 Hz supply frequency to the inverter. The experimental results are shown for 500 Hz and 1000 Hz gain crossover frequencies of the open loop transfer function designed at the maximum power (P_e=8.7 kW). Using (4.21), the values of K_p can be calculated as −0.0007 and −0.0014 for 500 Hz and 1000 Hz gain crossover frequencies, respectively. The integral time (T) of the controller is chosen as $1/(100\pi)$ as discussed in the previous section.

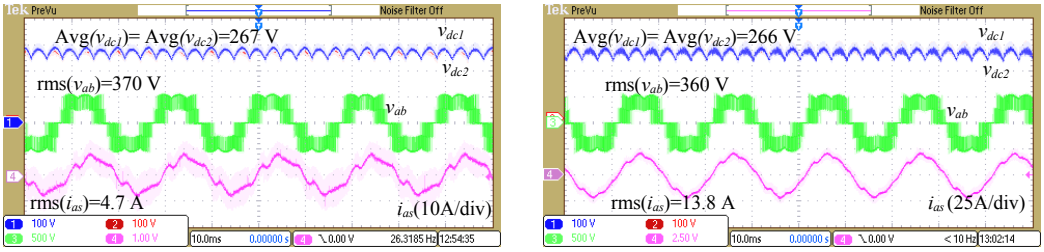
Figure 5-9 (a) and (b) show the DC-link voltages (v_{dc1}, v_{dc2}), the induction machine line current (i_A), and the machine line-line voltage (v_{AB}) at no load and full load at induction machine output. The results shown in Figure 5-9 are for K_p = −0.0007. This is designed to obtain the gain crossover frequency (ω_c) of 500 Hz at full load. The gain crossover frequency (ω_c) at no load will be approximately 50 Hz since the output power of the inverter is reduced to 10%. The low value of ω_c corresponds to the high time constant of the closed loop transfer function [4]. It can be seen in Figure 5-9 that v_{dc1} and v_{dc2} are not equal, and it affects the harmonic components of the machine voltage, which causes 1.9% weighted total harmonic distortion (WTHD) in the machine phase current at full load.



(a) (b)

Figure 5-9 v_{dc1}, v_{dc2}, machine phase current (i_{as}), and machine L-L voltage (v_{ab}) for ω_c=500 Hz and14 µF DC-link capacitors. (a) Induction machine at no load.
(b) Induction machine at 7.5 kW output mechanical power.

The response of the drive system for 1 kHz gain crossover frequency (ω_c) at maximum power is shown in Figure 5-10 with K_p = −0.0014. Figure 5-10 (a) and (b) show the DC-link voltages (v_{dc1}, v_{dc2}), the induction machine line current (i_A), and the machine line-line voltage (v_{AB}) at no load and full load at induction machine output. The gain crossover frequency (ω_c) at the no load on the induction machine will be 100 Hz. It can be seen that this choice of K_p = −0.0014 provides the performance with the neutral-point voltage balance in the whole power range. The waveforms for the DC-link voltages (v_{dc1}, v_{dc2}) are equal in this case, and the induction machine output phase current WTHD is reduced to 1.2% at full load.



(a) (b)

Figure 5-10 v_{dc1}, v_{dc2}, machine phase current (i_{as}), and machine L-L voltage (v_{ab}) for ω_c=1 kHz and14 µF DC-link capacitors. (a) Induction machine at no load.
(b) Induction machine at 7.5 kW output mechanical power.

The current harmonics in the induction machine depend on the voltage harmonics injected to the machine and the impedance offered by the leakage inductances of the machine at those frequencies [70]. Since the voltage harmonics injected to the machine do not change as the load increases, the current harmonics will also not change. Since the fundamental current value is lower, the WTHD at no load increases to 3.3%.

The results shown in Figure 5-9 and Figure 5-10 are having 300 Hz ripple in the DC-link voltages because of an equivalent 7 µF DC-link capacitor (series combination of two 14 µF capacitors) and 200 µH DC-link choke. This corresponds to the DC-link LC filter cutoff frequency of 4 kHz. To compare the performance of this converter with the converter having stiff DC-link voltage, the DC-link capacitor is changed to 1.65 mF (series combination of two 3.3 mF capacitors) without changing the DC-link choke. This corresponds to the DC-link LC filter cutoff frequency of 275 Hz. The DC-link voltages (v_{dc1}, v_{dc2}), the induction machine line current (i_{as}), and the machine line-line voltage (v_{ab}) at full load at induction machine output are shown in Figure 5-11. It can be seen from Figure 5-11 that the machine current waveform is less distorted, and the machine current WTHD is reduced to 0.9%, which is mainly caused by the switching frequency harmonics. On the other hand, the input line current waveform is deteriorated as shown in Figure 5-12(a) with 104% line current THD. Figure 5-12(b) shows the input line current and the output line-line voltage waveform of the drive system at full load condition with 14 µF DC-link capacitors. The input line current THD is 29.6% for 14 µF DC-link capacitors. The input line current THD and output machine current WTHD are given in Table 5-2.

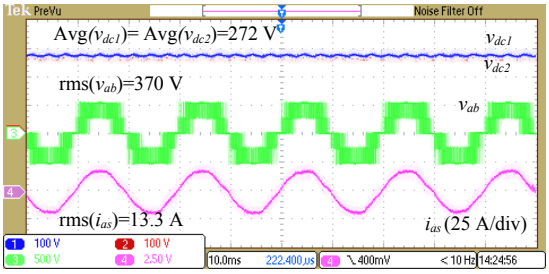
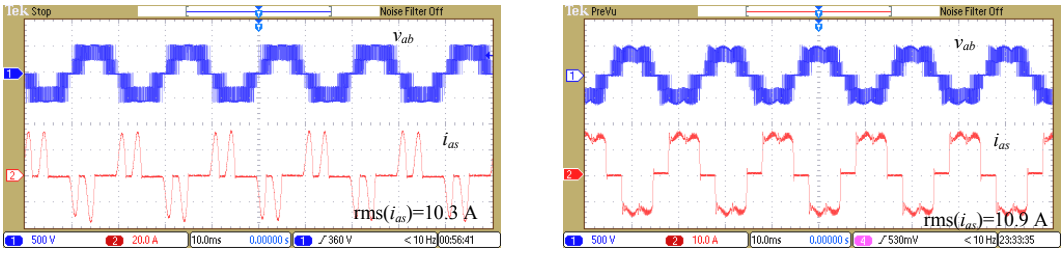


Figure 5-11 v_{dc1}, v_{dc2}, machine phase current (i_{as}), and machine L-L voltage (v_{ab}) for ω_c=1 kHz with induction machine at 7.5 kW output mechanical power and 3.3 mF DC-link capacitors.



(a) (b)

Figure 5-12 Input phase current (i_{s1}) and machine L-L voltage (v_{AB}) with induction machine at 7.5 kW output mechanical power. (a) C_{dc}=3.3 mF. (b) C_{dc}=14 µF.

Table 5-2 Input line current THD and output machine current WTHD at 7.5 kW output power

CONDITIONS	INPUT LINE CURRENT THD	MACHINE CURRENT WTHD
C_{dc}=3.3 mF & ω_c=1 kHz	104%	0.9%
C_{dc}=14 µF & ω_c=1 kHz	29.6%	1.2%
C_{dc}=14 µF & ω_c=500 Hz	31%	1.9%

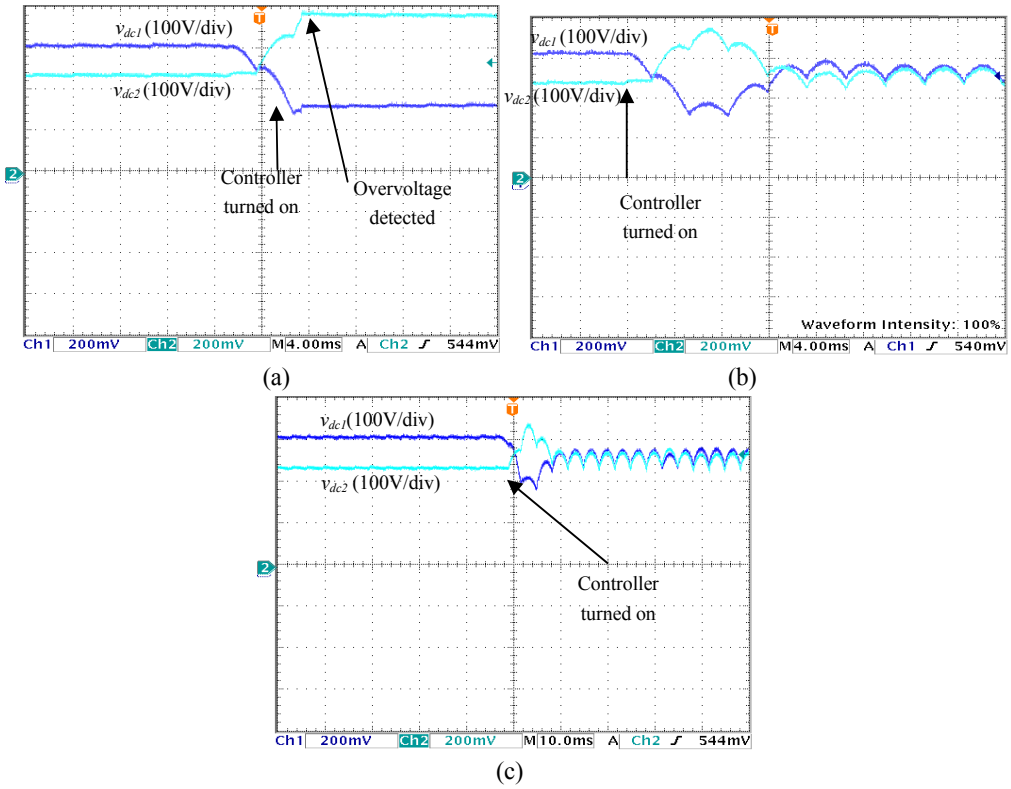


Figure 5-13 v_{dc1}, v_{dc2} response under unbalance. (a) K_p= −0.0007. (b) K_p= −0.0014. (c) K_p= −0.0028.

The results shown in Figure 5-9 and Figure 5-10 are for steady state with 30 kΩ resistances across the DC-link capacitors as shown in Figure 5-8. An unbalance in the DC-link voltages is created by changing 30 kΩ to 25 kΩ across the bottom DC-link capacitor, and it cuases a voltage difference of 50 V between the two capacitor voltages. The response of the DC-link voltage for different choices of K_p are shown in Figure 5-13. Figure 5-13(a) shows the response for K_p = −0.0007. A high overshoot, because of low crossover frequency, causes the overvoltage across the bottom DC-link capacitor, and the converter is switched off. Figure 5-13(b) shows the response for K_p = −0.0014. It can be seen that the DC-link voltage balance is achieved within 24 ms after the controller is turned on. The controller is turned on with the induction machine at no load, since there is no current controller for the induction machine. This condition corresponds to low gain crossover frequency (ω_c) for a given K_p. A faster response to correct the unbalance can be achieved by using a higher absolute value of K_p as shown in Figure 5-13(c) for K_p = −0.0028. The DC-link balance is achieved within 12 ms in this case with reduced overshoot. A higher

absolute value of K_p is not used to improve the response further, because it will cause very high bandwidth of the open loop transfer function $(G_{OL}(s))$ at maximum power which is not recommended. The response of the neutral-point voltage controller can be controlled by changing the gain of the PI controller. If an online tuning of the PI controller as a function of power is used, optimal performance can be achieved in the whole operating range, but it needs more computation in a switching period.

5.6 Summary and Conclusion

A NPC three-level converter with small DC-link capacitors is presented in this chapter. The converter utilizes a modulation strategy with zero average neutral-point current in a switching period. A new model describing the dynamics of the neutral-point voltage is proposed. This simplified model shows that the neutral-point current is proportional to the output power of the converter. A methodology to design the neutral-point voltage PI controller is presented using classical control theory. The controller output is used to calculate the modified reference phase voltage signals. The modified reference phase voltages are used for carrier-based implementation of the modulation strategy. The proposed controller does not require the information of the output phase current. The controller performance is verified experimentally for a 7.5 kW induction machine based drive with only 14 μF DC-link capacitors. The experimental results show the operation of the drive at the maximum modulation index of 1.1547. The experimental results show that the controller is able to maintain balanced capacitor voltages with 10 kHz switching frequency in the presence of 300 Hz ripple of the DC-link voltages caused by the six-pulse rectifier. It is also shown that the small DC-link capacitor based converter improves the line current THD, but the proposed modulation strategy causes low-order harmonics in the machine current since the average DC-link voltage is used for the duty cycle calculation. The performance for the DC-link unbalance condition is also studied for different gains of the PI controller. A fast settling time is achieved with the higher absolute gain.

The simple implementation of the controller and modulation strategy presented in this chapter requires minimal computation. The neutral-point voltage controller presented is verified for a small and big DC-link capacitor based drive, which shows that the approach is very general. It can be used for any NPC three-level converter in other applications, e.g., for grid connected three-level NPC converter.

Chapter 6

Performance Comparison of Two-Level and Three-Level Inverter with Small DC-Link Capacitors

The small DC-link capacitor based inverters have the advantages of reduced size and high reliability. The NPC three-level inverter can also be operated with small DC-link capacitors as described in the previous chapter. The NPC three-level inverter requires higher number of power semiconductors as compared to that of the two-level inverter. The NPC inverter requires 12 insulated gate bipolar transistors (IGBT) and 18 diodes as compared to 6 IGBTs and 6 diodes, which are required for a two-level inverter. This increases the control capability of the inverter with increased number of switching states as discussed in chapter 4 and 5, but it also increases the complexity of hardware realization of the inverter. This difficulty can be overcome by using the modules for realizing a leg of the NPC three-level inverter produced by different manufacturers [88], [90], [93], and [94]. However, each IGBT requires a gate drive circuit and an isolated power supply for the gate driver. The design of a simple power supply circuit for gate drivers of the NPC three-level inverter was proposed in [12]. This design does not require any isolated power supply for the gate drivers. In spite of increased number of active components in the NPC three-level inverter, it was shown in [77] that it have advantages of reduced common mode voltage and losses as compared to the two-level inverter. The comparison shown in [77] is valid for the inverters with standard PWM techniques, such as sinusoidal PWM or space vector PWM. However, it was shown in the previous chapters that it is not feasible to operate a small DC-link capacitors based drive with these PWM techniques. Therefore, it is required to compare the performance of small DC-link capacitors based two-level and three-level inverters.

In this chapter, the efficiency, the common mode voltage, the shaft voltage, and the EMC performance are compared for the two-level and three-level inverter with small DC-link capacitors. The common mode voltage, EMC performance, and efficiency of the inverters are compared since they are the major factors for deciding the size of passive components in inverters. Section 6.1 discusses the common mode voltage generated by the two-level and the three-level inverter. A small description of the setup for measuring the machine shaft voltage is also presented in Section 6.1.

The experimental results comparing the machine shaft voltages generated by the two-level and three-level inverter will be presented. Section 6.2 discusses the EMC measurement setup and results comparing the performance of the ASD fed by the two-level and three-level inverter. Section 6.3 presents the results comparing the efficiency of the two-level and three-level inverter fed drive system.

6.1 Common Mode Voltage and Shaft Voltage

Common mode voltage is defined as a voltage which appears in common at all the terminals of a device with respect to ground. For the inverter, it is a voltage that appears in common at all the output terminals of the inverter with respect to ground. A typical ASD system block diagram, which shows the connections between ASD and ground, is shown in Figure 6-1. It can be seen from Figure 6-1, that the output terminals (*a*, *b*, and *c*) of the inverter are connected to the machine. The common mode voltage for the inverter can be defined as the voltage (v_{nG}) between the neutral terminal *n* and the ground (*G*), since the sum of voltages of the output terminal of the inverter with respect to the neutral terminal is zero for a balanced load.

$$v_{an} + v_{bn} + v_{cn} = 0 \tag{4.30}$$

The common mode voltage (v_{nG}) can be expressed as the sum of two voltages, voltage (v_{OG}) of the neutral-point of the DC-link with respect to ground and voltage (v_{nO}) of the neutral terminal (*n*) with respect to the neutral-point of DC-link [55]. It can be given by

$$v_{nG} = v_{OG} + v_{nO} \tag{4.31}$$

It was shown in [35] that the first component (v_{OG}) of the common mode voltage (v_{nG}) is the low frequency amplitude modulated ripple component with frequency of six times the input grid frequency component, and the second component (v_{nO}) has high frequency component due to inverter switching. The high frequency component of the common mode voltage due to switching states of the inverter can be expressed as

$$v_{nO} = \frac{v_{aO} + v_{bO} + v_{cO}}{3} \tag{4.32}$$

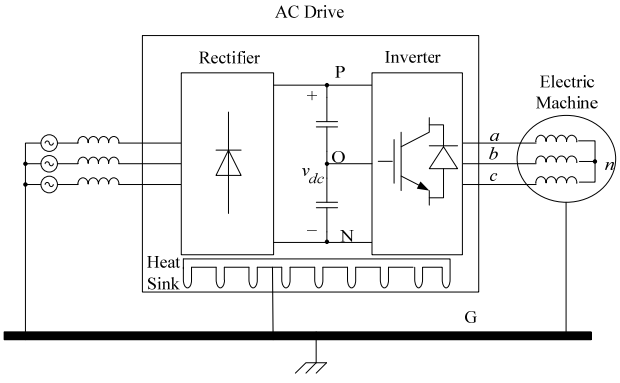


Figure 6-1 Block diagram of an ASD with ground connections.

The two-level inverter has 8 switching states and the three-level inverter has 27 switching states. Each switching state generates a common mode voltage (v_{nO}) as given by (4.32). The common mode voltages generated by the switching states of the two-level inverter and the three-level inverter are given in Table 6-1 and Table 6-2, respectively.

Table 6-1 Common mode voltage for two-level inverter

Switching States	Common Mode Voltage (v_{nO})
+ + +	$v_{dc}/2$
+ − +, + + −, − + +	$v_{dc}/6$
− + −,− − +, + − −	$-v_{dc}/6$
− − −	$-v_{dc}/2$

Table 6-2 Common mode voltage for three-level inverter

Switching States	Common Mode Voltage (v_{nO})
+ + +	$v_{dc}/2$
+ + 0, + 0 +, 0 + +	$v_{dc}/3$
+ − +, + + −, − + +, 0 0 +, 0 + 0, + 0 0	$v_{dc}/6$
0 0 0, + 0 −, + − 0, 0 + −, 0 − +, − + 0, − 0 +	0
− + −, − − +, + − −, 0 − 0, 0 0 −, − 0 0	$-v_{dc}/6$
0 − −, − 0 −, − − 0	$-v_{dc}/3$
− − −	$-v_{dc}/2$

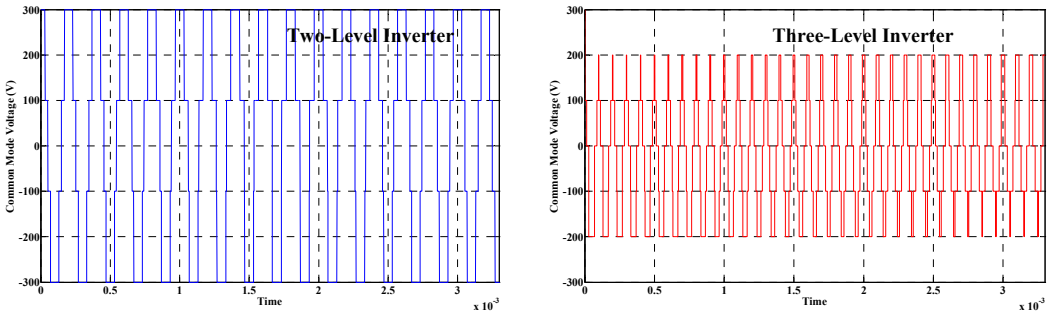
It can be seen from Table 6-1 that the common mode voltage generated by the switching states (+ + +) and (− − −) are $v_{dc}/2$ and $-v_{dc}/2$, respectively which are highest in magnitude. In the three-level inverter, if the switching state (0 0 0) is applied instead of the switching states (+ + +) and (− − −), the common mode voltage can be reduced, and the maximum magnitude of the common mode voltage generated by the inverter can be $v_{dc}/3$ and $-v_{dc}/3$.

Different PWM strategies were proposed for common mode voltage reduction for the two-level inverter. A review of different common mode reduction techniques for the two-level inverter can be found in [55]. Different modulation strategies for common mode voltage reduction have limitations in achieving either high or low modulation index. So the conventional space vector PWM method is used because it provides full utilization of the DC-link voltage with minimum switching.

Different PWM strategies for reducing or eliminating the common mode voltage generated by the NPC three-level inverter were presented in [20], [27], [53], [79], [61], and [69]. However, these modulation techniques require high value of the DC-link capacitance.

The modulation strategy used for small DC-link capacitor based three-level inverter is described in the previous chapter. It was shown that this modulation strategy is the same as proposed in [43] if k=0.5 is substituted in (5.8). The space vector representation of this modulation strategy was shown in Figure 4-19. It can be seen from Figure 4-19 that the virtual vector $\underline{V}_{Z0}$, which is used to realize the zero vector in the modulation strategy proposed in [43], uses only switching state (0 0 0) thus avoiding the switching states with high common mode voltage.

The PWM strategies used for the small DC-link capacitor based three-level inverter and two-level inverter are simulated. Space vector PWM is used for the two-level inverter. The common mode voltages (v_{nO}) for the two-level and three-level inverter are shown in Figure 6-2. The DC-link voltage is assumed to be 600 V. It can be seen from Figure 6-2 that the common mode voltage for the three-level inverter has peak-peak value of 400 V as compared to 600 V of peak-peak value for the two-level inverter.



(a) (b)

Figure 6-2 Common mode voltage (v_{nO}) for (a) three-level and (b) two-level inverter.

The common mode voltage has high frequency component with high dv/dt as shown in Figure 6-2. A portion of this common mode voltage appears across the shaft of the machine and ground [50] due to the parasitic capacitance between the shaft and the machine chassis. This voltage is referred as shaft voltage [50]. This voltage is one of the reasons for the parasitic bearing currents [23], [34], [36], and [50] which may lead to bearing failure of the machine.

6.1.1 Experimental Setup and Results

The common mode voltage and the shaft voltage generated by the two-level and the three-level inverter are measured. Both inverters have small DC-link capcitors. The two-level inverter and the machine used are from an existing product from Grundfos [89]. The power level of the product is 7.5 kW, and the inverter has the DC-link capacitor of 14 µF capacitance. Space vector PWM is used in the product with switching frequency of 9 kHz.

The product is an integrated drive system, where the two-level inverter is mounted on the stator frame of the machine. The three-level inverter is developed using the chassis of the same product in such a way that the three-level inverter can replace the two-level inverter without any mechanical modification in the machine

chassis. The three-level inverter details were presented in the previous chapter. The switching frequency used for the three-level inverter is 10 kHz.

The block diagram of the measurement setup for the common mode voltage and the shaft voltage is shown in Figure 6-3. The common mode voltage is measured across the star point of the three resistors with high resistances and the ground as shown in Figure 6-3. The value of resistance is 39.4 kΩ. The resistance network should be balanced to create a balance star point.

The shaft voltage is measured between the machine shaft and the machine frame, which is connected to ground. Since the shaft is rotating, an arrangement is made for the shaft voltage measurement. In this measurement setup, a contact, which has a cable of maintaining electrical connection even though one part is rotating, is used.

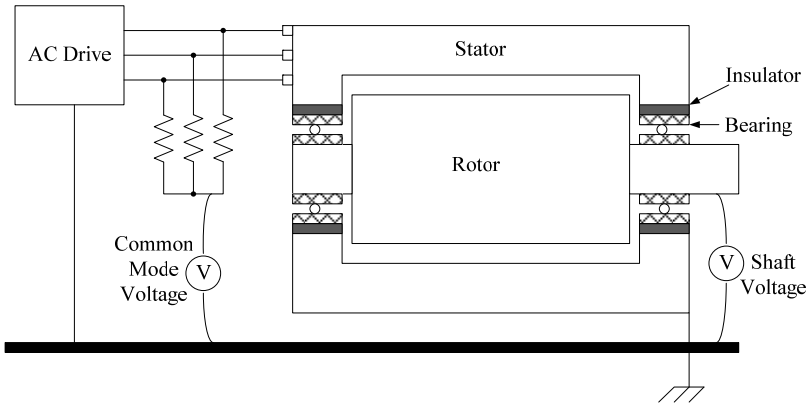
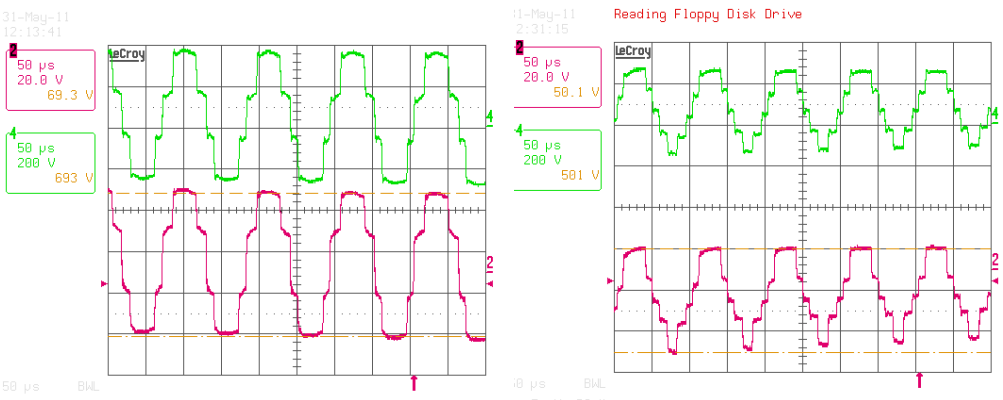


Figure 6-3 Experimental setup block diagram for common mode and shaft voltage measurement.

The common mode voltage and the shaft voltage measurements are shown in Figure 6-4. It can be seen from Figure 6-4 that the shaft voltage is proportional to the common mode voltage. The peak-peak common mode voltage for the two-level inverter is 693 V, which is equal to the DC-link voltage. The peak-peak common mode voltage for the three-level inverter is reduced to 500 V for the modulation technique used. The common mode voltage waveforms are having different voltage levels. Each voltage level corresponds to a common mode voltage level given in Table 6-1 and Table 6-2 for the two-level and three-level inverter, respectively. It can be seen from Figure 6-4 that the change in the common mode voltage level is lesser in case of the three-level inverter than that of the two-level inverter during each switching. This helps in reducing the parasitic bearing current. The number of transitions between the switching states in a switching period for the two-level inverter is six, while the number of transitions between the switching states in a switching period for the three-level inverter is eight. The increased number of switching is required for zero average neutral-point current of the three-level inverter as discussed in the previous chapter.



(a) (b)

Figure 6-4 Common mode voltage and shaft voltage for small DC-link capacitor based (a) two-level inverter. (b) three-level inverter.

6.2 Electromagnetic Interference (EMI) Measurements

High frequency switching action of the inverters creates high frequency noise in the drives, which can interfere with other systems. The inverter output current paths, which contribute to noise, are shown in Figure 6-5. The phase-phase parasitic capacitors give rise to differential mode current caused by high switching of the inverters. However, this current circulates inside the inverter and does not create problem for other equipments. On the other hand, the phase to chassis parasitic capacitors provides path for the common mode current into ground due to high frequency common mode voltages. This current may create a problem for low voltage susceptible equipment such as communication links, sensors, computer systems etc. [35]

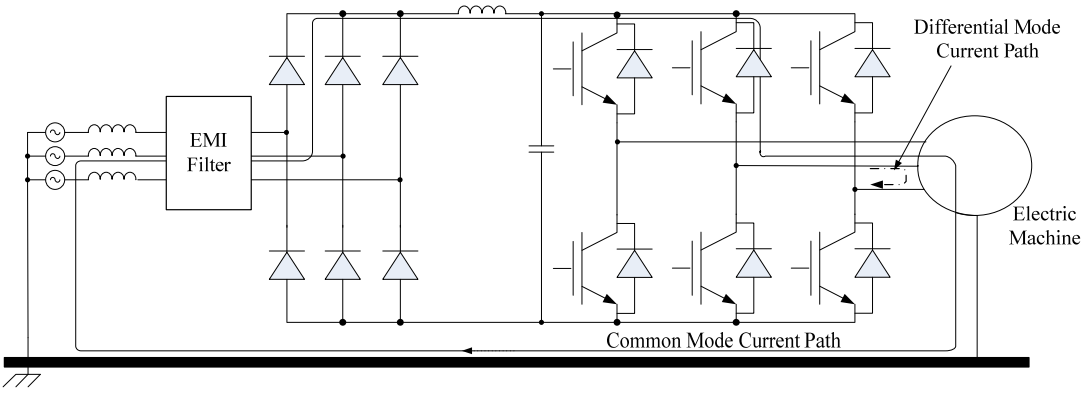


Figure 6-5 Common mode and differential mode current path for the inverter.

Different EMI standards are developed, which limit the allowable common mode current to be emitted by the drives. The test procedure to measure the common mode

current is also specified in the standards. The standard specifies line impedance stabilization networks (LISN) at the input to the EMI filter. For a three-phase system, they measure the common mode noise voltage at the MAIN supply since the common mode noise is greater than the differential mode noise.

EMI filters are required to limit the common mode and differential mode current. A schematic for a two stage EMI filter is shown in Figure 6-6. This filter is used in small DC-link capacitor based two-level and three-level inverter. The conducted emission tests are performed according to EN 61800-3 standard [31]. The software used for the conducted emission measurement is EMC32 from Rohde & Schwarz [96]. LISN network is PMM L3-100, which can be used for the frequency range from 9 kHz to 30 MHz [95]. The two-level inverter based drive used for the measurement is a product from Grundfos [89]. The two-level inverter has 14 μF DC-link capacitor. The EMI performance of the two-level inverter is compared with the EMI performance of the three-level inverter, which is described in the previous chapter, with 7 μF equivalent DC-link capacitor. The results for the two-level and the three-level inverter are shown in Figure 6-7 and Figure 6-8, respectively. It can be seen from Figure 6-7 and Figure 6-8, that conducted emission for both drives are low enough for Category C1 of EN 61800-3. However, the noise generated by the three-level inverter is lesser than that of the two-level inverter for low frequencies upto 500 kHz. This implies that the EMI filter can be reduced in size for the three-level inverter to achieve the same performance of the two-level inverter since the low frequency conducted emission is dependent on the EMI filter. The high frequency conducted emissions from the inverter are mainly decided the layout and the mechanical arrangement of the drive. The parasitic inductors and capacitors are small in value, and they may have resonance at high frequency. It can be seen from Figure 6-7 and Figure 6-8 that the conducted emission from the three-level inverter is high at 20 MHz range. This is due to the mechanical arrangement of the system and independent of EMI filter size. Recommendation for layout of the EMI filter, the mechanical arrangement of the drive system, and ground connections are discussed in [35].

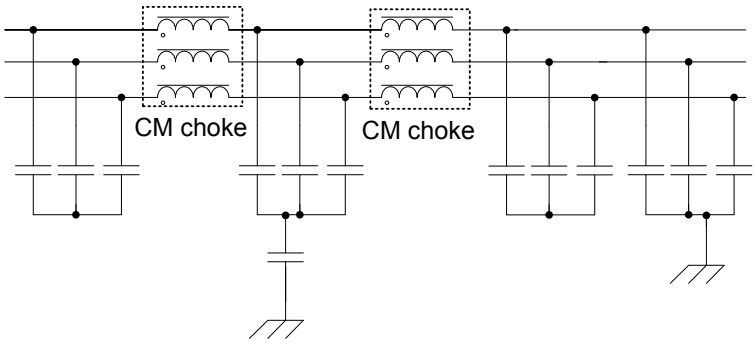


Figure 6-6 Two stage EMI filter.

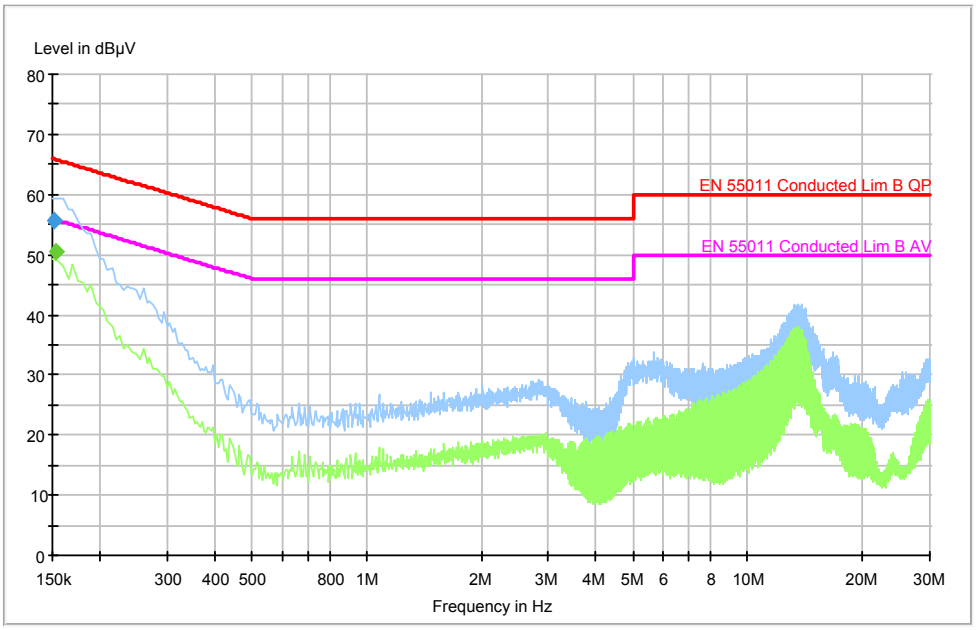


Figure 6-7 Conducted emission measurements for the two-level inverter acc. to EN 61800-3.

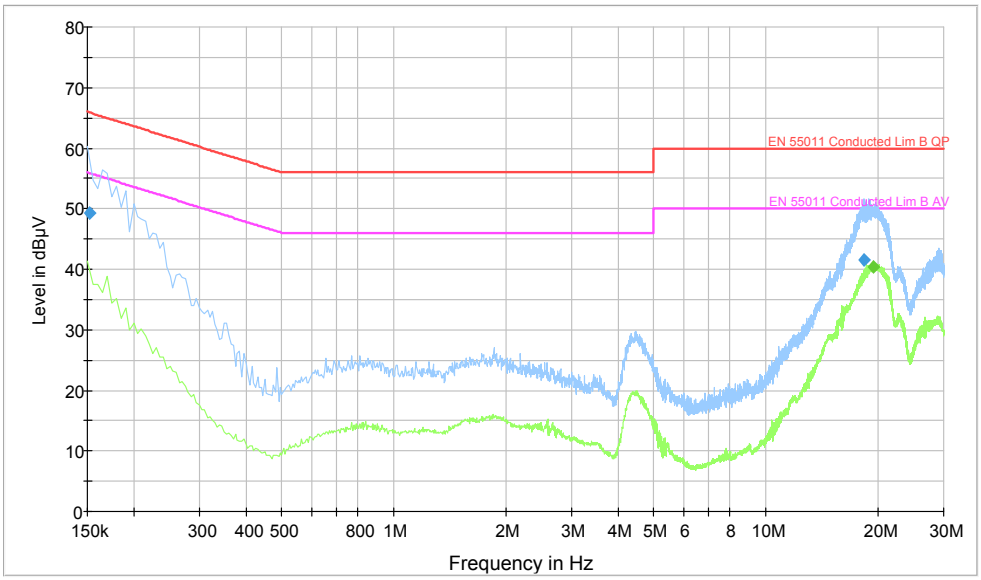


Figure 6-8 Conducted emission measurements for the three-level inverter acc. to EN 61800-3.

6.3 Efficiency Measurements

The small DC-link capacitor based drive efficiency is measured using Norma D6100 power analyzer. Power are measured at the input to the inverter (P_g), the

output of the inverter (P_{inv}), and the mechanical output of the machine (P_{mech}) as shown in Figure 6-9.

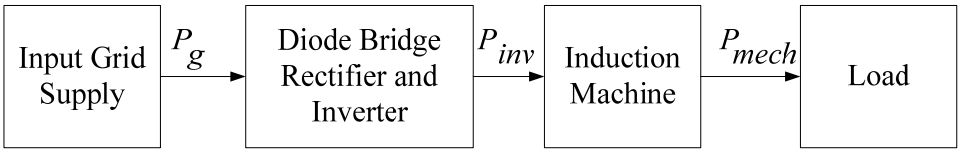


Figure 6-9 Block diagram of the drive for efficiency measurement.

The small DC-link capacitor based two-level inverter can be operated with discontinuous PWM to reduce losses. The two-level inverter used for efficiency measurement is operated with continuous PWM upto speed of 1500 rpm for low power and with 120° discontinuous PWM at higher speed for high power operation. On the other hand, the three-level inverter uses the PWM strategy, where the phase with the middle voltage value switches four times instead of two as discussed in the previous chapter. The three-level inverter is operated with 8 kHz and 10 kHz switching frequency, and the two-level inverter is operated with 9 kHz switching frequency. Power are measured from 1 kW to 7.5 kW mechanical output power with the increment of 500 W. The rectifier-inverter system efficiency is shown in Figure 6-10, and it is calculated as

$$\eta_{inv} = \frac{P_{inv}}{P_g} \tag{4.33}$$

It can be seen from Figure 6-10 that the three-level inverter efficiency is better than that of the two-level inverter. The three-level inverter efficiency is 97.4% and 97.3% for 8 kHz and 10 kHz, respectively at full power as compared to 97.15%, which is obtained by the two-level inverter. This corresponds to total loss reduction from 256 W (two-level inverter) to 233 W (Three-level inverter). Since the size of the heat sink of the inverter is decided by the loss, it can be said that the size of heat sink can be reduced by 9% or the requirement of the air flow can be reduced, which in turn can reduce noise from the fan.

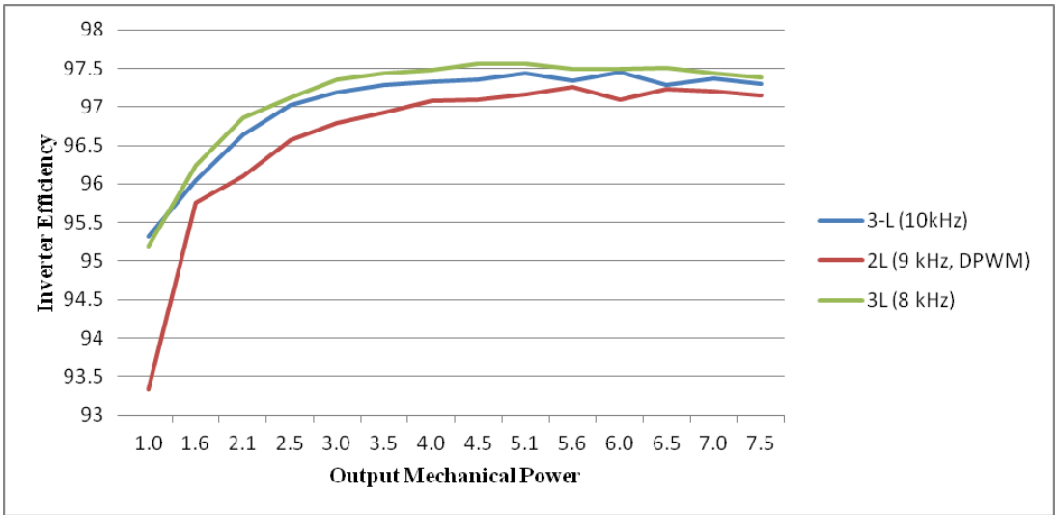


Figure 6-10 Rectifier-inverter system efficiency.

The efficiency of the three-level inverter can be increased with proper design of gate drive circuit in the present experimental setup. The gate driver used in the three-level inverter is HCPL-316J [85]. The gate driver High Level Output Voltage, which is equal to gate-emitter voltage applied to IGBT, is the gate driver supply voltage minus 1.2 V for 650 μA. There are 10 kΩ resistors across each gate and emitter pins of the IGBTs, and they draw current of approx. 1.5 mA from the gate driver (The gate driver supply voltage is 15 V). This causes the gate-emitter voltage of the IGBT to decrease by approx. 1 V, which in turn increases the conduction voltage drop of the IGBT. It can be seen from the typical output characteristics (Fig. 1) of the IGBT datasheet [98] that the conduction voltage of the IGBT decreases with the increase in the gate-emitter voltage. If the gate drive circuit is modified in such a way that the gate-emitter voltage will be 15 V when the IGBT is turned on, the losses in the three-level inverter can be reduced further.

The three-level inverter produces lower harmonic current components due to the switching of the inverter; the overall drive system efficiency is a better indicator that can show the advantage of the three-level inverter. The overall system efficiency is defined as

$$\eta_{sys} = \frac{P_{mech}}{P_g} \tag{4.34}$$

The output mechanical power is measured as a product of torque and speed. The system efficiency of the three-level inverter based drive is 84.3% and 83.9% for 8 kHz and 10 kHz, respectively at full power as compared to efficiency of 83.5% which is obtained by the two-level inverter based drive system.

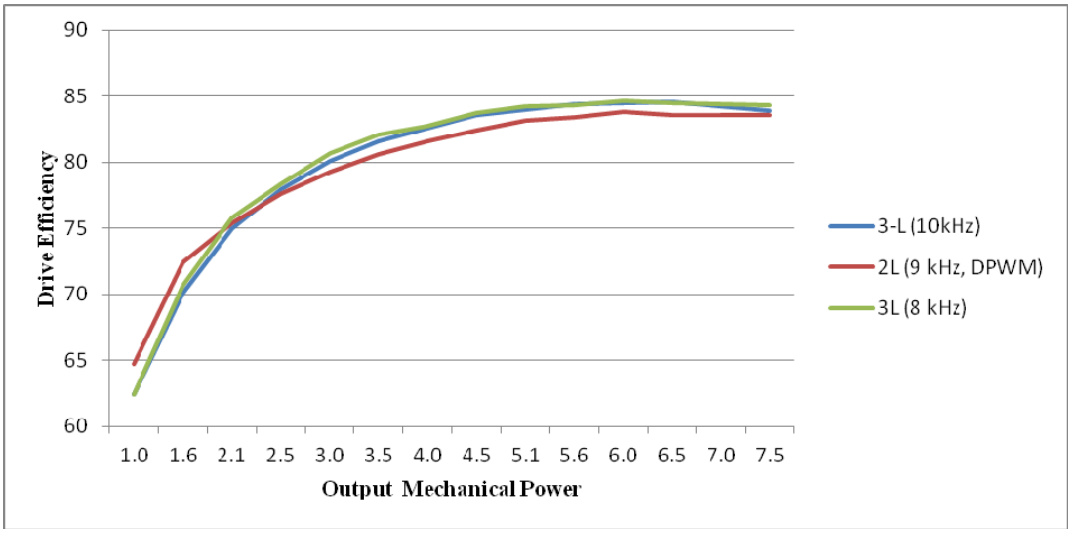


Figure 6-11 Drive efficiency.

6.4 Summary and Conclusion

The small DC-link capacitor based two-level and three-level inverter are compared in this chapter. The common mode voltage, conducted emission, and

efficiency are compared since the EMI filter and heat sink, which contribute to passive components, are decided by them. It has been shown in this chapter that the three-level inverter with small DC-link capacitor have lesser conducted emission and higher efficiency as compared to the two-level inverter. The converter losses are reduced by 9%, which corresponds to 9% reduction in the size of heat sink. The common mode voltage is decreased from $\pm v_{dc}/2$ to $\pm v_{dc}/3$, which helps in reducing the size of conducted EMI filter. This has been verified by conducted emission tests, which show that the conducted emission by the three-level inverter is 40 dBμV @150 kHz as compared to 50 dBμV@150 kHz in case of the two-level inverter with same EMI filter.

Chapter 7

Conclusion and Future Work

The adjustable speed drives has found its application in traction, utility, aerospace, and military industries. The main portion of size, weight, and volume of the ASDs are because of the passive components. Among passive components, capacitors are the major contributors to the size, weight, and volume of the ASD. This thesis focuses on the reduction of the size of the passive components for low voltage drives. The power range of the ASD is 1-10 kW. The most popular topology for this power application is a six-pulse diode bridge rectifier followed by a two-level inverter.

The two-level inverter with small DC-link capacitor was discussed in literature. However, it may cause an unstable operating point at high power. It was shown in this thesis that the overall drive system, which is nonlinear, is stable even though the operating point is unstable. Generally, nonlinear system exhibit limit cycles at unstable operating points and in this case, it was shown that the input LC filter exhibit limit cycle which causes high input line current THD and amplifies the harmonics component of the DC-link voltage.

An active damping technique is also proposed to improve the stability of the drive system in this thesis. The active damping terms add harmonic components of the DC-link voltage to the machine stator voltages. This causes the harmonics components of the machine current, which in turn cause the harmonic components in the current drawn by the inverter and stabilize the DC-link voltage. A first-order analysis, which describes the effect of the active damping terms on the machine current, the current drawn by the inverter, and the DC-link voltage, is presented in steady state. Using this analysis, it has been shown that the active damping term should be added to the in-phase component of the fundamental stator voltage for least harmonic distortion in the machine current.

The effect of active damping term for vector controlled drive is also discussed. It has been shown that the active damping terms, which are added to the machine stator voltage, can be added to the stator current reference command. This requires modification in the gain of the active damping terms, and it depends on the PI controller parameters.

In addition to reducing the DC-link capacitor for the voltage fed inverter, the passive components can be reduced further by using a three-level inverter. The three-level inverter has advantage of reduced switching losses, low conducted

emissions, and low harmonic distortion at the output voltage. However, the three-level inverter with small DC-link capacitors requires fast, robust, and stable controller for the neutral-point voltage. A new, simple modulation strategy, which adds scaled common mode offset to the machine voltage references, is presented in this thesis. With this modulation strategy, the dynamics of the neutral-point voltage is modeled as a first-order continuous equation. Based on this model, a PI controller is designed for controlling the neutral-point voltage of the three-level inverter. A fast and stable response is achieved for an induction machine based drive, and it is verified by the experimental results.

The NPC three-level inverter requires higher number of switching transition in a switching period with this modulation strategy. This increases the switching losses in the inverter. However, it has been shown that the efficiency of the inverter is higher than that of the two-level inverter. The overall efficiency of the system is also increased due to low output voltage harmonic distortion. The common mode voltage and the shaft voltage are also reduced in the three-level inverter as compared to the two-level inverter. The conducted emissions from the three-level inverter and the two-level inverter are measured. The same EMI filter is used for both measurements, and it is shown that the performance of the three-level inverter is better. With reduced losses (reduced heat sink) and conducted emission (reduced EMI filter), the three-level inverter with small DC-link capacitors can have reduced passive components.

Some ideas for future work related to the thesis are given below:

1. The active damping terms added to the stator voltage affect the machine current. A simple analysis using only first-order approximation was presented. An exact analysis considering the effect of second-order terms and PWM can be derived to calculate the torque and flux ripple in the machine caused by the active damping terms.
2. Active damping technique for the three-level inverter can be investigated.
3. The modulation strategy with scaled common mode offset proposed for the NPC three-level inverter can be extended to an n-level inverter.
4. The performance of the neutral-point voltage controller during the unbalanced input grid supply voltage needs to be verified.
5. The controller developed for the neutral-point voltage has poor performance at low power because it is based on the active power drawn by the inverter. A controller based on the reactive power can solve this problem, and it requires further investigations.
6. The small DC-link drive has oscillating DC-link voltage which may cause operation of the drive in overmodulation region. The operation of the three-level inverter with small DC-link capacitors in overmodulation region can be an interesting topic for further research.

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Appendix A

Space Phasor

Space phasor is defined for a three-phase system. In a three-phase system, the three quantities related to three-phases can be expressed as a phasor quantity, which can be defined as

$$\underline{\boldsymbol{f}} = \frac{2}{3}\left[f_a + e^{j(2\pi/3)} f_b + e^{j(4\pi/3)} f_c \right] \tag{A.1}$$

where f denotes a variable which should be represented in space phasor. Subscripts a, b, and c represent three phase quantity.

The space phasor transformation is used for the modeling of general AC machine. If α and β denote the real and imaginary axis of the reference frame of space phasor, (A.1) can be expressed as

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.2}$$

and the inverse transformation can be given as

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{A.3}$$

Stationary to Rotating Reference Frame Transformation

The space phasor represents the variables in a stationary reference frame with α and β axes. The change of variables from stationary reference frame to rotating reference frame was introduced in [A1] for synchronous machines. This transformation can be used for induction machine also. The induction machine represented in synchronously rotating reference frame has an advantage of easy control. The transformation used in this thesis for stationary (α-β) to arbitrary rotating reference frame (d-q), described in Figure A1, is given by

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} \cos\mu & \sin\mu \\ -\sin\mu & \cos\mu \end{bmatrix}\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{A.3}$$

and the inverse transformation is given by

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \begin{bmatrix} \cos\mu & -\sin\mu \\ \sin\mu & \cos\mu \end{bmatrix}\begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{A.4}$$

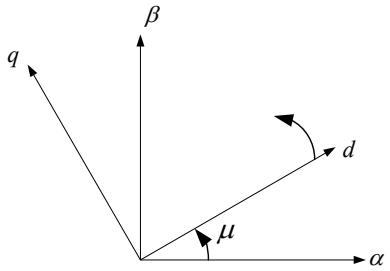

Figure A1 Stationary to rotating reference frame transformation

[A1] Park, R. H.; , "Two-reaction theory of synchronous machines generalized method of analysis-part I," *American Institute of Electrical Engineers, Transactions of the* , vol.48, no.3, pp.716-727, July 1929.

Appendix B

The following are the particulars of squirrel cage induction machine used in chapter 2. It is a 4kW, 415V, and star-connected machine.

Nominal Parameters	Value (SI Units)
Stator Resistance (r_s)	1.6 Ω
Rotor Resistance (r_r)	0.9 Ω
Stator Inductance (L_s)	0.205 H
Rotor Inductance (L_r)	0.205 H
Magnetizing Inductance (L_o)	0.199 H
Moment of Inertia (J)	0.02 Kg-m^2
Number of Poles (P)	4