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A Compact P$^+$ Contact Resistance Model for Characterization of Substrate Noise Coupling in Modern Lightly Doped CMOS Processes

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***Abstract*—Compact modeling of P$^+$ contact resistances is important for characterization of substrate noise coupling in mixed-signal System on Chips (SoCs). Existing contact resistance models can handle uniformly doped bulk or epitaxial substrates. However, compact contact resistance models feasible for modern lightly-doped CMOS processes with P-well layers are still unavailable. This paper presents a new compact resistance model aiming at solving this problem. A Conformal Mapping(CM) method was used to derive the closed-form expressions for the resistances in the model. The model requires no fitting factors, and it is scalable to layout/substrate parameters. The proposed model can also be used to predict noise coupling in terms of S-parameters. The model validation has been done by both EM simulations and measurements, and satisfactory agreement is found between the modeled and measured resistances as well as S-parameters.**

I. Introduction

The growing demand for powerful yet low cost electronic devices has resulted in an increasing need for mixed-signal System-on-Chips (SoCs). SoCs require mixed integration of both digital circuits and analog/RF circuits on the same chip. However, the analog circuits in mixed-signal SoCs often suffer from substrate noise interference generated by the digital circuits [1]. Substrate noise coupling through P$^+$ contacts is one of the three most significant noise coupling mechanisms leading to the interference [2], [3]. Fig. 1 illustrates the coupling between P$^+$ contacts located in digital and analog circuits on a mixed-signal SoC. The switching noise generated by the digital circuits is coupled through the P$^+$ contact (Aggressor) into the P-well and substrate. This noise propagates to reach analog circuits sharing the same substrate, here represented as a P$^+$ contact (Victim), and deteriorate the circuit performance. Compared to other coupling mechanisms, including the source/drain-bulk junction capacitive coupling and impact ionization caused by hot electron effects, the coupling effect of P$^+$ contacts is much more significant for current CMOS processes and is expected to remain so for future technologies [3], [4]. Various modeling approaches have been proposed and they can be categorized into two groups: electromagnetic methods and compact models [1], [3], [5]–[8]. Compact models can provide the insights into the dependence of the coupling on the layout/substrate parameters. Owing to its scalable feature compact models are efficient for large scale SoCs and consequently has attracted significant research attention [1], [3], [8].

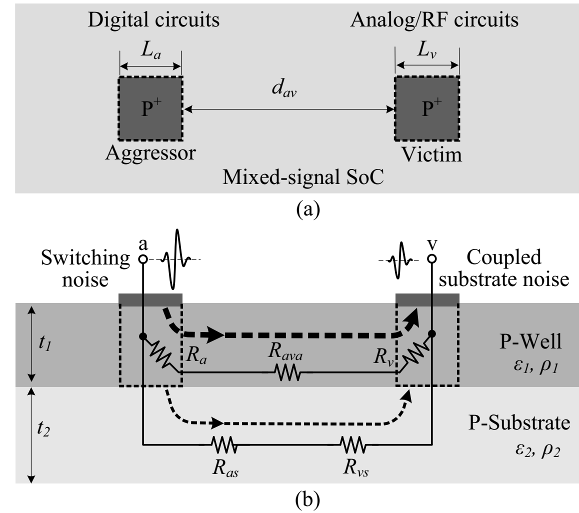

Fig. 1. (a) Top-view and (b) cross section view of two P$^+$ contacts implemented using a modern lightly doped CMOS process with a P-well layer. The proposed circuit model for the structure is also shown.

Compact contact resistance models for substrate noise characterization were proposed as early as 1993 [1]. However the early models are only feasible for epitaxial substrates. Another model, proposed in 2006, is able to handle both epitaxial and uniform bulk substrates [3]. However, it requires three fitting factors that need to be extracted from measurements. Thus the noise analysis has to be postponed to the post-layout design stage, resulting in longer design cycle and higher costs. One of the latest compact contact resistance models was proposed in 2007 [8]. It needs no fitting factors and can be used for both uniform bulk and epitaxial substrates. However, it is still infeasible for modern standard lightly doped CMOS processes that are increasingly used for mixed-signal SoCs. Unlike uniform bulk or epitaxial substrates, lightly doped substrates of standard CMOS processes have a thin P-well layer on the P-substrate (Fig. 1(b)). The P-well layer introduces a current constriction effect which has significant impact on the coupling between the P$^+$ contacts [9]. Existing compact contact resistance models do not include the parameters of the P-well (ρ_1, ϵ_1 and t_1), and therefore can not effectively characterize the coupling. To obtain accurate coupling predictions and help the SoC designers solve the

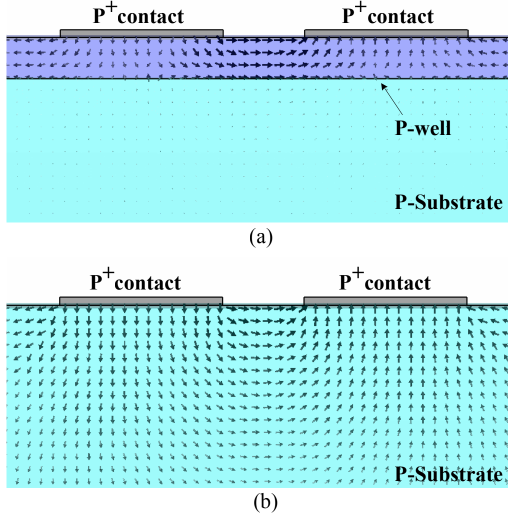

Fig. 2. The cross section view of the simulated currents between two P^+ contacts on (a) a typical lightly doped CMOS process with a P-well layer and (b) on a uniform bulk substrate. The parameters used for the simulation are: $L_a = 20\,\mu$m, $L_v = 20\,\mu$m, $d_{av} = 10\,\mu$m, $t_1 = 5\,\mu$m, $t_2 = 200\,\mu$m, $\rho_1 = 0.2\,\Omega{-}$cm and $\rho_2 = 20\,\Omega{-}$cm.

noise issues, new contact resistance models feasible for lightly doped substrates with a P-well layer are highly desired.

This paper proposes a two-port resistive network as shown in Fig. 1(b) to model the resistance between the contacts. The constriction effects introduced by the P-well layer are characterized using a Conformal Mapping approach. The model is based on the investigation of the physical geometry of the contact layout, taking into account all the layout and substrate parameters shown in Fig. 1(b). Thus it requires no fitting factors.

II. The Contact Resistance Model

The proposed circuit model is shown in Fig. 1(b). R_{ava}, R_{as} and R_{vs} represent the resistances between the dashed surfaces (Fig.1(b)). R_a and R_v model the current constriction effects for the aggressor and victim, respectively. The aggressor-victim contact resistance between port a and v, R_{av}, is divided into two parallel parts (Fig. 1(b)): the resistances in the P-well layer (R_a, R_v and R_{ava}) and the resistances in the P-substrate (R_{as}, R_{vs}). That is $R_{av} = (R_a + R_{ava} + R_v)||(R_{as} + R_{vs})$. This is based on the fact that the resistivity of the P-well is usually one or two orders of magnitude lower than that of the P-substrate. Thus the majority of the noise current flows horizontally from the aggressor to the victim in the P-well, while a small part of the current is coupled to the P-substrate at the area beneath the contacts. Fig. 2 illustrates the simulated current flows between two P^+ contacts on a typical lightly doped CMOS process with a P-well layer and on a uniform bulk substrate, respectively. It can be seen that the currents in the case with P-well are remarkably constricted in the P-well layer, while the currents in the case without P-well are spreading in a much larger region in the P-substrate [10].

To simplify the analysis, his paper approximates the layout of the square contacts in Fig. 1 using circular contacts. The approximation is based on the condition that the circular contacts have the same area as the corresponding square contacts. That is $r_a = L_a/\sqrt{\pi}$ and $r_v = L_v/\sqrt{\pi}$, where r_a and r_v are the radii of the circular contacts approximating the square aggressor and victim contact (with side length L_a and L_v), respectively. The same approximation has been widely used in previous work, and it has been proven that the approximation error is acceptable for practical use [8].

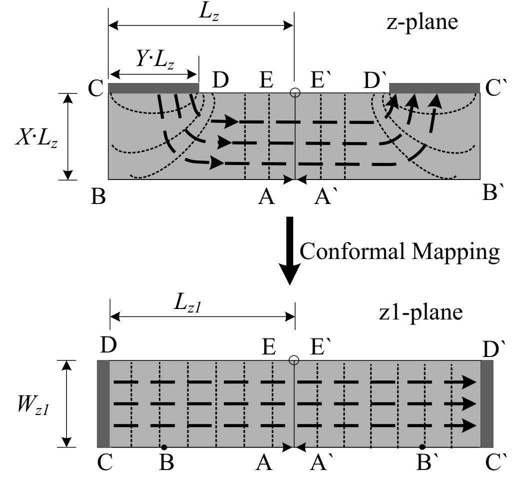

Fig. 3. Conformal mapping for the calculation of the constriction resistance of a contact on a thin film.

A. Calculating R_{ava}, R_a and R_v

Based on the contact approximation, the dashed blocks in the P-well are approximated as two cylinders with radii of r_a and r_v, respectively. As the relationship $R = \rho_1\epsilon_1/C$ stands for homogeneous mediums, the resistance between the lateral surfaces of the cylinders (R_{ava}) can be easily derived from the capacitance between the surfaces [11]

$$R_{ava} = \frac{\rho_1}{2\pi t_1}\text{acosh}\left[\frac{1}{2}\left(\frac{D^2}{r_a r_v} - \frac{r_a}{r_v} - \frac{r_v}{r_a}\right)\right], \qquad (1)$$

where $D = d_{av} + r_a + r_v$. ρ_1 and t_1 are the resistivity and thickness of the P-well, respectively. It should be noted that R_{ava} in (1) does not include the constriction resistances (R_a and R_v) in the areas close to the contacts. In this paper, this error is corrected by equivalently extending the real distance (d_{av}) with an equivalent distance L_e for each of the contacts. This is achieved using a Conformal Mapping approach.

The top figure in Fig. 3 shows the cross section view of two identical co-planar contacts (C-D and C′-D′) on a conductive layer. L_z represents half of the distance between the contacts plus the side length of the contacts. X and Y represent the ratio of the contact width and the thickness of the conductive layer. Simple expressions for the current flow lines (long dashed lines with arrows) and the equipotential surfaces (short dashed lines) at the constriction areas are usually unavailable in the original plane z [12], [13]. Hence the resistance between the two contacts can not be easily

derived. However, using Conformal Mapping, the contacts in the z-plane can be mapped to a new plane z1 (bottom figure in Fig. 3) with new distance L_{z1} and contact width W_{z1}, where the structure is simple and the resistance can be easily derived. Since the mapping is conformal, the current flows and equipotential surfaces are kept perpendicular to each other. This guarantees that the resistance value between the contacts in the z1-plane is the same as that in the z-plane. Therefore the equivalent distance for constriction resistance correction of the contact C-D can be easily found as

$$L_e = XL_zL_{z1}/W_{z1} - (1-Y)L_z. \quad (2)$$

In the case of $X << 1$, and $Y < 0.5$, L_e can be approximated as [12], [13]

$$L_e \approx \frac{Y}{X} - \frac{2}{\pi}\ln\left[\sinh(\frac{Y\pi}{2X})\right], \quad (3)$$

and for the case of $X << 1$, and $Y > 0.5$, L_e can be approximated as [13]

$$L_e \approx K(p)/K'(p) - (1-Y)/X, \quad (4)$$

where K is the complete elliptic integral of first kind and $p = \tanh[\pi(1-Y)/2X]$. In addition, $K'(k) = K(\sqrt{1-k^2})$.

Using (1) and (3) or (4) the resistance between the contacts in the P-well ($R_{avw} = R_a + R_v + R_{ava}$) in Fig. 1(b) can be found by

$$R_{avw} \approx \frac{\rho_1}{2\pi t_1}\text{acosh}\left[\frac{1}{2}\left(\frac{D_1^2}{r_a r_v} - \frac{r_a}{r_v} - \frac{r_v}{r_a}\right)\right], \quad (5)$$

where $D_1 = d_{av} + L_{ea} + L_{ev} + r_a + r_v$ is the extended distance between the contacts. L_{ea} and L_{ev} are the equivalent distances to correct the constriction resistances (R_a and R_v) for the aggressor and victim, respectively.

B. Calculating R_{as} and R_{vs}

A typical P-substrate is usually two or three orders thicker than the P-well . Thus the current in the P-substrate spreads over a much larger region than the thin P-well (Fig. 2(a)). This leads to different calculations of R_{as} and R_{vs} compared to the case of R_{ava}. A simple expression of the contact spreading resistance on a uniform bulk substrate has been reported in [8]. It is used here to calculate the contact spreading resistances in the P-substrate:

$$R_{as} \approx \frac{\rho_2}{4r_a}\left[1 - \frac{2}{\pi}\text{asin}\left(\frac{r_a}{r_a + d_{av}}\right)\right]. \quad (6)$$

Similarly, R_{vs} is formed using the same expression as (6) for R_{as} with r_a replaced by r_v.

III. Model Validation

A. EM simulation validations

The proposed model has been validated firstly by EM simulations using CST STUDIO SUITE^{TM}. The geometry in Fig. 1 is used for the simulations and the modeled and simulated results for substrates with five different P-well resistivities (ranging from $0.01\,\Omega$−cm to $0.2\,\Omega$−cm) are shown in Fig. 4.

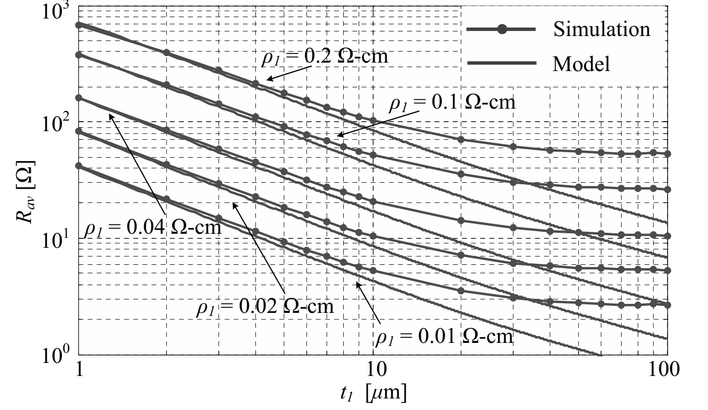

Fig. 4. Modeled and EM-simulated contact resistance versus thickness of the P-well. The parameters used for the simulation are: $L_a = 20\,\mu$m, $L_v = 40\,\mu$m, $d_{av} = 20\,\mu$m, $t_2 = 200\,\mu$m and $\rho_2 = 20\,\Omega$−cm.

TABLE I
Process parameters

	t [μm]	ϵ/ϵ_0	ρ [Ω-cm]
P-Well	1.2	12	0.11
P-Substrate	300	12	20

It can be seen that the modeled resistances match the simulated results very well especially for small thicknesses. The relative error is $< 5\%$ when the thickness is less than $5\,\mu$m, which is the case for most currently available lightly doped CMOS processes [9]. For relatively thicker P-wells, deviations between the modeled and simulated results are observed. This is because the approximation of horizontal current flow in the P-well layer is less accurate for thick P-well layers. The results shown in the figure also indicate that this model can be used for a wide range of substrates with different resistivities.

B. Experimental validations

Two test chips fabricated using a standard 0.18 μm CMOS process were used to validate the proposed model. The process parameters are given in Table I. The microphotographs of the test chips for verification of contact resistances and noise coupling in terms of S-parameters are shown in the embedded figures in Fig. 6 and Fig. 7, respectively. Pads on top metal layer are used for on-wafer resistance and S-parameter measurements. An example of the 3-D layout of the test fixture (cross section view) is shown in Fig. 5. The aggressor and victim contacts are connected to the pads on the top metal layer (metal-6) using vias. As the resistivities of the vias and metal pads are remarkably lower than those of the P-well and P-substrate, their resistances are neglected in the measurements.

The measured and calculated contact resistances versus distance of P^+ contact pairs with three different side lengths are shown in Fig. 6. It can be seen that the agreement between the modeled and the measured results is fairly good. The relative estimation error is less than 6.5% for all the results. Fig. 7 shows the measured and calculated $|S_{21}|$ between contact pairs with four different distances. As shown in the embedded figure

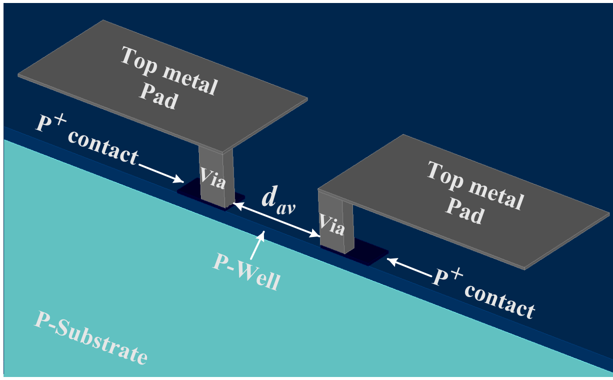

Fig. 5. The cross section view of an example layout showing the connection of the P^+ contacts to the measurement pads.

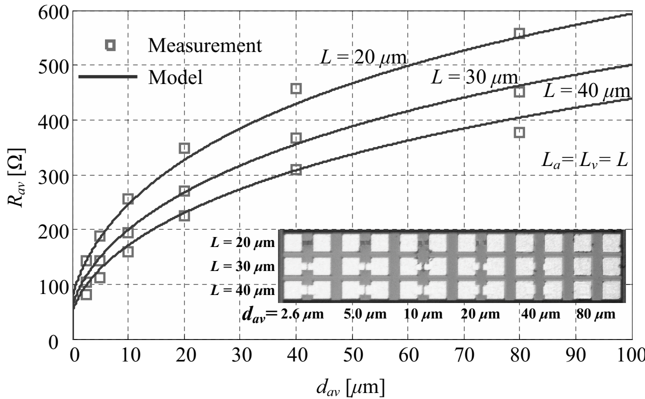

Fig. 6. Measured and modeled resistances versus distance of P$^+$contacts with different side lengths. The embedded figure is the microphotograph of the test chip. The parameters of the CMOS process are: $t_1 = 1.2\ \mu m$, $t_2 = 300\ \mu m$, $\rho_1 = 0.11\ \Omega{-}$cm and $\rho_2 = 20\ \Omega{-}$cm.

in Fig. 7, G-S-G pads are used for S-parameter measurements. The connection of the contacts to the top metal signal pads is the same as shown in Fig. 5. The ground pads only consist of metal-6 and are connected using two 10-μm wide metal-6 strip lines. Fig. 7 shows that the calculated results have quite good agreement with the measured results. The predict error of the coupling is within 5 dB for the results except for the case of $d_{av} = 525\ \mu$m from 3 to 10 GHz. It should be noted that the coupling for this case is very weak (-50 dB), and the relatively big error might be due to the lower measurement accuracy for weak coupling signals.

IV. Conclusion

A compact resistance model for P$^+$ contacts is proposed in this paper. The model can handle lightly doped substrates with a thin P-well layer, which are common in modern deep sub-micron CMOS processes for the implementations of mixed-signal SoCs. The model is scalable to layout/substrate parameters, while requiring no fitting factors. Test chips fabricated using a standard 0.18 μm CMOS process have been used for experimental verifications. Measured results show that the modeled contact resistances are accurate with estimation errors less than 6.5%. It has also been demonstrated that the noise

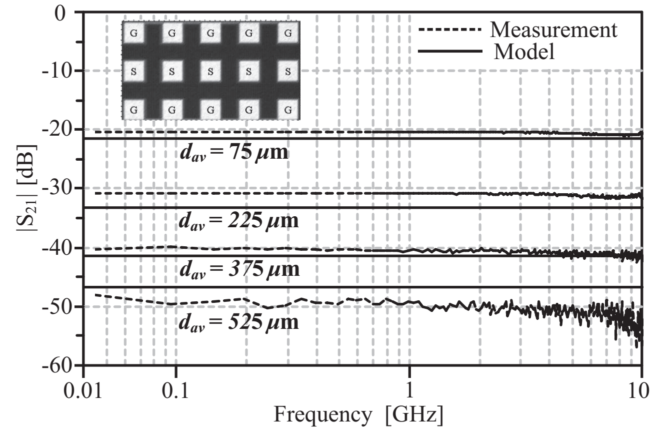

Fig. 7. Measured and modeled $|S_{21}|$s of P$^+$contact pairs with different distances. The side lengths for the aggressor and victim are both 75 μm The embedded figure shows the layout of the test chip.

coupling of contacts in mixed-signal SoCs can be accurately predicted using this model. This can be useful to solve the substrate noise issues in the early SoC design stage and reduce the design cost.

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