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Mitigation of Voltage and Current Harmonics in Grid-Connected Microgrids

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***Abstract*— In this paper, a control approach is proposed for selective compensation of main voltage and current harmonics in grid-connected microgrids. Two modes of compensation are considered, i.e. voltage and current compensation modes. In the case that sensitive loads are connected to the point of common coupling (PCC), voltage compensation mode is activated in order to provide a high voltage quality at PCC. Otherwise, grid current harmonics are mitigated (current compensation mode) in order to avoid excessive harmonic supply by the grid. In both modes, harmonic compensation is achieved through proper control of distributed generators (DGs) interface converters. The compensation effort of each harmonic is shared considering the corresponding current harmonic supplied by the DGs. The control system of each DG comprises harmonic compensator, power controllers, voltage and current controllers and virtual impedance loop. Virtual impedance is considered at fundamental frequency to enhance power control and also at harmonic frequencies to improve the nonlinear load sharing among DGs. Simulation results are presented to demonstrate the effectiveness of the proposed method.**

I. Introduction

DISTRIBUTED generators (DGs) often consist of a prime mover connected through a power-electronic interface converter to the utility grid or microgrid. Microgrid is a local grid consisting of DGs, energy storage systems and dispersed loads and is able to operate in both grid-connected and islanded modes [1]. The main role of an interface converter is to control power injection. However, compensation of power quality problems, such as voltage harmonics can be achieved through proper control strategies.

In [2]-[5], some methods are presented to control the DG unit as voltage harmonic compensator. Compensation approaches of [2]-[4] are based on making the individual DG units emulate a resistance at harmonic frequencies. The method of [5] has been proposed for compensation of voltage harmonics in an islanded microgrid. This method is also based on the resistance emulation. Furthermore, a droop characteristic based on the DG harmonic reactive power has been considered to achieve sharing of harmonic compensation effort.

The aforementioned harmonic compensation methods are designed for compensation of voltage harmonics at the DG terminal while usually the power quality at the sensitive load bus is the main concern. Furthermore, if the DGs try to compensate the local voltage harmonics, the harmonic distortion may be amplified in some of the other buses including the sensitive load bus. This phenomenon is called "whack-a-mole" [6]. Thus, a hierarchical control scheme is proposed in [7] in order to directly compensate the main harmonic orders of load bus voltage in islanded microgrids.

In the present paper, power quality of grid-connected microgrids in terms of voltage as well as current quality is addressed. Two control modes, i.e. voltage and current compensation modes are considered. In the case that sensitive loads are connected to the point of common coupling (PCC), voltage compensation mode can be activated in order to provide a high voltage quality at PCC. Otherwise, grid current harmonics are mitigated (current compensation mode) in order to avoid excessive harmonic supply by the grid.

II. Microgrid DGs Control System

Fig. 1 shows the single-line diagram of a grid-connected microgrid consisting of electronically-interfaced DGs and dispersed linear and nonlinear loads. Microgrid is connected to the utility grid through a tie line (Z_g) and a transformer with the equal impedance of Z_t.

As shown in Fig. 1, the harmonic orders of PCC voltage ($v_{PCC_{abc}}$) and grid current ($i_{g_{abc}}$) are extracted by the measurement blocks (v_{dq}^{h} and i_{dq}^{h} as the h[th] harmonic of voltage and current, respectively) and sent to all DGs. Compensation is performed selectively for the main harmonics of PCC voltage or grid current; thus, it is only necessary to extract and send the data corresponding to these harmonics (here, 5[th] and 7[th] orders).

Since PCC can be far from DGs, low bandwidth communication (LBC) is applied for sending harmonic data. In order to ensure that LBC is sufficient, the transmitted data should consist of approximately dc signals. Hence, the PCC voltage and grid current harmonic components are extracted in *dq* (synchronous) reference frame [7] and then transmitted to each DG controller. Afterwards, as shown in Fig. 2, harmonic voltages and currents are transformed to $\alpha\beta$ (stationary) reference frame [7] and fed to "Selective Harmonic Compensator" block.

The structure of each DG power stage and control system is shown in Fig. 2. A feedforward loop is included in order to consider small variations of dc link voltage (V_{dc}). The reference of the DG output voltage ($v_{\alpha\beta}^{*}$) is provided by power controllers, virtual impedance loop and harmonic compensator. On the other hand, instantaneous output voltage

($v_{o_{abc}}$) is measured and transformed to $\alpha\beta$ frame ($v_{o_{\alpha\beta}}$). Then, according to $v^*_{\alpha\beta}$ and $v_{o_{\alpha\beta}}$, the reference current ($i^*_{\alpha\beta}$) is generated. Furthermore, LC filter inductor current is transformed to $\alpha\beta$ frame ($i_{L_{\alpha\beta}}$) and controlled by the current controller to generate the reference voltage for the pulsewidth modulator (*PWM*). The main DG control blocks are explained in the following Subsections.

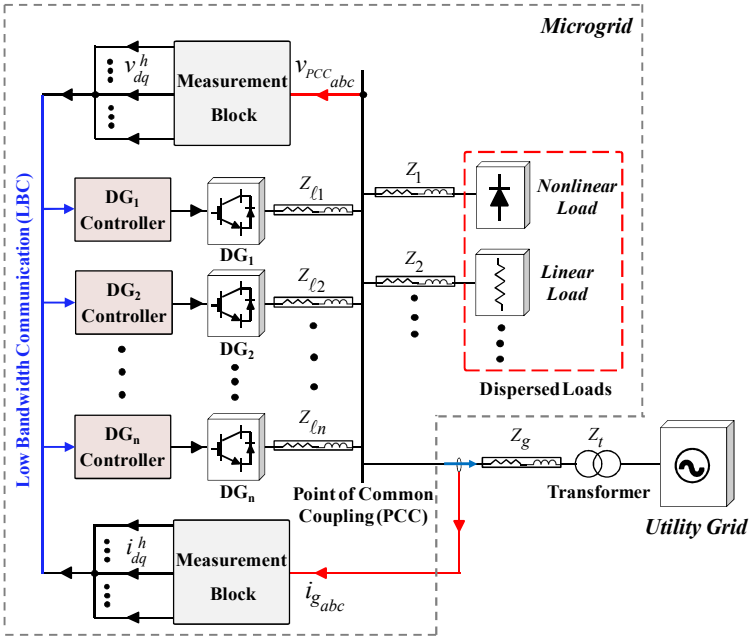

Fig. 1. Structure and control system of a grid- connected microgrid.

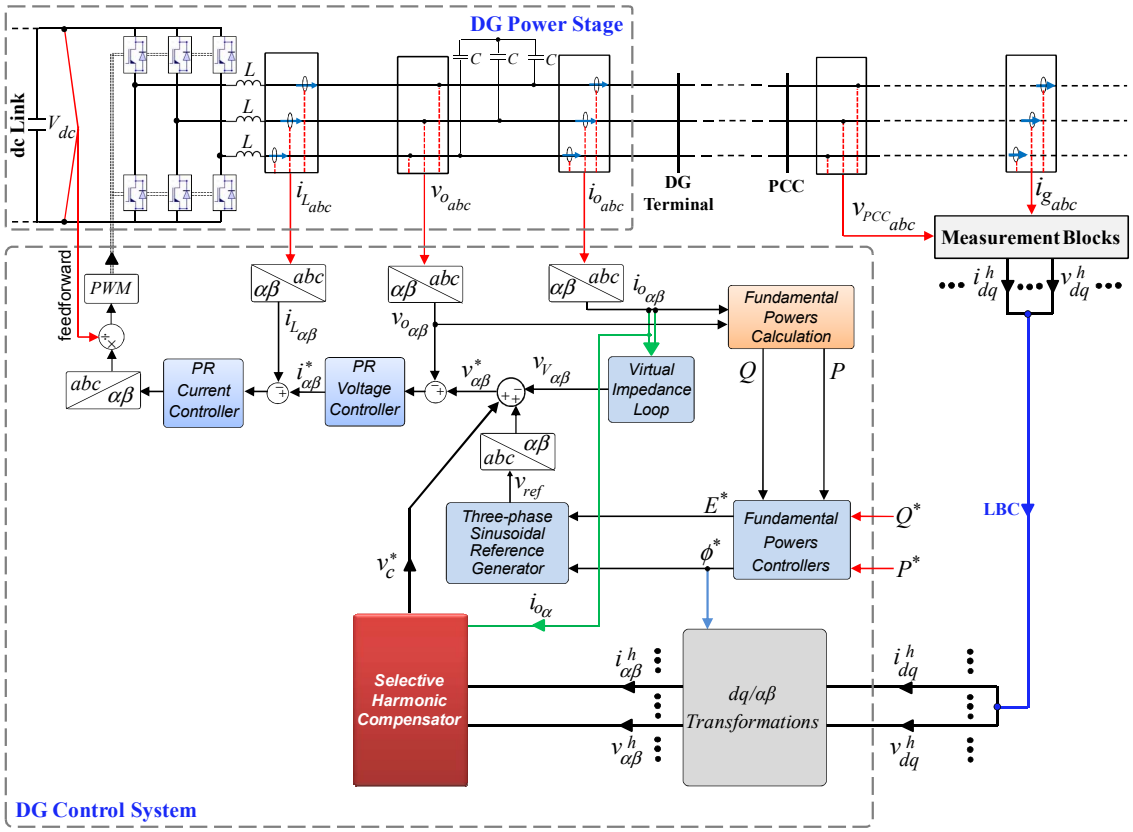

Fig. 2. DG power stage and control system.

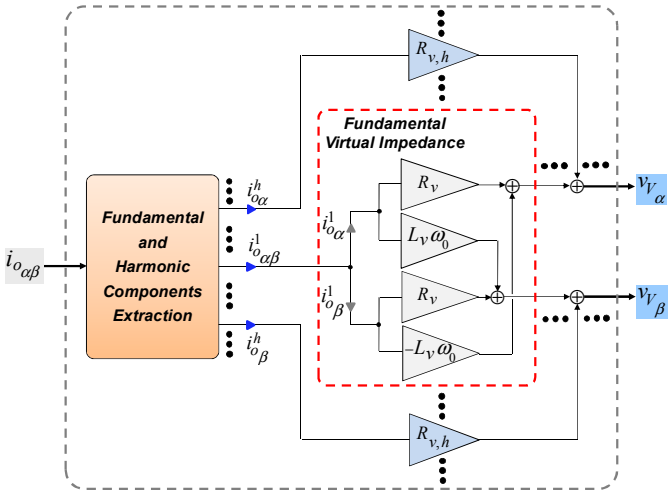

Fig. 3. Block diagram of selective virtual impedance.

A. Fundamental Powers Controllers

In a mainly inductive grid-connected microgrid, fundamental frequency active and reactive powers of each DG unit can be controlled by the following characteristics [8]:

$$\phi^* = \phi_0 + m_P(P^* - P) + m_I\int(P^* - P)\,dt \quad (1)$$

$$E^* = E_0 + n_P(Q^* - Q) + n_I\int(Q^* - Q)\,dt \quad (2)$$

where

- P: fundamental active power
- Q: fundamental reactive power
- P^*: fundamental active power reference
- Q^*: fundamental reactive power reference
- E^*: voltage amplitude reference
- ϕ^*: phase angle reference
- E_0: rated voltage amplitude
- ϕ_0: rated phase angle ($\int\omega_0 dt = \omega_0 \cdot t$)
- ω_0: rated frequency
- m_P: active power proportional coefficient
- m_I: active power integral coefficient
- n_P: reactive power proportional coefficient
- n_I: reactive power integral coefficient

Details of power calculation are presented in [7] and [8].

B. Voltage and Current Controllers

Proportional-resonant (PR) controllers are applied for voltage and current control. The resonant terms are tuned at fundamental and 5th and 7th harmonic frequencies [7].

C. Virtual Impedance Loop

Including virtual impedance at fundamental frequency enhances the performance and stability of power controllers. Furthermore, the virtual impedance can improve the sharing of nonlinear (harmonic) load among parallel converters [7]-[12].

The basic structure of virtual impedance for $\alpha\beta$ frame has been proposed in [10]. Here, this structure is extended as shown in Fig. 3 by adding the virtual resistances at harmonic frequencies. In this Fig., R_v and L_v are the fundamental frequency virtual resistance and inductance, respectively, and $R_{v,h}$ is the virtual resistance at h[th] harmonic (here, h=5,7 as the main harmonic orders). As seen in Figs. 2 and 3, $\alpha\beta$ components of instantaneous output current ($i_{o\,\alpha\beta}$) are fed to virtual impedance loop. Then, fundamental component ($i^1_{o\,\alpha\beta}$) and harmonic orders ($i^h_{o\,\alpha\beta}$ for h[th] harmonic) are extracted and applied to implement selective virtual impedance.

D. Selective Harmonic Compensator

The details of "Selective Harmonic Compensator" block of Fig. 2 are presented in Fig. 4 for DG number i (DGi). Harmonic compensation is performed selectively for the main harmonics of PCC voltage or grid current depending on the compensation mode. Voltage compensation mode is activated in order to provide high voltage quality for the sensitive loads connected to PCC, while the aim in current compensation mode is to mitigate the harmonic content of the grid current. This way, the thermal stress on the grid-connection transformer due to the current harmonic content will be alleviated; furthermore, the voltage of the buses in the main grid which are adjacent to PCC will not be distorted due to harmonic current flow.

As depicted in Fig. 4, compensator structure is the same for both modes, however, the proper input should be selected for each mode as shown by "Compensation Mode Selection" block, e.g. $v^h_{\alpha\beta}$ for voltage compensation mode (selector at tap 1). Compensation reference for h[th] harmonic ($v^*_{c,h}$) is generated separately and then, all compensation references are added together. Afterwards, the resultant value is multiplied by the ratio of DGi rated capacity ($S_{0,i}$) to the total capacity of the microgrid DGs ($\sum_{j=1}^{n} S_{0,j}$) to generate total compensation reference (v^*_c) which is inserted as a voltage reference in the control system of Fig. 2. This way, the compensation workload is distributed among microgrid DGs considering their rated capacities.

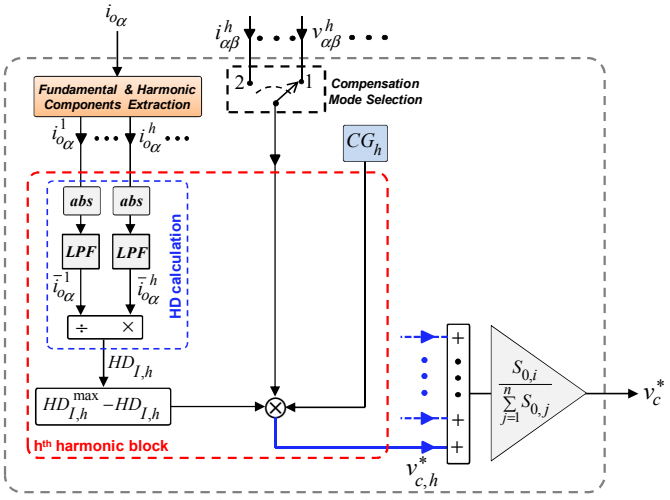

Fig. 4. Selective harmonic compensator block of DGi.

According to Fig. 4, $v^*_{c,h}$ is generated as follows:

$$v^*_{c,h} = \left(v^h_{\alpha\beta} \ \ or \ \ i^h_{\alpha\beta}\right) \cdot CG_h \cdot \left(HD^{\max}_{I,h} - HD_{I,h}\right) \quad (3)$$

where CG_h is the compensation gain for h[th] harmonic. CG_h is a constant which is the same for all DGs. $HD_{I,h}$ represents the h[th] harmonic distortion index of DG output current and $HD^{\max}_{I,h}$ is the maximum value of $HD_{I,h}$ (here, $HD^{\max}_{I,h} = 1$). $HD_{I,h}$ is defined as the magnitude ratio of h[th] harmonic to fundamental component of DG output current. Here, it is calculated as the ratio of rectified waveforms average values as shown in Fig. 4. Fundamental component and h[th] harmonic of α-axis output current ($i^1_{o\alpha}$ and $i^h_{o\alpha}$, respectively) are extracted. Then, $i^1_{o\alpha}$ and $i^h_{o\alpha}$ are rectified using absolute (*abs*) functions. Afterwards, *LPF*s are used to calculate average values ($\bar{i}^1_{o\alpha}$ and $\bar{i}^h_{o\alpha}$, respectively). Finally, $HD_{I,h}$ is calculated through dividing $\bar{i}^h_{o\alpha}$ by $\bar{i}^1_{o\alpha}$.

$HD_{I,h}$ is considered as the index of h[th] voltage harmonic compensation effort. In fact, compensation of each harmonic order of PCC voltage or grid current is achieved through injecting respective current harmonic by the DGs. Thus, including $\left(HD^{\max}_{I,h} - HD_{I,h}\right)$ term in equation (3) contributes towards harmonic compensation effort sharing among DGs. In fact, increase of compensation effort leads to $HD_{I,h}$ increase, $\left(HD^{\max}_{I,h} - HD_{I,h}\right)$ and consequently the effort is decreased. So, an inherent negative feedback exists in the compensation method.

III. Simulation Results

The electrical system of Fig. 5 which comprises a two-DG grid-connected microgrid and the utility grid is considered as the test system. DG1 is rated at double capacity comparing to DG2 ($S_{01}=2S_{02}$). It is assumed that the grid voltage is distorted by 3% (of fundamental voltage) 5[th] and 7[th] voltage harmonics. A diode rectifier is considered as the nonlinear load; also, a star-connected linear load (Z_L) is connected to PCC.

Power stage and control system parameters are listed in Tables I and II. As seen in Table I, $Z_{\ell 1} = 2 \cdot Z_{\ell 2}$ in order to simulate asymmetrical DG tie lines. The parameters of power controllers and virtual impedances are selected considering the different ratings of the DGs ($S_{01}=2S_{02}$) while the parameters of voltage and current controllers are the same for both DGs.

DG1 and DG2 reference values of fundamental active powers are $P^*_1 = 2000W$ and $P^*_2 = 1000W$, respectively, while the reference reactive powers are set to $Q^*_1 = 500VAr$ and $Q^*_2 = 250VAr$.

Four simulation cases are considered:

- Case1 $(0 \le t < 2s)$: DGs operate with only fundamental virtual impedance and harmonic compensation is not acting.
- Case2 $(2 \le t < 3.5s)$: Harmonic virtual resistances are added.
- Case3 $(3.5 \le t < 5s)$: PCC voltage compensation as well as fundamental and harmonic virtual impedances are acting.
- Case4 $(3.5 \le t < 5s)$: Grid current compensation as well as fundamental and harmonic virtual impedances are acting.

A. Case 1

As seen in Table III, before activating the harmonic virtual resistances, DGs output voltages are approximately free of harmonic distortion. It demonstrates the effectiveness of DGs controller in tracking the voltage reference. But, PCC voltage is distorted noticeably due to harmonic voltage drop on the DG tie lines. As depicted in Figs. 6(a) and (b), the reference of fundamental active and reactive powers are tracked properly in the interval comprising Cases1-3. It demonstrates the effectiveness of power controllers. The same results are obtained for Case 4. But, it can be noticed from Table IV that before addition of harmonic virtual resistances at t=2s, the total currents supplied by the DGs are not in proportion to their ratings due to improper sharing of harmonic components.

B. Case 2

Harmonic virtual resistances are added at t=2s. As seen in Table IV, the current sharing of DGs is improved noticeably, however, still is not in proportion to the DGs rated powers. The sharing improvement is achieved at the expense of voltage distortion increase at DGs terminals and consequently at PCC, as can be observed in Table III.

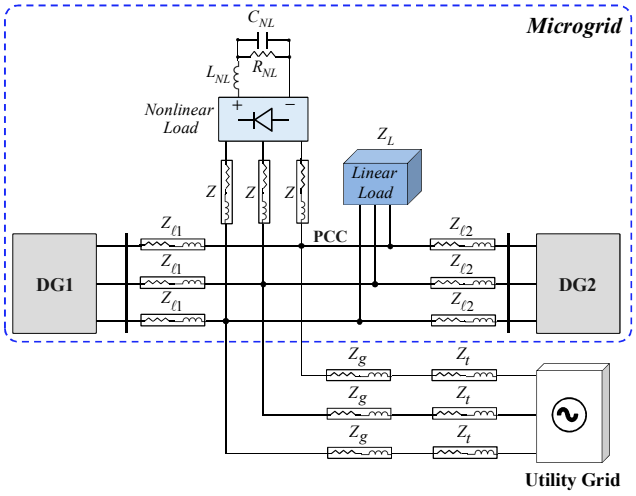

Fig. 5. Test system for simulation studies.

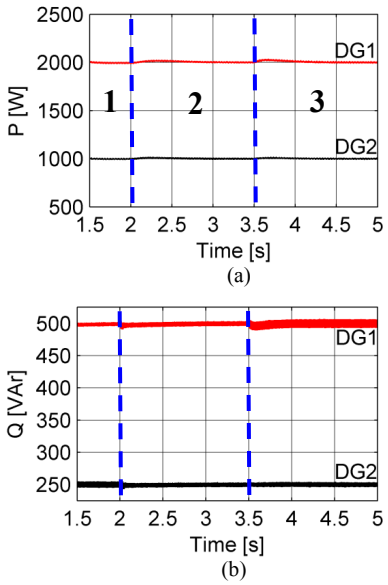

Fig. 6. Power sharing: (a) active power, (b) reactive power

C. Case3

Selective compensation of PCC voltage main harmonics is activated at t =3.5s. It leads to significant reduction of PCC voltage harmonic distortion as observed in Table III.

Also, it can be observed in Table III that the harmonic compensation is achieved by the increase of DG1 output voltage distortion. Note that DG1 tie line impedance is relatively high; also, the nonlinear load supplied by this DG is more than the amount supplied by DG2. Thus, after compensation activation, the output voltage of this DG has become distorted in order to compensate these harmonic voltage drops and provide approximately sinusoidal voltage at PCC. On the other hand, due to low value of the tie line impedance and non-fundamental power of DG2, harmonic distortion of PCC and DG2 change with approximately similar behavior as seen in Table III.

Moreover, as shown in Table IV, sharing of the current between DGs is significantly improved after harmonic compensation. The proper sharing of harmonic load is provided by harmonic virtual resistances as well as good sharing of compensation effort.

D. Case4

As seen in Table IV, the grid current is noticeably distorted in Cases 1-3. In this case current compensation mode is activated. According to Table IV, the quality of grid current is improved, significantly; furthermore, the current is properly shared between DGs. However, PCC voltage is made distorted as shown in Table III.

IV. Conclusions

A method has been proposed for selective compensation of PCC voltage and grid current main harmonics in a grid-connected microgrid. Harmonic compensation is achieved through proper control of DGs interface converters. A novel approach is proposed for sharing of compensation effort among DGs. Furthermore, a selective virtual resistance loop is included in order to improve nonlinear sharing. Simulation results show that by applying the proposed method, the quality of PCC voltage quality or grid current can be significantly improved, depending on the selected compensation mode; furthermore, DGs supplied currents are in proportion to their rated capacities.

TABLE I
Power Stage Parameters

dc link voltage	LC Filter Inductance	LC Filter Capacitance	Utility Tie line	Nonlinear Load Tie Line
V_{dc} (V)	L (mH)	C (μF)	$Z_g + Z_t$ (Ω,mH)	Z (Ω,mH)
650	1.8	25	1, 6	0.15, 1.5
DG_1/DG_2 Tie Line		Nonlinear Load		Linear Load
$Z_{\ell 1} / Z_{\ell 2}$ (Ω,mH)		$C_{NL} / R_{NL} / L_{NL}$ (μF)/(Ω)/(mH)		Z_L (Ω,mH)
0.3,3/0.15,1.5		235/100/0.084		50,20

TABLE II
DGs Control System Controller Parameters

Power Controllers					
DG1			*DG2*		
m_p (rad/W)	m_i (rad/W.s)		m_p (rad/W)	m_i (rad/W.s)	
10^{-5}	10^{-4}		2×10^{-5}	2×10^{-4}	
n_p (V/VAr)	n_i (V/VAr.s)		n_p (V/VAr)	n_i (V/VAr.s)	
0.5×10^{-1}	10^{-1}		10^{-1}	2×10^{-1}	
Virtual Impedance					
DG1			*DG2*		
R_v (Ω)	L_v (mH)	$R_{v,5}, R_{v,7}$ (Ω)	R_v (Ω)	L_v (mH)	$R_{v,5}, R_{v,7}$ (Ω)
0.2	2	4	0.4	4	8
Voltage Controller [7]					
k_{pV}	k_{rV_1}	k_{rV_5}	k_{rV_7}	ω_{cV} (rad/s)	
1	100	50	50	2	
Current Controller [7]					
k_{pI}	k_{rI_1}	k_{rI_5}	k_{rI_7}	ω_{cI} (rad/s)	
5	1000	100	100	2	
Selective Harmonic Compensator					
voltage compensation mode		current compensation mode			
CG_5	CG_7	CG_5	CG_7		
-70	-25	360	1000		

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TABLE III

VOLTAGE WAVEFORMS AT DIFFERENT SIMULATION CASES

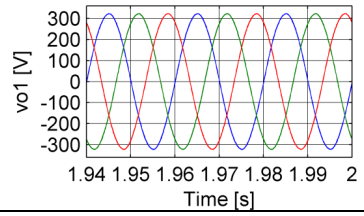
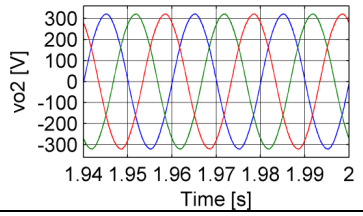
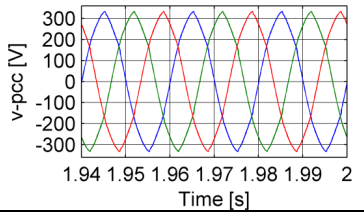
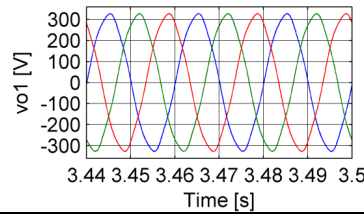
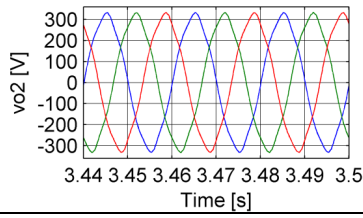
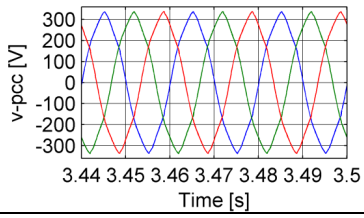
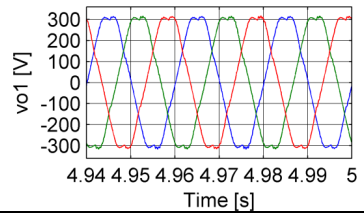
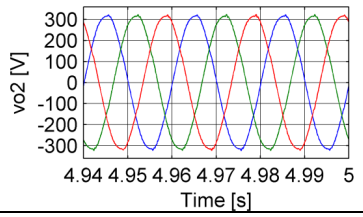
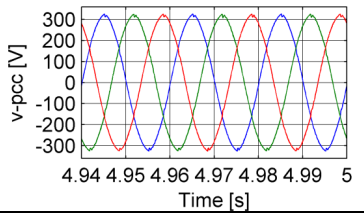
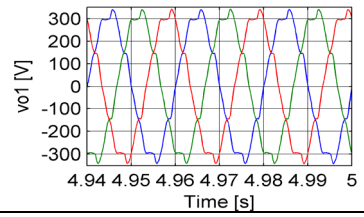
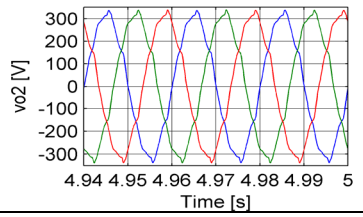
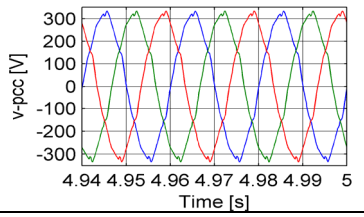
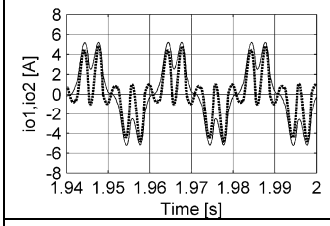
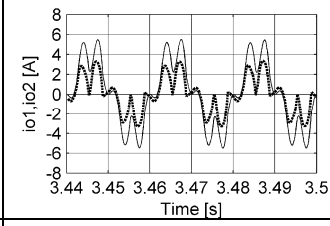
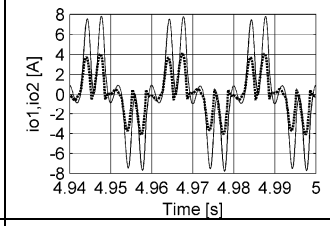
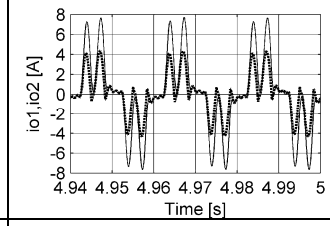
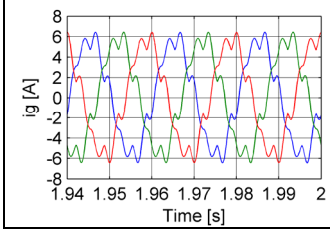
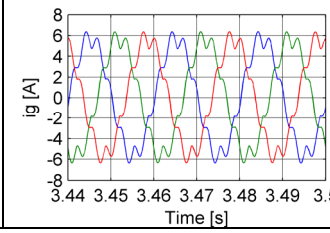
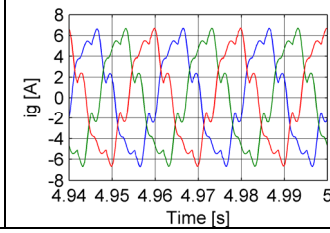
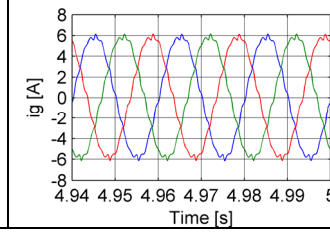
	DG_1	DG_2	PCC
Case1			
Case2			
Case3			
Case4			

TABLE IV

CURRENT WAVEFORMS AT DIFFERENT SIMULATION CASES

Second row: DGs output current, phase-a (DG1:solid line, DG2: tick dashed line), Third row: Three-phase grid current

Case1	Case2	Case3	Case4
			
			

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