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Autonomous Voltage Unbalance Compensation in an Islanded Droop-Controlled Microgrid

Mehdi Savaghebi, *Student Member, IEEE*, Alireza Jalilian, Juan C. Vasquez, and Josep M. Guerrero, *Senior Member, IEEE*

Abstract—Recently, there is an increasing interest in using distributed generators (DGs) not only to inject power into the grid, but also to enhance the power quality. In this paper, a stationary-frame control method for voltage unbalance compensation in an islanded microgrid is proposed. This method is based on the proper control of DGs interface converters. The DGs are controlled to compensate voltage unbalance autonomously while share the compensation effort and also active and reactive power, properly. The control system of the DGs mainly consists of active and reactive power droop controllers, virtual impedance loop, voltage and current controllers and unbalance compensator. The design approach of the control system is discussed in detail and simulation and experimental results are presented. The results demonstrate the effectiveness of the proposed method in compensation of voltage unbalance.

Index Terms—Distributed generator (DG), microgrid, voltage unbalance compensation.

I. INTRODUCTION

UNBALANCED voltages can result in adverse effects on equipment and power system. Under unbalanced conditions, the power system will incur more losses and be less stable. Also, voltage unbalance has some negative impacts on equipment such as induction motors, power electronic converters and adjustable speed drives (ASDs). Thus, the International Electrotechnical Commission (IEC) recommends the limit of 2% for voltage unbalance in electrical systems [1].

A major cause of voltage unbalance is the connection of unbalanced loads (mainly, single-phase loads connection between two phases or between one phase and the neutral).

Compensation of voltage unbalance is usually done using series active power filter through injection of negative sequence voltage in series with the distribution line [2]-[4].

However, there are a few works [5]-[9] based on shunt compensation to mitigate voltage unbalance. In these works, voltage unbalance caused by unbalanced load is compensated through balancing the line currents. But, in the case of severe load unbalance the amplitude of the current injected by active filter can be very high and exceed the filter rating.

On the other hand, it is well-known that the Distributed Generators (DGs) often consist of a prime mover connected through an interface converter (e.g. an inverter in the case of dc/ac conversion) to the ac power distribution system. The distribution system may be the utility grid or the local grid formed by a cluster of DGs which is called microgrid. The main role of DG inverter is to adjust output voltage phase angle and amplitude in order to control the active and reactive power injection. In addition, compensation of power quality problems can be achieved through proper control strategies [10]. In [11]-[14], some approaches are presented to use the DG for voltage unbalance compensation.

The control method presented in [11] and [12] is based on using a two-inverter structure one connected in shunt and the other in series with the grid, like a series-parallel active power filter [15]. The main role of the shunt inverter is to control active and reactive power flow, while the series inverter balances the line currents and the voltages at sensitive load terminals, in spite of unbalanced grid voltage. This is done by injecting negative sequence voltage. Thus, two inverters are necessary for the power injection and unbalance compensation. It can be considered as a negative point, especially in terms of the cost and volume of the DG interface converter.

A method for voltage unbalance compensation through injection of negative sequence current by the DG has been proposed in [13]. By applying this method, line currents become balanced in spite of the unbalanced loads presence. However, under severely unbalanced conditions, a large amount of the interface converter capacity is used for compensation and it may interfere with the active and reactive power supply by the DG.

The approach presented in [14] is based on controlling the DG as a negative sequence conductance to compensate the voltage unbalance in a microgrid. In this approach which is implemented in the synchronous (dq) reference frame, compensation is done by generating a reference for negative sequence conductance based on the negative sequence reactive power. Then, this conductance is applied to produce the

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compensation reference current. In [14] the compensation reference is injected at the output of the voltage control loop. However, such compensation will be considered as a disturbance to be rejected by the voltage control loop. In the other words, there is a trade-off between the unbalance compensation efficiency and voltage regulation adequacy.

To cope with this problem, the present paper proposes the direct change of the voltage reference to compensate voltage unbalance in a microgrid. This way, the compensation reference is considered as a command to be followed by the voltage controller. Also, since no design approach is presented in [14], the details of the control system design are discussed.

In the proposed method, the overall control system is designed in the stationary ($\alpha\beta$) reference frame. The main control loops are as follows:

- Voltage and current controllers
- Virtual impedance loop
- Active and reactive power controllers
- Voltage unbalance compensator

This paper is organized as follows. The DG interface inverter control strategy is discussed in Section II. In this Section the details of the whole control structure are explained. Section III is dedicated to the design of the control system. Simulation and experimental results are presented in Section IV. Finally, the paper is concluded in Section V.

II. DG INTERFACE CONVERTER (INVERTER) CONTROL METHOD

Fig. 1 shows the power stage of a DG and the proposed control strategy for its interface inverter. The power stage consists of a dc prime-mover (V_{dc}), an inverter and an LC filter.

As mentioned before, the control system of Fig. 1 is designed in $\alpha\beta$ reference frame. So, the Clarke transformation is used to transform the variables between abc and $\alpha\beta$ frames. The equations (1) and (2) are used for the transformation:

$$x_{\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot x_{abc} \quad (1)$$

$$x_{abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot x_{\alpha\beta} \quad (2)$$

where x_{abc} and $x_{\alpha\beta}$ can represent the instantaneous output voltage (v_{oabc} and $v_{o\alpha\beta}$), output current (i_{oabc} and $i_{o\alpha\beta}$) or LC filter inductor current (i_{Labc} and $i_{L\alpha\beta}$) in abc and $\alpha\beta$ frames, respectively:

$$x_{abc} = \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}, \quad x_{\alpha\beta} = \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix}$$

The three-phase instantaneous voltages are measured with respect to an artificial null voltage (v_n) which is calculated as follows:

$$v_n = \frac{v_{ab} + v_{bc} + v_{ca}}{3} \quad (3)$$

where v_{ab} , v_{bc} and v_{ca} represent the instantaneous phase-to-phase voltages.

As seen in (1) and (2), the stationary frame is formed by α and β components and zero component is not considered. It should be noted that in the present paper, a three-phase three-wire islanded microgrid is considered. Since, zero sequence current cannot flow in the three-wire ungrounded electrical systems [16]; zero sequence voltage drops will not affect the system voltages. Also, zero sequence which may be present in the main grid voltages has no effect on an islanded microgrid. Generally, zero sequence voltage cannot be present in the three-wire electrical systems in the absence of a fault (e.g. phase-to-ground short circuit) [17], [18].

As shown in Fig. 1, the voltage controller follows the references generated by power controllers and unbalance compensation block and generates the reference for the current controller. The output of the current controller is transformed back to abc frame and then divided by V_{dc} to provide three-phase voltage reference for the pulse width modulator (PWM). Finally, the PWM block controls the switching of the inverter based on this reference. It is noteworthy that V_{dc} is not constant. Thus, a feedforward loop is included to consider V_{dc} value for generation of the gate signals. This way, variations of V_{dc} inside the allowed limits can be compensated.

In Fig. 1, ω^* is the reference angular frequency of the microgrid. In fact, active and reactive power controllers provide the references of DG voltage phase angle (frequency) and amplitude in order to ensure proper parallel operation of the DGs. As explained in Subsection II-A, it is done by using phase angle and amplitude droop controllers.

More details about the control system are presented in the following Subsections.

A. Active and Reactive Power Control

Considering a three-phase DG which is connected to the grid through the impedance $Z \angle \theta$, the fundamental positive sequence (FPS) active and reactive powers injected to the grid by the DG (P^+ and Q^+ , respectively) can be expressed as follows [19]:

$$P^+ = 3 \cdot \left(\frac{E \cdot V}{Z} \cos \phi - \frac{V^2}{Z} \right) \cos \theta + 3 \cdot \frac{E \cdot V}{Z} \sin \phi \sin \theta \quad (4)$$

$$Q^+ = 3 \cdot \left(\frac{E \cdot V}{Z} \cos \phi - \frac{V^2}{Z} \right) \sin \theta - 3 \cdot \frac{E \cdot V}{Z} \sin \phi \cos \theta \quad (5)$$

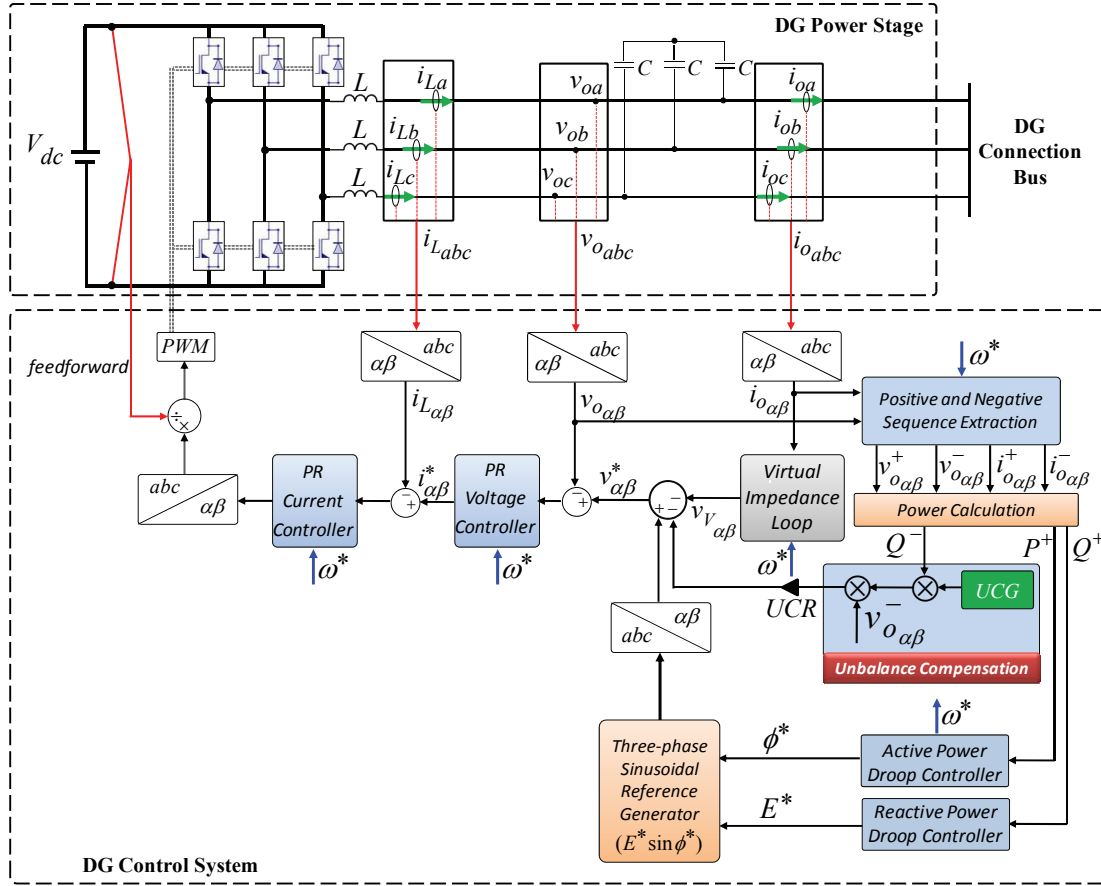


Fig. 1. DG power stage and control system.

where E is the phase *rms* value of the DG inverter output FPS voltage, V represents the grid phase *rms* voltage, ϕ is the load angle (the angle between E and V), and Z and θ are the magnitude and the phase of the impedance, respectively. Considering phase angle of the grid voltage to be zero, ϕ will be equal to phase angle of the inverter voltage.

Assuming a mainly inductive electrical system ($Z \approx X$ and $\theta \approx 90$), the FPS active and reactive powers can be expressed as the following equations:

$$P^+ \approx 3 \cdot \frac{E \cdot V}{X} \sin \phi \quad (6)$$

$$Q^+ \approx 3 \cdot \frac{E \cdot V \cos \phi - V^2}{X} \quad (7)$$

In practical applications, ϕ is normally small; thus, a P^+ / Q^+ decoupling approximation ($\cos \phi \approx 1$ and $\sin \phi \approx \phi$) can be considered as follows [19], [20]:

$$P^+ \approx 3 \cdot \frac{E \cdot V}{X} \phi \quad (8)$$

$$Q^+ \approx 3 \cdot \frac{V}{X} (E - V) \quad (9)$$

Thus, FPS active and reactive powers can be controlled by the DG output FPS voltage phase angle and amplitude, respectively. According to this, the following droop

characteristics are considered for sharing of FPS powers among the DGs of an islanded microgrid:

$$\phi^* = \phi_0 - (m_P P^+ + m_I \int P^+ dt) \quad (10)$$

$$E^* = E_0 - n_P Q^+ \quad (11)$$

where

- E_0 : rated voltage amplitude
- ϕ_0 : rated phase angle ($\int \omega_0 dt = \omega_0 t$)
- ω_0 : rated angular frequency
- m_P : FPS active power proportional coefficient
- m_I : FPS active power integral coefficient
- n_P : FPS reactive power proportional coefficient
- E^* : FPS voltage amplitude reference
- ϕ^* : FPS voltage phase angle reference ($\phi^* = \int \omega^* dt$)

In fact, equation (10) acts as a proportional-derivative controller for frequency. The derivative term (m_P) helps to improve the dynamic behavior of the power control [19]. It is noteworthy that according to the equations (10) and (11), no integral term is considered for voltage frequency and amplitude control. When the microgrid is operating in islanded mode (the case considered in this paper) the use of pure integrators is not allowed, since the total load will not coincide with the total injected power, and it leads to instability [21]-[23].

The design of the droop controllers is sufficiently studied in the literature (e.g. [19]-[22]) and will not be discussed in the present paper.

As it can be seen in Fig. 1, E^* and ϕ^* are used to generate the three phase reference voltages of the inverter. These voltages are FPS components; thus FPS powers (P^+ and Q^+) are used in equations (10) and (11). According to Fig. 1, in order to calculate these powers, at first DG three-phase instantaneous output voltage and current ($v_{o_{abc}}$ and $i_{o_{abc}}$, respectively) are measured and transformed to $\alpha\beta$ frame ($v_{o_{\alpha\beta}}$ and $i_{o_{\alpha\beta}}$, respectively). Then, instantaneous values of fundamental positive and negative sequence output voltage ($v_{o_{\alpha\beta}}^+$ and $v_{o_{\alpha\beta}}^-$, respectively) and output current ($i_{o_{\alpha\beta}}^+$ and $i_{o_{\alpha\beta}}^-$, respectively) are extracted [24], [25] and fed to power calculation block.

It is noteworthy that according to the symmetrical components theory [26] any set of the unbalanced three-phase quantities (e.g. voltages or currents) can be resolved into three sets of balanced sequence components, namely positive, negative and zero sequence components. Positive sequence components consist of three phasors with equal magnitudes and $\pm 120^\circ$ phase displacement. Negative sequence components include the similar phasors; but, the direction of rotation is opposite of the positive sequence phasors. Zero sequence components are three phasors with equal magnitude and zero phase displacement. As explained earlier, zero sequence components are not present in the microgrid studied in this paper.

The details of power calculation are presented in the following Subsection.

B. Power Calculation

Power calculation is done according to the instantaneous reactive power theory [27]. As explained in [27], the instantaneous values of three-phase active and reactive powers can be calculated according to the following equations, respectively:

$$p = v_{o_\alpha} i_{o_\alpha} + v_{o_\beta} i_{o_\beta} \quad (12)$$

$$q = v_{o_\alpha} i_{o_\beta} - v_{o_\beta} i_{o_\alpha} \quad (13)$$

Each of the instantaneous powers calculated using (12) and (13) consists of dc and ac (oscillatory) components. The dc components (average values of p and q) are FPS active and reactive powers which can be extracted using low pass filters (LPF_s) [28]. The oscillatory parts are generated by the unbalance and harmonic contents of the voltage and current.

Note that if FPS components of voltage and current ($v_{o_{\alpha\beta}}^+$ and $i_{o_{\alpha\beta}}^+$, respectively) are used in (12) and (13) instead of total instantaneous voltages and currents

($v_{o_{\alpha\beta}}$ and $i_{o_{\alpha\beta}}$, respectively) only the dc components of powers will remain. Thus, low pass filtering will not be necessary for power calculation.

In [27], no method is presented for calculation of fundamental negative sequence (FNS) powers; while as explained later, FNS reactive power is required for unbalance compensation. Thus, in what follows a method is proposed for calculation of this power. Also, in order to have consistent formulation for power calculation, the method of FPS power calculation is modified.

According to the symmetrical components theory and also IEEE Standard 1459-2010 [29] calculation of FPS and FNS powers can be done by applying the conventional power equations, but, using respective sequence voltage and current (e.g. FPS voltage and current for FPS powers).

Thus, equation (12) and (13) can be modified as follows in order to calculate instantaneous FPS active and reactive powers, respectively:

$$P'^+ = v_{o_\alpha}^+ i_{o_\alpha}^+ + v_{o_\beta}^+ i_{o_\beta}^+ \quad (14)$$

$$Q'^+ = v_{o_\alpha}^+ i_{o_\beta}^+ - v_{o_\beta}^+ i_{o_\alpha}^+ \quad (15)$$

where “+” and “-” superscripts indicate positive and negative sequence components, respectively.

A similar approach is applied in [14] for FPS powers calculation.

Also, according to the above explanations, equation (16) can be applied for calculation of instantaneous FNS reactive power:

$$Q'^- = v_{o_\alpha}^- i_{o_\beta}^- - v_{o_\beta}^- i_{o_\alpha}^- \quad (16)$$

As explained earlier, P'^+ , Q'^+ and Q'^- include only the dc power components and low pass filtering is not necessary for power calculation. However, in this paper, P^+ and Q^+ which are calculated according to the following Laplace domain equations are applied in the droop controllers of (10) and (11):

$$P^+(s) = P'^+(s) \cdot LPF(s) \quad (17)$$

$$Q^+(s) = Q'^+(s) \cdot LPF(s) \quad (18)$$

where s represents Laplace variable and $LPF(s)$ is the transfer function of low pass filter:

$$LPF(s) = \frac{\omega_c}{s + \omega_c}$$

ω_c is the cut-off frequency of low pass filters which is set to 1.25 (rad/sec).

As stated in [22] and [30] droop controllers emulate the function of the large synchronous generators by adding virtual inertia to the DGs. In fact, LPF_s are applied in (17) and (18) in order to have enough virtual inertia and prevent the microgrid sensitivity to the disturbances [20].

Similar to equations (17) and (18), the following equation is applied for FNS reactive power calculation:

$$Q^-(s) = Q'^-(s) \cdot LPF(s) \quad (19)$$

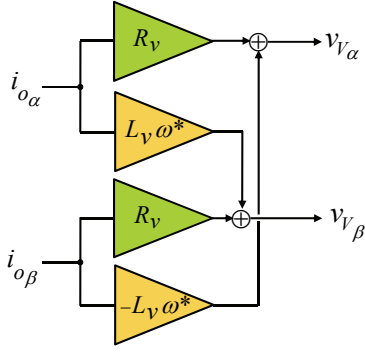


Fig. 2. Virtual impedance block diagram.

Using *LPF* in (19) improves the stability of unbalance compensation by preventing sudden change of Q^- as a result of compensation.

As mentioned earlier, FPS powers are used by the power controllers to generate the reference values for the inverter output voltage phase and amplitude, respectively. FNS reactive power is applied for voltage unbalance compensation as explained in Subsection II-E.

It is noteworthy that in [14] Q^- is calculated by multiplication of positive sequence voltage and negative sequence current. This calculation method doesn't comply with the basic knowledge of symmetrical components [26] and also proposal of the IEEE Standard 1459-2010 [29].

C. Virtual Impedance Loop

The accuracy of the power sharing provided by the droop controllers is affected by the output impedance of the DG units as well as the line impedances. The virtual impedance is a fast control loop which is able to fix the phase and magnitude of the output impedance. Moreover, the effect of asymmetrical line impedances can be mitigated by proper design of the virtual impedance loop [19], [22], [30], [31].

Addition of the virtual resistance makes the oscillations of the system more damped [19]. The damping can also be provided by a physical resistance at the expense of efficiency decrease due to ohmic losses. In contrast with a physical resistance, the virtual resistance has no power losses, since is provided by a control loop; thus, it is possible to implement it without decreasing the efficiency [22].

Also, virtual inductance is considered to make the DG output impedance more inductive in order to improve the decoupling of P^+ and Q^+ . Thus, the virtual impedance enhances the droop controllers performance and stability [30], [32].

Furthermore, the virtual output impedance can provide additional features such as hot-swap operation and sharing of nonlinear load [19], [22]. These features fall out of the present paper scope.

As shown in Fig. 1, the instantaneous output current is fed to the virtual impedance control loop. Then, the output of this loop is subtracted from the voltage reference.

The virtual impedance is implemented as shown in Fig.2, where R_v and L_v are the virtual resistance and inductance values, respectively [32]. Thus, the following equations express the virtual impedance in $\alpha\beta$ frame:

$$v_{V\alpha} = R_v \cdot i_{o\alpha} - L_v \cdot (\omega^*) \cdot i_{o\beta} \quad (20)$$

$$v_{V\beta} = R_v \cdot i_{o\beta} + L_v \cdot (\omega^*) \cdot i_{o\alpha} \quad (21)$$

D. Proportional-Resonant Voltage and Current Controllers

Due to the difficulties of using proportional-integral (PI) controllers to track non-dc variables, proportional-resonant (PR) controllers are usually preferred to control the voltage and current in stationary reference frame [33]. In this paper, PR voltage and current controllers are as (22) and (23):

$$G_V(s) = k_{pV} + \frac{k_{rV}s}{s^2 + (\omega^*)^2} \quad (22)$$

$$G_I(s) = k_{pI} + \frac{k_{rI}s}{s^2 + (\omega^*)^2} \quad (23)$$

where, k_{pV} (k_{pI}) and k_{rV} (k_{rI}) are the proportional and resonant coefficients of the voltage (current) controller, respectively.

As shown in Fig. 1, instantaneous filter inductor current ($i_{L\alpha\beta}$) is controlled by the current controller. By controlling this current rather than the DG output current, influence of the load current on the control system performance is rejected, properly [34].

E. Voltage Unbalance Compensation

It is well known that the voltage unbalance leads to appearance of the negative sequence voltage. Thus, compensation of the voltage unbalance can be achieved through reducing negative sequence voltage.

As shown in Fig. 1, the output of “Unbalance Compensation” block (“*UCR: Unbalance Compensation Reference*”) is injected as a reference for the voltage controller. To generate this compensation reference, FNS reactive power (Q^-) is multiplied by a constant (“*UCG: Unbalance Compensation Gain*”) and also by the instantaneous FNS voltage ($v_{o\alpha\beta}^-$).

UCG is a constant which controls the compensation effort of DGs and should be selected in a way that the voltage unbalance is compensated to an acceptable level without making the control system unstable. The method of *UCG* setting is presented in Subsection III-B.

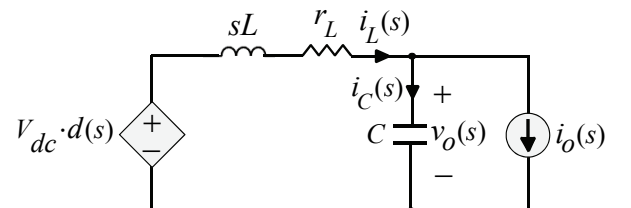


Fig. 3. Single-phase representation of the DG inverter.

Since, with the compensation of voltage unbalance (decrease of the negative sequence voltage) Q^- decreases, considering Q^- for generation of the compensation reference leads to the proper sharing of compensation effort among the DGs of the microgrid. Thus, DGs will be able to compensate voltage unbalance autonomously and there is no need to communication link among them.

Also, multiplying with $v_{o\alpha\beta}^-$ ensures that the compensation reference will act in the opposite-phase of the negative sequence voltage (the voltage which should be compensated), considering the negative sign used for the reference injection.

It is noteworthy that in the present paper unbalance compensation is based on the fundamental voltage component, since it has been generated by a linear single-phase load. Compensation of voltage harmonics which can be generated by a nonlinear unbalanced load is out of this work scope, but can be considered by separating positive and negative sequences of each harmonic order.

III. CONTROL SYSTEM DESIGN

In this paper, the results are presented for two cases. However, the control system is designed only for ‘‘Case 1’’. The same procedure can be performed about ‘‘Case 2’’.

A. Voltage, Current and Virtual Impedance Control Loops

In this Subsection, voltage, current and virtual impedance control loops are designed without considering the effect of unbalance compensation; then, in the next Subsection, compensation gain is selected in a way that the stability of the compensated system is ensured.

According to the symmetrical components theory [26], an unbalanced electrical system can be analyzed by separate positive and negative sequence balanced systems. Thus, the single-phase representation shown in Fig. 3 is assumed for positive (or negative) sequence modeling, where $d(s)$ and r_L are the duty cycle and filter inductor resistance, respectively.

On the other hand, considering Fig. 1 (without unbalance compensation) and Fig. 3, the block diagram of positive sequence control system and power stage is achieved as Fig. 4 where $G_{PWM}(s)$ represents the transfer function of *PWM* block which is usually modeled as a delay element. Here, the *PWM* delay is neglected ($G_{PWM}(s)=1$).

Based on Fig. 4, the following equation can be extracted:

$$v_o(s) = G(s)v^*(s) - Z_o(s)i_o(s) \quad (24)$$

where, $G(s)$ and $Z_o(s)$ are the control system closed-loop transfer function and output impedance, respectively:

$$G(s) = \frac{G_V(s) \cdot G_I(s)}{LCs^2 + (r_L + G_I(s)) \cdot Cs + G_V(s) \cdot G_I(s) + 1} \quad (24a)$$

$$Z_o(s) = Z'_o(s) + Z_v(s) \quad (24b)$$

$Z_v(s)$ represents the virtual impedance and $Z'_o(s)$ can be expressed as:

$$Z'_o(s) = \frac{r_L + Ls + G_I(s)}{LCs^2 + (r_L + G_I(s)) \cdot Cs + G_V(s) \cdot G_I(s) + 1} \quad (24c)$$

Equation (24) represents the equivalent Thévenin model of the closed loop system.

The positive and negative sequences Bode diagrams of $G(s)$ ($G^+(s)$ and $G^-(s)$, respectively) and $Z_o(s)$ ($Z_o^+(s)$ and $Z_o^-(s)$, respectively) by considering the control system and power stage parameters (listed in Tables I and II) are depicted in Figs. 5 and 6, respectively. Extraction of closed-loop gain and output impedance in the negative sequence is similar to positive sequence. But, it is necessary to replace ‘‘ s ’’ by ‘‘ $-s$ ’’ in the block diagram of Fig. 4.

As can be seen in Fig. 5, the magnitude of $G(s)$ is the same for positive and negative sequences. Also, as expected, positive and negative sequences are in the opposite phase. Furthermore, the gain and the phase angle of closed-loop transfer function at fundamental frequency are respectively unity and zero for both positive and negative sequences. Thus, proper tracking of voltage reference is provided.

As shown in Fig. 6, magnitude of $Z_o(s)$ is also the same for both sequences and $Z_o^+(s)$ and $Z_o^-(s)$ are in the opposite phase.

B. UCG Setting

At first, it is assumed that the electrical system is operating in sinusoidal steady state conditions. Thus, phasor analysis can be performed. Then, a small perturbation is applied and stability of the control system as a function of *UCG* is evaluated. It is well known that for the phasor analysis s is usually replaced by $j\omega$.

According to Fig. 1, *UCR* phasor (**UCR**) is calculated as:

$$\mathbf{UCR} = Q^- \cdot \mathbf{V}_o^- \cdot UCG \quad (25)$$

where \mathbf{V}_o^- represents the phasor of FNS output voltage.

On the other hand, if the output impedance of the DG is considered as follows:

$$Z_o^\pm(j\omega) = (R_v + R') \pm j\omega(L_v + L') \quad (26)$$

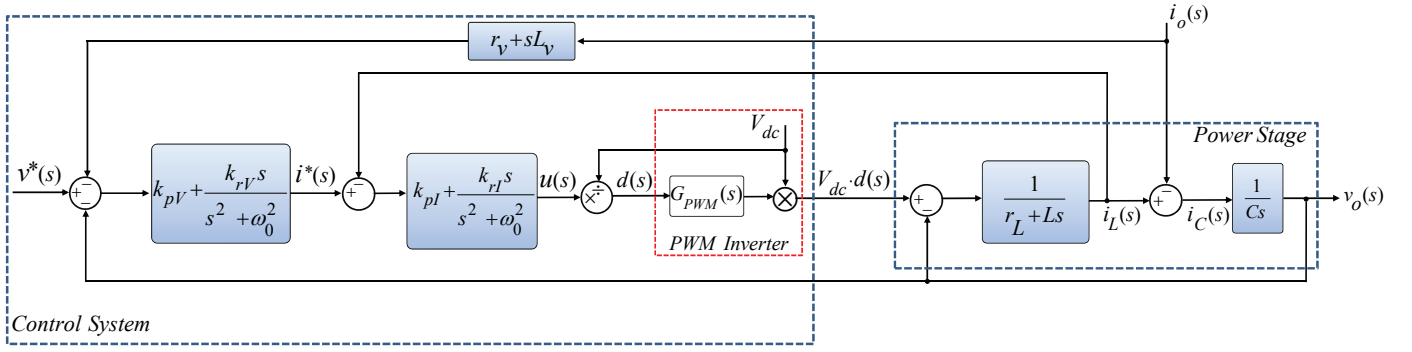


Fig. 4. Block diagram of power stage and positive sequence control system.

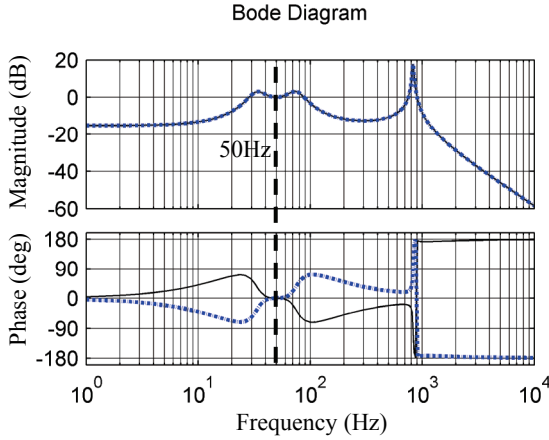


Fig. 5. Bode diagrams of positive (solid line) and negative (dashed line) sequence closed-loop transfer function.

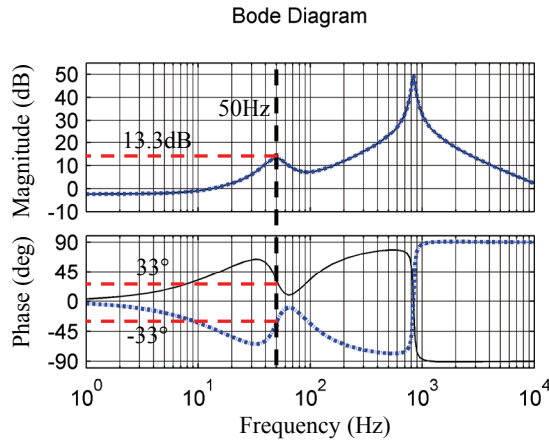


Fig. 6. Bode diagrams of positive (solid line) and negative (dashed line) sequence output impedance.

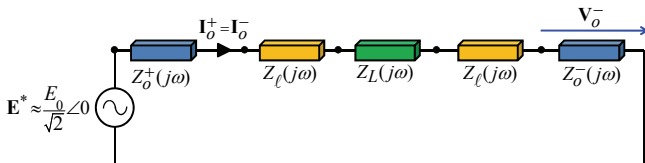


Fig. 7. Equivalent circuit for calculation of \mathbf{I}_o^- .

Based on Fig. 6, it can be concluded that at fundamental frequency $L' \approx 0$. Thus, Q^- can be approximated by the reactive power consumptions of L_v :

$$Q^- = 3 \cdot X_v \cdot (\mathbf{I}_o^-)^2 \cdot LPF(j\omega) \quad (27)$$

where \mathbf{I}_o^- and X_v are the phasor of FNS output current and virtual reactance, respectively.

By substituting (27) in (25) and linearizing the resultant equation, the following small-signal representation is achieved:

$$\mathbf{U}\hat{\mathbf{C}}\mathbf{R} = \left[3 \cdot X_v \cdot (\mathbf{I}_o^-)^2 \cdot \hat{\mathbf{V}}_o^- + 6 \cdot X_v \cdot \mathbf{I}_o^- \cdot \mathbf{V}_o^- \cdot \hat{\mathbf{I}}_o^- \right] \cdot UCG \cdot LPF(j\omega) \quad (28)$$

where the symbol $\hat{}$ represents the small signal value.

On the other hand, according to the symmetrical components theory [26] when a single-phase load is connected between two phases (the case considered in this paper), the circuit shown in Fig. 7 can be used for positive and negative sequence current calculation. In this Fig., $Z_L(j\omega)$ and $Z_\ell(j\omega)$ are respectively the load and distribution line (the line between DG and load connection point) impedances, and \mathbf{E}^* is the phasor of the FPS reference phase voltage which is generated by the reactive power droop controller as presented in (11).

The magnitude of \mathbf{E}^* is equal to the *rms* value of the phase voltage. As shown in Fig. 7, the *rms* value can be approximated by $\frac{E_0}{\sqrt{2}}$ ($E_0 = 330V$) assuming that the voltage drop caused by the droop controller is negligible.

In Case 1, a pure resistance equal to 73Ω is considered as the single-phase load ($Z_L(j\omega) = 73 + 0 \cdot j\omega$).

Thus, using Fig. 7 and considering this fact that usually the load impedance is much greater than the other impedances of this Fig., the following equation is achieved:

$$\mathbf{I}_o^- \approx \frac{\mathbf{E}^*}{Z_L(j\omega)} \quad (29)$$

In addition, (24) has the following form in the negative sequence ($v^*(j\omega) = 0$):

$$\mathbf{V}_o^- = -Z_o^-(j\omega) \cdot \mathbf{I}_o^- \quad (30)$$

Equation (30) can also be extracted according to Fig. 7. Then, substituting (29) and (30) in (28) leads to the following equation:

$$\mathbf{UCR} = \left[\left(\frac{3 \cdot X_v \cdot (\mathbf{E}^*)^2}{Z_L^2(j\omega)} \hat{\mathbf{V}}_o^- - \frac{6 \cdot X_v \cdot (\mathbf{E}^*)^2 \cdot Z_o^-(j\omega)}{Z_L^2(j\omega)} \right) \cdot \hat{\mathbf{I}}_o^- \right] \cdot UCG \cdot LPF(j\omega) \quad (31)$$

Thus, when the unbalance compensation is activated, the following small signal equation is achieved:

$$\hat{\mathbf{V}}_o^- = G_{closed-loop}(j\omega) \cdot \hat{\mathbf{I}}_o^- \quad (32)$$

being,

$$G_{closed-loop}(j\omega) = \frac{6 \cdot G^-(j\omega) \cdot X_v \cdot (\mathbf{E}^*)^2 \cdot Z_o^-(j\omega) \cdot UCG \cdot LPF(j\omega)}{Z_L^2(j\omega) + 3 \cdot G^-(j\omega) \cdot X_v \cdot (\mathbf{E}^*)^2 \cdot UCG \cdot LPF(j\omega)} \cdot \frac{Z_o^-(j\omega) \cdot Z_L^2(j\omega)}{Z_L^2(j\omega) + 3 \cdot G^-(j\omega) \cdot X_v \cdot (\mathbf{E}^*)^2 \cdot UCG \cdot LPF(j\omega)}$$

This equation is the negative sequence small signal form of (24) by considering $v^*(j\omega) = -\mathbf{UCR}$ (note to the negative sign used for injection of UCR in Fig. 1).

It is obvious that by increase of UCG , compensation effort will increase. However, UCG has to be selected in a way to maintain the control system stability. The poles of $G_{closed-loop}(j\omega)$ for $UCG=(0.9, 1.2, 1.5, 1.8)$ are shown in Fig. 8. As can be seen, for $UCG=1.8$, two poles are located in the right half of s -plane and thus, the control system becomes unstable. So, 1.5 is selected as the compensation gain.

IV. RESULTS

The results of two cases are presented in this Section. In “Case 1” the experimental and simulation results of voltage unbalance compensation considering a resistive load are presented and compared. Since, good agreement between simulation and experiment results is demonstrated in “Case 1”, only the experimental results are presented for “Case 2” in which a resistive-inductive (RL) load is considered.

The islanded microgrid shown in Fig. 9 is considered as the test system for simulation studies and also experimental evaluation of voltage unbalance compensation. This microgrid includes two DGs with the power stage and control system shown in Fig. 1. A single-phase load is connected between phase- a and phase- b to create voltage unbalance. The switch shown in Fig. 9 is closed after synchronization in order to form a microgrid. The synchronization method is explained in [22]. The three-phase inductors between each DG and load connection point (L_{l1} and L_{l2} for DG1 and DG2, respectively) model

the distribution lines. In order to consider asymmetrical distribution lines, $L_{l1} = 2 \cdot L_{l2}$.

The parameters of the control system and microgrid power stage are listed in Tables I and II, respectively. Unless otherwise specified, the parameters are the same for both cases. Also, L , C and V_{dc} are the same for both DGs. Switching frequency of DGs inverter is 10 kHz. The photo of experimental setup is shown in Fig. 10. In this Fig., the output inductors model the distribution lines.

A. Case 1-Resistive Load

In this case, simulation and experimental results of voltage unbalance compensation considering a resistive load are presented and compared.

In the experiment, the DGs are controlled by a DS1103 dSPACE controller card. “dSPACE Control Desk” is used as the user interface. Simulations are performed using MATLAB/Simulink software package.

TABLE I
CONTROL SYSTEM PARAMETERS

Power Controllers					Virtual Impedance	
m_P	m_I	n_P	E_0	ω_0	R_v (Ω)	L_v (mH) Case1/Case2
0.0001	0.001	0.18	330	$2\pi \cdot 50$	1	8/4
Voltage Controller		Current Controller		Unbalance Compensator		
k_{pV}	k_{rV}	k_{pI}	k_{rI}	UCG		
0.35	25	0.7	500	1.5		

TABLE II
ELECTRICAL SYSTEM PARAMETERS

average V_{dc} (V)	L (mH)	C (μF)	L_{l1} (mH)	L_{l2} (mH)	Z_L (Ω) Case1/Case2
650	1.8	25	3.6	1.8	73/57+4.7j

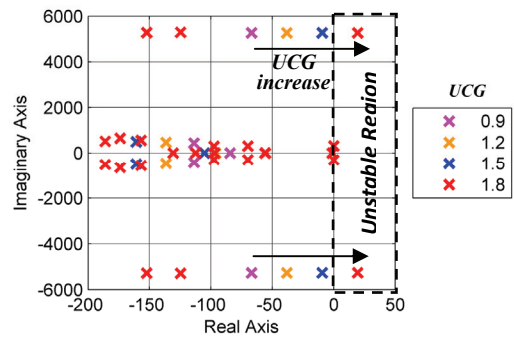


Fig. 8. Poles of $G_{closed-loop}$ for different UCG values.

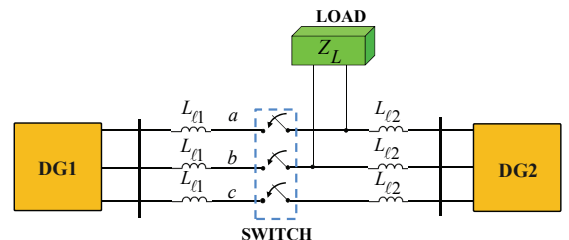


Fig. 9. Test system for simulations and experimental evaluation.

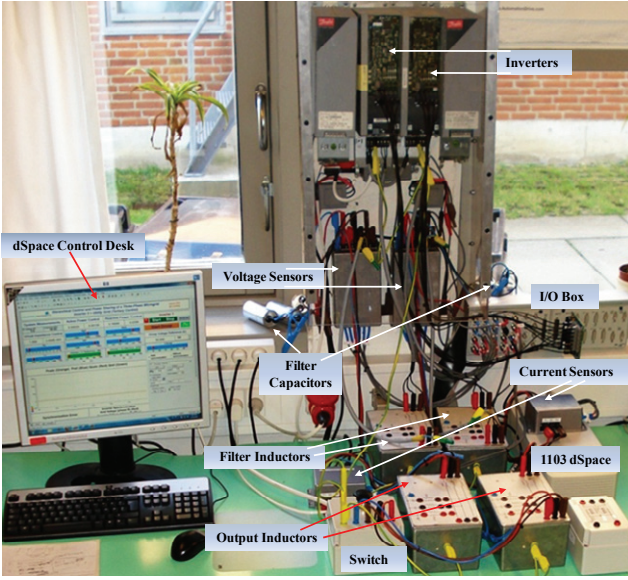


Fig. 10. Experimental setup.

In order to provide a correct comparison, all the control parameters are the same for the simulation and experiment. Although, experiments are performed in real time, in order to make the comparison easier, time scales of the experimental results are changed to match the simulation results. In the experiment, unbalance compensation is activated 0.9sec after the start of data capturing (at $t=5.9$ sec in the used time scale), while in the simulation, compensation is started at $t=6$ sec.

In this paper, "Voltage Unbalance Factor (VUF)" which is defined as follows is considered as the index of unbalance [16]:

$$VUF = \frac{V_{o_{rms}}^-}{V_{o_{rms}}^+} \cdot 100 \quad (33)$$

where $V_{o_{rms}}^-$ and $V_{o_{rms}}^+$ are the rms values of negative and positive sequences of the DG output voltage, respectively. Since, three phases of negative sequence and also positive sequence component are balanced; the value of VUF is independent of the phases used for its calculation.

Simulation and experimental results of DGs VUF are shown in Figs. 11(a) and 11(b), respectively. As seen, VUF values are decreased, significantly, as a result of compensation. These results show the effectiveness of the voltage unbalance compensation. Also, experimental and simulation results are in good agreement.

Considering this fact that $L_{\ell 1} = 2 \cdot L_{\ell 2}$, DG2 VUF should be a little higher. This fact is shown in Fig. 11(a). But, as shown in Fig. 11(b), VUF of DG1 is a little higher than DG2 value, (mainly before compensation activation). It seems that this difference between simulation and experimental results is originated from inverters tolerances.

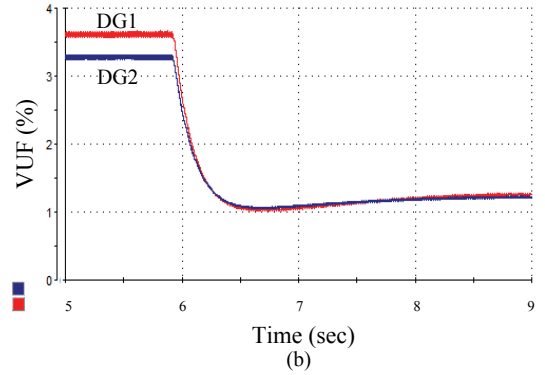
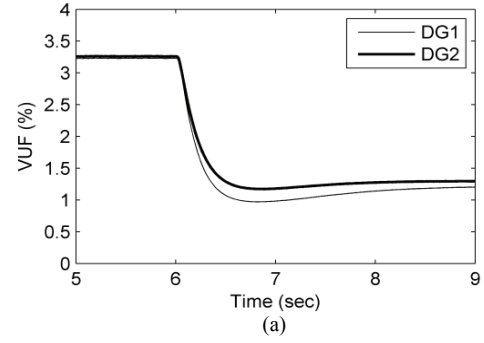


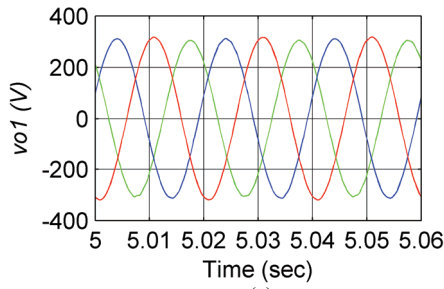
Fig. 11. Voltage unbalance factor- Case 1: (a) Simulation, (b) Experiment.

Also, it can be observed in Fig. 11 that at the beginning of compensation VUF is decreased considerably but it continues with a slight increase. As mentioned before and can also be seen in Fig. 14, compensation of voltage unbalance leads to decrease of Q^- and consequently decrease of the compensation effort. But, due to the time needed by the low pass filter to calculate Q^- , decrease of the compensation effort is slow. Thus, at the beginning of compensation, unbalance is compensated more than the steady state.

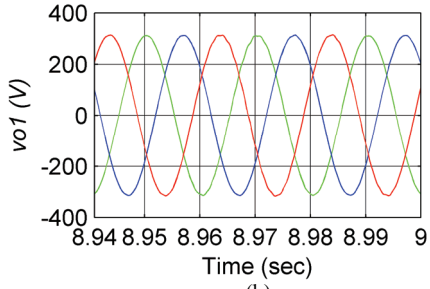
Before- and after-compensation waveforms of DG1 and DG2 three-phase output voltages are depicted in Figs. 12 and 13. These Figs. demonstrate the effectiveness of the proposed compensation method in balancing the DGs output voltages. In all the three-phase waveforms presented in this paper, green, blue and red colors represent phase- a , phase- b , and phase- c , respectively.

Simulation and experimental results of DGs negative sequence reactive power change as a result of compensation are presented in Figs. 14(a) and 14(b), respectively. As expected, Q^- is decreased by compensation. As mentioned before, decrease of Q^- due to compensation helps to share the compensation effort.

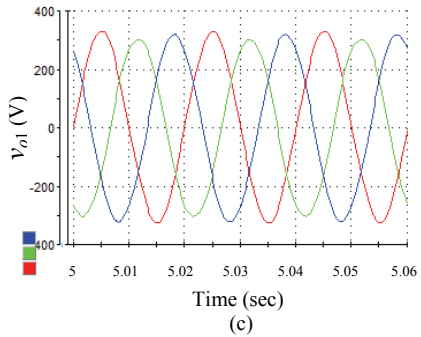
Simulation results of positive sequence reactive and active power sharing between two DGs are shown in Figs. 15(a) and 16(a), respectively. The corresponding experimental results are depicted in Figs. 15(b) and 16(b), respectively. As shown, simulation and experimental results are in good agreement.



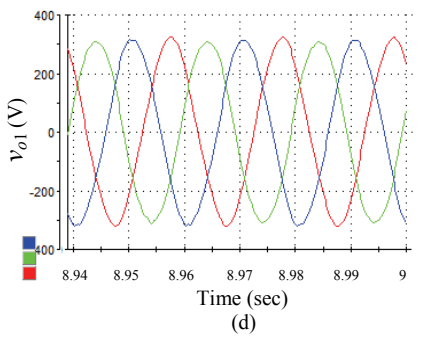
(a)



(b)



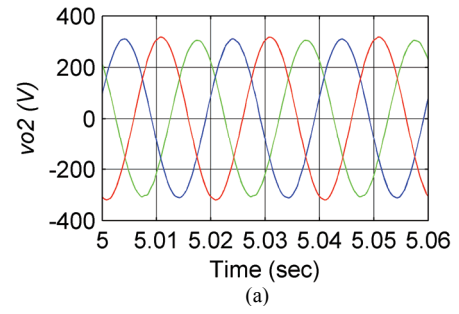
(c)



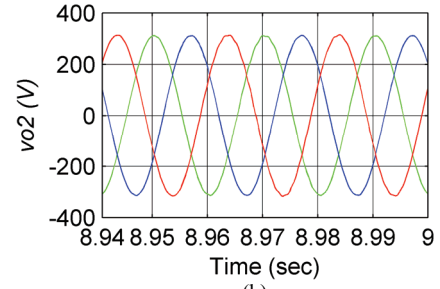
(d)

Fig. 12. DG1 output voltage.

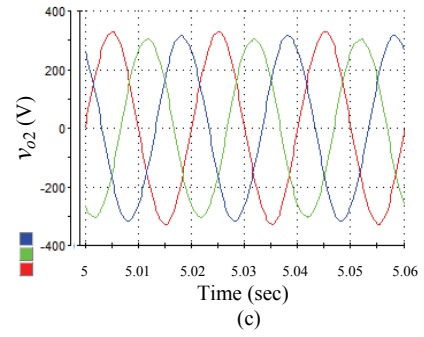
(a) before compensation (Simulation), (b) after compensation (Simulation)
 (c) before compensation (Experiment), (d) after compensation (Experiment)



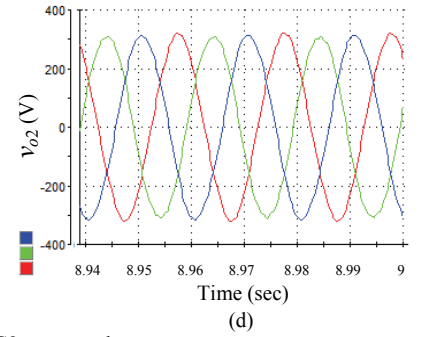
(a)



(b)



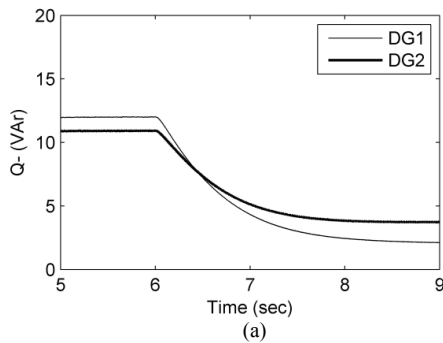
(c)



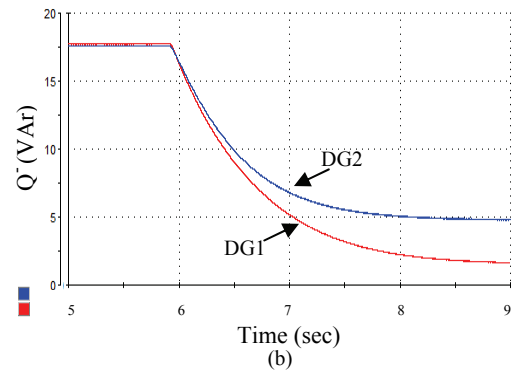
(d)

Fig. 13. DG2 output voltage.

(a) before compensation (Simulation), (b) after compensation (Simulation)
 (c) before compensation (Experiment), (d) after compensation (Experiment)



(a)



(b)

Fig. 14. Negative sequence reactive power- Case 1: (a) Simulation, (b) Experiment.

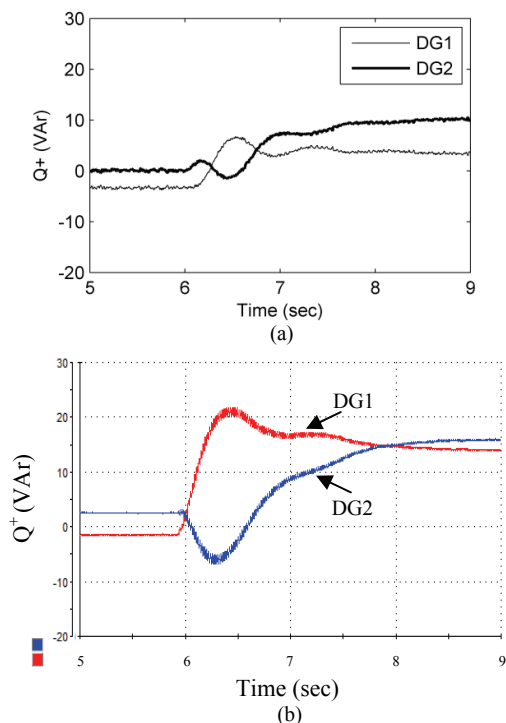


Fig. 15. Positive sequence reactive power- Case 1: (a) Simulation, (b) Experiment.

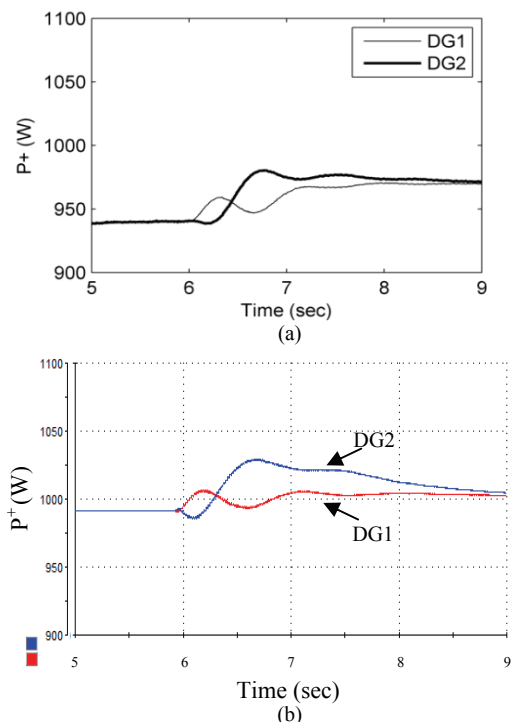


Fig. 16. Positive sequence active power- Case1: (a) Simulation, (b) Experiment.

Since, the unbalanced load is completely resistive, Q^+ values are very small. However, it is clear in Fig. 15 that in spite of asymmetrical distribution lines, reactive power circulating between DGs is effectively limited by Q^+ droop controller. Also, as can be seen in Fig. 16, P^+ is shared well before compensation and after the transient

state caused by compensation activation, the well-sharing is again achieved. These results show the effectiveness of the power control. Also, it can be concluded that the compensation has no negative impact on power sharing.

It is noteworthy that in order to show the effect of compensation clearly, compensation control loop is activated suddenly. However, in practical cases UCG can be increased slowly to avoid the transient behavior observed in Figs. 15 and 16.

Simulation and experimental results of DG1 three phase output current before and after compensation are presented in Fig. 17. The corresponding waveforms of DG2 are shown in Fig. 18. Since, the load is connected between phase- a and phase- b , the current of these phases are approximately the same (green and blue waveforms, respectively) and phase- c current (red waveform) is approximately zero. The unbalance load currents create voltage unbalance, thus, compensation control loop action leads to a slight increase of phase- c current to reduce voltage unbalance. These results also show good resemblance between simulation and experiment.

B. Case 2-Resistive-Inductive Load

In this case, experimental results considering an RL load are presented. As shown in Fig. 19, VUF of the DGs are efficiently decreased as a result of unbalance compensation which starts acting from $t=5.9$ sec. It demonstrates the effectiveness of the proposed compensation method. As expected, FNS reactive power decreases due to compensation as shown in Fig. 20. Experimental results of FPS reactive and active powers are presented in Figs. 21 and 22, respectively. As seen, reactive and active powers are properly shared between DGs in spite of asymmetrical line impedances and the transient behavior created by the compensation activation is quite acceptable.

V.CONCLUSION

A control approach is presented to compensate voltage unbalance in a microgrid. This approach is based on the proper control of DGs interface converter. The design procedure of the proposed control system is discussed in detail. The positive and negative sequence components of the voltage and current were applied to calculate positive sequence active and reactive powers. The positive sequence powers are used by the power controllers to generate the references of the DG output voltage amplitude and phase angle and negative sequence reactive power is applied for the generation of voltage unbalance compensation reference. The proposed method has been validated through simulation and experimental results. The obtained results show that voltage unbalance is well compensated by utilizing this control technique and also the compensation effort is properly shared between the DGs.

In this paper, a linear unbalanced load is considered. As the next step, we are working on the compensation when a nonlinear unbalanced load is supplied by the microgrid.

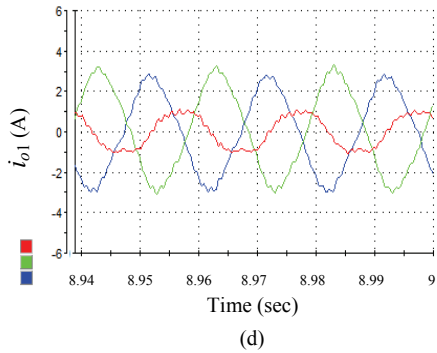
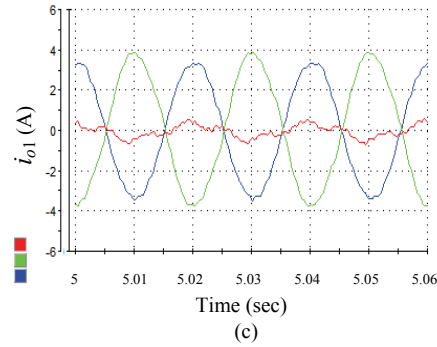
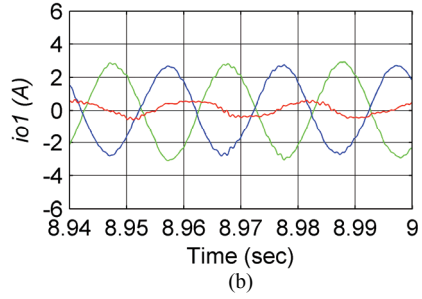
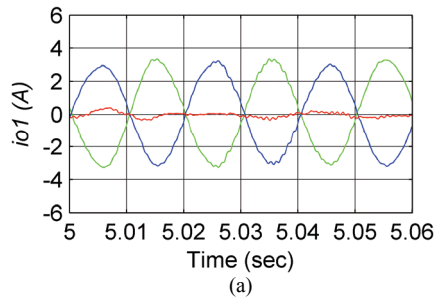


Fig. 17. DG1 output current:
 (a) before compensation (Simulation), (b) after compensation (Simulation)
 (c) before compensation (Experiment), (d) after compensation (Experiment)

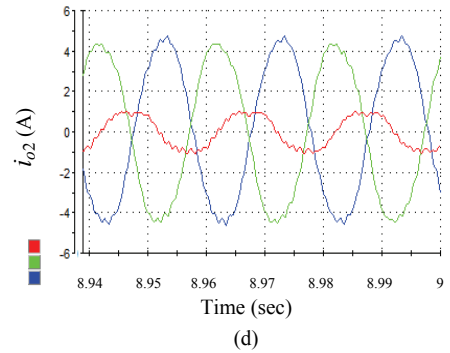
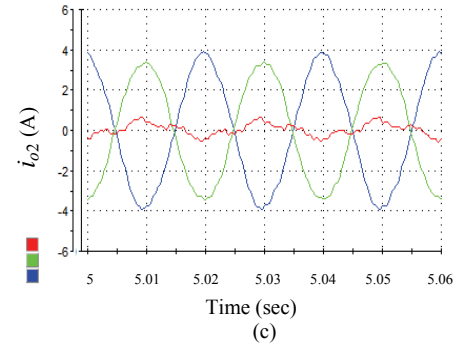
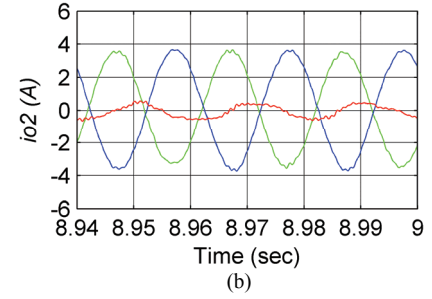
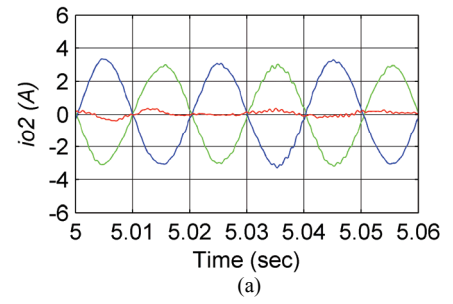


Fig. 18. DG2 output current:
 (a) before compensation (Simulation), (b) after compensation (Simulation)
 (c) before compensation (Experiment), (d) after compensation (Experiment)

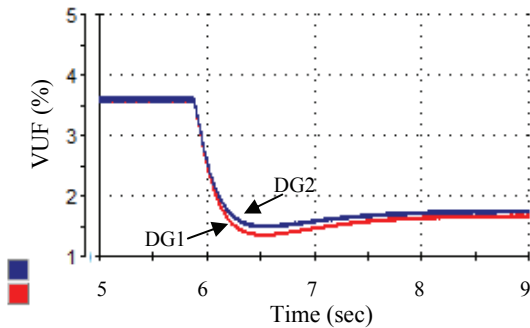


Fig. 19. Experimental result of voltage unbalance factor- Case 2

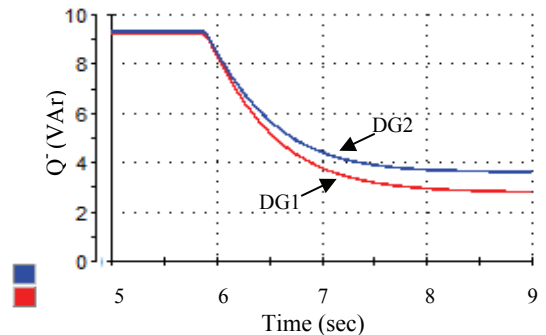


Fig. 20. Experimental result of negative sequence reactive power- Case 2

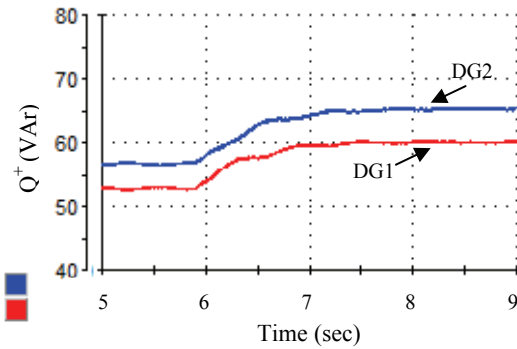


Fig. 21. Experimental result of positive sequence reactive power- Case 2.

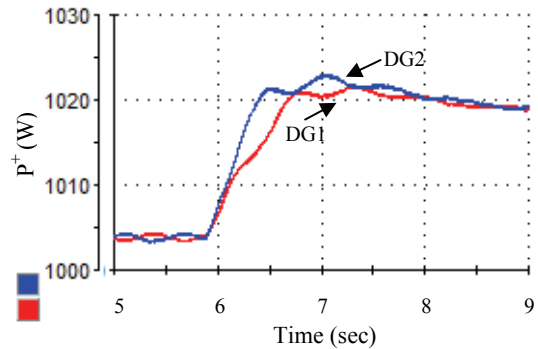


Fig. 22. Experimental result of positive sequence active power- Case 2.

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