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Multilayer control for inverters in parallel operation without signal interconnection

Hua, Ming ; Hu, Haibing ; Xing, Yan ; Guerrero, Josep M.

Multilayer Control for Inverters in Parallel Operation without Interconnection

Ming Hua[1], Haibing Hu[1], Yan Xing[1], Josep M. Guerrero[2]

1. Jiangsu Key Laboratory of New Energy Generation and Power Conversion, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, P.R. China. E-mail: huaming@nuaa.edu.cn

2. Dept. Energy Technology, Aalborg University, DK-9220, Aalborg, Denmark
E-mail: joz@et.aau.dk

Abstract- **A multilayer control is proposed for inverters with wireless parallel operation in this paper. It consists of three layers. The first layer is based on an improved droop method, which shares the active and reactive power in each module by adjusting the phase and amplitude of the output voltage respectively. The second layer is to compensate the droop voltage caused by the droop control and thus improve the load regulation performance of the inverter. The third layer limits the phase deviation between the inverter and the shared ac bus in order to ensure all the paralleled inverters keeping in phase. The operational principle and implementation are analyzed in details. A prototype, configured by two paralleled inverters, is set up. Experimental results verify the validity of the proposed control.**

I.   INTRODUCTION

More and more DC and AC power supply systems requiring large capacity, high reliability, and standard structure are realized by multiple power modules operating in parallel. Many methods for the parallel inverter system have been proposed. In general, these control methods may be categorized as centralized control, distributed control and wireless control [1]-[2]. Wireless control has been caught great attention due to its simplicity in hardware implementation [3]-[13]. The main idea of wireless control is based on droop method, which realizes the parallel operation by regulating the frequency and amplitude references according to the inverter output active and reactive power [14]. However, conventional wireless control has an unstable issue as it may introduce a positive feedback. For example, suppose the output active power from one inverter is larger than that from other inverter while the phase in the first inverter is lagging that in the second ones, under this condition, the system would end in instability if the conventional control is applied. To avoid the possible positive feedback, reference [15] proposed a decoupling control, which decouples both the frequency voltage droops with their voltage and frequency by taking into consideration the line impedance and load. But the decoupling control is complex because it depends on the parameters of lines and loads. The poor transient response and poor hot-swap performance are also the limitations of conventional droop method. What is

more, the main disadvantage is load-dependent external characteristics which causes poor load regulation and is hard to meet the standards [16].

Hierarchical control applied to power dispatching in AC power systems is well known and it has been used extensively for decades [17]. UCTE (Union for the Co-ordination of Transmission of Electricity, Continental Europe) has defined a hierarchical control for large power system, which is supposed to operate over large synchronous machines with high inertias and inductive networks [18]. With help of a hierarchical control, the amplitude and frequency deviations from the nominal values are limited and thus the power quality, system safety and stability are improved.

In this paper, referring to the hierarchical control, the multilayer control for wireless control is proposed and the coordinated control for all the control levels is studied. The dynamic characteristics, stability and reliability of the parallel system are enhanced, and the load regulation and external characteristics are improved as well.

II.   PRINCIPLE OF MULTILAYER CONTROL

Three-phase three-leg inverter is used for this study. The dual closed-loop PI control and space vector modulation are employed to realize stable output voltage for each module, while multilayer control is used for parallel operation. The principle of multilayer control is described as follows:

(1) The first layer is an improved PQ droop method. By the local active and reactive power of the inverter (P and Q), the droop values for given frequency f_r, phase angle and amplitude, Δf_P, $\Delta\theta_P$ and Δu, are obtained. With these fine adjustments of the frequency, initial phase angle and amplitude of voltage reference, the parallel operation can be realized.

(2) In order to compensate for the frequency and amplitude deviations caused by the control in the first layer, a second layer is proposed. Referencing the frequency regulation for large power system and RMS control loop for UPS, the amplitude and frequency of common ac bus are sensed and compared with the ac bus amplitude and frequency reference, U_{busr} and f_{busr}, respectively. The inverters' voltage reference is compensated by error regulator.

(3) To effectively suppress the inrush currents among inverters during the paralleling plugging-in operation and thus enhance the reliability, the third layer control, direct

synchronization control, is employed. The phase angle θ_{acl} of common ac bus voltage is sensed and used as the reference of this layer control. Before connecting the common ac bus, the phase angle of the inverter, θ, is regulated to be closed to θ_{acl} in order to suppress the inrush current at hot plug-in. In steady state, θ is measured in real time. The direct synchronization control is employed, in which θ is regulated rapidly and directly to follow θ_{acl} when the error between θ and θ_{acl} exceeds the limitation (for example 5^0). When the error between θ and θ_{acl} within the range (for example 3^0), the synchronization is regulated by the first layer control and the direct synchronization control is disabled.

A. First layer control

The principle of conventional droop method can be expressed as:

$$\begin{cases} f_{rm} = f_r - \Delta f_P = f_r - k_{Pf} * P \\ U_{refmr} = U_{refm} - \Delta u = U_{refm} - k_Q * Q \\ U_{dref} = U_{refmr} \\ U_{qref} = 0 \end{cases} \quad (1)$$

where U_{refm}, proportional to f_r in U/f mode, is the amplitude of the reference signal. f_{rm} and U_{refmr} are frequency and amplitude of new reference signal regulated by droop method. k_{Pf} and k_Q are the positive proportional coefficients of active-power-frequency and reactive-power-amplitude droops. U_{dref} and U_{qref} are voltages in the d and q axis references frame.

In order to improve the transient behavior, the improved droop method is proposed, which can be expressed as:

$$\begin{cases} f_{rm} = f_r - k_{Pf} * P \\ U_{refmr} = U_{refm} - k_Q * Q \\ \Delta\theta_P = k_{P\theta} * P \\ U_{dref} = U_{refmr} \cos(0^0 - \Delta\theta_P) \\ U_{qref} = U_{refmr} \sin(0^0 - \Delta\theta_P) \end{cases} \quad (2)$$

where $k_{P\theta}$ is the positive proportional coefficient of active-power-phase droop.

Taking two inverters in parallel operation as example, the phase angle of each inverter can be obtained as follows from (2).

$$\text{Inverter1: } \theta_1 = \int 2\pi(f_r - \Delta f_{P1})dt - \Delta\theta_{P1} \quad (3)$$

$$\text{Inverter2: } \theta_2 = \int 2\pi(f_r - \Delta f_{P2})dt - \Delta\theta_{P2} \quad (4)$$

Subtracting (4) from (3), the phase angle difference can be obtained:

$$\begin{aligned} \theta_1 - \theta_2 &= -\int 2\pi(\Delta f_{P1} - \Delta f_{P2})dt - (\Delta\theta_{P1} - \Delta\theta_{P2}) \\ &= 2\pi k_{Pf} \int [0 - (P_1 - P_2)]dt + k_{P\theta}[0 - (P_1 - P_2)] \end{aligned} \quad (5)$$

From (5), it is clear that the phase error, $\theta_1-\theta_2$, can be controlled by active power error (P_1-P_2).

If defining $k_{P\theta}$=0, equation (2) is simplified to conventional droop method. The frequency of the inverter is regulated by active power, and the phase error, $\theta_1-\theta_2$, is controlled using active power error (P_1-P_2) with I controller. Therefore during

steady state the active power of two inverters is equal ($P_1=P_2$) and the two inverters are kept in phase with each other ($\theta_1=\theta_2$). This control method has no steady error.

If defining k_{Pf}=0, the phase angle of the inverter is regulated by active power to realize the synchronization control. And the phase error, $\theta_1-\theta_2$, is controlled using active power error (P_1-P_2) with P controller, which has steady error. Even though the active powers of two inverters are not equal ($P_1 \neq P_2$), the paralleled system can still maintain stable. Compared to the I controller, the P controller has faster transient response. As indicated in expression (2), the performance of power sharing regulation both in steady state and dynamic state is improved.

B. Second layer control

Current sharing inductors, L_{pa}, are connected between the inverters and common ac bus. Because L_{pa} is not included in control loops, it induces the differences between the voltages of common ac bus and that of the inverters. The second layer control is introduced to improve the load regulation. The frequency and amplitude of the common ac bus are sensed and compared with the references and the errors are used to regulate the references of the inverters to correct the output voltage frequency and amplitude. The second layer control is shown in Fig. 1. f_{rm} and U_{refmr} are the frequency and amplitude references of the inverter. $f_{rm}+f_c$ and $U_{refmr}+U_{mc}$ are the regulated frequency and amplitude references of the inverter by the secondary control. f_c and U_{mc} are the compensation values of frequency and amplitude respectively.

As shown in Fig. 1, the frequency and amplitude deviate from the rated values when the active and reactive power increases. The control algorithm can be obtained as follows:

$$\begin{cases} f_{rm} = f_r - k_{Pf} * P + \underbrace{G_f * (f_{busr} - f_{buss})}_{f_c} \\ U_{refmr} = U_{refm} - k_Q * Q + \underbrace{G_u * (U_{busr} - U_{buss})}_{U_{mc}} \\ \Delta\theta_P = k_{P\theta} * P \\ U_{dref} = U_{refmr} \cos(0^0 - \Delta\theta_P) \\ U_{qref} = U_{refmr} \sin(0^0 - \Delta\theta_P) \end{cases} \quad (6)$$

where f_{busr} and U_{busr} are the frequency and amplitude references (rated values) of common ac bus, and f_{buss} and U_{buss} are the sensed frequency and amplitude of common ac bus. G_f and G_u are the frequency and amplitude compensators.
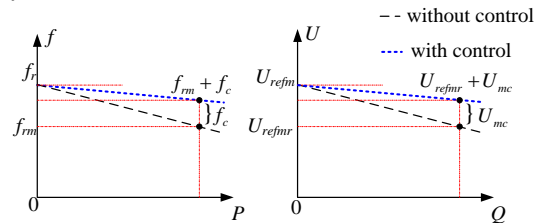

Fig. 1 Compensation principle of the secondary control

C. Third layer control

According to expression (1), only under the conditions where the differences of the amplitude and frequency are small, the approximation of the regulation among the active power, frequency, reactive power and amplitude are reasonable. On the other hand, during dynamic response such as hot swap, the circulating current could be high because of the slow power calculation using the conventional droop method. As a result, the phase and amplitude of the inverters should be controlled to be close to each other before paralleling. And the errors between each module should be regulated and limited within a small range during dynamic response. Simultaneously, the potential positive feedback of conventional droop control would cause out-of-phase, resulting in system unstable.

With the third layer control, which can be called direct synchronization control, the phase angles of each inverter, θ, are regulated to be close to the phase angle of common ac bus (θ_{acl}) so that the inrush current can be suppressed during hot plug-in. And the errors between θ and θ_{acl}, $\Delta\theta_s$, can be controlled within a setting range when the inverters operate in steady state in order to avoid losing synchronism. $\Delta\theta_s$ can be expressed as following:

$$\Delta\theta_s = \theta_{acl} - \theta \tag{7}$$

A positive $\Delta\theta_s$ means the phase angle of the inverter lagging the common ac bus and a negative $\Delta\theta_s$ means leading.

In steady state, $|\Delta\theta_s|$ is judged and the following expression is achieved:

$$SC\_S = \begin{cases} 1 & |\Delta\theta_s| \geq SC\_\theta_{ul} \\ 1\ or\ 0 & SC\_\theta_{ll} \leq |\Delta\theta_s| < SC\_\theta_{ul} \\ 0 & |\Delta\theta_s| < SC\_\theta_{ll} \end{cases} \tag{8}$$

where SC_θ_{ul} and SC_θ_{ll} are the upper and lower limits of the errors $|\Delta\theta_s|$, respectively. SC_S is the flag of starting the third layer control using hysteresis logic, where 1 (0) means starting (stopping) the third layer and 1or0 means intermediate state. 1or0 represents that SC_S remains the same value as previous. For example, if SC_S is equal to 1 in last period, it remains 1 in present period. The logic diagram is shown in Fig. 2.

With multilayer control, the phase angle θ_m of the inverter in one initial given frequency ($1/f_r$) can be expressed by:

$$\begin{aligned} \theta_m &= \int_0^{1/f_r} 2\pi f_m * dt \\ &= \int_0^{1/f_r} 2\pi(f_r + f_c - k_{Pf} * P) * dt - \\ &\quad k_{P\theta} * P + SC\_S * k_{sc} * \Delta\theta_s \end{aligned} \tag{9}$$

where k_{sc} is the positive proportional coefficient of error regulation, f_m is the output frequency of the inverter with multilayer control.

From (9), the frequency regulated by multilayer control can be obtained as

$$\begin{aligned} f_m &= f_r + f_c - k_{Pf} * P - \\ &\quad \frac{k_{P\theta} * P - SC\_S * k_{sc} * \Delta\theta_s}{2\pi} * f_r \end{aligned} \tag{10}$$
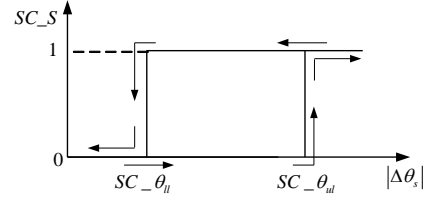

Fig. 2 Logic diagram of the third control

III. COORDINATED CONTROL OF ALL LEVELS

In a practical system, the amplitude error of references between each module is small, which largely depends on the parameter variations of devices. But the phase error is random and would be large without proper regulation. Since the control of the phase is dominant in all three control layers, the synchronization control of phase angle is the major purpose of coordinated control of all the levels.

In the first layer control, the phase is regulated slightly and the regulation speed is slow so that the frequency fluctuation is small, which could ensure that the parallel system operates smoothly. In third layer control, the phase is regulated directly and heavily so that the regulation speed is high, which results in high frequency fluctuations. The second layer control is of the outer control loop and the time-constant is large so that the regulation speed is slow. The good steady state performance of the second layer control is desired, while the dynamic performance is not so important in this layer. From above analysis, the first layer control can coexist with the second layer and they complement each other. And the activation of the third layer control depends on $\Delta\theta_s$. As a result, the coordinated control relies on values of SC_θ_{ul} and SC_θ_{ll} and two aspects should be taken into consideration: (1) The third layer control should not start when the inverter operates independently, (2) The third layer control should start in terms of the phase difference when N inverters operate in parallel with M loads (M≤N).

The PI controller in dq rotation frame is applied to control the inverter. In this manner, the model of the inverter can be viewed as a DC system and equivalent output impedance is 0. So, theoretically there is no difference in phase between output voltage and the references of the inverter. However, the current sharing inductors L_{pa} are connected between the inverter and common ac bus, which causes the phase shift $\Delta\theta_{Lpa}$ between the inverter's output voltage and common ac bus voltage.

Assuming the balanced three-phase loads, the equivalent circuit of N inverter modules in parallel with M loads is shown in Fig. 3. $U_{ann}\angle\theta_n$ is the phase-a output voltage of inverter n. $r_{Lpa}+sL_{pa}$ is the sum of output impedance and lines impedance and inductive impedance of current sharing inductors. Z is the load impedance. $U_{ao}\angle 0^0$ is the phase-a voltage of the common ac bus.
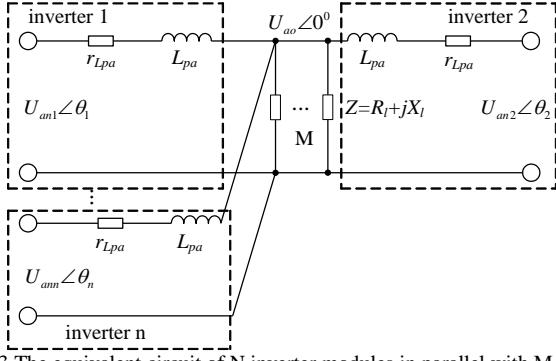
Fig. 3 The equivalent circuit of N inverter modules in parallel with M loads

(1) The inverter operating individually

From Fig. 3, assuming $r_{Lpa}=0$, $\Delta\theta_{Lpa}$ can be expressed as:

$$\Delta\theta_{Lpa} = \arctan\frac{R_l\omega L_{pa}}{R_l^2 + \omega L_{pa}*X_l + X_l^2} \quad (11)$$

When operating individually, the third layer control is disabled. So,

$$SC\_\theta_{ll} > \max(\Delta\theta_{Lpa}) \quad (12)$$

And the requirement should be satisfied simultaneously:

$$SC\_\theta_{ll} < SC\_\theta_{ul} \quad (13)$$

(2) N inverter modules in parallel with M loads (M≤N)

Under this condition, $\Delta\theta_{Lpa}$ can be expressed as (detailed proof is given in appendix I):

$$\Delta\theta_{Lpa} = \arctan\frac{\dfrac{M}{N}R_l\omega L_{pa}}{R_l^2 + X_l^2 + \dfrac{M}{N}\omega L_{pa}*X_l} \quad (14)$$

The third layer control is inactive when the parallel system operates in steady state. So,

$$SC\_\theta_{ul} > SC\_\theta_{ll} > \max(\Delta\theta_{Lpa}) \quad (15)$$

With coordinated control, each level can complement the other well and the stability and reliability of the parallel system are enhanced.

According to the analysis above, the control diagram of the inverter with multilayer control is shown in Fig. 4.
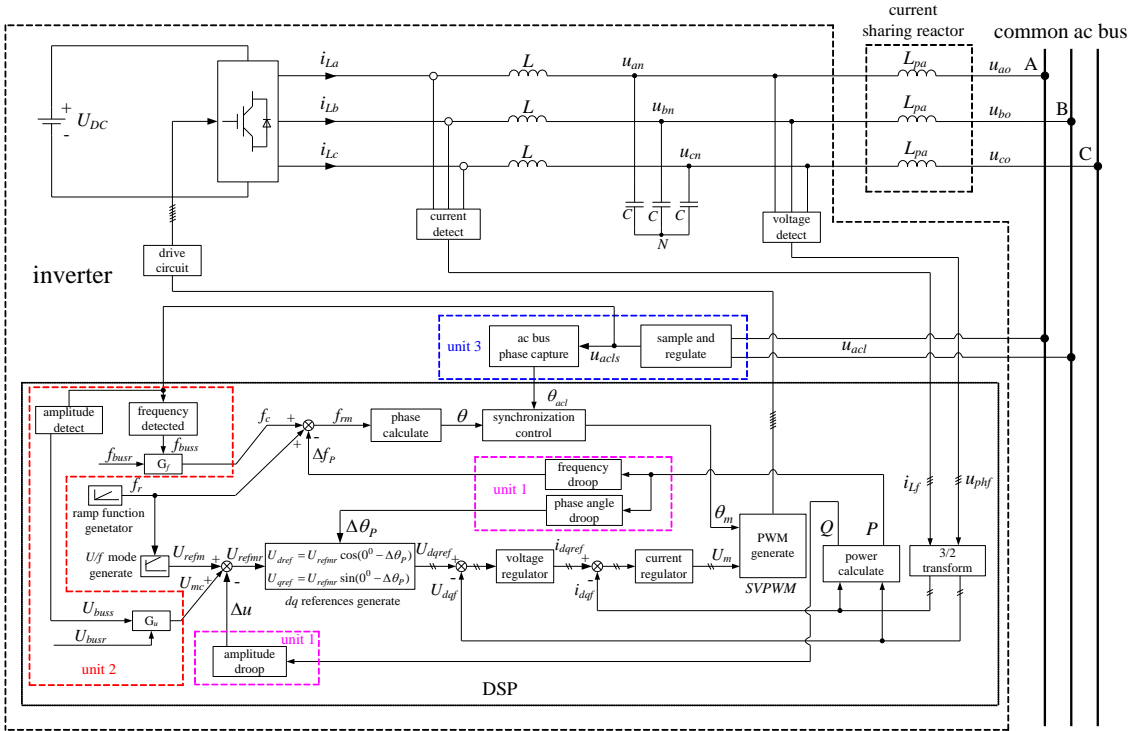

Fig. 4 The control diagram

In Fig. 4, unit 1, unit 2 and unit 3 are the first layer, second layer and third layer respectively. Unit 1 contains two parts which regulate the references with active power P and reactive power Q of the inverter according to (2). The regulated frequency reference f_{rm} and regulated voltage reference of dq axis U_{dqref} are achieved. The amplitude U_m for SVPWM is obtained after U_{dqref} being regulated by voltage and current controllers. The phase θ_m for SVPWM is achieved after f_{rm} getting through the phase angle calculation unit and synchronization control unit. And the drive signals

by SVPWM with U_m and θ_m are generated to drive the switches and the parallel control is realized. As for unit 2, u_{acls} is sensed. The frequency and amplitude of common ac bus are obtained. According to (6), the output of parallel system is compensated and the load regulation is improved. As for unit 3, θ_{acl} of common ac bus is achieved by regulation circuit and phase angle captured circuit. Before plugging into common ac bus, the phase angle of the inverter, θ, is regulated to be closed to θ_{acl} in order to suppress the inrush current during hot plug-in. In steady state, θ is detected in real

time. The direct synchronization control is employed and θ is regulated rapidly and directly to follow θ_{acl} when the error between θ and θ_{acl} exceeds the limitation. If the error between θ and θ_{acl} within the range, the synchronization regulation is based on the first layer control and the direct synchronization control is inactive.

In addition, the parallel system mainly feed the motor load and U/f control is adopted in order to avoid the current surge. And the given frequency f_r increases smoothly from 0 to its rated value (50Hz).

IV.   EXPERIMENTAL RESULTS

A prototype system with two DSP (TMS320F2812) controlled inverters in parallel is built for train's auxiliary supply. The configuration and control is shown in Fig. 4. The DC bus voltage is 600V and rated output voltage is 380V/50Hz. The designed capacity is 35kVA and switch frequency is 6kHz. The value of L is 0.6mH and C is 50μF while L_{pa} is 0.8mH. The resistive load is used in the experiment.

In Fig. 5, Fig. 6 and Fig. 7, u_{an1} u_{an2} are the phase a voltages of inverter 1 and inverter 2, and i_{La1} and i_{La2} are the phase a inductor currents. θ_{1out} and θ_{2out} are the representation signals of phase angle of inverter 1 and inverter 2. And the rising edge represents that the phase angle is crossing 0^0.

The result of transient performance under hot swapping is shown in Fig. 5. As shown in Fig. 5, the parallel system gets into steady state after the transient regulation with small inrush current and voltage fluctuation. The result shows a good performance of parallel control during hot plug-in.

The results of parallel operation with stepping load are shown in Fig. 6. Fig. 6 (a) shows load step up from 0 to 16kW while Fig.6 (b) shows the load step down from 16kW to no load. The results indicate that the proposed parallel control has good dynamic performance.

The steady-state parallel operation results are given in Fig. 7. Fig.7 (a) shows the steady state waveforms at 37kW. Fig. 7 (b) shows the phase error between two inverters in steady state. The results shows that the proposed parallel control has good performance at steady state and the phase error is smaller than 0.36^0 (± 20μs).

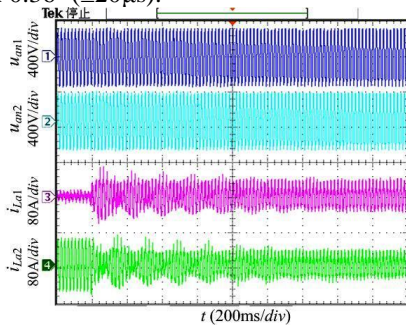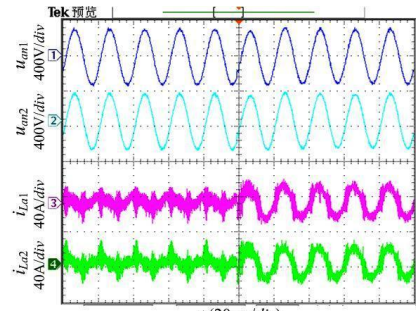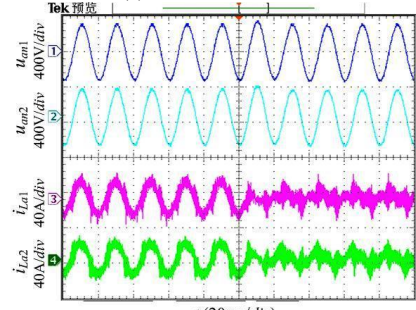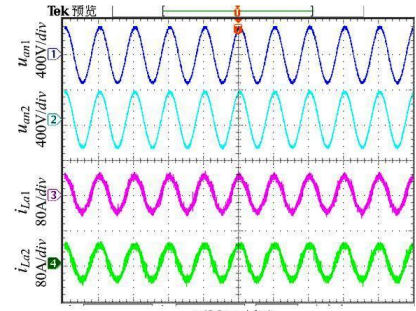Fig. 5 Experimental result with hot-plug in
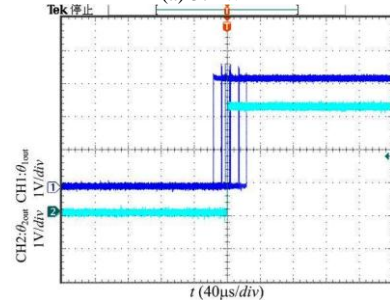

(a) No load to 16kW

(b) 16kW to no load
Fig. 6 Experimental result with stepping load

(a) 37kW

(b) Phase error between two inverters
Fig. 7 Experimental result in steady state

V.   CONCLUSION

A multilayer control for inverters in parallel operation without interconnection is proposed and analysis and implementation are given. The first layer control is based on the improved droop method, which regulates the frequency and phase angle of the inverter simultaneously. With the help of the first layer control, the dynamic and steady state performances are enhanced. The second layer control compensates the output voltage deviations, which are caused by droop method, through sensing the frequency and

amplitude of common ac bus. With the third layer control, the phase of common ac bus is sensed and the phase of inverter is regulated before hot-plug into the common ac bus and during dynamic response. As a result, the inrush currents are suppressed and losing synchronism is avoided.

APPENDIX I

Assuming r_{Lpa} is equal to 0, it can be achieved as follows from Fig. 3:

$$\frac{U_{an1}\angle\theta_1 - U_{ao}\angle 0}{j\omega L_{pa}} + \cdots + \frac{U_{ann}\angle\theta_n - U_{ao}\angle 0}{j\omega L_{pa}} = \frac{MU_{ao}\angle 0}{Z} \quad (A1)$$

Namely

$$\frac{U_{an1}\angle\theta_1 + \cdots + U_{ann}\angle\theta_n}{j\omega L_{pa}} = \frac{MU_{ao}\angle 0}{Z} + \frac{NU_{ao}\angle 0}{j\omega L_{pa}} \quad (A2)$$

The PI controller in dq rotation frame is applied to control the inverter so that the model of the inverter can be viewed as a DC system. It's easy to control voltage amplitude of each inverter equal to the other. So, assuming that amplitudes of voltages of all parallel inverters are equal ($U_{an1}=U_{an2}=\ldots=U_{ann}$) in steady state. By the first layer control, all the parallel inverters keep in phase with each other ($\theta_1=\theta_2=\ldots=\theta_n$). According to above, (A2) is approximately equivalent to

$$\frac{NU_{an1}\angle\theta_1}{j\omega L_{pa}} = \frac{MU_{ao}\angle 0}{Z} + \frac{NU_{ao}\angle 0}{j\omega L_{pa}} \quad (A3)$$

So

$$U_{an1}\angle\theta_1 = U_{ao}\angle 0 (1 + \frac{j\omega L_{pa}M}{NZ}) \quad (A4)$$

With substituting R_l+jX_l for Z, equation (A4) can be expressed as:

$$U_{an1}\angle\theta_1 = U_{ao}\angle 0 \frac{NR_l + j(NX_l + \omega L_{pa}M)}{NR_l + jNX_l} \quad (A5)$$

From equation (A5), it can be achieved:

$$\Delta\theta_{Lpa} = |\theta_1| = \arctan\frac{\frac{M}{N}R_l\omega L_{pa}}{R_l^2 + X_l^2 + \frac{M}{N}\omega L_{pa}*X_l} \quad (A6)$$

The maximal value of Equation (A6) is related to the number of parallel inverters and loads and the character of loads.

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