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A Centralized Control Architecture for Harmonic Voltage Suppression in Islanded Microgrids

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***Abstract*-This paper proposes a centralized control architecture for harmonic voltage suppression in islanded microgrids. The centralized selective harmonic compensator is developed in addition to the autonomous nonlinear load sharing loop in local controllers of inverter-interfaced Distributed Energy Resource (DER) units. Thus the harmonic voltage distortion caused by the mismatch between the harmonic conductance and characteristic impedance of distribution feeder can be reduced. Furthermore, to overcome the constraint on transmitting harmonic signals by a low-bandwidth communication line, a Park transformation aided signal modulation method is integrated to the centralized control architecture. The operation principle and case studies based on simulations are presented in this paper and validate the proposed control architecture.**

I. INTRODUCTION

The microgrid, among other envisaged grid architectures, is emerging as attractive way to accommodate the increasingly penetrated Distributed Energy Resources (DER). Microgrids interconnect several customers and multiple DER units, and can form intentional and non-intentional energetic islands in distribution network, thereby ensuring high efficiency and security of electricity services [1].

Switch-mode power converters are widely utilized to provide efficient and flexible interfaces for DER units and electric loads, thanks to the emerging power electronics technology. However, on the other hand, harmonic pollution produced by electronics equipments may degrade the power quality of distribution systems [2]. Moreover, during the intentional and non-intentional islanding operation modes, microgrids may become much weaker and more sensitive to harmonic disturbances. In addition, due to the increased use of LCL filter for grid-connected converters, harmonic resonance that results from those shunt-connected capacitors in LCL filters, capacitive loads and power factor correction (PFC) capacitors also becomes a power quality challenge for power system operations [3]. To preserve a sinusoidal power system voltage, IEEE Std. 519 recommended individual and total harmonic distortions limits on the system voltage [4].

Inverter-interfaced DER units are generally deemed to be able to provide the harmonic filtering function as an ancillary service [5]. To ensure the microgrid operates properly, it is important to share harmonic filtering burdens among multiple DER interface inverters. In [6]-[8], a virtual impedance concept was proposed for sharing nonlinear loads among multiple parallel-connected inverters. The main drawback of this scheme is the harmonic voltage distortion at the output of interface inverter is inevitable due to the virtual impedance loop. Secondary harmonic voltage control is therefore needed to reduce the harmonic distortions [9]. Recently, the voltage-detection active filter method has been implemented in an inverter-interfaced DER unit for nonlinear load sharing in islanded microgrids [10]. A droop relationship between the total harmonic VAR and harmonic conductance is designed to share nonlinear loads. Compared with the virtual impedance schemes, this method effectively damps harmonic voltage distortions at the outputs of interface inverters. Moreover, only a high bandwidth current control loop is needed in this method which simplifies the inner voltage and current control loop design. However, the performance of the method is deteriorated due to the so-called 'whack-a-mole' effect [11]. Harmonic voltages are magnified on other buses even though the output harmonic voltages of interface inverters have been reduced in this phenomenon. This is because of the mismatch between the harmonic conductance and characteristic impedance of distribution feeder. In view of this, a discrete conductance tuning method for selected harmonic frequency component was developed in [12]. But it is intended for single active filter applications. Hence, it is essential to develop proper control technique for multiple DER units that can alleviate the 'whack-a-mole' effect.

In this paper, a centralized control architecture enabled by low-bandwidth communication technique is proposed. A centralized selective harmonic compensator is developed in addition to the voltage-detection based nonlinear load sharing loop in local control systems of DER units. Harmonic voltage distortions caused by the 'whack-a-mole' problem can be effectively suppressed. Moreover it is known that transmitting signals at harmonic frequencies is subject to the constraint imposed by low communication bandwidth. To overcome this limit, the Park transformation is used to transform the content of transferred harmonic signals from time domain to constant vectors in the frequency domain. The operation principle and case studies based on computer simulations are presented in this paper.

II. OPERATION PRINCIPLE

Fig. 1 illustrates a simplified one-line diagram of a three-phase AC microgrid with multiple DER units and the proposed centralized current control architecture. The control architecture consists of two subsystems for harmonic voltage

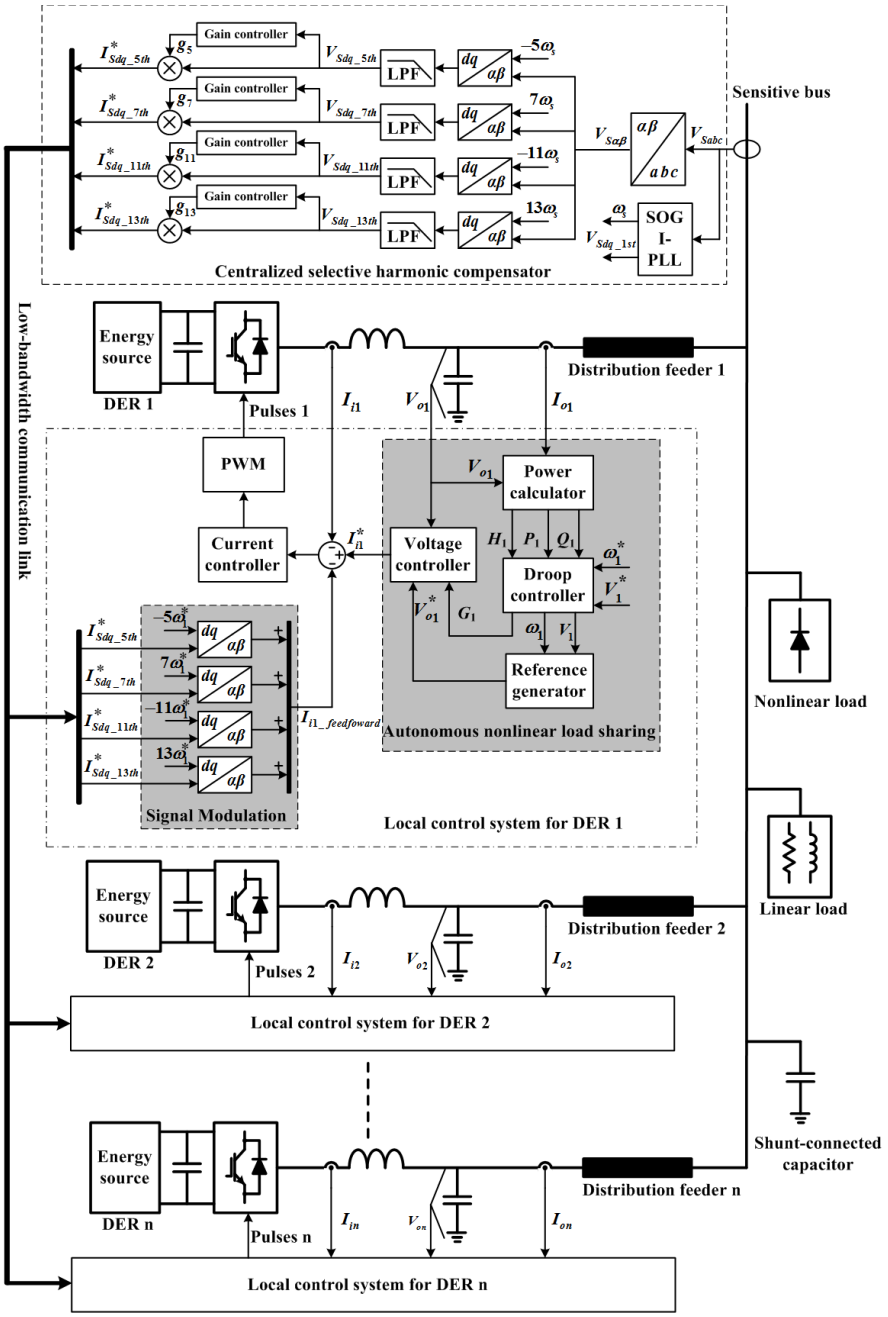

Fig. 1. A simplified one-line diagram of a three-phase AC microgrid with multiple DER units and the proposed centralized control architecture.

suppression, including autonomous nonlinear load sharing loop in the local control system of interface inverter, and a centralized selective harmonic compensator for the sensitive bus. The low-bandwidth communication system is used to link these two control subsystems. Because of the distribution of shunt-connected capacitors along the distribution feeders or large capacitive loads, it is possible to observe a 'whack-a-mole' phenomenon in this islanded microgrid. Hence, the common load bus here is assumed as the sensitive bus for the sake of simplicity, as shown in Fig. 1.

A. Low-Bandwidth Communication

It is well known that limited communication bandwidth of power system communication technique imposes constraint on regulating system voltage waveforms in a centralized way. To overcome this constraint, a Park transformation aided signal modulation/demodulation method is developed, as shown in Fig. 2. With the help of the Park transformation and low-pass filters (LPFs), the contents of harmonic frequency signals on the transmitter side (centralized harmonic compensator) are transformed from time domain information

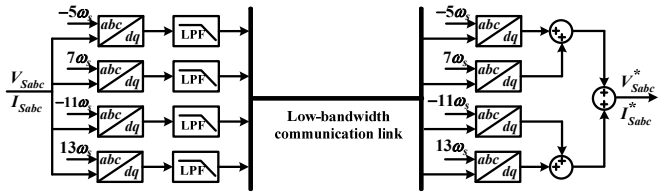

Fig. 2. The Park transformation aided signal modulation/demodulation method in a low-bandwidth communication link.

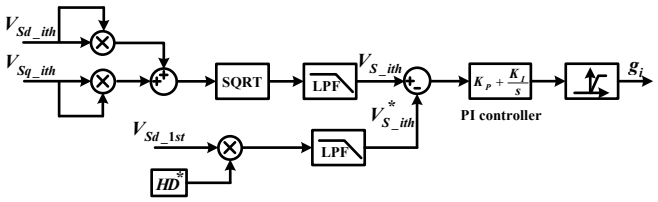

Fig. 3. The internal structure of the gain controller for tuning harmonic conductance.

to constant vectors in multiple rotating reference frames. After being transmitted by the low-bandwidth communication link, the messages in the form of constant vectors are transformed back to harmonic frequency signals on the receiver side (local controllers of DER units).

$$\begin{pmatrix} l_d \\ l_q \\ l_0 \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{pmatrix} \begin{pmatrix} l_a \\ l_b \\ l_c \end{pmatrix} \quad (1)$$

$$\begin{pmatrix} l_a \\ l_b \\ l_c \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos(\theta) & \sin(\theta) & \frac{\sqrt{2}}{2} \\ \cos(\theta-\frac{2\pi}{3}) & \sin(\theta-\frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \\ \cos(\theta+\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \end{pmatrix} \begin{pmatrix} l_d \\ l_q \\ l_0 \end{pmatrix} \quad (2)$$

where l is a general variable to denote the current variable i or voltage v.

Since phase angles of the transmitted signals are needed in using Park transformation, it is essential in this method to keep the phase synchronization between the transmitter side (sensitive bus) and the receiver side (outputs of DER units). This requirement can easily be achieved using Phase-Locked Loop (PLL) technique on the transmitter side, because the system frequency is regulated by DER units in islanded microgrids. The Second Order Generalized Integrator (SOGI) based PLL method is adopted in this paper to remove the influence of harmonic voltage distortion [13].

B. Centralized Selective Harmonic Compensator

Since several different types of loads are connected with the common load bus and the variations of those loads are generally stochastic, it is hard to suppress harmonic voltages by extracting the harmonic currents generated from nonlinear loads. Hence, the voltage-detection based active filter scheme is adopted in the centralized harmonic compensator.

As mentioned above, the Park transformation aided signal modulation/demodulation scheme facilitates communication of the harmonic signals in a selective way. Consequently, selective harmonic compensation rather than global harmonic compensation scheme is required in the centralized controller. Thus, in the voltage-detection based active filter method, both selective harmonic signals extraction and demodulation can be achieved at the same time by using multiple rotating reference frames and low-pass filters, as shown in Fig. 1. Moreover, another superiority of using selective harmonic compensation is the harmonic conductance for each harmonic voltage of interest can be tuned, respectively [12].

Fig. 3 shows the internal structure of the gain controller for tuning harmonic conductance. The constant HD^* represent the allowable individual voltage distortion limit for the selected harmonic voltages relative to the fundamental voltage of the sensitive bus. The extracted ith (i=5, 7, 11, 13) harmonic voltage are compared with the allowable distortion limits, and then the error are passed through a PI regulator, producing automatically the needed harmonic conductance g_i for the ith harmonic voltage. The harmonic conductance g_i should be larger than zero for the sake of control loop stability, thus a limiter is introduced at the output of PI regulator. It is noted that the use of LPF here does not affect the performance of the whole control system, since the delay brought by the LPF could be omitted compared with the delay in low-bandwidth communication system.

C. Autonomous Nonlinear Load Sharing

In the local control system of DER interface inverter, the droop relationship between the output harmonic var (H_n) and the harmonic conductance (G_n) is adopted for harmonic load sharing among multiple interface inverters [10]. The slope of the G_n - H_n droop characteristic is determined by the voltage total harmonic distortion (THD) and the available VA capacity of the DER units for harmonic filtering [14]. It is worth to note that the output LC filter resonance in the inverter also limits the maximum harmonic conductance G_n. Detailed analysis of the interactions between the design of harmonic conductance and the resonance of output LC filter will be presented in future research work.

III. MICROGRID WITH SHORT DISTRIBUTION FEEDER

A simplified, low-voltage (400V) three-phase AC microgrid that consists of two inverter-interfaced DER units is built in simulations. Fig. 4 shows the one-line diagram of the microgrid. Table I lists the simulation parameters. An aggregated capacitor (C_S = 660 μF) that could represent for the capacitors in the LCL filters of photovoltaic (PV) inverters, and household capacitive loads [3]. In addition, one more inductor ($L_{g1,\,2}$ = 400 μH) is introduced at the output of

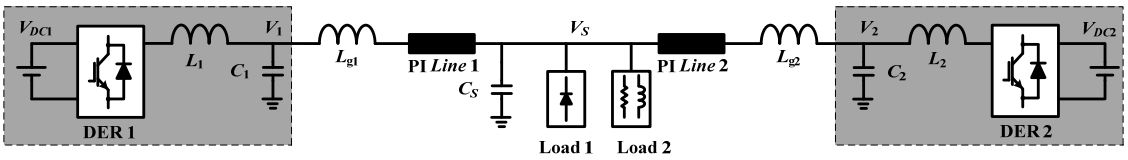

Fig. 4. The one-line diagram of microgrid including a short distribution feeder (2 km) and an aggregated capacitor.

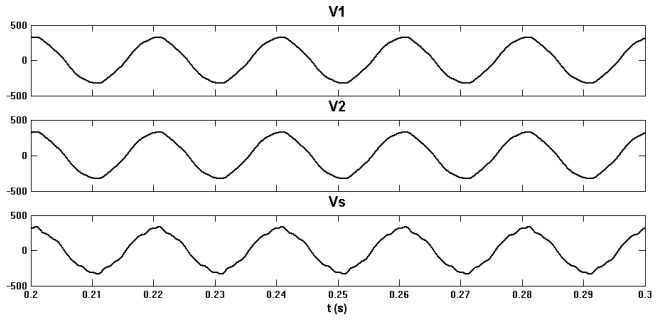

Fig. 5. The voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) without the centralized control architecture in the short distribution feeder case.

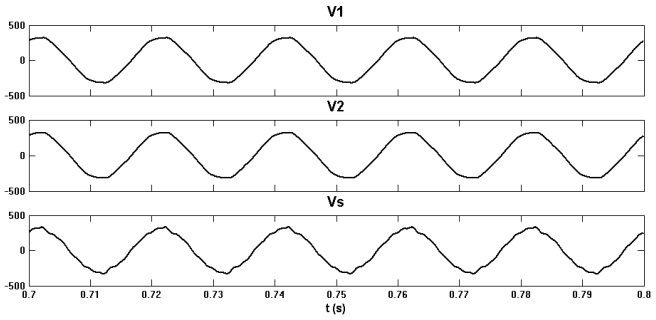

Fig. 7. The voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) with the centralized control architecture in the short distribution feeder case.

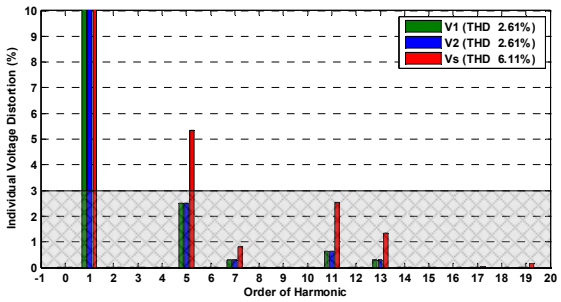

Fig. 6. The harmonic spectrums of voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) without the centralized control architecture in the short distribution feeder case.

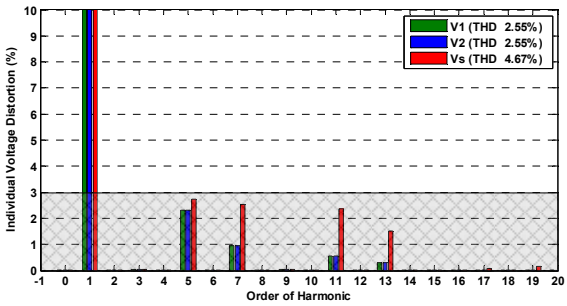

Fig. 8. The harmonic spectrums of voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) with the centralized control architecture in the short distribution feeder case.

interface inverter to form an LCL type filter, so as to test the influence of grid-side filter . The two inverters are uniformly connected with the common load bus by 1 km, 1 kV PI Section line in simulations.

A. No Centralized Control Architecture

Fig. 5 shows the voltage waveforms for the common load bus and the outputs of DER interface inverters. Harmonic spectrums of those voltage waveforms are shown in Fig. 6. In this test, only the autonomous nonlinear load sharing controller is applied [10]. The harmonic voltages at the outputs of interface inverters are effectively suppressed, whereas the fifth harmonic voltage on the sensitive bus is much higher than the individual voltage distortion limit (shaded area, 3%) defined in IEEE Std. 519 [4].

B. With Centralized Control Architecture

Fig. 7 shows the voltage waveforms with the centralized control architecture. It is difficult to see much improvement on the voltage waveform of common load bus compared with

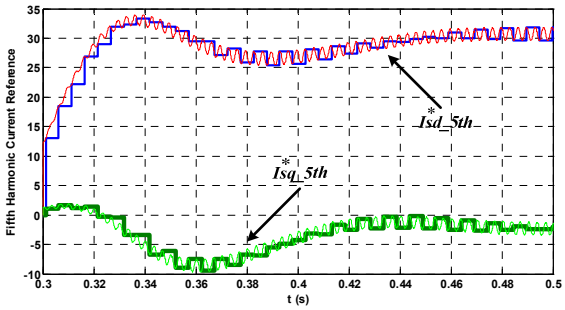

Fig. 9. The effect of communication delay on transmitting the fifth harmonic current reference.

the Fig. 5. This is because the seventh harmonic voltage is slightly increased when the fifth harmonic voltage is reduced. However, it can be clearly seen from the harmonic spectrum analysis that all the harmonic voltages of interest are reduced below the recommended individual voltage distortion limits

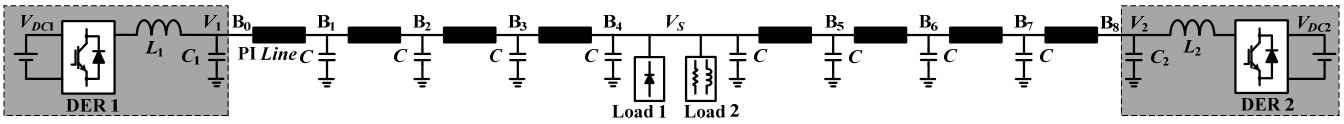

Fig. 10. The one-line diagram of microgrid including a long distribution feeder (8 km) and multiple uniformly distributed capacitors.

TABLE I
MAIN PARAMETERS OF ISLANDED MICROGRIDS

Equipments	Parameters	
DER inverters (DER 1 and DER 2)	Nominal frequency	50 Hz
	Nominal voltage	400 V
	Nominal power	50 kVA
	Filter inductance (L_1, L_2)	800 μH
	Filter capacitance (C_1, C_2)	47 μF
	DC voltage (V_{DC1}, V_{DC2})	800 V
Distribution feeders (1 kV PI line)	Series-connected inductance	230 μH/km
	Series-connected resistance	0.206 Ω/km
	Shunt-connected capacitance	0.98 μF/km
Three-phase diode rectifier load (Load 1)	AC-inductance	200 μH
	DC-capacitance	2200 μF
	DC-resistance	12 Ω
Inductive load (Load 2)	Resistance	20 Ω
	Inductance	20 mH
Low-bandwidth communication	Communication delay	5 ms

(shaded area 3%) after using centralized selective harmonic compensator, as shown in Fig. 8. Moreover, the THD of those three voltages are also lower than the recommended voltage THD limits (5%) in [4].

C. Emulation of Low-Bandwidth Communication

A sample and hold block with 5 ms delay is adopted to emulate the low-bandwidth communication system. Fig. 9 illustrates the communication delay on transmitting the fifth harmonic current feedforward reference from the centralized selective harmonic compensator to the local control system of interface inverters. The second-order butterworth low-pass filters with 10 Hz cut-off frequency are applied with multiple rotating reference frames to transform the harmonic signals into constant vectors.

IV. MICROGRID WITH LONG DISTRIBUTION FEEDER

Fig. 10 illustrates the microgrid structure in this study case. A long distribution feeder that consists of 8×1 km, 1 kV PI section line and eight uniformly distributed capacitors (C = 47 μF) is tested. These distributed capacitors could be shunt-connected PFC capacitors and capacitive loads [11]. The other parameters of the microgrid preserve the same value as the last case, which also can be seen in the Table I.

A. No Centralized Control Architecture

Fig. 11 shows the voltage waveforms for the outputs of two interface inverters and the common load bus. The harmonic spectral analysis on these voltage waveforms is presented in Fig. 12. The fifth harmonic voltage at the common load bus is magnified significantly because of the 'whack-a-mole' effect, even though the harmonic voltages at the outputs of interface inverters are damped significantly.

B. With Centralized Control Architecture

Fig. 13 contains the voltage waveforms for the outputs of two interface inverters and the common load bus after using the centralized control architecture. The harmonic spectrums of these three voltages are shown in Fig. 14. The fifth and seventh harmonic voltages on the outputs of inverters are increased after implementing centralized selective harmonic compensator. This is because the harmonic voltage damping on the sensitive bus results in an increase on the harmonic conductance (G_1 and G_2) in the autonomous nonlinear load sharing loops, whereas the allowable harmonic conductance is subjected to the stability of inner current control loop of interface inverters. Hence, the harmonic voltage damping on the sensitive bus is sometimes achieved at the expense of distorting output voltages of inverters, as shown in Fig. 13. Nevertheless, the harmonic voltage components of those three voltages are still lower than the individual voltage distortion limit (shaded area 3%) in this test case.

Table II lists voltage THD analysis results for the nodes (B_0…B_8) along the distribution feeder without and with the centralized control architecture. It can be clearly observed that the voltage THD at each node is effectively reduced by using the proposed centralized control architecture.

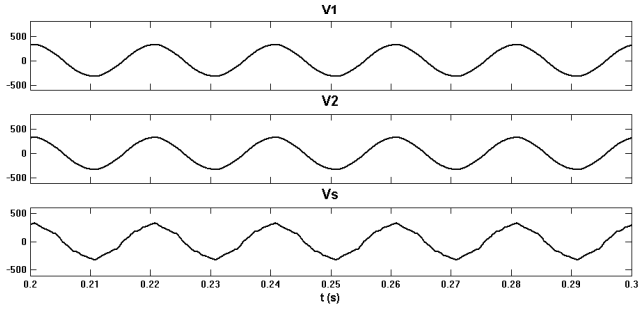

Fig. 11. The voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) without the centralized control architecture in the long distribution feeder case.

TABLE II
VOLTAGE THD RESULTS FOR THE NODES OF DISTRIBUTION FEEDER

Control system types	Node voltage THD results (%)								
	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8
Without centralized control architecture	1.28	2.49	3.87	5.18	6.37	5.18	3.87	2.49	1.28
With centralized control architecture	3.05	2.12	2.38	3.53	4.94	3.53	2.38	2.12	3.05

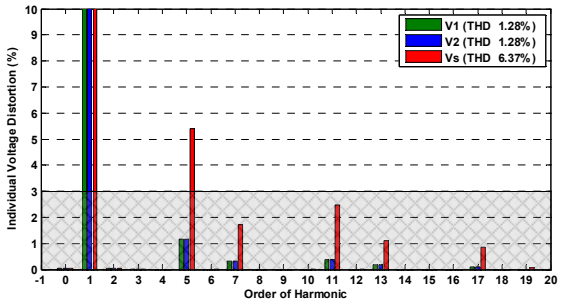

Fig. 12. The harmonic spectrums of voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) without the centralized control architecture in the long distribution feeder case.

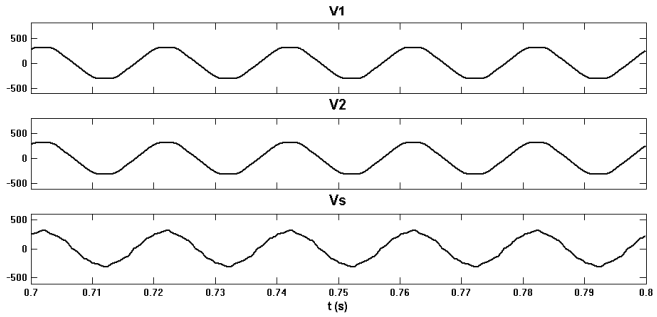

Fig. 13. The voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) without the centralized control architecture in the long distribution feeder case.

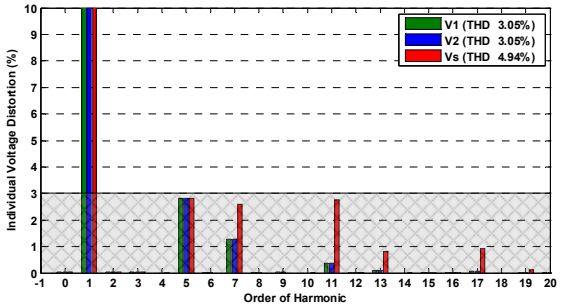

Fig. 14. The harmonic spectrums of voltage waveforms on the common load bus (V_S), outputs of interface inverters (V_1 and V_2) with the centralized control architecture in the long distribution feeder case.

V. CONCLUSIONS

In this paper a centralized control architecture for harmonic suppression in islanded microgrids has been presented. The proposed control system effectively alleviates the annoying 'whack-a-mole' effect on using the voltage-detection based active filter method, consequently achieving both harmonic suppression and nonlinear load sharing among multiple DER units in islanded microgrids. Moreover, the use of multiple rotating reference frames and low-pass filters facilitates utilizing low-bandwidth communication technique to transmit harmonic signals. Finally, case studies and test results show that the centralized control architecture is an effective and promising approach for future microgrid operations.

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