A 14-Bit Oversampled SAR ADC With Mismatch Error Shaping and Analog Range Compensation

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***Abstract*—DAC mismatch is a major challenge for high-resolution ADCs. This brief proposes an analog-detection-based input range compensation technique for high-resolution ADCs with mismatch error shaping (MES). By applying a pre-comparison and suitably switching the DAC MSB, the input loss caused by MES is compensated. By adopting a flying-capacitor sampling technique, the prediction errors found in prior solutions are avoided. The prototype 14-bit SAR ADC achieves 80.4 dB SNDR and 93 dB SFDR in a 4 kHz signal bandwidth with an OSR of 16. It only occupies 0.0034 mm^2 and consumes 0.656 μW under a 0.8 V supply, leading to a Schreier figure-of-merit of 178.3 dB. These features make it suitable for miniaturized high-performance IoT and biomedical systems.**

***Index Terms*—Analog-to-digital converter (ADC), flying capacitor sampling, input range compensation, mismatch error shaping (MES), successive approximation register (SAR).**

I. Introduction

THANKS to recent developments, high-resolution SAR ADCs are becoming more and more popular in IoT and bio-recording applications. For example, a 13-bit SAR ADC is used in [1] to read out fetal electrocardiogram signals. If better tolerance against motion artifacts is required, ADCs with even higher resolution are desired. In the above applications, power and area are two critical design concerns. A major challenge for high-resolution SAR ADCs is DAC mismatch, which imposes a minimum used capacitor value and thus has a negative impact on the required power consumption and area.

Many techniques have been proposed to address the DAC mismatch issue [2], [3], [4], [5], [6], [7], [8]. Among these techniques, mismatch error shaping (MES) is an efficient choice for high-resolution SAR ADCs thanks to its capability of being applied to binary-scaled cells [4]. One disadvantage of MES is that the ADC will lose half of the input range, which tightens the absolute noise requirements for high-resolution systems. To solve this problem, existing solutions can be divided into two categories. The first option is only applying MES to the least significant bits (LSBs) [4], [5]. For segmentation-based methods, part of the input range is still lost and data weighted averaging (DWA) is required to solve the most significant bit (MSB) capacitor mismatch. The second option is to compensate the input range by prediction [6], [7], [8]. The main challenge for prediction-based methods is that the prediction might be wrong. Its accuracy is highly related to the oversampling ratio (OSR) of the system (usually requires $\geq$16) and the existence of interferers.

In this brief, an input range compensation technique based on analog detection is proposed. By performing a pre-comparison and switching the DAC MSB accordingly, the input range is then recovered and no DWA is required while MES can be applied to all bits in the converter. By using a flying capacitor sampling technique, the pre-comparison is done after the sampling moment. Hence, prediction errors are avoided. A prototype SAR ADC with a 14-bit resolution is implemented in 65 nm CMOS. As a result, it achieves 80.4 dB SNDR with 0.656 μW in a 0.034 mm^2 area.

This brief is organized as follows: Section II reviews the principle of MES with input range compensation. Section III discusses the proposed analog detection and compensation technique with flying capacitor sampling. Section IV presents the circuit implementation in detail. Section V provides the measured results and Section VI draws the conclusion.

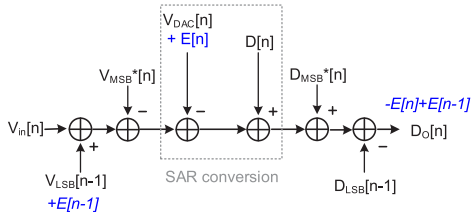

Fig. 1. Principle of MES with input range compensation.

II. Review of MES With Input Range Compensation

Fig. 1 shows the principle of MES with input range compensation. Mismatch is a relative error. Taking the DAC MSB

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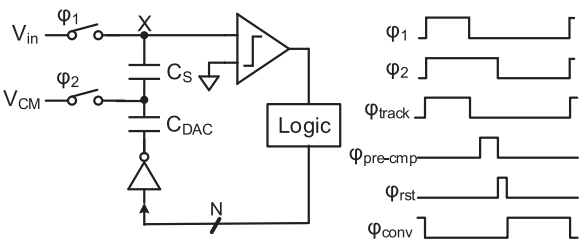

Fig. 2. A simplified diagram of a SAR ADC with the proposed input range compensation technique and its timing diagram.

(1-bit) as a reference, the mismatch of the LSBs (i.e., all bits except the 1-bit MSB) can result in conversion errors $E[n]$ at the nth conversion cycle. For ADCs with MES, the previous LSB code ($D_{LSB}[n-1]$), together with its conversion error $E[n-1]$, will be fed back to the current input signal ($V_{in}[n]$) before SAR conversion. Afterwards, $D_{LSB}[n-1]$ will be subtracted in the digital domain. During the nth SAR conversion, a new $E[n]$ is generated. This results in a function of $-E[n]+E[n-1]$ at the output, which behaves as a high-pass filter for DAC mismatch errors. Thus the DAC mismatch errors are 1st-order shaped to high frequencies and can be filtered out in an oversampled system.

However, the LSB feedback results in a loss of input signal range. Assume that the original input range of a differential ADC is $[-V_{ref}, V_{ref}]$. $D_{LSB}[n]$ can be any value within $[-½V_{ref}, ½V_{ref}]$. Hence, half of the original input range is occupied. The available MSB capacitors, which can generate a $\pm\frac{1}{2}V_{ref}$ voltage step, can be used to compensate for the input range loss.

A prediction can be done to estimate the direction of overrange. Depending on the predicted signal range, a compensating voltage shift created by the available MSB capacitors can be applied to the input prior to sampling to avoid overrange. Then, this compensation voltage is removed again in the digital domain. In this way, DAC mismatch errors can be shaped without input range loss. Depending on the actual design, either analog or digital, 2-level or 3-level prediction can be adopted [6], [7], [8].

One drawback of prediction-based methods is that the prediction accuracy is sensitive to OSR and interference. Hence, a certain OSR is required to ensure the prediction accuracy, which is necessary to avoid conversion errors.

III. Proposed Input Range Compensation With Analog Detection

A. Architecture and Operation

This brief adopts the same principle described in Fig. 1. However, instead of prediction, this brief proposes an input range compensation technique based on analog detection. A simplified diagram of a SAR ADC with the proposed input range compensation technique and its timing diagram are shown in Fig. 2. Note that C_{DAC} represents an N-bit binary-scaled array of capacitors, as required for the SAR operation. Further, a single-ended diagram is shown here for simplicity. Compared to a conventional top-plate sampled SAR ADC,

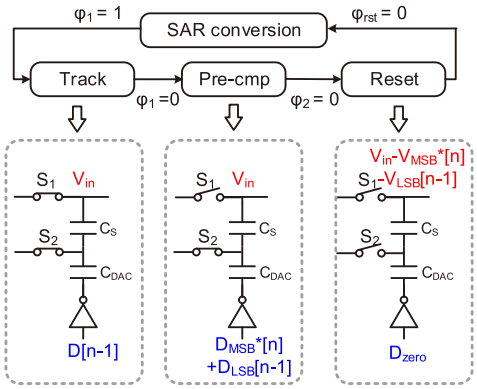

Fig. 3. Circuit operation of the proposed input range compensation technique.

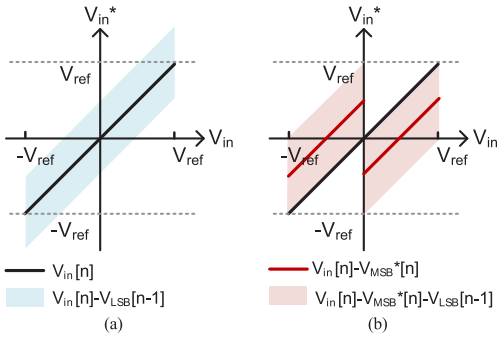

Fig. 4. A conceptual diagram of the equivalent input signal without (a) and with (b) input range compensation.

a separate sampling capacitor (C_S) in series with the DAC capacitors (C_{DAC}) and an extra sampling switch are introduced. The two sampling switches (S_1 and S_2) are controlled by φ_1 and φ_2, respectively. Besides, an extra pre-comparison phase is generated after the sampling moment and the reset phase is positioned after the pre-comparison phase and before the SAR conversion phase.

As shown in Fig. 3, the circuit-level operation consists of 4 phases, tracking, pre-comparison, reset and SAR conversion. The signal processing for the nth cycle starts at the rising edge of φ_1. First, during the tracking phase, the sampling capacitor (C_S) tracks the input. The DAC capacitors remain at their state of the previous cycle. After V_{in} is sampled on C_S at the falling edge of φ_1, a pre-comparison using the existing comparator of the ADC will be done to determine the polarity of V_{in}. While the sampling capacitor continues holding the input, the DAC MSB capacitors are now set to the polarity of the input signal ($D_{MSB}^*[n-1]$), which was detected by the pre-comparison. For example, if $V_{in} > 0V$, the MSB capacitors are set to V_{ref}. The DAC LSB capacitors still remain at their previous value ($D_{LSB}[n-1]$). Then, at the falling edge of φ_2, S_2 is opened. The sampling capacitor is now floating. Both MSB and LSB capacitors are reset by changing the control codes from $D_{MSB}^*[n]+D_{LSB}[n]$ to D_{zero}. Here, D_{zero} represents the DAC code in the reset state. The equivalent sampled signal at the comparator input (V_{in}^*) becomes $V_{in}[n]-V_{MSB}^*[n]-V_{LSB}[n-1]$, where V_{LSB} enables the MES operation, and V_{MSB}^* creates the compensation to prevent overrange. As what is conceptually shown in Fig. 4, the input range of the ADC

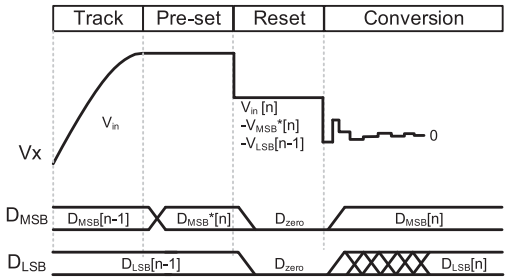

Fig. 5. An example of the time-domain behavior for the signal at the comparator input and the DAC control signals.

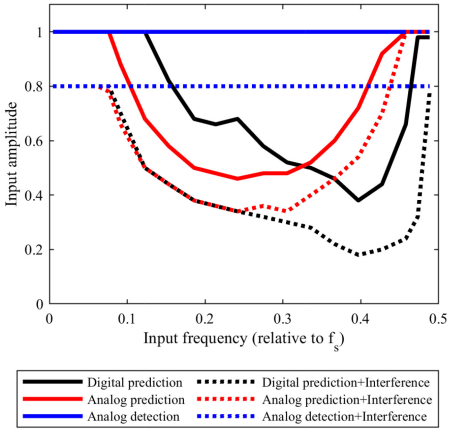

Fig. 6. Simulated input amplitude as a function of input frequency with and without interference.

is recovered to $[-V_{ref}, V_{ref}]$ when compensation is applied. A regular SAR conversion starts afterwards and sets the DAC control code to $D[n]$, which represents the DAC value at the n^{th} cycle. An example of the time-domain behavior for the signal at the comparator input (V_x) and the DAC control signals are shown in Fig. 5.

The main advantage of this detection scheme is that it determines the compensation voltage after sampling, whereas previous prediction methods determine the compensation prior to the sampling moment. As a result, the proposed method does not suffer from prediction errors.

B. Discussions

By using the proposed analog-detection-based input range compensation, two samplings steps are performed and now the sampling noise power is equal to:

$$\frac{2kT}{C_S} + \frac{2kT}{C_{DAC}} \tag{1}$$

To minimize the noise overhead, C_S could be set to for instance 2.7 C_{DAC}, which degrades the SNR by only 1.4 dB.

On the other hand, by performing two samplings steps, the information of the current input signal can be known without prediction, and thus without errors. For comparison against prior prediction schemes, Fig. 6 shows the maximum input amplitude without overrange as a function of the input frequency with and without an interference tone, simulated using a behavioral model. If interference is enabled, it is set to

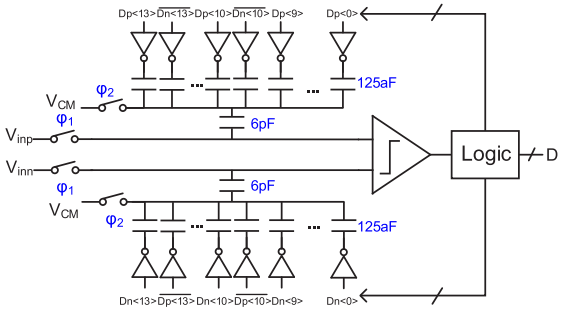

Fig. 7. Proposed SAR ADC with MES and analog range compensation.

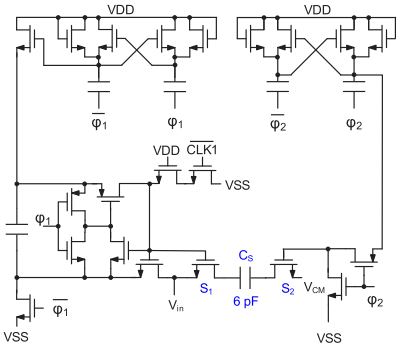

Fig. 8. Schematic of the proposed flying capacitor sampling circuit.

a 20% full-scale tone at $0.4f_s$, so it can be compared against the results in [6], [8]. Thus, ideally, the input signal should reach 100% full-scale without interference or 80% full-scale with interference, unless prediction errors occur. As can be seen, with digital [6] or analog [8] prediction schemes, the maximum input amplitude drops for higher input frequencies due to prediction errors, which thus implies a minimum required OSR to limit the signal bandwidth. Besides, the existence of interference will further degrade the prediction accuracy and thus an even higher OSR is required. The proposed analog detection method can avoid these concerns and the performance remains constant regardless of OSR.

IV. Circuit Implementation

Fig. 7 shows the schematic of this brief, which consists of a track and hold circuit, a 14-bit capacitive DAC, a dynamic biased comparator and asynchronous logic.

A. Track and Hold

The schematic design of the new track and hold circuit is shown in Fig. 8, which consists of sampling switches S_1, S_2 and a sampling capacitor C_S. S_2 is driven by a boosted clock for simplicity and lower power overhead. S_1 is driven by a bootstrapping circuit for higher linearity requirements.

Theoretically, the absolute value of C_S does not affect the operation of the ADC. In the actual implementation, the mismatch of C_S and the mismatch of parasitic capacitances may result in even order distortion and affect the SNDR for a high-linearity system. A large C_S results in lower sampling noise and better matching. However, it may also degrade the

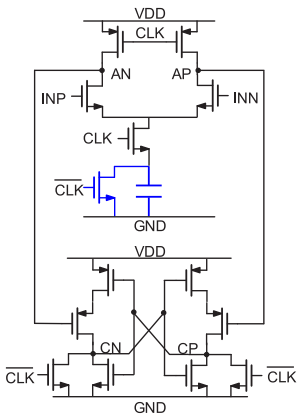

Fig. 9. Schematic of the comparator [9].

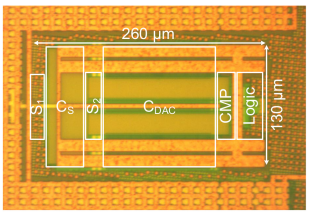

Fig. 10. Chip micrograph.

maximum operation speed of the ADC and costs more area. Fortunately, since C_S is only one capacitor, its implementation is relatively area-efficient compared to DAC capacitors. As a trade-off, in this brief, C_S is implemented by regular metal-oxide-metal capacitors with a minimal spacing of 100nm and its value is chosen to be 6 pF. It occupies 15% of the ADC area and results in 93 dB SNR with 2.2 pF DAC capacitance for an input range of 1.6 V and an oversampling ratio of 16. A 7% mismatch of C_S versus C_{DAC} can be tolerated to achieve above 100 dB SFDR, which is easy to satisfy with a 6 pF capacitance in the used technology.

B. Comparator

The comparator is another bottleneck for high-resolution SAR ADCs and one of the dominant power consumption sources. Similar to a regular SAR ADC, comparator offset in this brief occupies a small part of the ADC input range, but it does not affect the linearity of the ADC. Fig. 9 shows the schematic design of the used dynamic comparator, which consists of a dynamic bias pre-amplifier and a latch. A tail capacitor and a NMOS switch are added to the bottom of the pre-amplifier to reduce the energy consumption by means of self quenching and to pre-dominantly operate in weak inversion for maximizing its gm/Id [9]. In this brief, a 300 fF tail capacitor is used, which reduces the comparator power by about 23%.

V. Measurement Results

The prototype ADC is implemented in 65 nm CMOS as shown in Fig. 10. It occupies an active area of 0.034 mm^2 and was measured to consume 0.656 μW at a sampling rate of 128 kHz from a 0.8 V supply.

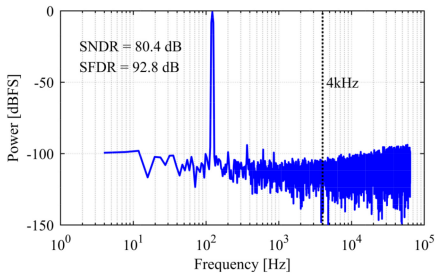

Fig. 11. Measured spectrum for f_{in} = 122 Hz, at 128 kS/s and an OSR of 16.

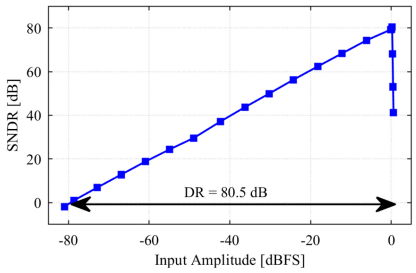

Fig. 12. Measured SNDR versus input amplitude.

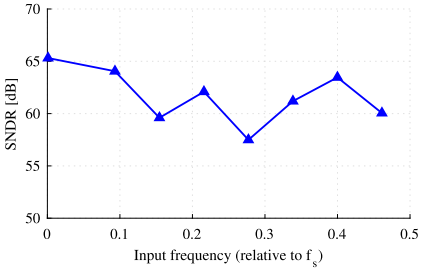

Fig. 13. Measured SNDR versus input frequency for a full range input (OSR = 1).

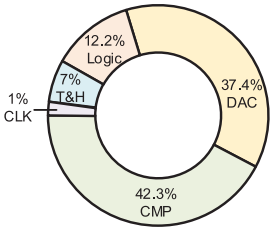

Fig. 14. Power breakdown of the ADC.

The measured spectrum with a 128 kHz sampling rate and a 122 Hz input frequency is shown in Fig. 11. The peak-to-peak input signal range is around 1.36 V. With an OSR of 16, the prototype ADC achieves 80.4 dB SNDR and 92.8 dB SFDR in a 4 kHz signal bandwidth. The DAC mismatch error is first order shaped. Fig. 12 shows the measured SNDR versus input amplitude. The measured dynamic range (DR) of this prototype is 80.5 dB.

Fig. 13 shows the measured SNDR versus input frequency for a full range input and an OSR of 1. Due to the lack of

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[2]	[3]	[4]	[5]	[6]	[7]	[8]	This work
DAC mismatch calibration	Vector-based DEM	Dither	MES +DWA	MES +DWA	MES +Digital prediction	MES +Digital prediction	MES +Analog prediction	MES +Analog detection
Technology [nm]	40	65	55	40	40	65	65	65
Supply voltage [V]	1.1	0.8	1.2	1.1	1.1	1.2	0.8	0.8
Sample rate [kS/s]	32000	128	1000	12800	2000	1000	128	128
Oversampling ratio	64	16	250	64	25	16	16	16
Bandwidth [kHz]	250	4	4	100	40	31.25	4	4
Power [μW]	4700	1.37	15.7	1998	67.4	7.3	0.98	0.656
SNDR [dB]	94.8	79.1	96.1	98.3	90.5	80	84.5	80.4
SFDR [dB]	103.0	87.1	105.1	108.5	102.2	98	103	93
DR [dB]	96	-	-	101.2	94.3	81.4	85	80.5
FoM$_W$ [fJ/conv-step] [1]	209.3	23.2	37.61	148.6	30.77	14.3	9.4	9.57
FOM$_S$[dB][2]	172.1	173.8	180	175.3	178.2	176.3	180.6	178.3
Area [mm^2]	0.37	0.18	0.072	0.48	0.061	0.043	0.033	0.034

[1] $FOM_W = Power/(2^{ENOB} \times 2 \times BW)$
[2] $FOM_S = SNDR + 10 \times \log 10(BW/Power)$

oversampling, the SNDR in this case is lower than before since all noise and distortion contributions count. However, this result confirms that the ADC does not saturate for any input frequency, as this would otherwise lead to a major SNDR reduction. For prior-art prediction methods, their SNDR will quickly drop for high input frequencies due to prediction errors.

Fig. 14 shows the post-layout simulated power breakdown of the ADC. Thanks to MES, small DAC capacitors can be used and the DAC switching requires only 37.4% of the total power.

Table I summarizes the performance of this brief and compares it to state-of-the-art designs with on-chip DAC mismatch calibration techniques. Compared to [2], [3], [4], [5], [6], [7], [8], this brief achieves competitive energy and area efficiency with a simple architecture and zero prediction errors.

VI. CONCLUSION

This brief presents a 14-bit SAR ADC with mismatch error shaping and analog-detection-based input range compensation. The proposed pre-comparison technique with flying capacitor sampling, can detect the input range without prediction errors. Combined with MES and suitable MSB switching, the DAC mismatch error can be shaped without input range loss. The prototype ADC fabricated in 65 nm CMOS occupies an area of 0.034 mm^2 and consumes 0.656 μW at a sampling frequency of 128 kHz. The achieved SNDR and SFDR are 80.4 dB and 92.8 dB, respectively. The resulting Schreier FoM is 178.3 dB and the resulting Walden FoM is 9.57 fJ/conversion.

ACKNOWLEDGMENT

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