Barrier Properties of ALD $W_{1.5}N$ Thin Films

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ABSTRACT

$W_{1.5}N$ films grown by ALD from WF_6, NH_3, C_2H_4 and SiH_4 as precursors were tested as Cu diffusion barriers in p^+/n diodes and capacitors with SiO_2 as a dielectric. I-V and C-V, C-t characteristics were measured before and after anneal. The layers exhibit excellent barrier properties against both Cu and Al interaction with silicon. No changes of current and capacitance attributed to a barrier failure were observed after annealing at 400 ^oC. Samples without the barrier showed a drastic change of the I-V characteristics. The composition of the films was $W_{1.5}N$ as determined with RBS, being a mixture of WN and W_2N phases The RMS- roughness was as low as 0.5-0.7 nm for a film with a thickness of 25 nm.

INTRODUCTION

Continuous scaling of Cu interconnect features requires very thin and conformal barriers against the diffusion of Cu into dielectrics and silicon. For this purpose Atomic Layer Deposition (ALD) is superior to PVD and CVD. Tungsten nitride is a possible candidate as a diffusion barrier. ALD using WF_6 and NH_3 as precursors was reported to produce films with resistivities as high as ~ 4500 μΩcm [1, 2]. For the first time we present ALD tungsten nitride layers with a resistivity as low as 480 μΩcm [3]. This improvement is ascribed to the additional use of C_2H_4 and SiH_4 in the deposition process.

EXPERIMENTAL

The diffusion properties were evaluated on p^+/n diodes and capacitors with 200 nm of wet thermal oxides grown in water vapor. Diodes and capacitors were made on separate 100 nm

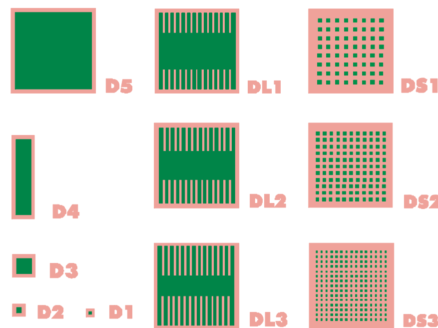

Figure 1. Diodes with varying active area D1÷D5 (100x100 ÷ 1600x1600 μm^2) and different geometry of the contacts openings DL1÷3, DS1÷3 and constant active area (1600x1600 μm^2).

(100) n-type Si substrates. This is done to avoid the capacitor to become contaminated during diode test. Diodes with an area varying between (100 μm)^2 and (1600 μm)^2 had a different geometry of the contacts openings and a varying perimeter to area ratio (see figure 1). A 0.25 micron deep p^+/n junction was fabricated with BF_2^+ ion implantation. Diodes were tested with a barrier thickness of 7 or 10 nm, capacitors with 10 nm. Cu reference diodes were made with an ultra thin (~3 nm) adhesion layer of $W_{1.5}CN$. Cu reference capacitors were made with a direct Cu contact to SiO_2. Cu or Al was used as a metal for electrodes. Both as prepared and annealed devices were measured to monitor Cu-diffusion. Annealing was done at 200 and 400 ºC in N_2/ 5% H_2 ambient for 30 min.

C-V tests of diodes were done under reverse bias. I-V measurements were performed using a HP 4256A parameter analyser and the Material Development Corporations (MDC) CSMWin program. The leakage current is measured at –5 V. Leakage of the set up was $5x10^{-15}$ A.
C-V and C-t tests of capacitors were done at 10 kHz with a HP 4140B pA meter as a DC voltage source, a HP 4275 multi- frequency meter and the MDC CSMWin computer program.

RESULTS AND DISCUSSION

Diode measurements

Capacitance- Voltage (C-V) and Current- Voltage (I-V) characteristics of diodes with Cu/barrier, Al/barrier and Cu contacts were measured. Results of the C-V test are used to calculate the effective carrier density and build- in voltage in the junction. Analysis of I-V characteristics gives a generation and a diffusion current component. These values serve as an input for the calculation of generation and minorities lifetime, respectively. C-V measurements of diodes appeared not to be sensitive enough to conclude about Cu diffusion.

Cu reference

The Cu reference without barrier was measured to monitor Cu diffusion. Figure 2 shows the leakage current at -5 V before and after annealing at 200 and 400 ^{o}C for diodes D1÷D5. No increase of the leakage current is observed after the 200 ^{o}C treatment.

Some devices annealed at 400 ^{o}C show an increase of the leakage current of 3 orders of magnitude. This can be attributed to the diffusion of Cu. The leakage current of large diodes

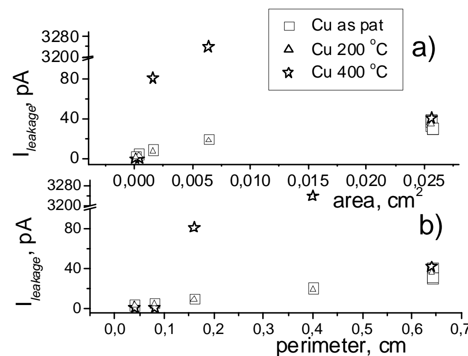

Figure 2. Leakage current versus area and perimeter for diodes (D1÷ D5) with Cu, no barrier.

with a varying area of metal/Si contact (see DS1÷ DL3 in figure 1) increases randomly after the annealing. No direct relation was observed between this rise and the area or perimeter of the metal contact to the Si. However, these structures showed more failures compared to the structures with one large contact opening to the Si (D1÷ D5), probably because of the large active area of the devices. The increase of the reverse current is accompanied with a change of the forward current as well.

Figure 3 shows the forward (I-V) characteristics. The current has two components: a diffusion current in the neutral region and a recombination current in the space charge region of the diode. Diffusion current under zero bias $I_{dif}(0)$ is obtained from (lgI-V) plots as an intercept of the line slope ~[V/(kT)] with the y- axis. The recombination current at zero bias $I_R(0)$ is obtained by extrapolating of the current slope ~[V/(2kT)] to zero voltage. For as patterned samples the recombination process in the space charge region is so much slower that no change in slope is observed over the complete voltage range. Thus the diffusion current in the neutral region dominates in the present voltage range. After the 400 ^{o}C annealing the current increases. The slope of I-V curves alters at a bias < 0.6 V (dashed lines). This is due to the increase of the current in the space charge region. The increase of the diffusion current in the neutral region is very small.

Diodes with barriers

Diodes with Cu metallization and a barrier layer of 7 and 10 nm are measured before and after the annealing. Samples with Al metallization on the 10 nm barrier serve as a reference. The leakage current density for devices with different area of contact increases with decreasing area. This is due to higher perimeter to area ratio. This means the contribution of the perimeter current component becomes dominant. After annealing the decrease of the leakage is larger for diodes with a small area. Thus, the contribution of the perimeter component to the leakage decreases. This decrease of leakage and lowering of the perimeter component of current is due to the annealing of plasma damage, introduced during the etching of the barriers.

Figure 4 shows the leakage current density for Cu/7nm and 10 nm barrier, Al/10 nm barrier and Cu contacts after 400 ^{o}C. Cu contacted diodes without barrier demonstrate a huge rise of the leakage current, while diodes with Al/barrier and Cu/barrier contacts show very low leakage current. For each type a number of diodes have been measured, they all show similar behavior. Obviously the concentration of Cu reached the level at which Cu behaves as a trapping center. For large diodes with the area of (1600 μm)^2 and different area of the contact to Si (DL1÷3, DS1÷3 in figure 1) there is no dependence of the leakage current on the contact area. Also, no

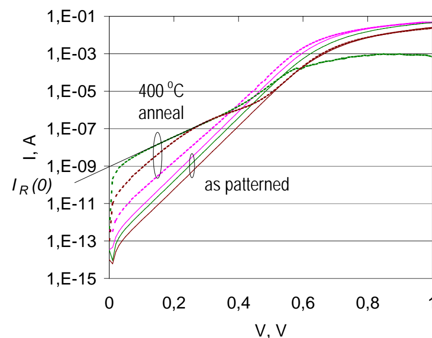

Figure 3. Forward I-V characteristics of the as patterned samples with Cu metallisation and no barrier and annealed at 400 ^{o}C.

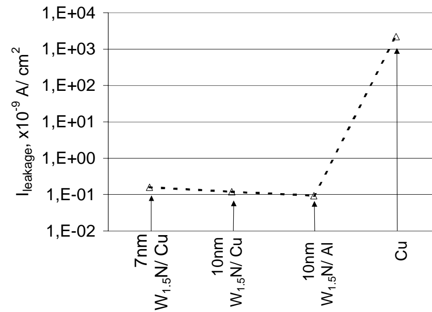

Figure 4. Leakage current density of annealed diodes at -5 V with area of 1600x1600 μm^2 (D5).

influence of the perimeter of this contact was observed. The average measured leakage of the diodes is the same as for the large diode with a massive contact (~1600 μm)^2 to the active area of a diode (D5). Essential in this picture is that a huge increase is only observed for samples without barrier. In all other cases the current decreases due to plasma damage anneal. The conclusion can be drawn that 7 and 10 nm of $W_{1.5}N$ withstand Cu and Al diffusion at least up to 400 ^oC for 30 minutes.

Generation lifetime and minority lifetime in the neutral region

The generation lifetime in the space charge region was calculated using the leakage current minus diffusion current for devices with area of 1600x1600 μm^2. Results are presented in Table 1. For the Cu reference there is a decrease of generation lifetime from ~100 down to 0.2 μs. This can be explained by a Cu diffusion and the formation of Cu trapping centers, which are very effective lifetime killers [4]. For the diodes with barriers (with the Al/barrier and the Cu/barrier combinations) the generation lifetime is increasing after annealing treatment. This increase is owed to the leakage value used in calculations, which was not corrected by the perimeter component of current. After annealing the contribution of current component into leakage reduced. At the same time the area current component and a real generation lifetime, respectively, might remain unchanged. As a result, the calculated generation lifetime after anneal becomes closer to the actual one. Thus, no Cu diffusion occurred after the 400 ^oC anneal through the 7 and 10 nm barriers. The minority lifetime in a neutral region, which is calculated using a diffusion current component in this region at zero bias $I_{dif}(0)$, decreases after the anneal for Cu contacted diodes only. This confirms the Cu diffusion in annealed diodes without barriers.

Capacitors tests

C-V and C-t measurements were done on capacitors with Al/barrier contact to SiO_2 and Cu/barrier. Figure 5 shows the results of the measurements before and after annealing at 400 ^oC.

Table 1. Generation lifetime

	generation lifetime, μs			
T, ^oC	Cu /10nm WN	Cu/7nm WN	Al /10nm WN	Cu
25	40	260	26	100
400	1200	1660	1310	0,2

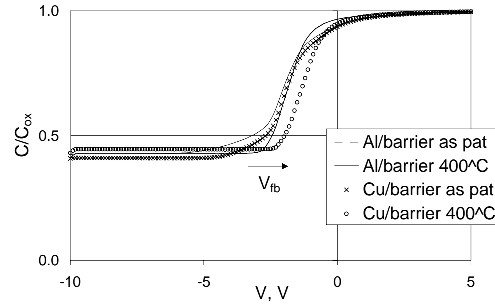

Figure 5. Normalized capacitance versus alplied voltage for as patterened and annealed at 400 ^{o}C capacitors with Cu/barrier and Al/barrier contacts.

The flat band voltage for capacitors with both types of contacts shifted towards positive voltage, while positive Cu^{+} ions should give a negative shift.

The calculated oxide charge is shown in Table 2. It becomes lower after anneal. Probably, the plasma during the etching of barriers creates charged traps in oxide, which density can be decreased at 400 ^{o}C. The interface state density, presented in this table, was calculated with the Terman method. The density of interface states decreases after 400 ^{o}C anneal from ~4x10^{10} down to 1x 10^{10} cm^{-2}eV^{-1} for both samples. Thus this heat treatment results in the annealing of both the interface states and oxide charges.

Results of C-t tests are presented in figure 6 as Zerbst plots. The slope of Zerbst plot is inversely proportional to generation lifetime. Annealed devices showed a longer lifetime. No deterioration of oxide properties or interface state density, accompanying a diffusion of Cu, was measured with C-V and C-t tests.

CONCLUSIONS

Functional ALD $W_{1.5}N$ barrier layers were obtained with our ALD process with a resistivity as low as 480 μΩ·cm. The $W_{1.5}N$ layers with a thickness of 7 and 10 nm did not show any failure of diodes after 400 ^{o}C anneal for 30 min.

C-V and C-t measurements of capacitors with 10 nm barrier did not reveal any Cu diffusion after heat treatment. The $W_{1.5}N$ films serve as a good barrier for both Cu and Al metallisation.

Table 2. Oxide charge N_{SS} and surface state density D_{it}

contact to SiO_2	N_{ss}, cm^{-2}		D_{it}, cm^{-2}V^{-1}	
	as patterned	400 ^{o}C	as patterned	400 ^{o}C
Al/ barrier	2,0E+11	1,6E+11	3E+10	1,0E+10
Cu/ barrier	1,5E+11	1,0E+11	3,5E+10	1,0E+10

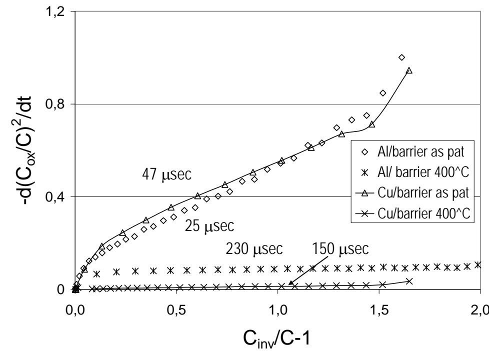

Figure 6. Zerbst plot for capacitors with Al/ barrier and Cu/ barrier contacts before and after 400 ^{o}C annealing.

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