An Improved Combined Current Control for Single-Phase Operation Mode of Single-/Three-Phase EV Charging System With Voltage Ripple Suppression

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***Abstract*—In this article, the control stage of an interesting versatile single-/three-phase electric vehicle (EV) charging system is studied in details. Therein, a typical three-phase two-level voltage source rectifier can be reconfigured to operate as a single-phase rectifier where two phase-legs operate with a pulsewidth modulation interleaving method and the grid neutral is connected to the midpoint of the dc-bus capacitors with the third leg operating as an active power decoupling (APD) circuit to reduce the current stress in the capacitors. To improve the performance of the single-phase operation while considering external grid voltage disturbances, first, an improved hybrid current control method combining deadbeat prediction current control (DPCC) with repetitive control (RC) is proposed in this article, where a modified RC is adopted to suppress the influence of the internal dc-bus capacitor voltage disturbance and to improve the harmonic control performance. Thereafter, via introducing the weighting factor K_f of the DPCC and by multiplexing the filter of RC in the DPCC output, the stability of the current loop under the influence of grid voltage distortion and grid impedance can be improved remarkably. Moreover, a grid-frequency voltage ripple suppression function implementing zero-voltage-switching turn-ON for the APD circuit is achieved, improving the reliability of the converter. Finally, a 7.4-kW single-phase ac–dc converter prototype is built to verify the feasibility and effectiveness of the proposed method in the single-/three-phase EV charging system.**

***Index Terms*—Deadbeat predictive current control (DPCC), repetitive control (RC), single-phase ac–dc converter, total harmonic distortion (THD), voltage ripple suppression (VRS).**

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I. Introduction

TRADITIONALLY, electric vehicles (EVs) implement an on-board charger (OBC) mainly used for the several hours when the car is parked at home, at work, or at public places where a dedicated AC grid connection is available [1], [2], [3]. In this context, to adapt to various charging power supplies, a versatile OBCs employing a power-factor-correction (PFC) rectifier technology, which is compatible to both the single- and three-phase AC charging, could be highly attractive [4], [5] (cf., Fig. 1).

However, incorporating this functionality poses inherent challenges and multiple considerations for the design of the OBC. For example, it could be important that independent of the utilized AC connection (single- or three-phase), the operational dc-bus voltage range and rated power of the ac–dc PFC converter are similar, which will facilitate the design and control of the galvanic isolated dc–dc converter. A single-phase ac–dc converter, which could be adapted for enabling the three-phase connection, is proposed in [6]. Therein, in addition to the typical H-bridge rectifier, an active power decoupling (APD) circuit composed of a half-bridge leg, an inductor, and a capacitor is utilized to realize the suppression of the dc-bus voltage ripple at twice the grid frequency caused by the inherent AC ripple power of the single-phase operation. Based on this structure, a discontinuous pulsewidth-modulation (DPWM) method is adopted in [7] to further improve the efficiency of the converter. In addition, some three-phase two-level and three-level topologies can form a single-phase totem-pole PFC converter under the single-phase grid input [8], [9]. The phase-loss operation of three-phase rectifiers have been extensively shown in the literature (e.g., [10]), proving that the three-phase rectifiers can operate well delivering PFC functionality with a two-phase connection. However, as the power switches are of the same type, the rated power of these converters when operating at the single-phase power grid is only one-third of that at the three-phase power grid. In [11] and [12], a single-phase ac–dc converter is implemented. In this case, the dc-bus voltage boost ratio becomes higher than that of the conventional single-phase system, and is relatively close to that of a three-phase voltage source rectifier. Moreover, through the interleaved connection of two phases, the rated power of

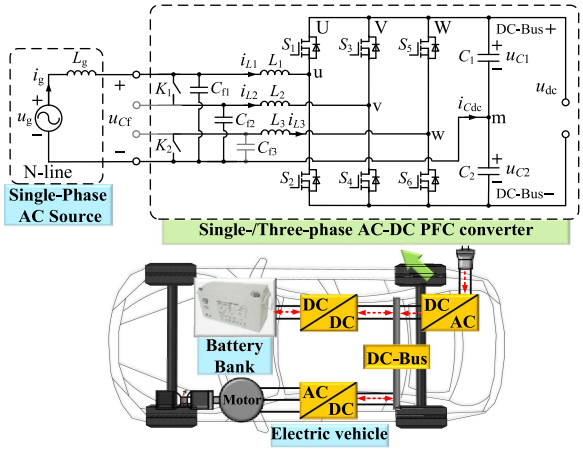

Fig. 1. Structural diagram of the proposed versatile single-/three-phase EV charging system. Under single-phase grid connection, the mechanical switches K_1 and K_2 are kept closed, whereas for the three-phase connection, these switches are kept opened.

the converter at single-phase power grid can reach two-thirds of that at a three-phase input operation. This configuration makes the converter quite interesting for single-/three-phase EV charging system. However, in this configuration, the phase current flows through the dc-bus capacitors, which will worsen the current stress and low-frequency voltage ripple of these capacitors, thus reducing the lifetime [7]. This can affect the lifetime and reliability of the charging system, calling for the incorporation of additional energy storage in the dc-link to what is needed in a three-phase rectifier. In order to improve the steady-state performance and reliability of the charging system, a single/three-phase ac–dc converter is adopted in this article (cf., Fig. 1).

In Fig. 1, the PFC part is composed of U and V phases in three-phase operation mode to control the input current waveform. However, traditional power grid contains different kinds of harmonic contents, which will deteriorate the current quality and the stability of EVs chargers [13], [14]. Therefore, it is necessary to adopt an appropriate current controller to improve the gird-side power quality of the converter. In order to further improve the steady-state current control performance of the converter and reduce the total harmonic distortion (THD) of the input current, repetitive control (RC) has been widely studied. However, due to one power grid period time delay in its internal model, its dynamic response is slow [15]. A common solution is to combine RC with another current controller with fast dynamic response [16], [17], [18], [19]. With the development of digital control technology, deadbeat predictive current control (DPCC) [20] and other predictive controllers [21] have attracted extensive attention. DPCC features the advantages of fast-tracking performance and easy implementation, and it is based on the internal model principle, which is a design principle of implanting a suitably reduplicated model of the external signal into the controller to form a high-precision feedback control system [22]. Therefore, DPCC and RC are combined in the current loop of the ac–dc converter in this article.

However, when the converter is connected to the grid with the traditional current controllers, the external grid voltage disturbance, such as grid voltage harmonics, line impedance, and internal dc-bus capacitor voltage ripple disturbance, will still affect the control performance and stability of the current loop [12], [23]. In [15], the influence of the RC parameters on the stability of the current control closed loop is analyzed and an infinite impulse response low-pass filter is used in RC, so as to improve the robustness of the control loop. Nevertheless, the current control performance of this method is worse than that with the traditional scheme in the steady state. An improved DPCC method for the three-phase inverter is proposed in [23]. To suppress the harmonic current caused by the grid voltage distortion, the grid voltage feedforward component in the current loop is obtained through a parallel proportional resonant (PR) structure. However, in the single-phase power grid, the frequency spectrum of harmonics is not limited to $(6n \pm 1)$ times the grid frequency, and excessive PR controllers will significantly increase the burden of the digital controller [24]. In [16], a DPCC based on repetitive prediction of the current control error is proposed to improve the current control performance. However, from the Bode diagrams of this control loop, it can be seen that the gain of this method for low-frequency harmonics is still lower than that of the resonant controllers. In [17], a control method combining DPCC and RC is proposed, and a frequency adaptive RC is designed to reduce the current harmonics at the grid side of the ac–dc converter in vehicle-to-grid mode. However, the influence of the dc-bus capacitor voltage disturbance on the current control performance is not considered in the abovementioned literature. In addition, it is also necessary to consider the existence of power grid harmonics and line impedance.

To tackle the aforementioned problems, an improved hybrid current control method for a single-phase ac–dc converter is proposed in this article. In this method, a modified $Q(z)$ in RC is adopted, so that the stability of the current loop is immune of the dc-bus capacitor voltage disturbance in the control loop, while maintaining a fair low-frequency harmonic current suppression performance. Moreover, a weighting factor K_f is introduced into the input current controller, and the filter in RC is multiplexed to the output of the DPCC, in order to improve the stability of the current loop of the single-phase ac–dc converter under the influence of grid disturbance, and further improve the power quality at the grid side. At the same time, in the ac–dc converter applied in this article, the third phase-leg is multiplexed to further suppress the grid-frequency voltage ripple of the dc-bus capacitors and to advantageously prolong the lifetime of the converter. Finally, the feasibility and effectiveness of the proposed method are verified by experimental results in a 7.4-kW prototype.

The rest of this article is organized as follows. In Section II, the single-phase operation of the ac–dc converter and the improved current control method are elaborated in detailed. In Section III, the suppression method of the grid-frequency voltage ripple of the dc-bus capacitors in the ac–dc converter is given. In Section IV, the experimental results of the 7.4-kW converter prototype are illustrated and discussed. Finally, Section V concludes this article.

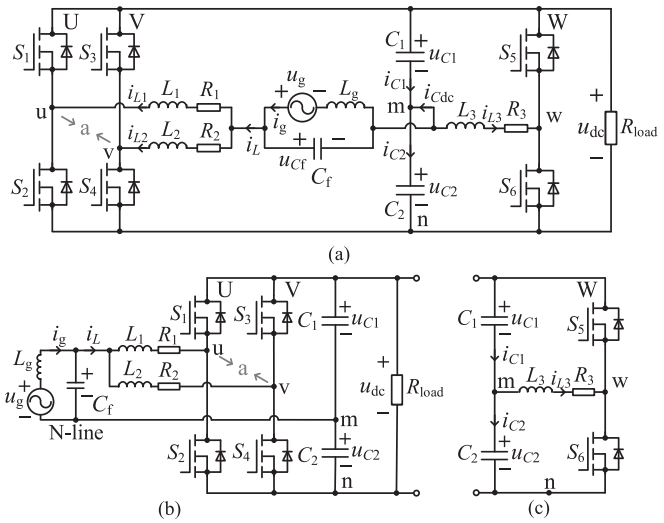

Fig. 2. Equivalent circuit configured for single-phase AC–DC converter operation. (a) Topology of the AC–DC converter. (b) PFC part of the converter. (c) VRS part of the converter.

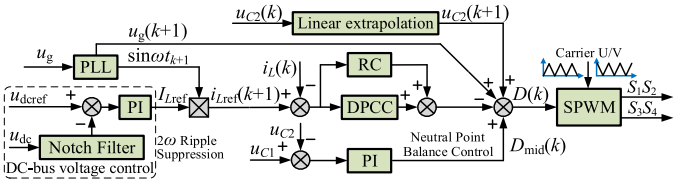

Fig. 3. Basic control block diagram of U and V phases corresponding to the single-phase AC–DC converter.

II. Proposed Input Current Control Method for the Single-Phase AC–DC Converter

A. System Description of the PFC Part

The topology of the single-phase ac–dc converter adopted in the single-phase EV charging system in this article is shown in Fig. 2, corresponding to the situation that the switches K_1 and K_2 in Fig. 1 of the single-/three-phase ac–dc converter are closed. In this converter, the midpoint of the capacitors C_1 and C_2 is directly connected to the N-line, and the phases U and V are used to realize the unity power factor (PF) operation of the input current and obtain a stable dc-bus voltage [12], and the PFC part of the converter is shown in Fig. 2(b). The phase W is used to realize the grid-frequency voltage ripple suppression (VRS) function, together with the dc-bus capacitors and input inductor L_3, and thus, the VRS part of the converter is shown in Fig. 2(c). Due to the symmetry of the converter topology, the filter inductance, and the internal resistance of the inductors at the grid side can be designed in the same value, i.e., $L_1 = L_2 = L_3 = L_f$ and $R_1 = R_2 = R_3 = R$, respectively. In addition, the capacitance of C_f in Fig. 2 is equal to the sum of C_{f1} and C_{f2}.

The basic control block diagram of the phases U and V is shown in Fig. 3. In the dc-bus voltage control loop, a PI controller is used to achieve no-static-error tracking of the

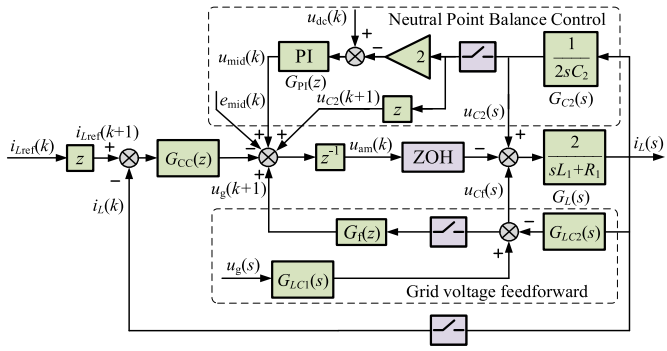

Fig. 4. Structural diagram of the input current control loop of the PFC part of the single-phase AC–DC converter.

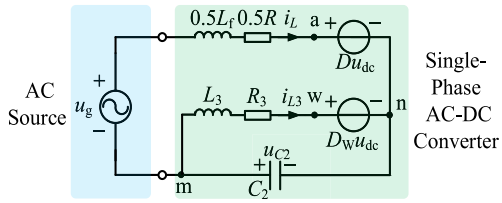

Fig. 5. Equivalent circuit of the single-phase AC–DC converter satisfying the KVL.

dc-bus voltage reference u_{dcref}. At the same time, a combined DPCC and RC current controller is adopted to realize the unity PF operation of the input current. In addition, in order to maintain the voltage ripple balance between the upper and lower dc-bus capacitors C_1 and C_2, a neutral point voltage balance PI controller is added to the control loop. Finally, the phases U and V are interleaved connected by the modulation part to reduce the high-frequency ripple of input current.

Through Figs. 2 and 3, the input current control loop diagram of the PFC part of the single-phase ac–dc converter is shown in Fig. 4, in which $G_{CC}(z)$ corresponds to the input current controller, and $G_f(z)$, $G_{LC2}(z)$ and $G_{LC2}(z)$ represent the filter of the grid voltage feedforward component and the grid impedance, respectively. The zero-order hold in Fig. 4 represents the pulsewidth-modulation (PWM) process, and is adopted as the interface from discrete domain to continuous domain. It can be seen from Fig. 4 that the input current control loop will be affected by the internal neutral point balance control and the external grid disturbance, and the input current of the converter, respectively. The equivalent circuit diagram of the single-phase ac–dc converter satisfying Kirchhoff's voltage law (KVL) is shown in Fig. 5, where the node "a" is the equivalent neutral point of the phase legs U and V. D_U and D_V are the duty cycle of the phases U and V, respectively, and it can be defined as $D_U = D_V = D$ as the phases U and V are interleaved connected. Then, it can be derived that the terminal a-to-n voltage is $u_{an} = Du_{dc}$, where u_{dc} is the total dc-link voltage. In addition, the input filter inductor of the PFC part is equivalent to L_1 and L_2 connected in parallel, and thus, its equivalent inductance and internal resistance are $0.5L_f$ and $0.5R$, respectively. From Fig. 5,

the voltage equation of the adopted single-phase ac–dc converter can be obtained as

$$\begin{cases} \frac{L_{\rm f}}{2}\frac{{\rm d}i_L}{{\rm d}t}+\frac{R}{2}i_L+Du_{\rm dc}=u_{\rm g}+u_{C2} \\ L_{\rm f}\frac{{\rm d}i_{L3}}{{\rm d}t}+Ri_{L3}+D_{\rm W}u_{\rm dc}=u_{C2}. \end{cases} \tag{1}$$

Since the internal inductor winding resistance R is relatively small, the influence of R can be ignored in the design of the controller. Through discretization and prediction of the input current at the $(k+1)$th and the $(k+1)$th samples [12], [25], the expression of the DPCC adopted in this article can be derived as

$$D(k)=\frac{u_{\rm g}(k+1)+u_{C2}(k+1)-\frac{K_L L_{\rm f}}{4T_{\rm s}}\left[i_{L\rm ref}(k+1)-i_L(k)\right]}{u_{\rm dc}} \tag{2}$$

where K_L is the ratio of the input inductance adopted in the control algorithm to the actual inductance, and $T_{\rm s}$ is the control and sampling period of the system. With the increase of K_L, the low-frequency harmonic suppression capability of the current loop is improved, while the stability margin of the system is reduced [12], [25]. In order to achieve better dynamic response and steady-state control performance of the current loop, K_L is generally selected between 0.5 and 1. However, the current control performance of the DPCC is affected not only by the inductance parameter mismatch and control delay, but also by the feedforward component of the grid voltage. On the one hand, the existence of grid impedance and grid voltage harmonics will distort the input current and even make the system unstable; on the other hand, under the light-load condition, the feedforward component of the grid voltage in the current loop will lead to a larger reactive power control error and lower *PF*.

In order to reflect the reactive power control error, it can be analyzed in the *d–q* coordinate system. From (1), (2), and [12], the circuit equations of the PFC part at the kth sample in the *d–q* coordinate system are derived as follows:

$$\begin{cases} u_{\rm gd}=\frac{L_{\rm f}{\rm d}i_{L\rm d}}{2{\rm d}t}-\frac{\omega L_{\rm f} i_{L\rm q}}{2}-\frac{K_L L_{\rm f}}{4T_{\rm s}}\left[I_{L\rm ref}(k+1)-i_{L\rm d}(k)\right] \\ \qquad +u_{\rm gd}\cos\frac{2\pi T_{\rm s}}{T_{\rm grid}} \\ u_{\rm gq}=\frac{L_{\rm f}{\rm d}i_{L\rm q}}{2{\rm d}t}+\frac{\omega L_{\rm f} i_{L\rm d}}{2}-\frac{K_L L_{\rm f}}{4T_{\rm s}}\left[0-i_{L\rm q}(k)\right]+u_{\rm gd}\sin\frac{2\pi T_{\rm s}}{T_{\rm grid}} \end{cases} \tag{3}$$

where $u_{\rm gd}$ and $u_{\rm gq}$ are the instantaneous grid voltages in the *d–q* coordinate system, which can be obtained from PLL. In the steady state, $u_{\rm gq}$ is equal to zero [23]. In (3), as the converter needs to operate at a unity PF, it can be considered that $i_{L\rm qref}(k+1)=i_{L\rm qref}(k)=0$. Since $T_{\rm s}<<T_{\rm grid}$, it can be approximately considered that ${\rm d}i_{L\rm q}/{\rm d}t\approx 0$ and $i_{L\rm q}=[i_{L\rm q}(k+1)+i_{L\rm q}(k)]/2$ in this sampling period, when the system is in steady state. Therefore, the control error of $i_{L\rm q}$ can be expressed as

$$\Delta i_{L\rm q}(k)=i_{L\rm q}(k)-0=-\frac{2T_{\rm s}\omega}{K_L}i_{L\rm d}(k)-\frac{4T_{\rm s}}{K_L L_{\rm f}}u_{\rm gd}\sin\frac{2\pi T_{\rm s}}{T_{\rm grid}}. \tag{4}$$

It can be seen from (4) that there exists a control error on the q-axis current in the steady state with the DPCC scheme, and the magnitude of this error is related to the active power [26] and the feedforward component of the grid voltage, resulting in the reduction of the PF and the degradation of the power quality at the grid side.

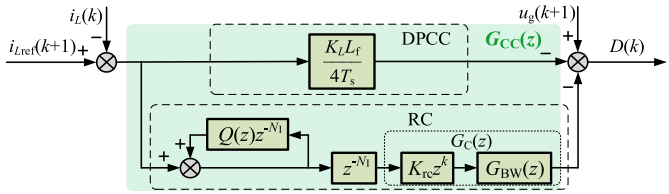

Fig. 6. Traditional input current controller of a single-phase AC–DC converter.

In addition, when the harmonic content of the grid voltage is large, the current control performance of the DPCC in the steady state will be affected due to the limited control gain at the harmonic frequency [23]. Therefore, an RC is added to the current control loop of the single-phase ac–dc converter to increase the reactive power control performance and the harmonic suppression ability.

The RC has satisfying control performance on periodic signals, and thus, it is suitable for input current control in the case of grid voltage distortion. In practice, as shown in Fig. 6, the traditional RC and DPCC can be used in parallel in the current loop of the converter, in which the transfer function of the RC can be expressed as

$$G_{\rm RC}(z)=\frac{z^{-N_{\rm I}}G_{\rm C}(z)}{1-Q(z)z^{-N_{\rm I}}} \tag{5}$$

where $N_{\rm I}$ is the integer obtained by rounding the ratio of the grid voltage period to the control period, i.e., $N_{\rm I}=$ round $(f_{\rm s}/f_{\rm g})$. $G_{\rm C}(z)$ is the compensator of RC, and its expression can be given as follows:

$$G_{\rm C}(z)=K_{\rm rc}z^k G_{\rm BW}(z)=K_{\rm rc}z^k K_{\rm b}\frac{z^2+2z+1}{z^2+b_1 z+b_2}. \tag{6}$$

In (6), $K_{\rm rc}$ is the gain of the RC and z^k is a delay compensator, which is used to compensate the phase delay caused by the filters and control delay, so that the system can achieve zero-phase-shift in the low-frequency band. At the same time, in order to stabilize the system, a Butterworth filter $G_{\rm BW}(z)$ is adopted in $G_{\rm C}(z)$ to suppress the high-frequency noise.

The $Q(z)$ in Fig. 6 is a gain attenuation block to increase the robustness of the system, and its selection has a great impact on the performance of RC [17], [19]. In the traditional RC, $Q(z)$ is often selected as a constant $K_{\rm q}$, which is slightly lower than 1 or a low-pass filter. When $Q(z)$ is selected as a low-pass filter, the most commonly used conventional $Q(z)$ is as follows:

$$Q(z)=Q_{\rm LPF}(z)=0.25z^{-1}+0.5+0.25z. \tag{7}$$

However, due to the influence of the dc-bus capacitor voltage disturbance, in the control loop of the single-phase ac–dc converter, the introduction of the neutral point voltage balance control will affect the selection of $Q(z)$. Thus, the impact of the neutral point voltage control on the input current will be analyzed in the next section.

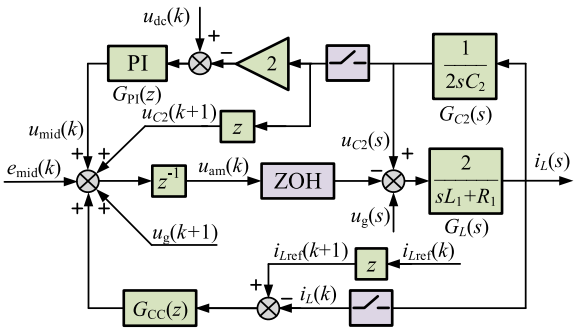

Fig. 7. Structural diagram of the neutral point voltage control disturbance in the input current control loop.

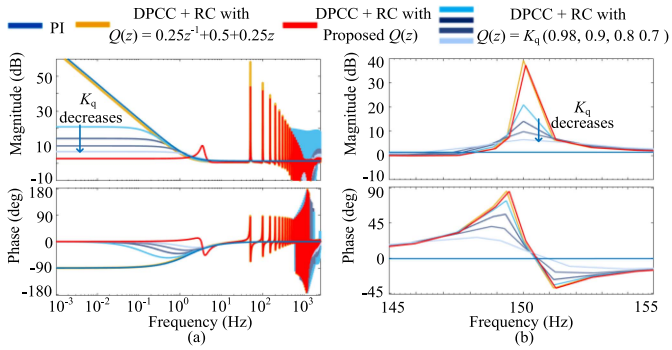

Fig. 8. Bode diagram of transfer function of the current controller using PI and DPCC+RC. (a) From low- to high-frequency band. (b) At the third harmonic of the grid voltage.

B. Impact of the Neutral Point Voltage Balance Control

The control error of the neutral point voltage balance control is generally caused by the sampling error, the parameter mismatch of the power semiconductors and passive energy storage devices, and the parasitic parameters of the circuit, and thus, it is usually a DC error signal, which might affect the input current control performance. From Fig. 4, when the grid disturbance is small, the transfer function of the current loop can be written as

$$\frac{i_L(z)}{i_{Lref}(z)} = \frac{zG_{CC}(z)G_L(z)}{z + G_{CC}(z)G_L(z) - 2G_L(z)G_{PI}(z)G_{C2}(z)}. \quad (8)$$

Accordingly, the structural diagram of the neutral point voltage control disturbance in the input current control loop can be derived, as shown in Fig. 7. The transfer function from control error $e_{mid}(z)$ to input current $i_g(z)$ can be obtained as follows:

$$\frac{i_L(z)}{e_{mid}(z)} = \frac{-G_L(z)}{z + G_{CC}(z)G_L(z) - 2G_L(z)G_{PI}(z)G_{C2}(z)}. \quad (9)$$

It can be seen from (9) that the neutral point voltage control error will have an impact on the input current control. In the denominator of (9), the PI controller in $G_{PI}(z)$ of the neutral point voltage balance control loop has an infinite gain for the DC error signal. If current controller $G_{CC}(z)$ also has an infinite DC gain, it may affect the stability of the current loop. Common current controllers used in the static coordinate system, such as proportional (P), PR, and DPCC, do not have infinite gain for the DC signal [27], and thus, the influence of the DC error signal on the current control could be reduced. In order to make the RC suitable for this converter, to suppress its gain to DC error signal and to maintain its harmonic current suppression performance, the following $Q(z)$ filter is adopted in this article:

$$Q(z) = \frac{(1 - nT_s)(0.25z^3 + 0.25z^2 - 0.25z - 0.25)}{z^2 - (1 - nT_s)z} \quad (10)$$

where n is an integer between 0 and $1/T_s$. Fig. 8 is the Bode diagram of the current loop transfer function composed of DPCC and RC with different $Q(z)$ and the transfer function of typical PI controllers. It is worth noting that when a constant K_q or a low-pass filter $Q_{LPF}(z)$ is used as $Q(z)$, the gain of DPCC and RC combined current controller in the low-frequency band has higher gains for DC signal and low-frequency signal. When $Q(z) = Q_{LPF}(z)$, the RC has a high gain similar to a PI controller in the low-frequency band. In addition, as shown in Fig. 8(b), when $Q(z) = K_q$, the gain of the RC at the third harmonic is reduced with the decrease of K_q, while it has a relatively high gain in the high-frequency band. This will affect the control performance of the input current in the steady state. At the same time, when the value of K_q is large, it might cause high-frequency oscillation of the input current, resulting in the degradation of the power quality at the grid side. When the proposed $Q(z)$ is used, the RC has the lowest gain for the DC signal, and it has a relatively high gain for each harmonic of the grid voltage in the low-frequency band, which is close to that when $Q_{LPF}(z)$ is used. In addition, it has obvious attenuation in the high-frequency band, which is favorable for improving the antiinterference performance of the system against high-frequency noise.

According to (8) and (9), the pole diagram of the transfer function from the neutral point voltage control error to the input current can be obtained, as shown in Fig. 9. In Fig. 9(a), the poles of the system in the high-frequency band with the proposed $Q(z)$ are further away from the unit circle than when $Q(z) = K_q$, and thus, the current loop is less prone to high-frequency oscillation. Moreover, it can be seen from Fig. 9(b) that due to the high gain of the DC signal, the pole of transfer function falls on the unity circle when $Q(z) = Q_{LPF}(z)$ in the RC, which may make the system unstable due to the existence of a DC control error. When $Q(z) = K_q$, the stability of the system in the low-frequency band will increase with the decrease of K_q. When the proposed $Q(z)$ is adopted, the poles of the system in the low-frequency band is within the unity circle, which improves the stability of the system. Similarly, as shown in Fig. 9(c), when $Q(z) = Q_{LPF}(z)$, the gain from the neutral point voltage control error to the input current in the low-frequency band is greater than 0, which will increase the DC component of the input current and affect the stability of the current loop. When the proposed $Q(z)$ is adopted, the gain of the input current to the control error is much lower than 0, and the controller has a fine suppression performance on the DC error signal.

C. Impact Analysis of Grid Disturbance

Two main causes of harmonic current of the single-phase ac–dc converter are the internal feedback control error and the

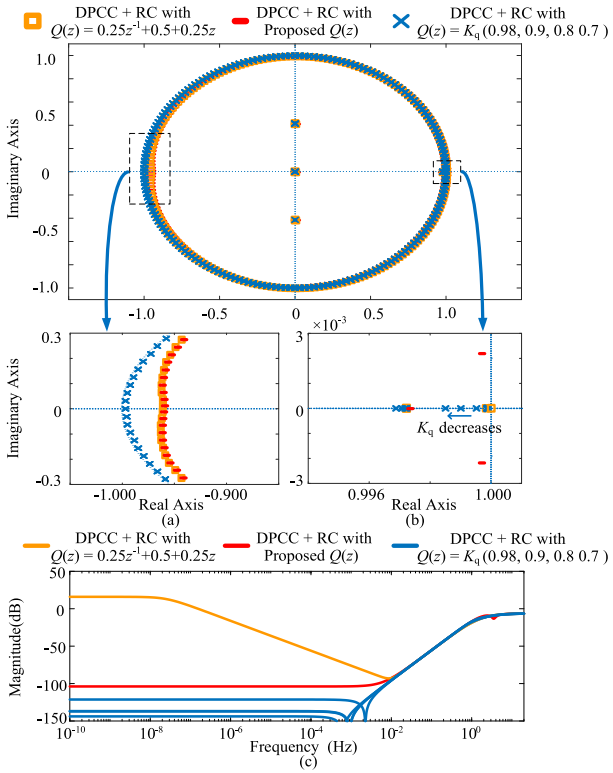

Fig. 9. Closed-loop poles and Bode diagram of the transfer function from the neutral point voltage control error to the input current. (a) Pole diagram at the high-frequency band. (b) Pole diagram at the low-frequency band. (c) Bode diagram at the low-frequency band.

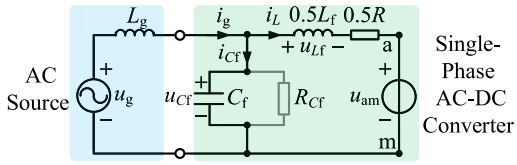

Fig. 10. Equivalent circuit of the converter when considering grid impedance.

external harmonic components of the grid voltage [28], [29]. As analyzed in Section II-A, the feedforward component of the grid voltage will affect the current loop, and the harmonic component of the grid voltage will generate harmonic current on the filter inductors and grid impedance at the grid side of the converter. Fig. 10 is the equivalent circuit diagram of the converter when considering grid impedance, in which $L_{\rm g}$ is the equivalent line inductance of the power grid, $C_{\rm f}$ is the input filter capacitor of the converter, and R_{Cf} is the equivalent parallel resistance at the grid side.

The corresponding voltage equation can be listed as follows:

$$u_{\rm g} - L_{\rm g}\frac{{\rm d}i_{\rm g}}{{\rm d}t} = u_{Cf}. \tag{11}$$

In (11), it follows that

$$\begin{cases} \frac{C_{\rm f}{\rm d}u_{Cf}}{{\rm d}t} + \frac{u_{Cf}}{R_{Cf}} = i_{Cf} \\ i_L = i_{\rm g} - i_{Cf} \end{cases} \tag{12}$$

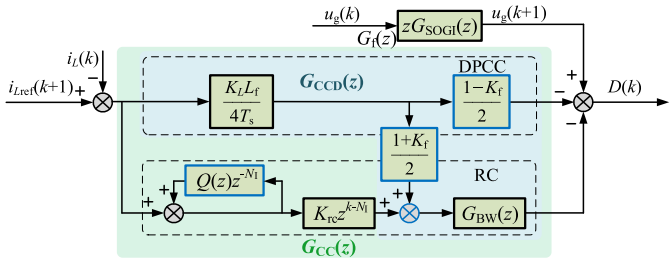

Fig. 11. Proposed input current controller for single-phase AC–DC converter.

where R_{Cf} is the equivalent parallel resistance at the grid side.

After Laplace transform, the relationship between grid-side voltage $u_{\rm g}$, capacitor voltage u_{Cf}, and input current i_L of the converter can be deduced as

$$u_{Cf}(s) = \frac{R_{Cf}u_{\rm g}(s) - R_{Cf}L_{\rm g}si_{Lf}(s)}{R_{Cf} + L_{\rm g}s + R_{Cf}L_{\rm g}C_{\rm f}s^2} = G_{LC1}u_{\rm g}(s) + G_{LC2}i_L(s). \tag{13}$$

As derived in Section II-B, the influence of the neutral point voltage control of the dc-bus capacitors on the current loop in the low-frequency band can be eliminated by adopting $Q(z)$ shown in (10). Therefore, to simplify the derivation, the neutral point voltage control loop can be omitted. Combining (13) and Fig. 4, the open-loop transfer function of the input current loop when considering the grid impedance is as follows:

$$G_{\rm open}(z) = \frac{G_L(z)G_{\rm CC}(z)}{z + zG_L(z)G_{LC2}(z) + G_L(z)G_{\rm f}(z)G_{LC2}(z)}. \tag{14}$$

Different from the disturbance caused by the neutral point voltage balance error, the influence of the grid disturbance generally needs to attenuate the gain of the controller in the high-frequency band to ensure the stability of the current loop [30], [31]. In order to improve the input current control performance in the case of grid voltage harmonics and grid impedance, and to enhance the stability of the current control loop, a hybrid input current controller structure combined DPCC with RC is proposed in this article. This is shown in Fig. 11.

The current loop transfer function can be expressed as

$$G_{\rm CC}(z) = \left[\frac{K_{\rm rc}z^{k-N_{\rm I}}}{1 - Q(z)z^{-N_{\rm I}}} + \frac{(1+K_{\rm f})K_LL_{\rm f}}{8T_{\rm s}}\right]G_{\rm BW}(z) + \frac{(1-K_{\rm f})K_LL_{\rm f}}{8T_{\rm s}} \tag{15}$$

where $K_{\rm f}$ is the weight coefficient of the DPCC output, and its value range is within $-1 < K_{\rm f} < 1$. In the proposed current loop, to stabilize the current loop, $u_{\rm g}(k+1)$ derived from $u_{{\rm g}\alpha}(k)$ and $u_{{\rm g}\beta}(k)$ obtained by the second-order generalized integral phase-locked loop (SOGI-PLL) in the $\alpha-\beta$ coordinate system at the kth sample is used as the feedforward component of the current loop [25], and it can be obtained that

$$G_{\rm f}(z) = zG_{\rm SOGI}(z). \tag{16}$$

In the proposed method, part of the DPCC output flows through the Butterworth filter of the RC, and the other part

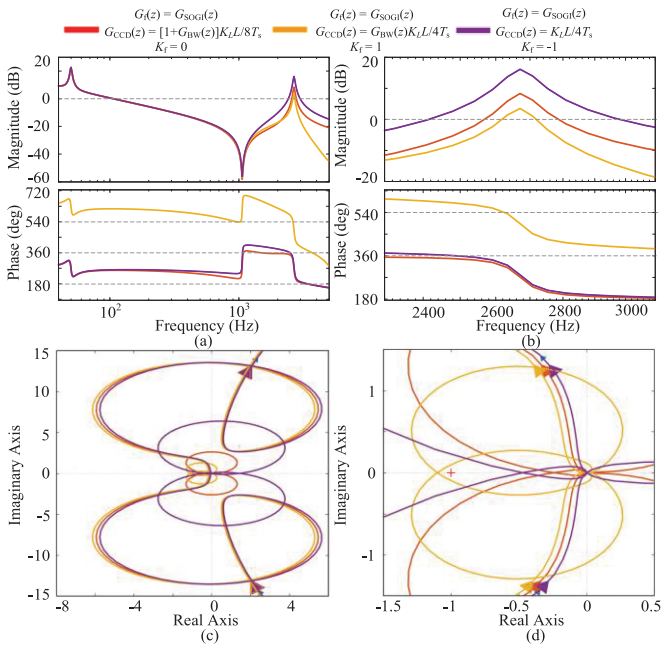

Fig. 12. (a) Bode diagram of $G_{\mathrm{open}}(z)$. (b) Partially enlarged bode diagram of $G_{\mathrm{open}}(z)$ near 2.6 kHz. (c) Nyquist graph of $G_{\mathrm{open}}(z)$. (d) Locally enlarged nyquist graph of $G_{\mathrm{open}}(z)$ near $(-1, \mathrm{j}0)$.

outputs directly. The current loop expression of the DPCC $G_{\mathrm{CCD}}(z)$ can be expressed as

$$G_{\mathrm{CCD}}(z) = \frac{K_L L}{8T_{\mathrm{s}}}\left[(1+K_f)G_{\mathrm{BW}}(z) + 1 - K_f\right]. \qquad (17)$$

Since the structure of the RC in the proposed current loop remains unchanged, and it is known from the selection and analysis of $Q(z)$ in Section II-B that the adopted RC has little impact on the high-frequency band, the RC is not considered for the purpose of simplifying the subsequent analysis. The Bode diagram comparison between the traditional DPCC scheme and the proposed scheme when K_{f} is 0, 1 and -1, respectively, is shown in Fig. 12. It can be seen from (17) that when $K_{\mathrm{f}} = 0$, half of the output of the DPCC passes through the Butterworth filter and half is directly output; when $K_{\mathrm{f}} = 1$, all the output of DPCC passes through the Butterworth filter; when $K_{\mathrm{f}} = -1$, all the output of the DPCC outputs directly. It can be seen in Fig. 12 that when considering the grid impedance, there is a resonance peak near 2.6 kHz in the Bode diagram, which is due to the resonance between the line impedance and the filter capacitors and inductors of the converter. The gain of the DPCC in the high-frequency band is equivalent to increasing the R in the filter inductors [32], which is supposed to suppressing the resonance peak. However, the existence of control delay will make the current loop unstable when the gain is large. In the proposed control method, the gain of the current controller in the high-frequency band can be reduced by increasing the value of K_{f}, and the resonance peak can be suppressed, so as to increase the stability margin and avoid the high-frequency oscillation of the input current. However, it is worth noting that when K_{f} is taken as 1, the current controller has no control ability at the high-frequency band, and its open-loop transfer function drops at the phase of resonance peak and passes through 540 °, which will make the system unstable. The corresponding results can be verified in the Nyquist diagram in Fig. 12(c) and (d).

It can be seen that with the improved current control method of the single-phase ac–dc converter, the current control performance and the stability of the current loop under the influence of grid voltage distortion and grid impedance can be improved.

D. Comparison Between the Existing Control Schemes and the Proposed Method

A detailed comparison between several existing current control methods and the proposed current control method for the ac–dc converters have been listed in Table I, mainly containing the following nine aspects.

1) *Current controller type:* Predictive controllers, such as DPCC and model predictive current control (MPCC), are increasingly adopted in the current control loop of the converter, which are often combined with the PR or RC to achieve improved harmonic suppression performance.
2) *Input current control:* Compared with the limited current gain of the DPCC and MPCC [23], PR and RC have satisfactory static tracking performance on periodic signals.
3) *Grid harmonics effect for current control:* The harmonic component in the grid voltage has a great impact on the input current control performance [21], [23], requiring additional PR or RC. However, it may be necessary to add multiple PRs according to the frequency analysis of the harmonics when adopting the PR controller.
4) *Grid impedance effect for current control:* The existence of grid impedance may make the current loop unstable. In the proposed scheme, K_{f} is introduced to improve the stability of the current loop under the influence of grid disturbance. In addition, the grid impedance has minor impact on the control performance of the control method in [23], while it requires additional sensors.
5) *Neutral point voltage balance control effect for current control:* According to Section II-B, the current controller should have low gain for the DC signal in the adopted single-phase ac–dc converter. Therefore, when the PI or traditional RC controller is used, the input current control loop may be unstable.
6) *Calculation burden:* Due to the addition of RC, the calculation burden of the proposed method is higher than that of the DPCC in [12].
7) *Deadtime compensation:* The deadtime will distort of the input current. The deadtime compensation can be achieved by adopting the compensation schemes or adding the current controllers with improved low-frequency harmonic suppression performance.
8) *Dynamic performance:* The dynamic responses of the DPCC and PR controllers are relatively faster than that of RC, whereas the dynamic response performance of the dc-bus voltage loop is basically the same.
9) *VRS function:* In the adopted converter, the input current directly flows through the dc-bus capacitors, and resulting

TABLE I
COMPARISON BETWEEN THE EXISTING CONTROL SCHEMES AND THE PROPOSED CONTROL METHODS

Aspects \ Methods	[12]	[23]	[24]	[17]	Traditional scheme	Proposed scheme
Controller type	DPCC	DPCC, PR	MPCC	DPCC, RC	DPCC, RC	DPCC, RC
Input current control	Moderate	Good	Moderate	Good	Moderate	Good
Grid harmonics effect for current control	No	Yes	No	Yes	Yes	Yes
Grid impedance effect for current control	No	Yes	No	--	No	Yes
Neutral point voltage balance control effect for current control	Yes	Yes	Yes	No	Yes/No	Yes
Calculation burden	Low	High	High	High	Medium	Medium
Dynamic performance	Good	Good	Good	Moderate	Moderate	Moderate
Deadtime compensation	Yes	No	No	Yes	Yes	Yes
VRS function	No	No	No	No	No	Yes

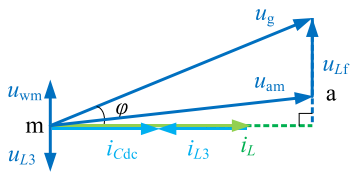

Fig. 13. Vector diagram of the VRS part.

in the degradation of their lifetime. Therefore, the VRS function is added to the converter in this article.

III. VRS FUNCTION OF THE SINGLE-PHASE AC–DC CONVERTER

Although the influence of neutral point voltage balance control error on the input current loop can be reduced, the grid-frequency voltage ripple will still affect the input current quality and capacitor lifetime. Therefore, as shown in Fig. 2, the capacitors C_1 and C_2 and phase W's switches are used to realize VRS function to reduce the current $i_{C\mathrm{dc}}$ flowing into the dc-bus capacitors through point m, so as to reduce the low-frequency voltage ripple and heating of the capacitors and prolong the lifetime of the converter. Based on the Kirchhoff's current law, it can be deduced that

$$i_{C\mathrm{dc}} = i_{L1} + i_{L2} + i_{L3} = i_L + i_{L3} = i_{C1} - i_{C2}. \tag{18}$$

The voltage and current vector diagram of the VRS part of the single-phase ac–dc converter is shown in Fig. 13, where φ is the PF angle between the grid voltage and input current, and u_{Lf} is the voltage of the equivalent filter inductor of U and V phases. Corresponding to (1), it can be obtained that

$$u_{Lf} = \frac{L_f}{2}\frac{\mathrm{d}i_L}{\mathrm{d}t}. \tag{19}$$

The current stress flowing into the capacitors can be reduced by controlling the phase W switches to make the phase of i_{L3} opposite to the phase of the input current i_L. However, since more switching actions are introduced into the phase-leg W, the addition of the VRS function may reduce the efficiency of

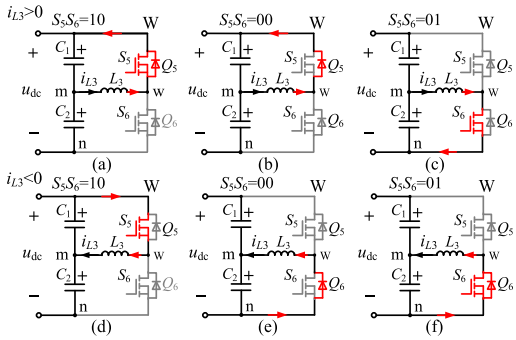

Fig. 14. Operation mode diagram of the half-bridge leg W in the process of S_5 turn-OFF and S_6 turn-ON. When $i_{L3} > 0$ in the process, (a) $S_5S_6 = 10$, (b) $S_5S_6 = 00$, and (c) $S_5S_6 = 01$. When $i_{L3} < 0$ in the process, (d) $S_5S_6 = 10$, (e) $S_5S_6 = 00$, and (f) $S_5S_6 = 01$.

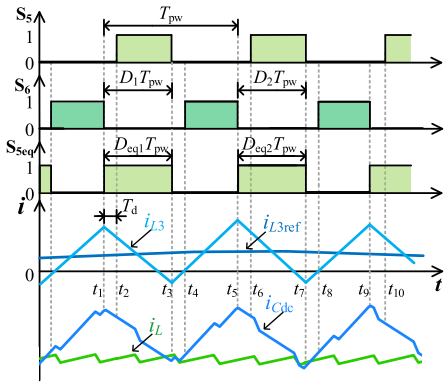

Fig. 15. Schematic diagram of the inductor current i_{L3}.

the converter. Fig. 14 shows the operation mode diagram of the half-bridge leg W in the process of S_5 turn-OFF and S_6 turn-ON, and Fig. 15 shows the schematic diagram of the inductor current i_{L3}, where T_{pw} is the switching period of the phase W switches, and $S_{5\mathrm{eq}}$ is the equivalent switch signal of S_5 after adding the deadtime T_{d} in the modulation. It can be seen that when the waveform of i_{L3} has a zero-crossing point in a switching cycle, the switch can be turned ON with zero-voltage switching (ZVS)

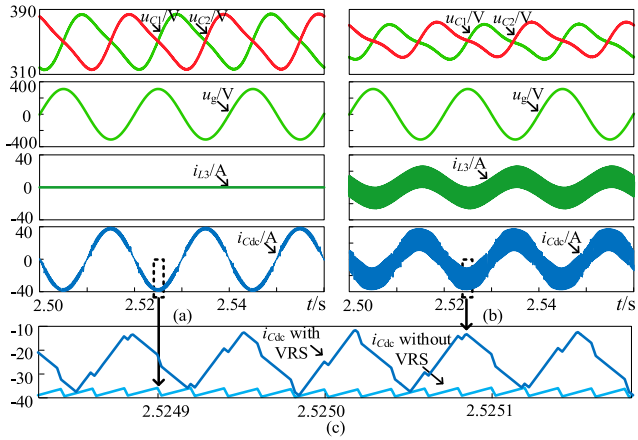

Fig. 16. Main single-phase AC–DC converter simulation waveforms with (a) the PFC part, (b) the PFC and VRS parts, and (c) i_{Cdc} waveforms comparison.

[33], [34], [35], and the dc-bus capacitors C_1 and C_2 can get charged and discharged through L_3 and W phase. In the VRS part used in this article, a reference current i_{L3ref} is calculated to make the phase W switches to realize ZVS in the full load range. Fig. 16 shows the simulation results with and without the VRS part. It can be seen from Figs. 15 and 16 and (18) that without the VRS part, the amplitude of i_{Cdc} will be the same as i_L. By adopting the VRS function, the i_{Cdc} flowing through the dc-bus capacitors can be significantly reduced, so as to decrease the low-frequency voltage ripples of the capacitors and prolong their lifetime.

The reference current i_{L3ref} of the VRS part can be expressed as

$$i_{L3ref} = -K_V i_{Lref} \tag{20}$$

where K_V is the reference coefficient of the VRS current i_{L3}. Considering the current stress of the switches and the suppression performance of the voltage ripples of the dc-bus capacitors, the value of K_V ranges from 0.3 to 0.5. Similar to the derivation of the DPCC in the input current loop [12], [25], the expression of the VRS current loop can be obtained as

$$D_w(k) = \frac{u_{C2}(k+1) - \frac{K_L L_f}{2T_s}\left[-K_V i_{Lref}(k+1) - i_{L3}(k)\right]}{u_{dc}}. \tag{21}$$

As shown between t_5 and t_{10} in Fig. 15, if the switches S_5 and S_6 operates in the critical current mode, it follows that

$$u_{C1} = L_f \frac{\Delta i_{L3}}{\Delta t} + D_w u_{dc} \tag{22}$$

where $\Delta i_{L3} = -2i_{L3ref}$ and $\Delta t = D_w(k)T_{pw}$. Therefore, it can be further deduced that the expression of K_V is

$$K_V = -\frac{D_w(k)T_{pw}}{L_f i_{Lref}(k+1)}(u_{C1} - D_w u_{dc}). \tag{23}$$

During t_5–t_7, it can be approximately considered that $S_5/S_6 = 1/0$, that is, the modulation index D_w is 1. When S_5 and S_6 operates in the critical ZVS conduction mode, the simulation waveform of the VRS part is shown in Fig. 16(b). According to

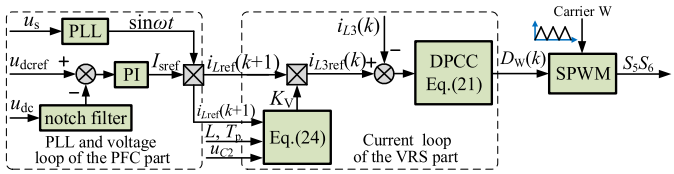

Fig. 17. Control block diagram of the VRS part of the single-phase AC–DC converter.

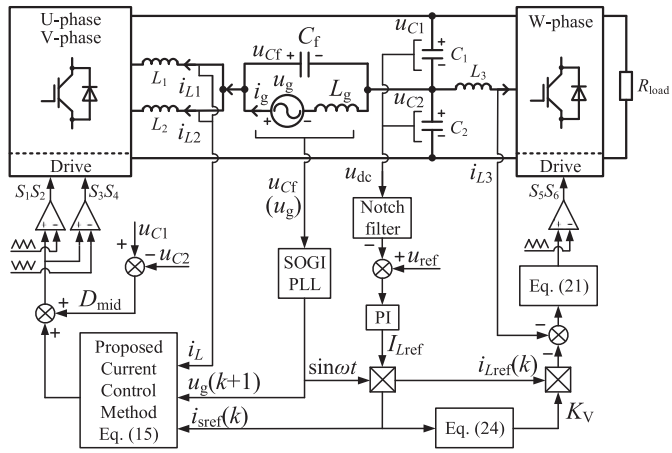

Fig. 18. Block diagram of the single-phase AC–DC converter and the improved current control method proposed in this article.

(21), it can be obtained that $u_{C1} = u_{C2}$ and $D_w(k) = 0.5$ during t_5–t_7.

Therefore, (23) can be further derived to

$$K_V = \frac{T_{pw}u_{C2}}{2L_f I_{Lref}} = \frac{T_{pw}U_s u_{C2}}{2L_f P_{out}}. \tag{24}$$

From (24), the maximum K_V ensuring the ZVS operation of the phase W switches can be deduced. While considering the current stress balance of the switches of U, V, and W phases and the efficiency of the converter, K_V is generally limited to 0.5. The control block diagram of the VRS part is shown in Fig. 17. The PLL and the dc-bus voltage control loop of the PFC part is multiplexed to obtain i_{Lref}. The phase W switches are controlled with the DPCC scheme to realize the VRS function, so as to suppress the current and voltage ripples at the grid fundamental frequency of the dc-bus capacitors and to prolong the lifetime of the converter.

IV. Experimental Results and Analyses

The block diagram of the single-phase ac–dc converter and the improved current control method proposed in this article are shown in Fig. 18. In order to verify the feasibility and effectiveness of the improved control strategy, a single/three-phase ac–dc converter prototype with 7.4 kW rated power during single-phase operation is developed, as shown in Fig. 19. The control methods are implemented in the digital signal processor TMS320F280049 of Texas Instruments. The experimental parameters are given in Table II.

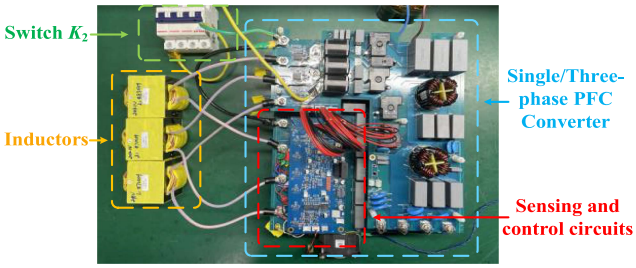

Fig. 19. Prototype of the single/three-phase AC–DC converter.

TABLE II
EXPERIMENTAL PARAMETERS

Parameters	Values
AC voltage RMS U_g/V	230
AC voltage frequency f_g/Hz	50
DC voltage reference u_{dcref}/V	720
Input filter inductor L_1, L_2, L_3/μH	470
Input filter capacitor C_f/μF	10
DC-bus capacitor C_1, C_2/μF	4×660
PWM frequency of U, and V phases f_{p1}/kHz	25
PWM frequency of W phase f_{p2}/kHz	15
Sampling frequency f_s/kHz	10
Rated output power P_{out}/W	7400

TABLE III
CURRENT THD_i AND PF WITH DIFFERENT $Q(z)$ IN THE RC WHEN P_{OUT} = 7400 W AND $L_G = 0$

Methods	THD_i	PF
$Q(z) = Q_{LPF}(z)$	9.06%	0.9833
$Q(z) = K_q$	4.83%	0.9983
Proposed $Q(z)$	3.13%	0.9992

The experimental waveforms and the Fourier analysis diagram of the input current when $P_{out} = 7400$ W with different $Q(z)$ in the RC are shown in Fig. 20, whereas the THD of the grid current THD_i and the PF are listed in Table III. In this experiment, the ac–dc converter is directly connected to the single-phase power grid without additional grid impedance, and the THD of the grid voltage THD_u is about 3.00%. As shown in Fig. 20(a), when the low-pass filter $Q_{LPF}(z)$ is used as $Q(z)$, the THD_i is 9.06% and the PF is 0.9833. It can be seen that the grid current is distorted greatly, the current waveform is asymmetric, and there is a large DC component. Therefore, as analyzed in Section II-B, $Q(z)$ of the RC in the input current loop of the adopted ac–dc converter cannot be selected as a low-pass filter. When a constant 0.96 is used as $Q(z)$ in the RC, the experimental waveform is shown in Fig. 20(b). It can be seen that the distortion of the grid current is significantly reduced, the THD_i is 4.83%, and the PF is 0.9983. With the proposed $Q(z)$, the THD_i is further reduced to 3.13% and the PF increases to 0.9992. According to the Fourier analysis diagram of the grid current in Fig. 20(d), when the DC gain of the current loop is reduced by selecting $Q(z)$ in the RC, the input current loop of the converter can operate stably, and its DC component under full load is also significantly reduced. The second-, third-, and fifth-order harmonic current components of the proposed scheme are reduced by 36.25%, 11.47%, and 53.81%, respectively, compared with those of the scheme with $Q_{LPF}(z)$ used as $Q(z)$, and it lessens the harmonic currents with the THD_i decreasing by 1.71% compared with the scheme in which K_q is used as $Q(z)$. It can be seen that the proposed scheme not only reduces the DC component of the grid current, but also improves the control performance on the low-order harmonics. Therefore, the power quality at the grid side is improved, making the converter more suitable for the application in the power grid with harmonic voltage.

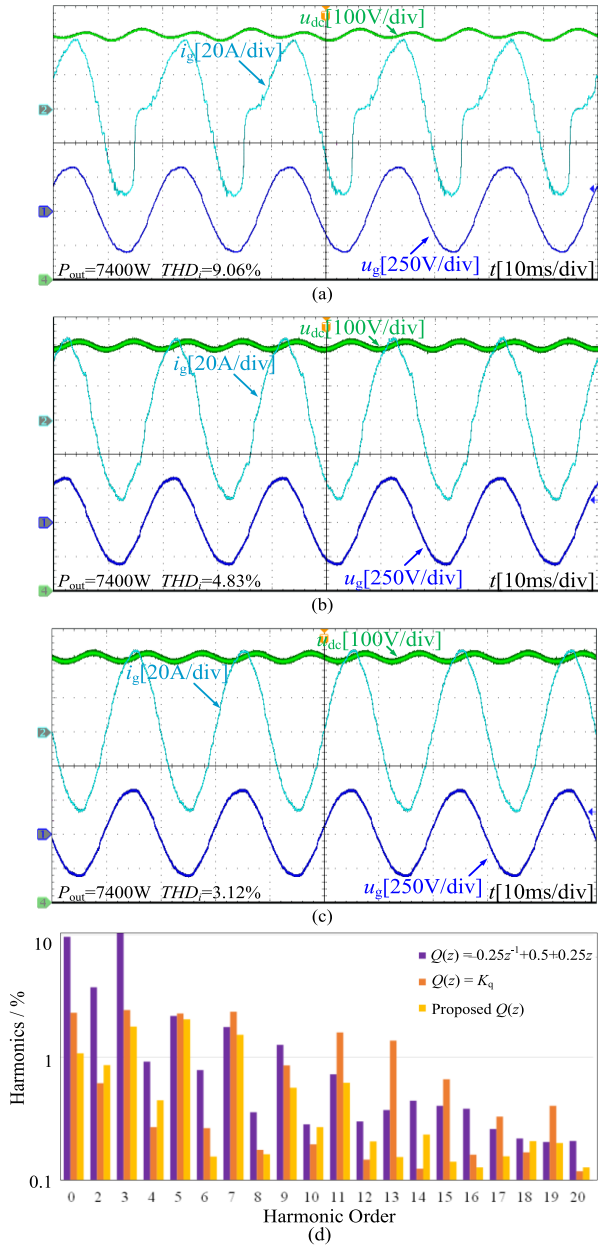

Fig. 20. Experimental waveforms of the grid voltage, input currents, and DC output voltage. (a) $Q(z) = Q_{LPF}(z)$. (b) $Q(z) = K_q$. (c) Proposed $Q(z)$. (d) Fourier analysis of the grid currents when $P_{out} = 7400$ W and $L_g = 0$.

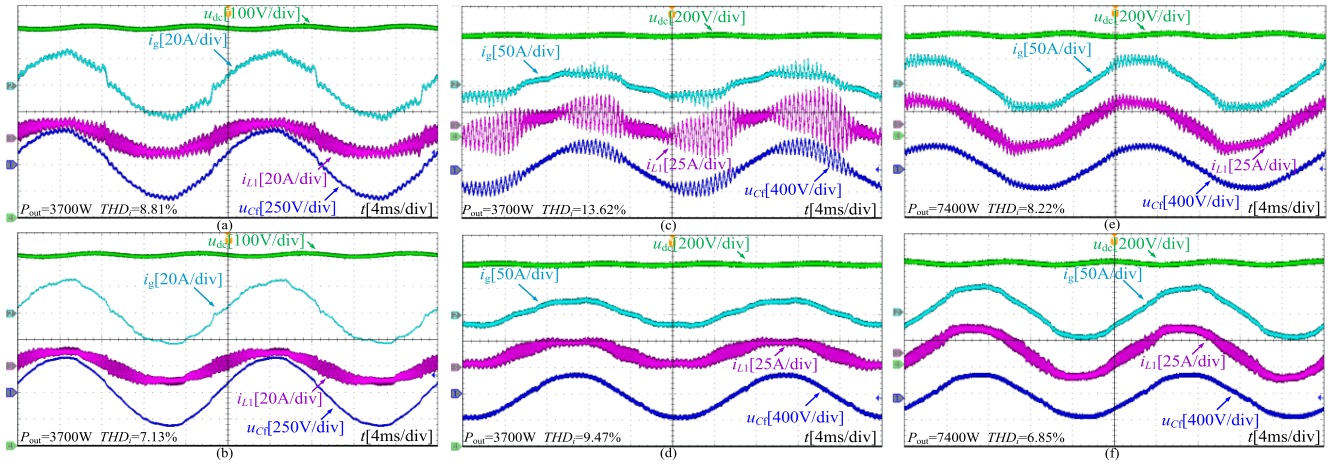

Fig. 21. Experimental waveforms of grid voltage, input currents, and DC-bus voltage. (a) Traditional scheme when $P_{\rm out} = 3700$ W and $L_{\rm g} = 2.5L_{\rm f}$. (b) Proposed scheme when $P_{\rm out} = 3700$ W and $L_{\rm g} = 2.5L_{\rm f}$. (c) Traditional scheme when $P_{\rm out} = 3700$ W and $L_{\rm g} = 3.2L_{\rm f}$. (d) Proposed scheme when $P_{\rm out} = 3700$ W and $L_{\rm g} = 3.2L_{\rm f}$. (e) Traditional scheme when $P_{\rm out} = 7400$ W and $L_{\rm g} = 3.2L_{\rm f}$. (f) Proposed scheme when $P_{\rm out} = 7400$ W and $L_{\rm g} = 3.2L_{\rm f}$.

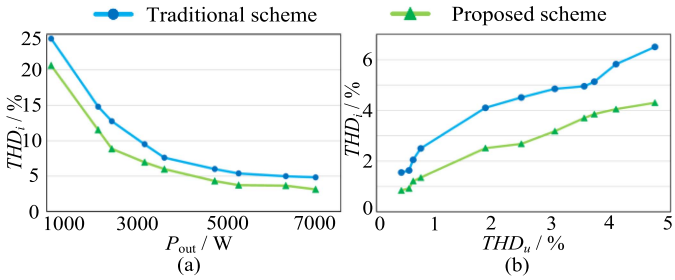

Fig. 22. Grid current THD_i curves. (a) THD_i at different input powers. (b) THD_i at different grid voltage THD_u when $P_{\rm out} = 7400$ W and $L_{\rm g} = 0$.

TABLE IV
CURRENT $THD_{\rm i}$ WHEN ADOPTING DIFFERENT CURRENT CONTROL SCHEMES WITH DIFFERENT $P_{\rm OUT}$ AND $L_{\rm G}$

$P_{\rm out}$	$L_{\rm g}$	Methods	THD_i
3700 W	$2.5L_{\rm f}$	Traditional scheme	8.81%
		Proposed scheme	7.13%
	$3.2L_{\rm f}$	Traditional scheme	13.62%
		Proposed scheme	9.47%
7400 W	$3.2L_{\rm f}$	Traditional scheme	8.22%
		Proposed scheme	6.85%

However, in addition to the harmonic voltage, there are often grid impedance in the power grid, which may form a resonant loop with the input filter capacitors and inductors at the grid side of the converter under the harmonic voltage of the power grid, resulting in the reduction of the efficiency of the converter, the deterioration of the power quality at the grid side and even trigging the overcurrent protection of the system. Therefore, it is necessary to further improve the stability of the input current control method when considering the grid disturbance. After adding an inductor $L_{\rm g}$ as the grid impedance between the converter and the power grid, a comparative experiment between the traditional input current control method and the improved method is carried out. In the traditional method, the grid voltage feedforward is obtained by SOGI-PLL, and $Q(z) = 0.96$, to verify the effectiveness of the proposed method while maintain stable operation.

With the addition of $L_{\rm g}$, it is worth noting that u_{Cf} refers to the grid voltage near the converter, and it is the grid voltage signal that the controller samples, while $u_{\rm g}$ can be seen as the voltage of the remote power grid. Therefore, the waveforms of u_{Cf}, input currents, and the dc-bus voltage are shown in Fig. 21, and the grid current THD_i when adopting the traditional and proposed current control schemes are listed in Table IV. When $P_{\rm out} = 3700$ W, $L_{\rm g} = 2.5L_{\rm f}$, and the traditional control method is adopted, as shown in Fig. 21(a), the grid current THD_i of the converter is 8.81% and the PF is 0.9783. Moreover, there are 2.55 kHz high-frequency harmonics on i_{L1} and $i_{\rm g}$, and this frequency is basically consistent with the 2.6 kHz resonant peak frequency obtained from the open-loop transfer function analysis of the current loop in Fig. 12(b). When the improved scheme is adopted, the PF of the grid current rises to 0.9912, and the grid current $THD_i = 7.13\%$, in which the reactive power at the grid side is reduced from 786 Var to 494 Var, and the THD_i is reduced by 1.68% at half load.

When $P_{\rm out} = 3700$ W, $L_{\rm g} = 3.2L_{\rm f}$, and the traditional scheme is adopted, the THD_i increases to 13.62%, and the current distortion rises with the increase of the grid impedance, and there is a large high-frequency current harmonic at 2.4 kHz, which will cause the noticeable distortion of u_{Cf} at the grid side of the converter. When the proposed scheme is used, it can be seen that the high-frequency oscillation components in i_{L1} and $i_{\rm g}$ are eliminated, and the THD_i is reduced to 9.47%. Similarly, at full load operation, when the THD_u is about 4.00% and $L_{\rm g} = 3.2L_{\rm f}$, compared with the traditional method, the proposed current control method reduces the THD_i by 1.37% to 6.85% and suppress

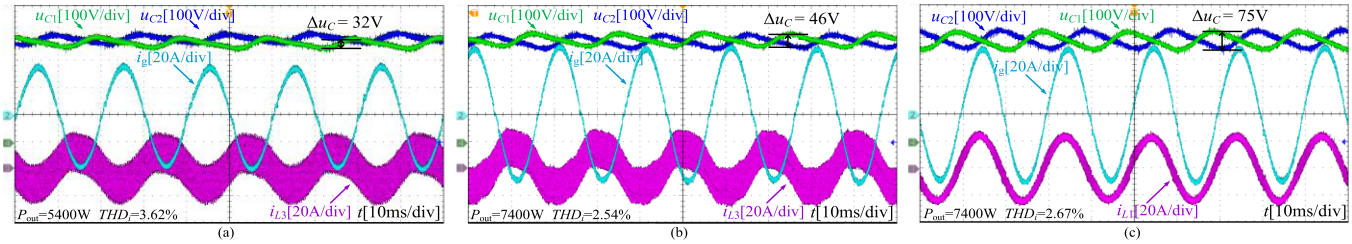

Fig. 23. Experimental waveforms of input currents and DC-bus voltages with (a) the PFC and VRS parts when $P_{\rm out} = 5400$ W, (b) the PFC and VRS parts when $P_{\rm out} = 7400$ W, and (c) the PFC part when $P_{\rm out} = 7400$ W and $L_{\rm g} = 0$.

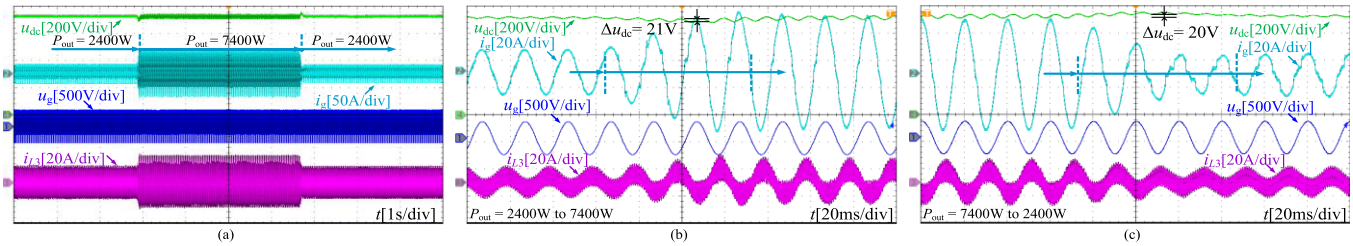

Fig. 24. Experimental waveforms of grid voltage, input currents, and DC-bus voltage. (a) Process of the load mutation with PFC and VRS parts. (b) Transient process when $P_{\rm out}$ steps from 2400 to 7400 W. (c) Transient process when $P_{\rm out}$ steps back from 7400 to 2400 W.

the oscillation current at the grid side. It can be seen that the improved scheme not only improve the power quality at the grid side, but also improve the stability and control performance of the current control loop when the power grid has harmonics and line impedance. Fig. 22 illustrates the THD_i of the grid current of the single-phase ac–dc converter when using the traditional and the proposed control methods at different output powers and different THD_u of the grid voltage, without additional grid impedance. In Fig. 22(a), the THD_u of the grid voltage is about 3.00%. With the increase of $P_{\rm out}$, the THD_i of the grid current with both current control methods will decrease. The THD_i of the proposed scheme is lower than that of the traditional scheme. It is worth noting that the THD_i of the grid current has been about 5% at 0.6 times the rated power, while the THD_i meets the limitations at about 0.9 times the rated power with the traditional scheme. Fig. 22(b) is the curve of grid current THD_i under different grid voltage distortion when $P_{\rm out} = 7400$ W. It can be seen that with the rising of the grid voltage THD_u, the THD_i of the grid current with both control methods is increased, and the THD_i with the improved method is lower than that of the traditional scheme.

In order to verify the VRS function of the ac–dc converter, the comparison experiments before and after the VRS function is added are carried out in this article. Fig. 23 shows the waveforms of the PFC and VRS parts when the output power is 2/3 load and full load, respectively. It can be seen that under different output powers, the phase of i_{L3} is opposite to the input current with the VRS control method, so as to reduce the low-frequency voltage ripples of the dc-bus capacitors and prolong their lifetime. As shown in Fig. 23(c), when only the PFC part of the converter operates at rated power, the low-frequency voltage ripple Δu_C of the dc-bus capacitors C_1 and C_2 is 75 V. It can be seen from Fig. 23(b) that when the PFC and VRS operate at the same time, the capacitor voltage ripple can be reduced to 46 V, which is about 40% lower, without affecting the input current control performance. In addition, under different power levels, the waveform of i_{L3} always has zero crossing point in one switching cycle, and the W-phase switches realizes ZVS, thus reducing the loss of the VRS part.

TABLE V
DYNAMIC RESPONSE OF THE SINGLE-PHASE AC–DC CONVERTER TO LOAD MUTATION

$\Delta P_{\rm out}$	$\Delta u_{\rm dc}$	$\Delta u_{\rm dc}$ / $u_{\rm dcref}$	Transition time
2400–7400 W	21 V	2.92%	64 ms
7400–2400 W	20 V	2.78%	75 ms

In order to verify the dynamic performance of the converter with the PFC and VRS parts, Fig. 24 and Table V show the experimental results. It can be seen from Fig. 24 that the output power $P_{\rm out}$ steps from 1/3 of the rated load to full load, and then switched back to 1/3 of the rated load. The converter can maintain stable operation throughout the process. In the transient process when $P_{\rm out}$ steps from 2400 to 7400 W shown in Fig. 24(b), it can be seen that the dynamic process lasts about 64 ms, and the dc-bus voltage of the converter drops about 21 V, and $\Delta u_{\rm dc}$ is only 2.92% of the rated $u_{\rm dc}$. There is no obvious overshoot in the grid current $i_{\rm g}$ and the inductor current i_{L3} of the VRS part. i_{L3} changes with the change of $i_{\rm g}$, and thus reducing the current ripple flowing into the dc-bus capacitors under different output power. In the transient process of the load step-down shown in Fig. 24(c), it is noted that system reaches the steady state within approximately 75 ms, and the dc-bus voltage drop is about 20 V, while $\Delta u_{\rm dc}$ is within 3.0% of rated

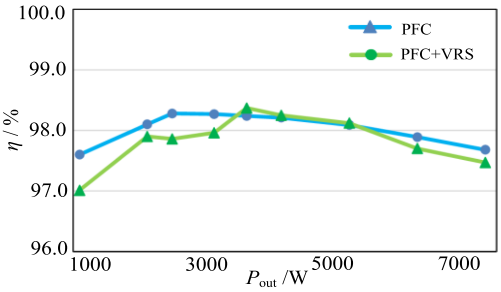

Fig. 25. Efficiency of the single-phase AC–DC converter at different input powers.

u_{dc}. Due to the application of the RC, when the amplitude of the input current is relatively small, the distortion caused by the deadtime will be relatively obvious during this dynamic process. In contrast, the current loop of the VRS part adopting the DPCC has fast dynamic tracking performance.

Fig. 25 shows the efficiency comparison of the adopted ac–dc converter when only the PFC part operates and the PFC and VRS parts operate at the same time, which is measured by the power analyzer. It can be seen that the VRS part has a greater impact on the converter efficiency under light load. However, when the converter operates at a power greater than half loading, the heating loss of the capacitors increases due to the parasitic resistance of the dc-bus capacitors. Therefore, the operation of the VRS part, with the switches achieving ZVS turn-ON, has little impact on the efficiency of the converter, which is less than 0.2%, and is favorable to extending the lifetime of the converter.

V. Conclusion

An improved current control method, which is based on the combination of DPCC and RC, for the single-phase operation mode in single/three-phase charging system is proposed in this article to cope with the degraded performance caused by the external grid disturbance and internal control errors. In this scheme, a modified $Q(z)$ in the RC is selected to make the input current loop avoid the influence of the control error and have a better control performance on current harmonics. At the same time, by introducing the weighting factor K_f of the DPCC output and by multiplexing the filter in the RC, the stability of the current control loop can be increased under the nonideal grid condition, while the grid-side power quality of the converter can be improved, which makes the charging system adapt better to a wide range of application scenarios. In addition, in the adopted ac–dc converter, the phase-leg W is used to form a VRS part, which reduces the low-frequency voltage ripple of the dc-bus capacitors, thus reducing the heating of the capacitors and improving the reliability of the converter. Finally, the experimental results show that the proposed method has better steady state performance and improved stability than the traditional method, and is more suitable for single/three-phase EV charging system.

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