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Fast System to measure the dynamic on-resistance of on-wafer 600 V normally off GaN HEMTs in hard-switching application conditions

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Abstract: This study presents a novel system to investigate the on-wafer level dynamic properties of GaN-based power transistors in hard-switching application conditions. The system is able to analyse devices with an on-resistance (R_{DSON}) in the range from few ohms to hundreds of ohms, and can be effectively used to improve the development process of GaN high electron mobility transistors (HEMTs) power devices at the wafer level. Contrary to the conventional double-pulse setup, where a resistive load is usually used in combination with a very low duty cycle, the dynamic R_{DSON} is acquired during realistic operating conditions, in a boost converter circuit. Consequently, the authors' system is able to study not only the field-activated trapping processes, but also those induced by hard-switching conditions, i.e. promoted by hot electrons and self-heating. The maximum working voltage (600 V) and the minimum R_{DSON} measurement time after turn-on (2 μs) allow evaluating the operation limit of the devices in a voltage/frequency range close to real switching conditions. Working on the wafer level allows a more realistic assessment of the dynamic R_{DSON} behaviour before the packaging phase, which is very important to improve the production and development process of GaN-HEMT devices.

1 Introduction

GaN high electron mobility transistors (HEMTs) are promising devices for high-power and high-voltage applications [1]. Thanks to their high breakdown voltage and their high switching speed, GaN HEMTs permit a great improvement of power electronic circuits in terms of conversion efficiency and size. For rapid market penetration, a deep understanding of device dynamic properties is crucial. One of the main problems of power GaN HEMTs is the dynamic R_{DSON}, i.e. the recoverable increase in on-resistance induced by the exposure to high voltage [2, 3]. The main causes of the R_{DSON} increase are (i) the charge trapping during high-voltage off-state biasing due to the high electric field [4], (ii) the charge trapping due to hot electrons created during hard-switching transients [5] and (iii) the increase of the junction temperature (T_j) due to self-heating [6].

Typically (see for instance [4–6]), the devices are tested in particular laboratory conditions in order to study R_{DSON} variation. This approach (based on conventional double-pulse measurements) suffers from the problem that (i) the devices are tested far from the switching operation conditions which may occur in a real power converter, namely with a very low duty cycle (<0.01, corresponding to negligible self-heating) and with resistive load. In addition, (ii) all the stress conditions (e.g. high electric field, high gate bias etc.) are applied separately, which is not the case in a real power converter where high temperature, voltage and current levels may be simultaneously present. Moreover, the assessment of the real switching operation is crucial for the reliability of GaN-HEMT power devices [7, 8], and in the literature some reports have already highlighted the importance of characterising the dynamic R_{DSON} during real operation [9, 10]. These reports have some limitations: in [10] a resistive load is used to emulate the real hard-switching operating mode. In [9] the measurement is carried out via a controlled current power supply: this approach increases the accuracy in the R_{DSON} measurement but can affect the switching power losses with respect to the real inductive load environment. Finally, contrary to our work, the authors in [9, 10] use the package level devices.

This work presents a novel system which is able to study the dynamic R_{DSON} of on-wafer GaN-HEMT devices working under switching operation conditions, by adopting – for the first time in the authors knowledge – an on-wafer device as switching transistor for a diode-based boost DC – DC converter. In this way, the on-wafer device under test (DUT) is analysed while working in hard-switching conditions – i.e. with high voltage and current transients simultaneously applied to the device.

The system emulates the switching application conditions responsible for the R_{DSON} variation: (i) the change of T_j, (ii) the hard-switching 'locus' i.e. the hard-switching working bias points set (which also crosses the semi-on state) and (iii) the high electric field due to the high-voltage operation. With such a system, a more realistic performance assessment of on-wafer GaN power HEMTs is now available, thus shortening the loop in the development process of such technology. In fact, the operation in a power converter is typically evaluated only after the device packaging at the end of the production process because it is very difficult to make an on-wafer device working close to real application conditions due to the contacting system, which inserts the additional series resistance and inductance.

In order to compare the system developed within this paper and some of the most widespread previous state-of-the-art techniques used in the literature to measure the R_{DSON}, Table 1 reports a comparison of the most important papers regarding the GaN-HEMT dynamic R_{DSON} characterisation. For each technique, the main results achieved in this paper are reported. Moreover, Table 2 reports a comparison of transistors typology, maximum testing voltage, testing load type and type of switching (hard or soft switching) used for each work. In [11] Bisi *et al.* developed a technique that is able to investigate the impact of the high off-state voltage on the dynamic R_{DSON}. Such a system works in soft switching and is useful to characterise the trapping mechanisms

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activated by the high off-state electric field. The technique proposed by Rossetto *et al.* [12] is useful to analyse the impact of hot electrons during hard-switching conditions but cannot emulate the real application environment. Rossetto *et al.* [12] demonstrated that during hard-switching operation hot electrons could appear within the structure of the device causing an increase of the dynamic R_{DSON}. Badawi *et al.* [13] tested GaN-HEMT package devices in real hard-switching conditions demonstrate that increasing of voltage, current, temperature and frequency causes an increase of the dynamic R_{DSON}. Finally, Hwang *et al.* [5] and Lu *et al.* [10] tested GaN HEMTs in hard switching, showing that this condition is detrimental in terms of increase of the dynamic R_{DSON}.

Table 1 Boost converter mesaurement settings

Symbol	Quantity	Value
D	duty cycle	0.80
F_{SW}	switching frequency	100 kHz
R_{LOAD}	load resistor	150 kΩ
V_{IN}	input voltage	from ∼12 to ∼120 V
V_{OUT}	output voltage	from ∼60 to ∼600 V

Table 2 Boost converter mesaurement settings

Reference	Main result	Type of devices	Max voltage/ load type	Type of switching
Bisi *et al*. [11]	comprehensive characterisation of the charge-trapping phenomena under high-voltage operation	on-wafer normally on	200 V resistive	soft switching
Rossetto *et al*. [12]	under hard-switching conditions, GaN HEMTs show a measurable increase in dynamic R_{DSON} and hot electrons appear	on-wafer normally on	600 V resistive	soft switching hard switching
Badawi *et al*. [13]	high off-state voltage, high switched drain current at high junction temperature and high-frequency operation cause an increase of the R_{DSON}	on-package normally off normally on	300 V inductive	hard switching
Hwang *et al*. [5]	hot electrons in the channel generated in the high power state during switching causes significant current collapse	on-wafer normally off	400 V resistive	hard switching
Lu *et al*. [10]	off-state drain voltage is the main cause for the increase of the dynamic R_{DSON}. Switching losses in hard-switching transient could cause additional R_{DSON} increase due to hot-electron trapping	on-package normally off	200 V resistive inductive	soft switching hard switching
this work	off-state drain voltage can cause increase of the dynamic R_{DSON}. Hard switching can cause additional R_{DSON} increase due to increase of the channel temperature and hot electrons trapping	on-wafer normally off	600 V inductive	hard switching

2 Device description and pulsed characterisation

In order to show the capabilities of the system, devices from two different GaN on Si wafers with different performance in terms of R_{DSON} variation during operation have been analysed: wafer 1 and wafer 2, respectively, named WF1 and WF2 in the following. The analysis was carried out on transistors with gate width $W_G = 1.5$ mm, grown on a silicon substrate. The epitaxial structure consists in a semi-insulating buffer layer, an undoped AlGaN barrier, and a regrown p-GaN gate. The wafers come from two different production lots representing the evolution of the quality of the epi layers and process maturity. WF2 is an updated version of WF1 with slight adjustment of both the AlGaN barrier and metal-organic chemical vapour deposition (MOCVD) deposition parameters. The transistors are normally off, with a threshold voltage of 1.2 V, and an on-resistance of ∼15 Ω mm. The transistors under the test are on-wafer and are connected via external micro tips, which have current and contact resistance limitations. By testing such transistors, it is possible to assess the physical causes responsible for the dynamic R_{DSON}. The study of prototypal on-wafer devices is fundamental to improve the design and production processes of GaN HEMTs, and to provide rapid feedback at the foundry level. The results of this analysis can be used to estimate the performance of the final on-package scaled transistor, which have R_{DSON} in the tens of mΩ range.

Fig. 1 shows the dc output characteristics and the output double-pulse characteristics of two typical transistors of the two wafers. In the double-pulse characterisation, the device is kept in the off-state with $V_{GS} = 0$ V and fixed V_{DS} voltage (V_{DSOFF}). Starting from this bias condition, two properly synchronised voltage pulses are applied on the gate and drain terminals for a very short time (40 µs) in order to acquire the device output pulsed characteristic (I_{DS}–V_{DS} @ fixed pulse $V_{GS} = 6$ V). By varying the V_{DSOFF} voltage, we investigate the impact of the high electric field induced in the off-state on the R_{DSON} of the transistor. The typical R_{DSON} curves as a function of the V_{DSOFF} voltage can be extracted from the curves of Fig. 1 for the two wafers — a more detailed analysis will be reported in Section 4. As can be noticed from Fig. 1, WF1 has a strong dependence of the R_{DSON} on V_{DSOFF}, with a maximum increase in the 200–300 V range. On the contrary, WF2 shows good performance and the R_{DSON} is not affected by V_{DSOFF} as desired. It is worth noticing that with this kind of measurement the transistor is tested in a 'soft' regime condition. In fact, primarily the V_{DS} imposed by external electronics is lowered and then the transistor is turned on with the gate signal. Moreover, the device does not suffer from self-heating during the R_{DSON} double-pulse measurement due to the very low duty cycle (0.01) and the very short on time ($T_{ON} = 40$ µs).

3 Characteristics of the developed system

The system developed within this work consists of a boost DC–DC converter where the switching transistor is an on-wafer device. The boost converter electronic board is directly mounted on a microscope-based probe station to allow the user to contact the power HEMT with micro tips. Moreover, the system is equipped with the measurement instrumentation, which allows studying the HEMT transistor during the hard-switching operation in the DC–DC converter.

The system meets two main requirements: (i) the need for the converter working with an on-wafer device and (ii) the need for measuring the R_{DSON} during operation, starting from 2 µs after the turning on of the device.

Therefore, the system can be divided into three main blocks (see Fig. 2). (i) The equipment used to contact the investigated

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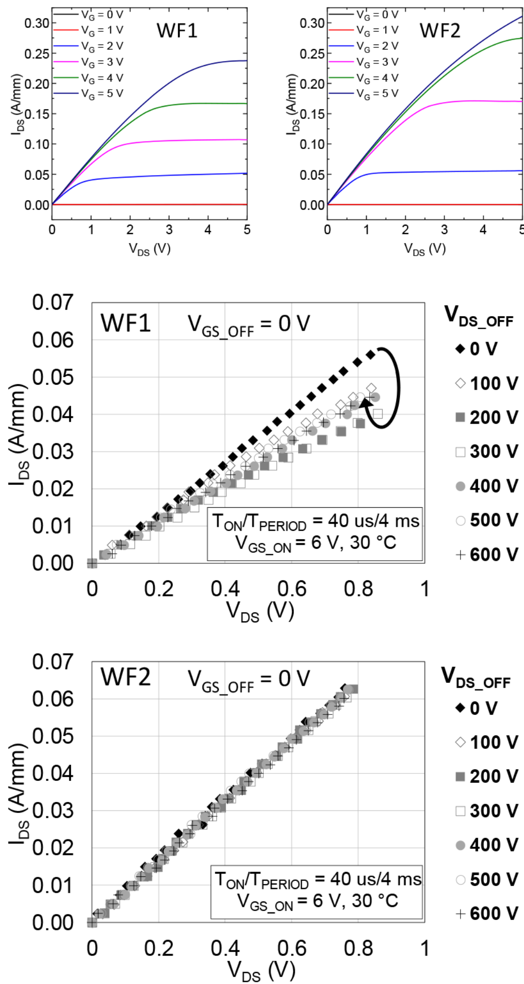

Fig. 1 *(Top) Dc characteristics of the analysed devices. (Bottom) Typical pulsed characteristics of 1.5 mm transistors of the two wafers*

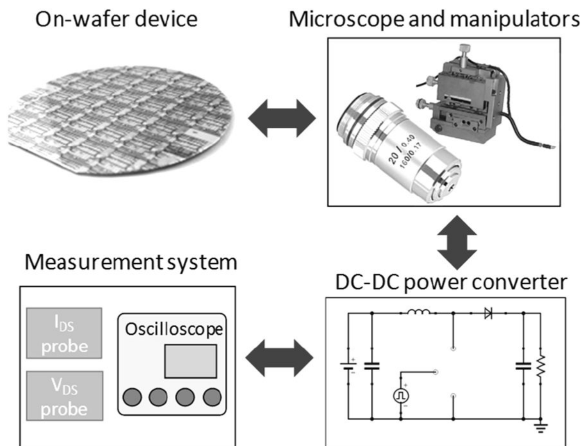

Fig. 2 *Schematic representation of the system. There are three main blocks: (i) the equipment used to contact the device including the microscope and the manipulators, (ii) the DC–DC boost power converter board and (iii) the measurement system*

transistor on the wafer including the microscope and the micromanipulators. (ii) The power converter board, which emulates the real application. (iii) The R_{DSON} measurement equipment including probes for the measurement of the voltage and the current during the transistor operation and an oscilloscope. Fig. 3 shows some photos of the setup. As can be noticed, the converter board is directly mounted on the microscope, and three wires connect the power converter board and the three tips of the manipulators [respectively gate (G), drain (D) and source (S)]. The converter board and the entire arrangement have been studied in order to minimise the length of these interconnections to minimise parasitic effects. In the following, the two most important blocks of the setup are described: the power converter board and the R_{DSON} measurement system.

3.1 Power converter board

The power converter board consists of a basic DC–DC boost converter topology. The board is equipped with all the components except for the switching transistor which is located on the wafer and has to be connected through the three manipulators previously described (respectively gate, drain and source connectors). Fig. 4 shows the schematic of the board. In order to guarantee the continuous mode operation continuous-conduction mode (CCM) in the entire range of measurements, a 20 mH inductor (L) was adopted. The diode (D) is a zero recovery silicon carbide 600 V device. The gate driving is of crucial importance in switching power converters. In fact, driving large-area power transistors requires high-pulsed gate currents and oscillations have to be avoided in order to fully exploit the performance of GaN HEMTs [14]. The high-speed integrated circuit gate driver MIC4452YN by Micrel® has been used. This driver is based on a half-bridge output stage which is able to provide high peak current (12 A) with a very low output resistance (<1.5 Ω) and it is able to provide pulses with very short rise and fall times (∼0.75 V/ns). Moreover, in order to prevent the gate voltage oscillation, an external gate series resistor of 22 Ω has been added. In turn, an external pulse generator drives the gate driver and provides the proper switching frequency and duty cycle. The power converter board is equipped with connectors in order to connect the voltage and current probes used to measure the transistor on-state drain-to-source voltage (V_{DSON}) and the on-state drain-to-source current (I_{DSON}).

3.2 Measurement equipment

In order to measure the R_{DSON} of the GaN HEMT under test, V_{DSON} and the I_{DSON} were measured with a Tektronix DPO4104B oscilloscope (see Fig. 5*a*). For the current measurement, the DC 100 MHz bandwidth Tektronix TCP0030 current probe connected to the drain wire has been used. The sensitivity of the current probe is 1 mA. On the other hand, the measurement of the on-state voltage is more complicated. In fact, the high off-state voltage leads to the oscilloscope input channel saturation [15] i.e. the distortion of the measured voltage due to the high voltage applied to the oscilloscope channel when the V_{DS} drops down from the value in the off-state (100–600 V) to the on-state one in the linear region (<2 V). To better understand the problem, Fig. 6 shows a preliminary result obtained with the system: the inductor current (I_L) and the V_{DS} of the converter are depicted in the case of constant V_{OUT} = 400 V and load resistor R_{LOAD} = 150 kΩ. As can be noticed, the V_{DS} has a rectangular shape and swings between a few volts during the on-state of the transistor and hundreds of volts (up to 600 V as maximum rating) during the off-state. In order to calculate the R_{DSON} with enough resolution the vertical scale of the oscilloscope has to be reduced at least to 1 V/div. With such a low vertical scale setting and the high voltage applied at the same time, usually oscilloscopes suffer from saturation effects resulting in the distortion of the measured voltage signal due to the overdrive of the oscilloscope input stage. In the literature, many solutions have been proposed to solve this problem (see for instance [15, 16]). In this work, the clamp circuit described in [16] was adopted. The circuit is based on a high-voltage MOSFET ($M1$) and a Zener diode ($D1$) as depicted in Fig. 5*b*. The power supply $V1$ provides a voltage (9 V) to the gate of $M1$ higher than its threshold voltage (∼1.5 V) and keeps it on when the voltage to be measured (V_{DS}) is low (less than $V1$–V_{TH}∼ 7.5 V). In fact, when $V_{DS} < (V1 - V_{TH})$, the source voltage of $M1$ is less than $(V1 - V_{TH})$, and the condition $V_{GS} > V_{TH}$ is met. When V_{DS} to be measured drops down to typically hundreds of mV, a low current flows thorough $M1$ (I_{DSM1}) because the Zener $D1$ is turned off and very low current flows thorough $R2$ due to the very high input impedance of the

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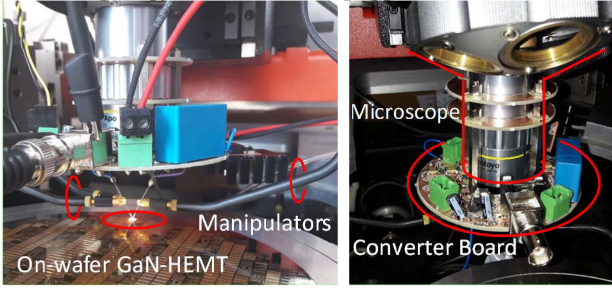


Fig. 3 *Picture of the experimental setup*

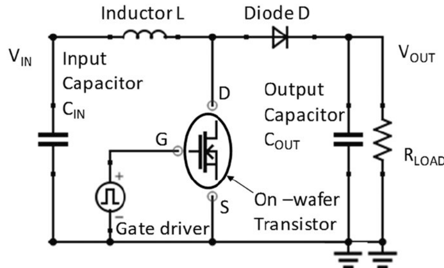


Fig. 4 *Schematic of the boost converter used for the power converter board*

oscilloscope probe. In this condition, $M1$ is turned on in linear region with a very low I_{DSM1} thus we can neglect its drain-to-source on voltage (V_{DSM1}), and the V_{DSON} of the GaN HEMT under test can be measured on the cathode of $D1$ (i.e. $V_{DS_CLAMPED} \sim V_{DSON}$ during the on phase of the DUT). On the other hand, if $V_{DS} > (V1 - V_{TH})$, the current flowing through $M1$, $D1$ and $R3$ raises, the source voltage of $M1$ increases, thus the V_{GS} of $M1$ decreases. This causes the MOSFET $M1$ to shut down when the condition $V_{GS} < V_{TH}$ is met. The voltage on the cathode of $D1$ is clamped to its Zener reverse voltage (V_Z) and the high voltage reached by V_{DS} is not applied to the oscilloscope input, thus avoiding the saturation of the oscilloscope channel. Referring to Fig. 5*b* the components resistor $R2$, fuse $F1$, diodes $D3$ and $D4$ are auxiliary and act as a safety circuit to prevent the overvoltage on the input of the oscilloscope in the case of $M1$ failure. By using this circuit, the R_{DSON} can be calculated by using the equation:

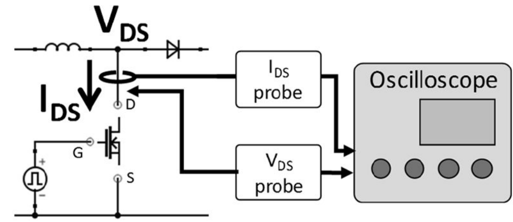
$$R_{DSON} = \frac{V_{DS_CLAMPED}}{I_{DSON}}$$

where $V_{DS_CLAMPED} \sim V_{DSON}$ during the on phase of the DUT.

Considering the noise in the V_{DS} measurement, the sensitivity of the current probe and the 8 bits resolution and the average mode of the oscilloscope, an error in the R_{DSON} measurement of ~0.5 Ω in typical measurements ($V_{OUT} \sim$ 200 V) has been estimated. Finally, it is worth mentioning in this section that by adjusting the inductor and load values, the system can also be used to measure transistors with shorter W_G (i.e. we were able to measure transistors with W_G = 150 µm). The lower limit is due to the minimum measurable on current level, which can be improved by changing the current probe.

4 Experimental details and results

This section reports the experimental details and the results of the system. The analysis is divided into five subsections in order to show (A) the measurement experimental parameters, (B) the preliminary results obtained with the voltage clamp circuit, (C) the R_{DSON} analysis on the two different wafers, (D) the strengths and potentiality of the system and (E) its limitations.



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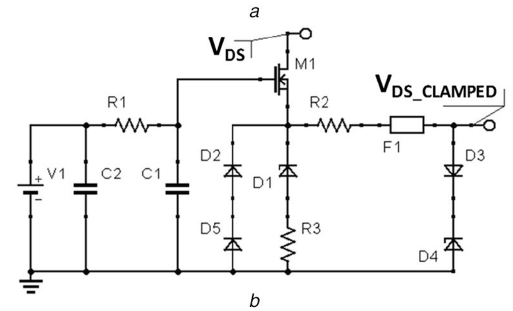

b

Fig. 5 *Schematic of the R_{DSON} measurement hardware*

(a) A current probe and a voltage probe measure the I_{DSON} and V_{DSON}, respectively. The current probe is a high sensitivity 100 MHz current probe, ***(b)*** The voltage probe is a custom voltage probe equipped with a voltage clamp circuit

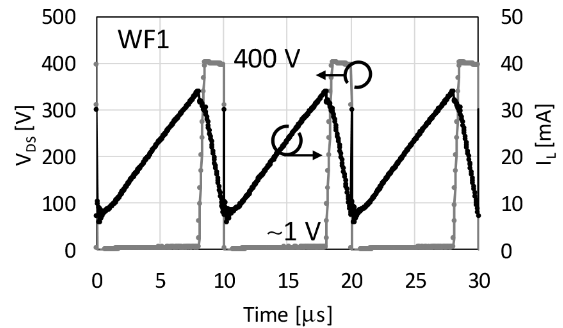

Fig. 6 *Inductor current I_L and V_{DS} voltage of the GaN HEMT under test during operation with switching frequency of 100 kHz, V_{IN} = 72.5 V, V_{OUT} ~ 400 V, load resistor R_{LOAD} = 150 kΩ. Related clamped V_{DS} waveform is reported in Fig. 7*

4.1 Measurement experimental parameters

In order to investigate the GaN-HEMT R_{DSON} variation during operation in the wafer-level boost power converter as a function of the output voltage (V_{OUT}), measurements with increasing output voltage from ~60 to ~600 V were carried out. The main parameters (duty cycle D, switching frequency F_{SW} and load resistor R_{LOAD}) of the converter were kept fixed. It is worth noticing that with this approach also the impact of the junction temperature (T_j) on the R_{DSON} is taken into account since the load is fixed and the output current and power increase with rising V_{OUT}. Table 1 summarises the boost converter settings used for the analysis of the GaN-HEMT R_{DSON}. In order to obtain the output voltage in the range from 60 to 600 V, the input voltage (V_{IN}) was adjusted between ~ 12 and ~ 120 V. For each V_{OUT}, the R_{DSON} value of the GaN HEMT is measured. It is worth noticing that the output voltage is equal to the drain-to-source voltage of the GaN HEMT when it is in the off-state ($V_{OUT} = V_{DSOFF}$) thus with this kind of measurement, the overall impact of the high voltage, temperature and hot electrons on R_{DSON} was investigated. It should be noted that the typical DC-link voltage in 230 V AC/DC converter is at around 400 V, so the output voltage range up to 600 V allows for highly accelerated stress testing of the devices. All the measurements are carried out with the substrate of the HEMT under test grounded. Parameters are chosen in order to let the boost converter work in the CCM mode (in order to obtain the hard

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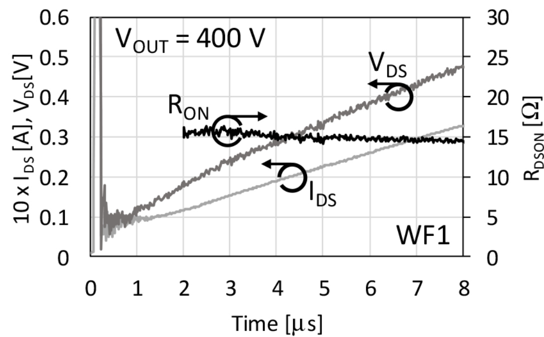

Fig. 7 *R_{DSON} measurement of the GaN HEMT under test during operation in the boost converter. V_{DS} is measured with the clamp circuit and can be considered valid after 2 µs from the turn-on gate commutation. R_{DSON} is calculated as the ratio between V_{DS} and I_{DS} during the on-state*

switching) and with a current level minimum set to obtain a V_{DSON} ∼ 0.5 V (see Fig. 7).

In this way the hard-switching condition is met, and the system can measure the R_{DSON} by measuring the V_{DSON}.

4.2 Preliminary experimental results: clamp circuit

This paragraph reports the results of the preliminary measurements carried out in order to evaluate the accuracy of the R_{DSON} measurement. Fig. 7 shows the results obtained with $V_{\text{OUT}} = 400$ V. The V_{DSON} and I_{DSON} waveforms during the on-state of the transistor are reported. The two curves are triggered with the rising edge of the gate signal i.e. the turn-on commutation of the gate signal. As can be noticed the V_{DS} and I_{DS} waveforms have a little ringing immediately after the drop of the V_{DS} from 400 V to a few volts due to the parasitics of the connection wires and the circuit. After 2 µs from the turn-on gate transition, the V_{DSON} signal can be considered valid and the R_{DSON} can be calculated as the ratio of the voltage and the current during the on-state. This timing is perfectly suitable for the assessment of the state-of-the-art GaN HEMTs, which are supposed to work up to 600 V and close to 1 MHz frequency range. The slight decrease in R_{DSON} observed after 2 µs can be ascribed to a moderate charge de-trapping.

4.3 R_{DSON} analysis results

Fig. 8 reports the R_{DSON} waveforms as a function of the on time for V_{OUT} varying from 62 to 586 V (only for WF1). The R_{DSON} values are calculated 5 µs after the turn-on of the transistor by taking the mean value of the R_{DSON} in a range of 100 ns centred in 5 µs (see a black circle in Fig. 8). As can be noticed, the R_{DSON} changes as a function of V_{OUT}, due to (i) the increase of the device temperature, which is not considered in conventional double-pulsed measurements and to (ii) the increase of the trapping mechanisms. It is worth noticing that, with increasing V_{OUT}, also an increase of the junction temperature is expected due to the fixed load.

Fig. 9 shows the comparison of the two wafers (see filled marker curves). Results show that for WF1 the R_{DSON} increases with V_{OUT} whereas for WF2 the R_{DSON} remains almost constant with V_{OUT}. The different behaviour of the two wafers can be ascribed to the combined effect of charge trapping and self-heating of the transistors on the R_{DSON} for two different wafers. In particular, WF1 has a stronger dependence of the R_{DSON} on the high-voltage trapping and temperature. On the contrary, WF2 has a better behaviour and shows a much more stable R_{DSON}. It is worth noticing that during the measurement the linear current density is expressly kept at a low level (<35 mA/mm – not shown) to limit as much as possible the self-heating of the device and study the charge trapping effects in more detail.

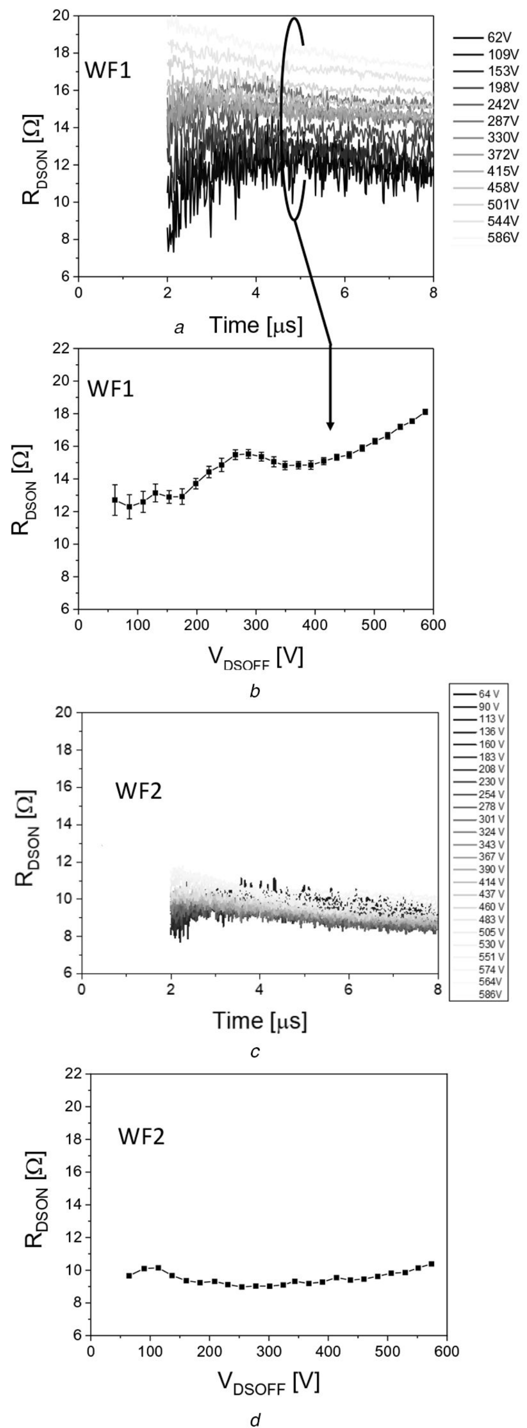

Fig. 8 *R_{DSON} measurement during the operation*

(a), (c) R_{DSON} measurements during the operation for WF1 and WF2, V_{OUT} from 62 to 586 V, ***(b), (d)*** R_{DSON} increases with increasing stress voltages for WF1 and WF2

4.4 Comparison with the conventional double-pulse system

Fig. 10 shows the different measurement concepts of the standard double pulse and the boost converter used in this work. For the double-pulse measurement, an updated version of the system reported in [11] has been adopted, which can reach 600 V as a maximum voltage. The double-pulse system (Fig. 10*b*) mimics soft-switching conditions by using a resistive load. In order to prevent high-power transients during turn on and turn off, the drain and gate pulses provided to the device are properly synchronised. First, the external drain voltage pulser lowers the drain voltage to V_{DSTEST} and then the gate pulser turns on the transistor by providing a positive gate signal. The turn on of the device causes the lowering of the V_{DS} from V_{DSTEST} to V_{DSON}. Due to the

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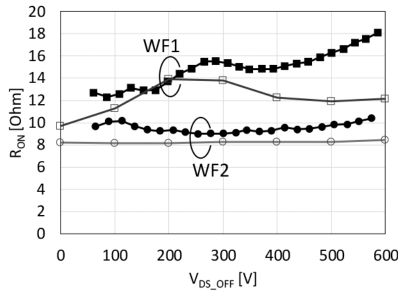

Fig. 9 *R_{DSON} measurement during operation in the boost converter (filled marker curves) and R_{DSON} measurement carried out with double-pulse system (empty marker curves) for WF1 and WF2*

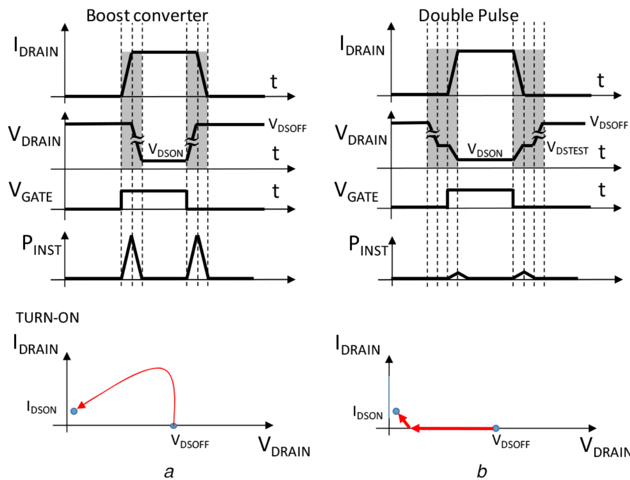

Fig. 10 *Visual representation of device operation*
(a) Real-application hard-switching measurement regime, ***(b)*** Double-pulse soft-switching measurement regime

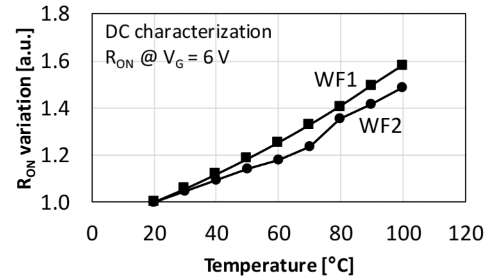

Fig. 11 *Typical DC R_{DSON} variation with temperature for the two wafers analysed. WF2 shows better results in terms of R_{DSON} variation*

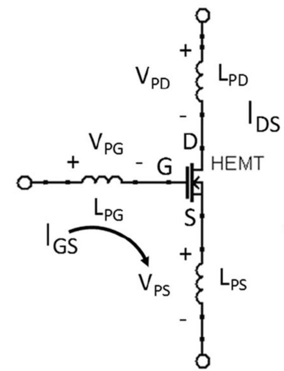

Fig. 12 *Parasitics of the system due to connections*

resistive load and the lower values of V_{DSTEST} with respect to V_{DSOFF}, the switching power is minimised (see P_{INST} curve in Fig. 10*b*). Moreover, the measurement is carried out with a very low duty cycle (0.01); therefore, the device does not suffer from self-heating. With this approach, the double-pulse measurement is able to investigate only the impact of the high off-state electric field on the R_{DSON}.

It is worth noticing that the off-state time (~40 ms) of the double-pulse measurement is much longer compared to the boost converter application: in fact, the GaN power transistors are expected to work in power converter applications in the hundreds of kHz frequency range with obviously shorter off-state time [17]. On the contrary, the boost converter system of this study is able to mimic hard-switching operating conditions and to take into account the effects of switching losses, self-heating and high electric field on the R_{DSON}. Fig. 10*a* shows the hard-switching concept, which is the regime of operation where the devices work in the boost converter of this study. As can be noticed, due to the inductive load, after the gate turn-on transition, first the current raises and then the voltage lowers. This switching operation mode causes a high transient instantaneous power (see P_{INST} curve in Fig. 10*a*). Similar considerations also apply to the turn-off transition. The presence of high transient instantaneous power and the simultaneous presence of high voltage and high current is the main difference between the hard and soft-switching modes as reported in Fig. 10 (see P_{INST} curves).

In order to better understand the results obtained with the novel measurement system, Fig. 9 reports the comparison of the R_{DSON} measured in the boost converter with that measured with the double-pulse system extracted from the plots of Fig. 1. The waveforms of WF1 (see square marker curves) show that there is a hump centred at about 270 V both in the curve of the double pulse and the boost on-wafer measurement. This can be ascribed to the impact of charge trapping due to the high electric field in the off-state. It is known in the literature that the R_{DSON} increases for increasing drain voltage, due to the ionisation of buffer acceptors [18]. On the other hand, at very high voltage (> 250 V) the electric field within the vertical epitaxial structure of the device favours charge de-trapping, and the corresponding decrease in R_{DSON} [18]. Moreover, as can be noticed, the boost on wafer R_{DSON} curve increases more at high voltage with respect to the double-pulse measurement for WF1. This can be ascribed to the contribution of the hard-switching charge trapping and temperature. During hard-switching events, devices reach (a) high levels of power dissipation, which can lead to temporary self-heating; in addition, (b) the simultaneous presence of high current and high voltage can favour hot electron effects. In these conditions, electrons can be highly accelerated, and have enough energy to be injected at trap states located either at the surface, or deep in the buffer. As a consequence, the hard-switching operation results in a stronger charge trapping, compared to soft-switching conditions. The curves of WF2 (see circle indicators curves in Fig. 9) show that this second wafer has a more stable behaviour. In particular, the double-pulse analysis confirms that this wafer only slightly suffers from charge trapping up to 600 V. Moreover, the curve obtained with the boost converter shows that WF2 has better performance also in terms of hard switching and temperature robustness. In order to better understand the R_{DSON} thermal dependency of the two wafers analysed, DC measurements at different temperatures have been carried out by changing the chuck temperature of the wafer. Fig. 11 reports the obtained results. As can be noticed WF1 has a slightly stronger dependency of the R_{DSON} on temperature, possibly due to a higher interface scattering at the AlGaN/GaN interface, related to non-optimised growth conditions.

4.5 Limitations of the system

Parasitics represent the main limiting factor for our proposed system. Fig. 12 shows a schematic representation of the parasitics introduced by the connection wires of the drain, gate and source of the transistor. The three wires have a parasitic series inductance (L_{PG}, L_{PD} and L_{PS}, respectively) of about 30 nH. Due to the change of the current flowing through the transistor's terminals during the switching operation, these inductors can cause parasitic voltage

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drops ($V_{PD,}$ V_{PG} and V_{PS}, respectively), which can modify the V_{GS} and V_{DS} of the HEMT. $V_{P(D/G/S)}$ can be calculated as follows:

$$V_{PD} = L_{PD}\frac{dI_{DS}}{dt}$$

$$V_{PG} = L_{PG}\frac{dI_{GS}}{dt}$$

$$V_{PS} = L_{PS}\frac{d(I_{DS} + I_{GS})}{dt}$$

where $V_{P(D,G,S)}$ are the parasitic voltage drops through the parasitic inductance, respectively, of the drain, gate and dource terminals and $L_{P(D,G,S)}$ are the parasitic inductance, respectively, of the drain, gate and source terminals.

The parasitics analysis can be divided into two parts: (i) the effects of parasitics on the V_{DSON} and (ii) the effects on the V_{GS}. As far as the V_{DSON} is concerned, L_{PD} and L_{PS} affect the V_{DSON} measured by the system due to the parasitic voltage drops V_{PD} and V_{PS} (see Fig. 12). However, due to the low operating currents (∼50 mA) and the low dI_{DS}/dt, the parasitics have a negligible effect on the V_{DS}. In fact, by considering the maximum current (∼50 mA) and by calculating the T_{ON} as follows:

$$T_{ON} = T_{PERIOD} * D = 10\,\mu s * 0.8 = 8\,\mu s$$

we obtain

$$V_{PD} + V_{PS} < 0.5\,mV$$

This voltage level is negligible compared to the measured V_{DSON}, which is in the range of hundreds of mV.

As far as the V_{GS} is concerned, we have to consider the effects of L_{PG} and L_{PS} on the gate drive circuit. These inductors can lead to the ringing of the gate signal and to the slowdown of the switching speed [19]. In order to limit these effects, a series-dumping resistor on the gate and/or a slowdown circuit for the gate signal can be adopted. In the system proposed in this work, a series resistance of 22 Ω was adopted: this prevents the gate ringing but slows down the maximum dV_{DS}/dt reachable and increases the switching losses.

Despite parasitics introduced by the connection wires, we were able to mimic hard-switching application conditions with the on-wafer device obtaining good results in terms of accuracy on the R_{DSON} measurement and in terms of minimum measurement time (2 µs). Such a time frame is comparable with those reported in previous studies on conventional setups, see for instance [20] and references therein. The proposed approach allows to obtain more realistic waveforms (as in a boost power converter) compared with other reports where hard switching is obtained by artificially varying the overlap between gate and drain waveforms [12, 21].

It is worth noting that one of the main critical issues of our proposed system is that during operation it is difficult to discriminate the impact of temperature on the R_{DSON} increase. In fact, by comparing results of the R_{DSON} variation obtained in the boost DC–DC converter with respect to the double-pulse system, we were able to discriminate the effects of the high-voltage electric field with respect to that induced by hard switching and temperature together. We were not able to separate the effects of temperature and hard switching on R_{DSON}. This could be a topic for future work. The developed setup cannot test ultra-large periphery samples, due to the parasitic resistance introduced by the microprobes, and to the related current limitations. In our opinion, the setup is ideal for on-wafer testing of devices down to 0.5–1 Ω.

Finally, it is worth mentioning that our system cannot reproduce perfectly the hard-switching regime of a package level device. In fact, parasitics introduced by connections of our system cannot match the parasitics introduced by the package of a real transistor. In particular, due to the connections and the tip contacts, our system can be considered as the worst case of parasitics level and it is useful to test devices in a detrimental hard-switching regime. At last, it is important to clarify that usually GaN HEMTs real applications use a half-bridge configuration; namely the freewheeling diode, used in the boost converter of this work, is replaced with a high side device connected to the power supply. The choice of a freewheeling diode in the system was due to its ease of operation and because it would be very complicated to connect another on-wafer device for the high side transistor.

5 Conclusions

In this work a novel system able to measure the dynamic R_{DSON} of on-wafer 600 V normally off p-type GaN HEMTs working in hard-switching conditions was presented. The system enables testing the device in a hard-switching environment at the wafer level, thus taking into account all the physical phenomena responsible for the R_{DSON} variation (temperature, off-state charge trapping and hot switching trapping). With this setup, transistors from two different wafers were analysed showing different performance in terms of R_{DSON} variation as a function of temperature and voltage. With respect to conventional double-pulse measurements, the novel system enables a faster and more realistic assessment of in-circuit device performance. By comparing the results of our novel measurement technique with the conventional double-pulse system, more detailed information on the dynamic R_{DSON} physical causes have been obtained. Finally, our in-application measurement technique allows a novel performance and reliability assessment of on-wafer GaN-HEMT devices working close to real operating conditions, thus enabling a powerful method that shortens the loop in the development process of emerging and established technologies. The proposed measurement system is very useful in the compound semiconductor industry (i) for testing the transistors in hard switching at wafer level avoiding the packing process and (ii) for studying in more detail the performance and reliability of such devices. In fact, the system can be easily integrated into the production and development process of GaN-HEMT devices to provide a fast assessment of the dynamic R_{DSON} in real application conditions.

6 References

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