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Review

Recent Advances in Seeded and Seed-Layer-Free Atomic Layer Deposition of High-K Dielectrics on Graphene for Electronics

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Abstract: Graphene (Gr) with its distinctive features is the most studied two-dimensional (2D) material for the new generation of high frequency and optoelectronic devices. In this context, the Atomic Layer Deposition (ALD) of ultra-thin high-k insulators on Gr is essential for the implementation of many electronic devices. However, the lack of out-of-plane bonds in the sp^2 lattice of Gr typically hinders the direct ALD growth on its surface. To date, several pre-functionalization and/or seed-layer deposition processes have been explored, to promote the ALD nucleation on Gr. The main challenge of these approaches is achieving ultra-thin insulators with nearly ideal dielectric properties (permittivity, breakdown field), while preserving the structural and electronic properties of Gr. This paper will review recent developments of ALD of high k-dielectrics, in particular Al_2O_3, on Gr with "in-situ" seed-layer approaches. Furthermore, recent reports on seed-layer-free ALD onto epitaxial Gr on SiC and onto Gr grown by chemical vapor deposition (CVD) on metals will be presented, discussing the role played by Gr interaction with the underlying substrates.

Keywords: graphene; atomic layer deposition; electronics

1. Introduction

Graphene (Gr), a two dimensional (2D) sheet of carbon atoms with hexagonal (sp^2) structure, was the first member of the 2D materials family produced experimentally 15 years ago, in 2004 [1]. It is still the most studied 2D-material due to its peculiar features [2], such as the high carrier mobility (from ~10^3 up to ~10^5 cm^2 $V^{-1}s^{-1}$) [3] and micrometer electron mean free path [4,5], nearly constant transmittance in a wide wavelength range [6], high thermal conductivity [7], and excellent mechanical strength [8]. The combination of these properties give rise to great interest for future applications in electronics, optoelectronics, and sensing.

As a matter of fact, the deposition of thin layers of high-k dielectrics (such as HfO_2 or Al_2O_3) onto the Gr is an essential requirement for the realization of many of these Gr applications. In fact, the insulating layers can act as a gate dielectric in Gr-based field-effect transistors (GFETs) [9–11], as tunneling barriers in vertical transistors, like the Gr-base hot electron transistor (GBHET) [12–14], as protection [15] and functionalized over-layer to achieve specific chemical, environmental, or biological Gr-based sensors [16].

Atomic Layer Deposition (ALD) is the most advantageous technique to deposit several kinds of materials in the form of ultra-thin layers, due to the peculiarities of the deposition mechanism. It is based on self-limited reactions between gaseous precursors and the substrate, which by a sequential repetition ensure a layer-by-layer growth mode [17,18]. This deposition mechanism guarantees a sub-nanometer control of thickness, a conformal and uniform coating on a large area, at relatively

low deposition temperatures (100–400 °C). Thanks to these peculiarities, the ALD technique has been employed in several innovative industrial fields. Most of its success has been related to the progressive scaling down of microelectronic devices, and the consequent need for ultra-thin layers of "high-k" dielectrics (such as Al_2O_3, HfO_2) as gate insulators in complementary metal oxide semiconductor (CMOS) technology. Besides microelectronics, the number of technological applications demanding for ALD advantages is constantly increasing. These include photovoltaic devices [19,20], biotechnological systems [21], water purification apparatus [22] and 2D material growth [23].

In the last years, ALD has also been widely explored regarding the deposition of ultra-thin insulators in Gr-based devices. Early studies on the growth of thin insulators (SiO_2, HfO_2, etc.) on Gr by alternative physical deposition approaches, such as electron beam evaporation (EBE), pulsed laser deposition (PLD), and Radio Frequency (RF) sputtering, showed that a significant amount of damage is introduced in the Gr lattice during the deposition [24]. On the contrary, thermal ALD of high-k oxides does not significantly modify the structural properties of Gr. However, due to the lack of out-of-plane bonds in the sp^2-hybridized Gr structure, the chemisorption of the ALD precursors and, consequently, the nucleation and growth of the expected material are typically hindered on the Gr surface, with the exception of regions where structural defects (sp^3 bonds) are present.

As an example, in the case of high quality Gr flakes mechanically exfoliated from highly oriented pyrolytic graphite (HOPG) onto SiO_2, the ALD deposition was found to occur preferentially close to the edges, where most of structural defects and dangling bonds, active sites of nucleation, are localized [25]. Analogously, the polycrystalline Gr grown by chemical vapor deposition (CVD) on catalytic metals, such as Cu and Ni, and transferred on SiO_2 was characterized by an island-like ALD growth localized on the grain boundaries, edges, and on Gr corrugations (wrinkles). In particular, the enhanced reactivity in proximity of the wrinkle regions is due to the curvature of the Gr membrane which involves the distortion of the sp^2 structure and the strain of C–C bonds [26]. Density functional theory (DFT) calculations of the reaction energy between the ALD precursor and strained Gr demonstrated that such enhanced reactivity originates from the balance between the breaking of ALD precursor bonds, the formation of bonds between the precursor and Gr surface, and the release of strain due to Gr buckling [27]. As a matter of fact, the transferred Gr surface is typically characterized by polymeric residues and little cracks associated to the transfer procedure. Although these can act as seeds of the nucleation, on the other hand they adversely influence the electrical properties of Gr.

To overcome the above-mentioned issues, direct functionalization of Gr or the physical deposition of seed-layers on its surface are the typically adopted approaches to enable the ALD nucleation and therefore the uniformity of the deposition [28]. The functionalization of the Gr surface is achieved by exposure to reactive chemical species, such as O_3 [29] and XeF_2 [30], or by plasma treatments with different gases, mainly N_2 [31], O_2, and H_2 [32]. Such surface treatments are effective methods for the improvement of the ALD-precursor chemisorption directly on the Gr surface, because, in most cases, they partially convert the sp^2 bonds to out-of-plane sp^3 bonds [32,33]. Ultra-thin dielectric films can be obtained on Gr by these approaches. However, the loss of the sp^2-hybridization typically results in a partial degradation of the Gr electrical properties.

The seeding-layer method consists of the physical deposition on Gr of a very thin layer of polymer [25], metal-oxide [34], or metal (naturally oxidized in air) [35,36], which act as seed of nucleation. The main advantage of this approach is that it does not introduce defects in the Gr lattice and, therefore, does not significantly affect Gr mobility. The seed-layer deposition is usually performed "ex situ", i.e., outside the ALD reactor chamber. As a matter of fact, this ex situ procedure can be responsible for contaminations and impurities, which can be detrimental for the reliability of the deposited material. Hence, "in- situ" seed-layer depositions, namely nucleation seeds directly deposited inside the ALD reactor just before the dielectric growth, are highly desirable. Significant progress in this direction has been made in the last years by the introduction of two step ALD processes, consisting of the deposition of a few nanometer seed-like layer at a lower temperature step, followed by a higher temperature one for the growth of a high quality metal-oxide (HfO_2 or Al_2O_3) film [37–41].

The structure (amorphous or crystalline) of the metal-oxide layers grown by ALD on Gr depends on the high-k material, on the deposition conditions (especially the temperature), as well as on the specific seed layer at the interface. As an example, Al_2O_3 layers grown by ALD process are typically amorphous, although some authors reported the formation of Al_2O_3 nanocrystals at the interface using an oxidized Ti seed layer on Gr [36]. In the case of HfO_2, amorphous films have been grown on Gr at low deposition temperatures of 180 °C, whereas polycrystalline HfO_2 films have been obtained by a two-step deposition, with the first step at 170 °C, followed by the second step at higher temperature (300 °C) [37].

The main disadvantage of seed-layer-assisted ALD is that this interfacial layer ultimately limits the minimum film thickness that can be achieved. As an example, Fallahazad et al. [36] reported a minimum thickness of ~2.6 nm for an oxide stack consisting of a ~0.6 nm oxidized Ti seed-layer and a ~2 nm Al_2O_3 film deposited by thermal ALD. Furthermore, the final seed layer/insulator stack typically exhibits an increased equivalent oxide thickness with respect to a dielectric film deposited by pure thermal ALD. Finally, the presence of electrically active defects at the interface between Gr and the seed layer can be responsible for charge trapping effects commonly observed in Gr devices.

From the discussion above, it is clear that ALD of dielectrics on Gr without pre-functionalization and seed layers would be highly desirable. Previous investigations focused on thermal ALD on the pristine (i.e., untreated and seed-layer-free) Gr surface showed that the uniformity of the deposited films can be tailored, to some extent, by properly tuning the deposition parameters, especially the temperature and the precursor residence time [42]. Furthermore, for similar deposition conditions, the quality of the deposited films strongly depends on the Gr synthesis method and the Gr substrate. Interestingly, in some specific cases, direct ALD deposition could be obtained on pristine monolayer Gr, by exploiting the peculiar interaction of Gr with its substrate. As an example, uniform Al_2O_3 thin films were grown by thermal ALD with H_2O and trimethylaluminum (TMA) on monolayer CVD Gr when it was residing on the native metal substrate (Cu or Ni-Au), and the enhanced nucleation was ascribed to the presence of polar traps at the interface with the metal [43]. More recently, highly uniform Al_2O_3 films were obtained by seed-layer-free thermal ALD on highly homogeneous monolayer epitaxial graphene (EG) grown on on-axis 4H-SiC (0001), with the enhanced nucleation behavior related to the peculiar of the EG/SiC interface, i.e., the presence of the so-called buffer layer beneath Gr [44].

A comprehensive review of the research status on ALD for Gr devices integration has been recently reported by Vervuurt et al. [28]. Hence, a general overview of this topic is out of the scope of the present paper. The aim of our work is to provide a focused discussion about recent developments of "in-situ" seeding-layer and seed-layer-free approaches for efficient atomic layer deposition of high-k insulators, in particular Al_2O_3, on Gr for electronic applications.

Section 2 is devoted to the discussion of two-step ALD growth of high-k dielectrics on Gr with an "in-situ" seed layer deposited at low temperature. This has been described in all its aspects, starting from the seed layer optimization to the description of the morphological, structural, and electrical properties of the deposited dielectric. The drawbacks related to this seed-layer based ALD process are also discussed.

Section 3 is devoted to recent advances in the seed-layer-free ALD of oxides on Gr. The role played by the deposition parameters, the Gr/substrate interaction, and the Gr thickness homogeneity on the oxide nucleation onto pristine Gr is extensively discussed. The structural and electrical properties of seed-layer-free Al_2O_3 grown on Gr/Cu or Gr/Ni substrates and on epitaxial graphene on silicon carbide are presented.

2. Two-Step ALD Growth on Graphene with an "In-Situ" Seed Layer

The two-step ALD growth of metal oxides (including Al_2O_3, HfO_2 and Ga_2O_3) with the "in-situ" seed layer obtained by a low-temperature water-assisted process has been recently explored in several experimental works [37–40,45].

This approach provides the initial physical adsorption, by the van der Waals interactions, of H_2O molecules on the Gr surface. The physisorbed H_2O molecules behave as activation sites for a

low-temperature deposited Al_2O_3, which in turn acts as seed layer of nucleation for a subsequent standard ALD process. In order to ensure uniform physisorption of the H_2O molecules on the Gr surface, it is necessary to operate within an adequate temperature window [46], i.e., not too low to avoid the water condensation and not too high to prevent the escape of molecules. As an example, for the Al_2O_3 seed layer, obtained by using TMA and H_2O precursors, the optimal temperature window is 100–130 °C [46]. Besides the deposition temperature, other key parameters (such as the precursor's exposure and purging times) need to be optimized to achieve uniform coverage of Gr with the seed-layer. Figure 1 shows the optimization study (carried out by atomic force microscopy, AFM, measurements) of the deposition conditions for a 3–4 nm Al_2O_3 seed-layer on the surface of CVD-grown Gr transferred onto a Al_2O_3−Si substrate [41]. For a fixed number of ALD cycles (60) at a deposition temperature of 100 °C, optimal coverage was achieved using 100 ms exposure time to H_2O and TMA precursors, and 6000 ms purging time.

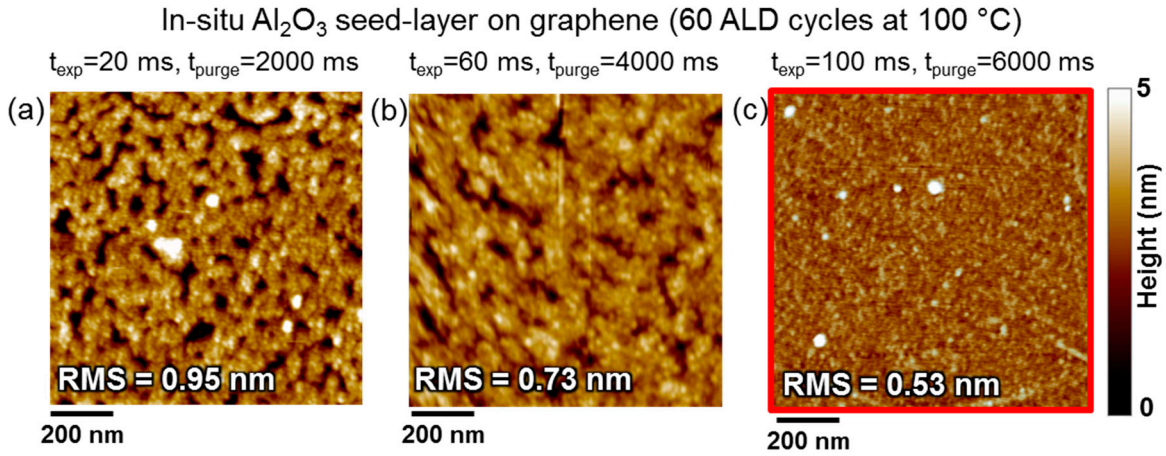

Figure 1. Optimization study of the Al_2O_3 seed-layer deposition on CVD graphene (Gr) transferred onto an Al_2O_3−Si substrate. Atomic force microscopy (AFM) images of the Al_2O_3 seed layer deposited by 60 Atomic Layer Deposition (ALD) cycles at 100 °C using H_2O and trimethylaluminum (TMA) precursors, for incrementally long precursor exposure time (t_{exp}) and purging periods (t_{purge}): (**a**) t_{exp} = 20 ms, t_{purge} = 2000 ms; (**b**) t_{exp} = 60 ms, t_{purge} = 4000 ms; (**c**) t_{exp} = 100 ms, t_{purge} = 6000 ms. The root-mean-square roughness (RMS) estimated by the AFM images is also reported. Images adapted with permission from [41]. Copyright of American Chemical Society, 2017.

As a matter of fact, the used temperature (100 °C) for the first deposition step is far below the temperature range for optimal thermal ALD process of Al_2O_3 (200−250 °C), resulting in a poor structural and electrical quality of the seed layer. For this reason, the low-temperature seed layer deposition was completed with a second step, where the Al_2O_3 film growth is carried out at the optimal temperatures [41]. Figure 2 shows the comparison of the AFM morphologies for the pristine Gr monolayer transferred onto the Al_2O_3-Si substrate (Figure 2a), after the optimized seed layer deposition at 100 °C (Figure 2b), and (Figure 2c) after the second ALD growth at 250 °C, resulting in a final Al_2O_3 thickness of ~22 nm [41]. Both the seed layer and the complete film exhibit a conformal coverage Gr without pinholes and a low surface roughness.

The electrical uniformity of the seed-layer and of the two-step Al_2O_3 film was also investigated by conductive atomic force microscopy (C-AFM) [41]. The C-AFM experimental setup for nanoscale resolution mapping of the current through the dielectric layer is illustrated in Figure 3a, whereas the morphology and current maps for the seed-layer and the two-step Al_2O_3 on Gr are reported in Figure 3b–e. Although the Al_2O_3 seed layer is characterized by a continuous morphology, it shows a conductive behavior in the Gr wrinkle regions due to the insufficient structural quality related to the low growth temperature. However, excellent electrical uniformity with negligible leakage current is observed in the case of the final Al_2O_3 deposited by the two steps.

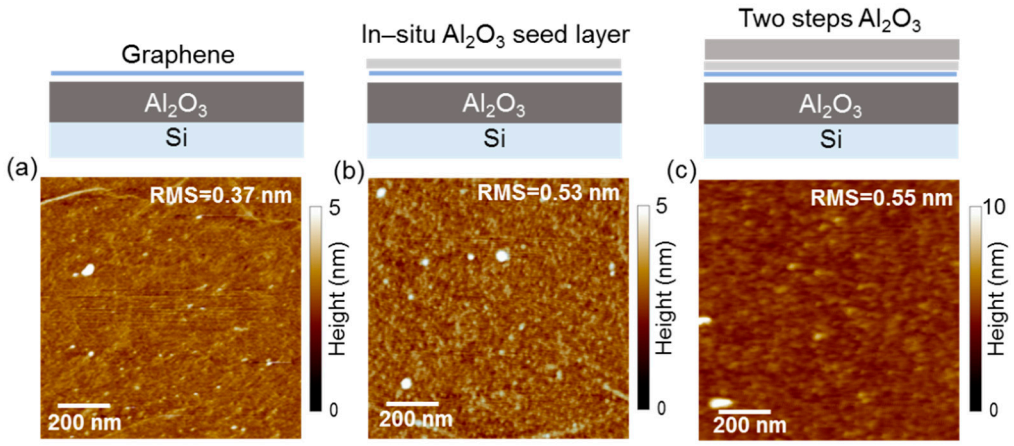

Figure 2. Morphological images of (**a**) as-transferred CVD Gr onto an Al_2O_3–Si substrate, (**b**) after the optimized seed layer deposition at 100 °C and (**c**) after the two-step ALD growth at 250 °C. Images adapted with permission from [41]. Copyright of American Chemical Society, 2017.

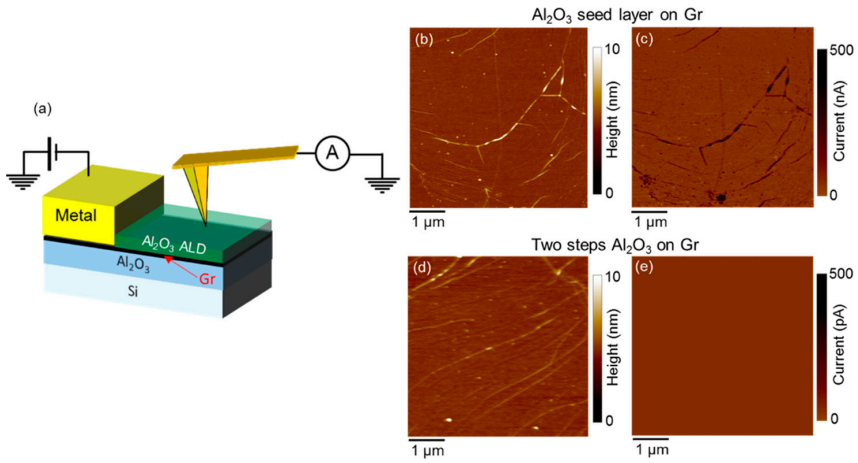

Figure 3. (**a**) Schematic of the conductive atomic force microscopy (C-AFM) setup for mapping of leakage current through the dielectric on Gr. Morphology (**b**) and current map (**c**) on the ~4 nm thick Al_2O_3 seed layer with an applied bias of −1.5 V. Morphology (**d**) and current map (**e**) on the final 22 nm thick film deposited by the two-step ALD process with an applied bias of −8 V. Images adapted with permission from [41]. Copyright of American Chemical Society, 2017.

The water-assisted seed-layer deposition does not introduce defects in the Gr. Figure 4 shows three typical Raman spectra collected on as-transferred CVD Gr and after each deposition step [41]. The spatial uniformity of the main Raman features (D, G, and 2D peaks) of transferred Gr on the Al_2O_3 substrate are reported in [47]. Negligible changes can be observed in the D peak intensity (related to lattice disorder), indicating no changes in the defect density after the ALD process. The increase of the ratio between the 2D and G peaks intensities (I_{2D}/I_G) and the red-shift of the G peak after the seed-layer deposition and the second step Al_2O_3 deposition can be ascribed to a reduction of the starting unintentional p-type doping of transferred CVD-Gr [37].

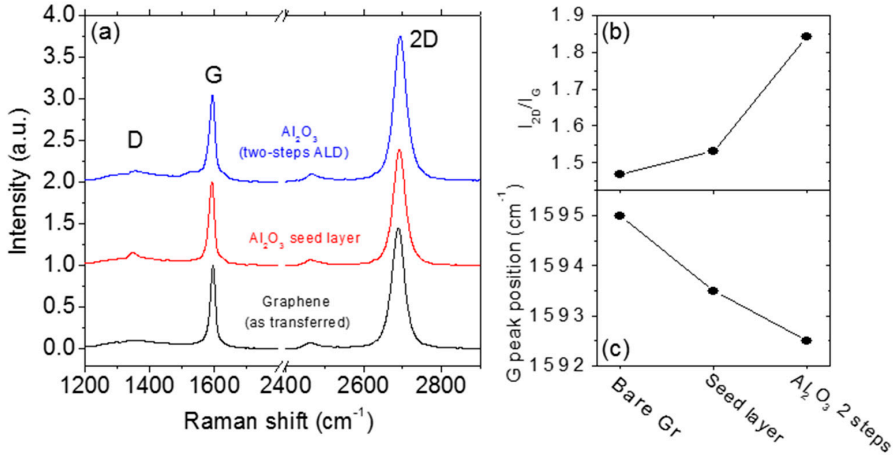

Figure 4. (**a**) Raman spectra of as-transferred Gr (black), after the Al_2O_3 seed-layer deposition at 100 °C (red) and after the two-step ALD deposition (blue). Behavior of the 2D over G peak intensity ratio I_{2D}/I_G (**b**) and of the G peak position (**c**) on the three different samples. Images adapted with permission from [41]. Copyright of American Chemical Society, 2017.

The electrical characterization of top-gated Gr field effect transistors with the 22 nm Al_2O_3 top gate dielectric (see schematic in Figure 5a) allowed to evaluate the dielectric properties (breakdown dielectric field, permittivity) of the Al_2O_3 film on Gr, as well as the interface trap density at Al_2O_3/Gr interface and the Gr carrier mobility [41]. A relative dielectric permittivity ($\varepsilon = 7.45$) was first evaluated from capacitance-voltage measurements between the top-gate and source electrodes. Figure 5b shows the gate leakage current I_G as a function of the electric field across the gate oxide, from which a breakdown field $E_{BD} = 7.4$ MV/cm was estimated for the Al_2O_3 insulator on Gr. Finally, Figure 5c shows the transistor's transfer characteristics (I_D–V_{TG} at a drain bias $V_{DS} = 0.3$ V) measured under forward and backward sweep of V_{TG}. A Gr field effect mobility of ~1200 $cm^2\ V^{-1}s^{-1}$ was obtained from these electrical characteristics, after excluding the effects of the contacts and access resistances [41]. The hysteresis between the two curves in Figure 5c was ascribed to electron trapping by traps located at Gr/Al_2O_3 interface and in the Al_2O_3 near-interface region. A total traps density of 4×10^{12} cm^{-2} was estimated from the relative shit of the current minima. The interface traps can be related, in part, to residual polymeric contaminations from the polymethylmethacrylate (PMMA) aided Gr transfer [15]. On the other hand, the near-interface traps can be due to the lower structural quality of the interfacial Al_2O_3 seed-layer deposited at low temperature (100 °C).

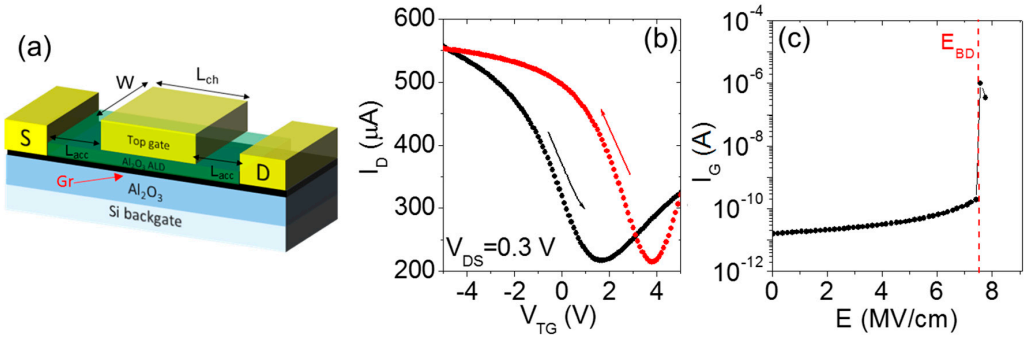

Figure 5. Electrical characterization of a Gr field effect transistor with 22 nm Al_2O_3 top-gate dielectric deposited by a two-step ALD process. (**a**) Schematic representation of the device. (**b**) Transfer characteristics (drain current I_D vs. top-gate bias V_{TG} at fixed drain bias $V_{DS} = 0.3$ V) measured under forward and backward sweep of V_{TG}. The hysteresis between the two curves is ascribed to electron trapping by Al_2O_3 near interface traps. (**c**) Gate leakage current I_G as a function of the electric field E across the top gate oxide. A dielectric breakdown field of 7.4 MV/cm is indicated by the vertical dashed line. Images adapted with permission from [41]. Copyright of American Chemical Society, 2017.

As an example, Zheng et al. [37] performed cross-sectional TEM analyses (see Figure 6a) for direct imaging of the lower density of a 4 nm Al_2O_3 seed layer (deposited by 60 ALD cycles at 100 °C) with respect to the upper 5 nm Al_2O_3 layer (deposited by 75 ALD cycles at 200 °C). An energy bandgap E_g = 7.3 eV was evaluated from XPS energy loss measurements performed on the two steps deposited Al_2O_3 (see Figure 6b), whereas a significantly smaller bandgap (E_g = 6.3 eV) was obtained for a reference Al_2O_3 film deposited with only one step by 135 cycles at 100 °C (see Figure 6c).

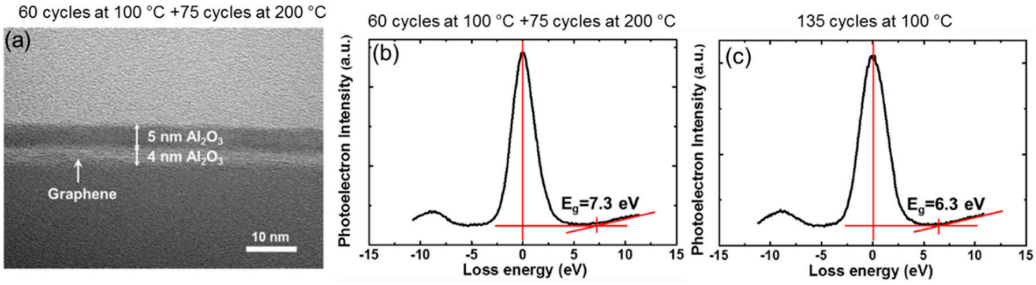

Figure 6. (**a**) Cross sectional TEM image and (**b**) XPS energy loss spectrum of an Al_2O_3 film deposited on Gr by a two-step ALD process (60 cycles at 100 °C + 75 cycles at 200 °C). (**c**) XPS energy loss spectrum of an Al_2O_3 film deposited on Gr by single low temperature step (135 cycles at 100 °C). Images adapted with permission from [38]. Copyright of American Chemical Society, 2014.

As a conclusion of this section, the current status of the ALD of metal oxide on Gr with water-assisted in situ seed layers is illustrated in Table 1, where the experimental conditions employed by different authors and the characteristics of the deposited films are reported.

Table 1. Summary of state-of-the-art of ALD processes for the growth of metal oxides on Gr with a water-assisted in situ seed layer.

High-κ	Graphene Type	Substrate	Method	Seed Layer	Temperature	Thickness	Graphene Damage
Al_2O_3 [46]	Exfoliated from HOPG	SiO_2	One-step ALD process	-	100 °C	11 nm	No defects
HfO_2 [37]	Exfoliated from HOPG	SiO_2	Two-step ALD process	H_2O-based Low temperature HfO_2 layer	170 °C/300 °C	1 nm/20–30 nm	No defects
Al_2O_3 [38]	Transferred CVD-Gr	SiO_2	Two-step ALD process	H_2O-assisted low temperature Al_2O_3 layer	100 °C/200–250–300 °C	1–5 nm/8–3 nm	Defects introduction at 250 °C and 300 °C
Al_2O_3 [41]	Transferred CVD-Gr	Al_2O_3	Two-step ALD process	H_2O-assisted low-temperature Al_2O_3 layer	100 °C/250 °C	4 nm/18 nm	No defects
Al_2O_3, HfO_2 [45]	CVD-Gr	Gr/Cu	Two-step ALD process	H_2O-assisted low-temperature Al_2O_3/HfO_2 layer	90 °C/200 °C	10 nm	Defects after Gr-transferring
Al_2O_3 (seed-layer) /Gd_2O_3 [40]	Transferred CVD-Gr	SiO_2	Two-step ALD process	H_2O-assisted low-temperature Al_2O_3 layer	100 °C/200 °C	5 nm/20 nm	No defects

3. Recent Approaches to "Seed-Layer Free" ALD on Graphene

Although the water-assisted seed-layers, as the other seed-layers species, do not significantly affect the sp^2 structure of Gr, the seed-layer/dielectric stack results in a higher equivalent oxide thickness compared to a single dielectric layer grown by a direct ALD process. Moreover, the low structural quality of the seed-layer can be responsible for charge trapping phenomena, which adversely affect the electrical performance of the Gr-based devices. For the above-mentioned reasons, direct ALD processes of dielectric materials on Gr, without pre-functionalization and seed-layer deposition, would be the highly desirable for device applications.

Great attention has been paid towards the possible approaches to enhance the direct ALD deposition of high-k dielectrics on the Gr surface. Some reports demonstrated that the uniformity of the dielectric nucleation is heavily dependent on the ALD deposition parameters, mainly the residence time of the precursors and the temperature. As an example, Aria et al. [42] have shown that, by optimizing the pulse length and using a conveniently long precursor residence time, sub-2-nm thin homogeneous aluminum oxide (AlO_x) layers can be obtained, without intermediate steps of functionalization and seeding, at a deposition temperature of 200 °C and on different substrates (Gr/Cu, HOPG, Gr/Ge, Gr/SiO_2). Figure 7a,b illustrates two different ALD processes adopted by the authors [42]. In the first process (the typically employed one), the H_2O and TMA were dosed alternatingly into the reaction chamber by separated pulses and purging periods. In the second process (Figure 7b), a H_2O/TMA soaking period was introduced by stopping the flow to create a static atmosphere in the process chamber for several seconds (t_{hold}) right after the H_2O/TMA was dosed. Before the subsequent pulse, the flow was continued, and the chamber was purged. The results of the AlO_x growth on different graphitic substrates using the two process modes are illustrated in Figure 7, showing a relatively low surface coverage of ~57% on HOPG (Figure 7c), ~47% on Gr/Ge (Figure 7e), and ~38% on Gr/SiO_2 (Figure 7g) using the first mode, and >97% coverage ((Figure 7d), (Figure 7f) and (Figure 7h)) using the second one.

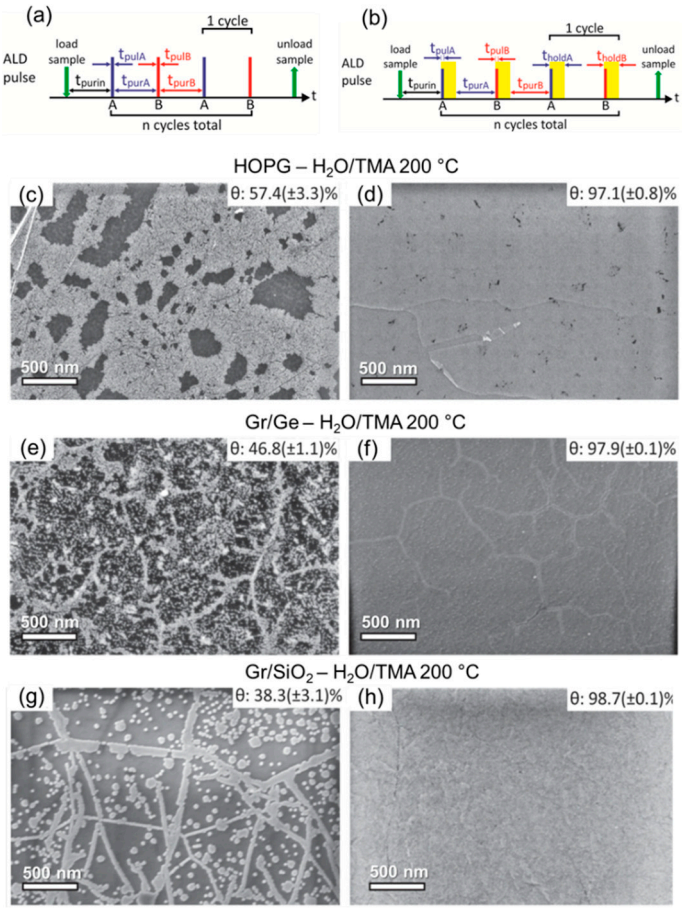

Figure 7. Schematic illustration of two ALD processes (**a**) with the typical oxidant/precursor pulse sequence and (**b**) with a modified sequence by the introduction of a soaking period after each pulse. A denotes the oxidant (H_2O vapor), and B denotes the metal precursor (TMA). AlO*x* nucleation on highly oriented pyrolytic graphite (HOPG), Gr/Ge, and G/SiO_2 at T_{dep} = 200 °C using the first and the second pulse sequence. The first process yields a relatively low surface coverage of ~57% on HOPG (**c**), ~47% on Gr/Ge (**e**), and ~38% on G/SiO_2 (**g**). The second process results in an almost perfectly conformal AlO*x* nucleation with surface coverage of ~97.1% on HOPG (**d**), ~97.9% on Gr/Ge (**f**), and ~98.7% on G/SiO_2 (**h**). Images adapted with permission from [42]. Copyright of American Chemical Society, 2016.

In some cases, the nucleation of amorphous or nanocrystalline metal oxides on Gr can be obtained by properly tuning the deposition parameters. As an example, some atomic resolution TEM investigations on the nucleation of TiO_2 on single layer Gr have been recently reported, showing the formation of an amorphous layer with uniform coverage was at a low temperature of 60 °C, and the nucleation of ~2 nm nanocrystals at a high temperature of 200 °C [48].

Besides the process parameters, the peculiar interaction between Gr and the underlying substrate greatly acts on the ALD nucleation and, consequently, the uniformity of the deposited films on Gr. As an example, Dlubak et al. [43] observed, under the same ALD conditions, an improved Al_2O_3 coverage on monolayer CVD Gr laying on the native substrates (Cu, Ni-Au), as compared to monolayer Gr transferred to SiO_2. On the contrary, a poor coverage was found in the case of multilayer CVD Gr on Cu or Ni-Au, similarly to the case of HOPG. Figure 8a illustrates the behavior of the Al_2O_3 coverage (%) as a function of the ALD growth temperature in the different cases. The enhanced nucleation in the case of monolayer CVD Gr on the native metal substrates was ascribed to the wetting transparency of Gr in the form of monolayer [49] and to the presence of peculiar polar traps (generated by the 2D-lattice/metal interactions) at the interface. As schematically illustrated in Figure 8b, the polar traps promote the adsorption of water molecules, namely the oxygen precursor of a standard thermal ALD process and, consequently, the nucleation degree on the Gr surface. Clearly, the number of Gr layers is a crucial aspect for this growth mechanism. In fact, the strength of the electrostatic interaction between the water precursor and the Gr polar traps is weakened for multilayer Gr due to a decreased transparency.

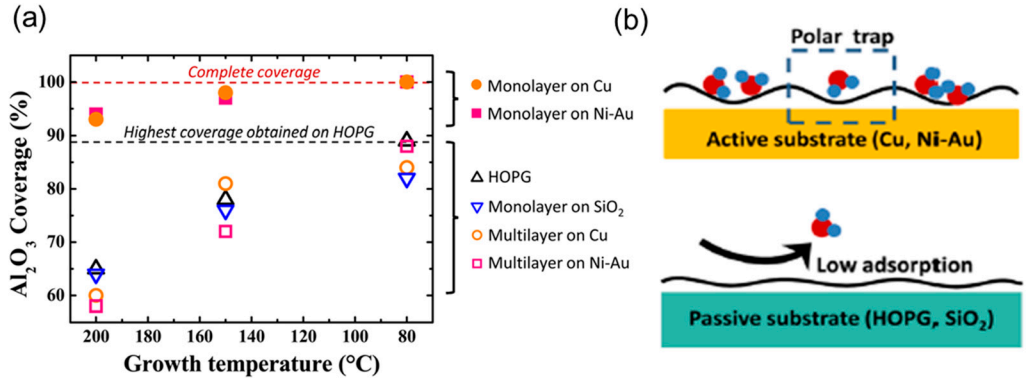

Figure 8. (**a**) Comparison of the coverage of the Al_2O_3 grown by ALD on different Gr materials as a function of the growth temperature. High coverage was observed on monolayer Gr on Cu or Ni-Au, whereas low coverage was found on HOPG, monolayer Gr on SiO_2, and multilayer Gr on Cu or Ni-Au. (**b**) Schematic illustration of the enhanced adsorption of water molecules arising from interfacial polar traps in the case of monolayer Gr/metal samples, as compared to the low adsorption for monolayer Gr on passive substrates. Images adapted with permission from [43]. Copyright of AIP, 2012.

The direct growth of Al_2O_3 or HfO_2 on Gr residing on the native metal substrate (Cu or Ni) has the advantage of providing a protective layer for Gr, avoiding the direct contact of Gr with the polymeric films typically used for the transfer process [15,45]. Furthermore, after transfer to an insulating substrate, the oxide layer on Gr can be exploited as a passivation layer of back-gated Gr transistors or as gate dielectric for top-gated Gr FETs. As an example, Cabrero-Vilatela et al. [15] showed greatly reduced hysteresis and residual doping in the transfer characteristics of back-gated Gr transistors with an Al_2O_3 protective layer. Although the ALD grown protective layer allows to overcome the problems related to polymeric contaminations on Gr surface, the transfer of the oxide/Gr stack from the native metal substrate to the target substrate still remains a critical step. In the early work by Dlubak et al. [43], the transfer process was carried out by using spin-coated PMMA as a support on top of the Al_2O_3/Gr stack, as illustrated in the scheme in Figure 9a. Raman spectroscopy analyses on the Al_2O_3/Gr stack transferred on a SiO_2 substrate (see Figure 9b,c) showed a very small I_D/I_G peak ratio, i.e., very low defects density in monolayer Gr, indicating no significant degradation of

Gr due to the transfer. More recently, comparative studies of different oxide protective layers (Al_2O_3, HfO_2, TiO_2) grown by ALD onto Gr/Cu and of different transfer processes (i.e., with and without a polymeric capping layer) have been reported [15,45]. Although transfer of the protective oxide/Gr stack without any polymer capping was found to be possible (by etching the copper substrate followed by gentle fishing of floating oxide/Gr), the use of an additional PMMA film on the oxide/Gr stack made the handling easier [45]. Furthermore, these studies revealed that the protective oxide layer did not contribute to a major overall strain of Gr [45].

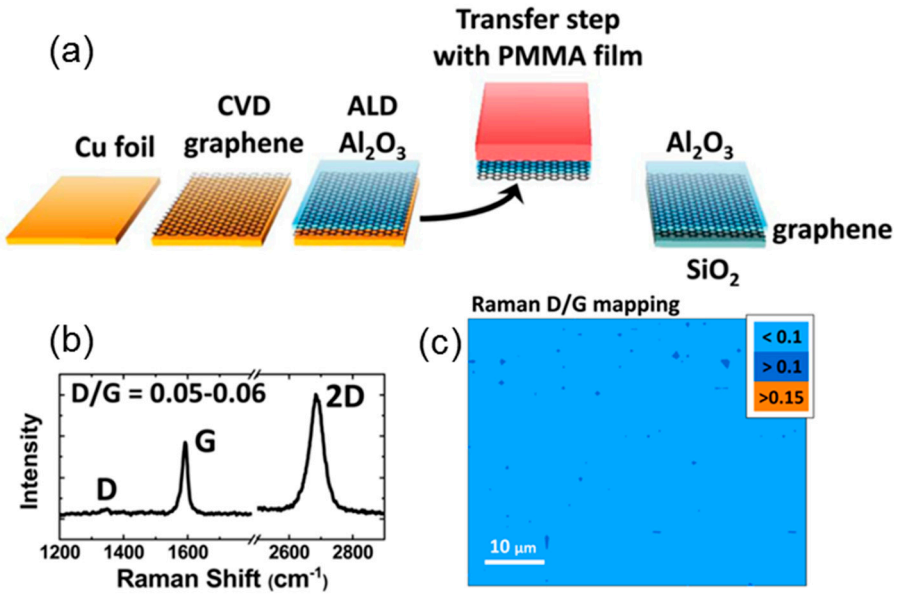

Figure 9. (**a**) Schematic illustration of the CVD growth of monolayer Gr on Cu, of the direct Al_2O_3 deposition, and of polymethylmethacrylate (PMMA) assisted transfer onto the final SiO_2 substrate. (**b**) Typical Raman spectrum of the Al_2O_3/Gr stack transferred onto SiO_2 and (**c**) map of the ratio between the D and G peaks' intensities. Images adapted with permission from [43]. Copyright of AIP, 2012.

The above-mentioned issues related to the Gr transfer process can be avoided by using another kind of Gr, namely epitaxial graphene (EG) grown by the thermal decomposition of silicon carbide (SiC) [50–52]. In fact, compared to the CVD Gr grown on metals, the EG is directly grown on a semiconductor/semi-insulating substrate and is ready for device fabrication. Due to its outstanding electronic quality, monolayer EG on semi-insulating SiC has been employed to build quantum Hall effect standards [53], and to demonstrate top-gated high frequency transistors (f_T > 100 GHz) with a 10 nm HfO_2 gate oxide deposited by ALD [9]. In spite of its high cost, SiC is gaining increasing interest as the material of choice for high power electronics, with applications in energy efficient power conversion, automotive, and aerospace [54]. These strategic interests are also the driving forces leading to the improvement of the quality of 4H-SiC substrates, nowadays available on 150 mm sizes with very low defects density. The possibility of integrating both high power and high frequency (Gr-based) devices on the same material platform represents an important advantage of the SiC/graphene system for future electronic applications.

EG grown on the silicon face (0001) of SiC is characterized by single-crystal alignment with the substrate and by the presence of an interfacial carbon layer (buffer layer) with partial sp^3 hybridization [55,56]. These structural properties make the EG compressively strained, as compared to transferred Gr [44]. Furthermore, the existence of electrostatic interactions between the EG and the dangling bonds at the buffer layer/SiC interface is responsible for a high n-type doping (in the order of 10^{13} cm^{-2}) of the overlying Gr [57,58]. The EG thickness uniformity is a function of the growth conditions, namely temperature and pressure [59], but also of the SiC morphology, in particular the miscut angle [60], with better uniformity achieved for low miscut angle SiC. The EG grown under

typical growth conditions (T = 1650 °C, p = 900 mbar in Argon gas) on "nominally" on-axis SiC (0001) is commonly composed of homogeneous monolayer regions on the micrometer wide SiC terraces, separated by narrow bilayer (2L) or trilayer (3L) strips at the step edges [59]. The direct ALD growth of thin insulators (such as Al_2O_3 or HfO_2) on such pristine EG samples typically resulted in a non-uniform coverage [61,62], with poor or no oxide nucleation in the vicinity of the step edges, corresponding to 2L or 3L EG regions.

Recently, uniform Al_2O_3 layer deposition has been demonstrated by seed layer-free thermal ALD at 250 °C using highly homogeneous monolayer EG (over >98% of SiC surface) grown under optimized sublimation conditions [44].

Figure 10a shows a high resolution cross-sectional TEM image of the deposited Al_2O_3 film (with ~12 nm thickness), characterized by an amorphous structure and uniform contrast on all thickness, indicating a uniform density. Figure 10b shows a large scale (20 μm × 20 μm) AFM image of the deposited Al_2O_3 film, showing a uniform and conformal coverage, with small depressions corresponding to bilayer Gr areas. These features of the Al_2O_3 morphology are further elucidated in Figure 10c, where the boundary region between the 2L and 1L areas is reported. Raman spectroscopy measurements on EG before and after the Al_2O_3 deposition (see Figure 10d) indicated that the ALD process does not significantly affect the doping and strain of the EG. For comparison, the same ALD process was also performed on monolayer Gr transferred on on-axis SiC, showing an inhomogeneous nucleation and 3D Al_2O_3 islands growth, similarly to the case of monolayer Gr on other substrates, like SiO_2. These results indicated that the uniformity of the ALD deposition of Al_2O_3 on the monolayer EG is not related to the SiC substrate itself, but to the peculiar properties of the interface between the EG and SiC, i.e., the presence of the buffer layer, responsible for a high n-type doping and strain of EG. An enhanced chemical reactivity of Gr subjected to significant mechanical strain or doping has been reported by several authors [63,64]. In particular, ab-initio DFT calculations showed an enhanced adsorption energy for water molecules (working as co-reactant in the thermal ALD process) on highly n-type doped monolayer Gr, indicating the doping of EG induced by the underlying buffer layer as the origin of the excellent Al_2O_3 nucleation [44].

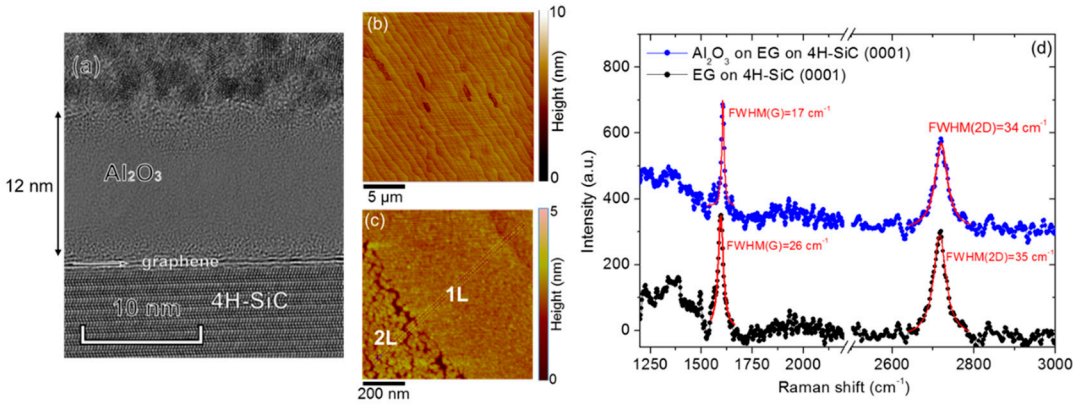

Figure 10. (**a**) Cross-sectional TEM image of a 12 nm Al_2O_3 film deposited on monolayer epitaxial graphene (EG) on SiC. (**b**) AFM morphology on 20 μm× 20 μm scan area, showing uniform and conformal Al_2O_3 coverage on 1L Gr and small depressions on 2L Gr. (**c**) Higher resolution AFM morphology, showing a compact Al_2O_3 film with small grains on top of 1L EG, and Al_2O_3 with larger grains separated by small depressions (up to 2 nm) on the 2L EG region. (**d**) Typical Raman spectra of virgin 1L EG and after the Al_2O_3 deposition. Images adapted with permission from [44]. Copyright of Wiley, 2019.

The electrical quality of the Al_2O_3 film on EG was also evaluated by nanoscale resolution current maps and local I–V analyses based on C-AFM [65], as illustrated in Figure 11a.

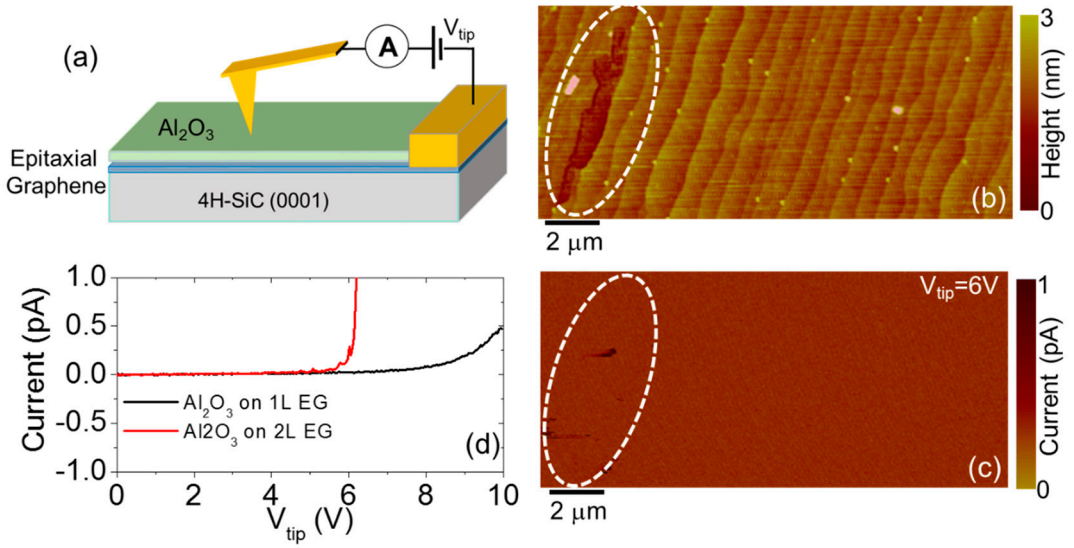

Figure 11. (**a**) Schematic representation of the C-AFM setup for local current mapping through the Al_2O_3 thin film deposited onto EG on axis 4H-SiC (0001). (**b**) Morphology and (**c**) current map (at a tip bias of 6 V) of a sample area including both uniform Al_2O_3 on 1L EG and Al_2O_3 on a 2L EG patch. (**d**) Two representative local current-voltage characteristics collected by the C-AFM probe on Al_2O_3 in the 1L and 2L EG regions. Images adapted with permission from [44]. Copyright of Wiley, 2019.

Figure 11b,c reports a morphology and the corresponding current map, collected applying a tip bias V_{tip} = 6 V on a sample area which includes both uniform Al_2O_3 on 1L EG and Al_2O_3 on a 2L EG patch. While uniform low current values are detected in all the considered bias range through the 12 nm Al_2O_3 film onto 1L EG, the presence of high current spots is observed in the 2L EG region. Figure 11d illustrates two representative local current-voltage characteristics collected by the C-AFM probe on Al_2O_3 in the 1L and 2L EG regions. While current smoothly increases with the bias for Al_2O_3 on 1L EG, an abrupt rise of current is observed for $V_{tip} > 6$ V in the case of Al_2O_3 on 2L EG, indicating the occurrence of local premature breakdown events probably due to the less compact Al_2O_3 structure and the lower average thickness in these regions. Assuming planar capacitor model for the tip/Al_2O_3/EG system, a breakdown field $E_{BD} > 8$ MV cm^{-1} was estimated for Al_2O_3 on 1L EG, whereas $E_{BD} \approx 6$ MV cm^{-1} was evaluated for Al_2O_3 on 2L EG. Of course, when fabricating macroscopic devices (capacitors or transistors) based on the Al_2O_3/EG stack, the 2L regions (even with a very low areal density) represent the weaker points for device reliability, indicating the need to improve the EG thickness homogeneity, up to 100% 1L coverage.

4. Conclusions and Outlooks

In conclusion, the main challenges related to the ALD of ultra-thin insulators on Gr for electronics were discussed, with special attention to the state-of-the-art approaches employed to promote the nucleation on the sp^2 Gr surface. Recent developments in two-step ALD processes with "in- situ" H_2O-assisted seed-layer at low temperature were reviewed, as this approach presents many advantages with respect to conventional ALD on Gr with ex-situ seed-layer deposition in terms of purity of the grown film. The drawbacks of the seed-layer aided approaches in electronic applications, e.g., the increase of the equivalent oxide thickness and charge trapping at the Gr/seed-layer interface, were also discussed. Hence, due to their huge interest, the status of seed-layer free ALD growth of dielectrics on pristine Gr was also reviewed. The approaches aimed at tailoring the deposited films uniformity by tuning deposition parameters (e.g., temperature and the precursors residence time) were discussed. Furthermore, the role played by the interaction of Gr with the underlying substrate on the ALD nucleation was elucidated. In particular, the peculiar polar charges generated at the Gr/metal interface are considered as responsible for very homogeneous ALD deposition on CVD Gr residing on the native

metal substrates (Cu or Ni-Au). Highly uniform Al_2O_3 films were also obtained by seed-layer-free thermal ALD on highly homogeneous monolayer epitaxial Gr on on-axis 4H-SiC (0001), where the enhanced nucleation behavior is related to the buffer layer between the Gr and the underling substrate.

Several open challenges remain in the ALD of high-k dielectrics on Gr for electronics applications. The majority of studies reported so far concern the ALD of binary metal-oxides on Gr, whereas very limited work has been devoted to the development of ALD approaches for the growth of other important insulators on Gr, such as the nitrides (including SiN_x, AlN, etc.). To date, plasma assisted CVD has been mainly employed for the integration of these insulators on Gr [66,67]. Although plasma assisted-ALD allows a superior control on the uniformity of SiNx [68] and AlN [69] thin films, the main issue is the plasma-induced damage or doping in Gr. Considering the increasing interest in the integration of nitrides with Gr for optoelectronics and high frequency electronics [70], optimized ALD approaches for the growth of these materials on Gr is envisaged for the next years.

Besides Gr, other 2D materials (including transition metal dichalcogenides, phosporene, silicene, and other X-enes) need the integration of insulators for applications such as electronics, optoelectronics, and sensing [71,72]. Additionally, in these cases, ALD has been employed as the method of choice for low temperature deposition of thin high-k dielectric layers [73]. Detailed studies on the nucleation mechanisms and seed layer approaches to achieve optimal coverage and dielectric properties on these 2D materials will be necessary in the next future.

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