Symmetrical three-phase seven-level E-type inverter for PV systems: design and operation

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Abstract: Solar photovoltaic (PV) is one of the most favourable renewable energy types today, the use of which has grown throughout the world, and much more is expected in the future due to the continuous price drop. It is important to further develop renewable systems to generate green energy, which results in the reduction of air pollution and in enabling a future sustainable society for the next generation of people. Accordingly, new topologies of the multilevel converter have been proposed and investigated for PV applications to achieve high efficiency and high-power density. This study presents the analysis and design of the symmetrical three-phase E-type inverter (S-3Φ7L E-type). The proposed topology is directly derived from the T-type converter and exhibits seven voltage levels at the output offering interesting performance in terms of power semiconductors current and voltage stress. The hardware design process of the converter has been carried out to enhance the efficiency conversion. Finally, theoretical results are carefully verified by testing the converter prototype, featuring a peak efficiency of 99%.

1 Introduction

In modern society, the high demand for energy comes from transportation, the industry, and the commercial applications, as well as the urgent need to solve the global environmental concern has been the major driving force in seeking and developing clean and renewable energy [1]. Today, wind and solar photovoltaic (PV) energy are the most used and implemented renewable energies [2]. To limit both the DC, which strongly reduces the ohmic losses, and the cost of PV modules, today, the aim is to grow the size of PV plants [3–5]. Increasing the DC-link voltage, while keeping the power constant, results in a current reduction, which helps to reduce the size, weight, and costs of the whole PV system [6, 7]. In this scenario, interfacing PV systems to the grid and/or loads is a tough task due to the different nature of the energy; thus, power electronic systems underpinned by advanced control strategies are the key to achieve high reliability and high-efficiency conversion.

A power electronic system is composed of four main parts: (i) a set of power semiconductors, (ii) a network of passive devices (inductors, transformers, and capacitors), (iii) a control platform, and (iv) a control algorithm. The efficiency and power density of power conversion systems are essentially influenced by the power semiconductors and their arrangement, as well as by the passive devices such as transformers, inductors, and capacitors. The heart of the power semiconductors is the silicon material, whereas the passive devices are manufactured with iron, copper, and aluminium. The idea to enhance the performance of power conversion systems is to use more power devices and less iron, copper, and aluminium. Furthermore, the cost of silicon material is reduced compared to the cost of the iron, copper, and aluminium in the last few decades. Accordingly, even if the power converter switch count increases, there is no guarantee that the cost of the whole system increases [8].

Power converters need to be selected and designed optimally to provide maximum energy efficiency, ensuring high quality of the waveforms, reliability, and safety of the overall PV system. Multilevel converters, due to their ability to work only with a fraction of the total DC-bus voltage, are key elements in many applications, such as PV systems, where the efficiency, the power density, and the quality of the voltage and current waveforms are dominant features in the conversion system [9]. In fact, by working

on a fractional DC-bus voltage instead of full DC voltage, the devices with low-voltage ratings exhibit good performance in terms of switching and conduction losses. Thus, the use of power devices with low-voltage rating in multilevel converter structures is one of the most important challenges to reach the desired converter performance. Furthermore, the multilevel converters allow having low common-mode voltages, reduced voltage derivatives (dv/dt), lower high-order harmonics that can be easily filtered increasing the power quality [10–12]. Hence, this characteristic jointly to their aptitude to work at the high-switching frequency, allow limiting the filter weight and volume [11, 13, 14]. The downside is that the selection of the voltage levels number is not a random process, but it depends on several aspects, such as the rated/maximum DC-bus voltage, current and voltage stress on the power semiconductors, the device switching speed, the commutation inductance etc. [13].

Over the last few decades, many multilevel and multi-cell topologies have been developed being still under investigation [9, 10]. Each one of multilevel topologies has its own pros and cons which gives great flexibility to select the right topology for each application [14–23]. For instance, the cascaded H-bridge converter in [15, 16] is widely used in PV applications, thanks to its ability to be fed by separated DC sources, resulting in individual module maximum power point tracking capability. Recently other multilevel topologies such as neutral point clamped (NPC) converter [17], flying capacitor (FC) converters [18], T-Type converters [12, 19, 20], modular multilevel converters [10, 21], and hybrid multilevel converters [22, 23] are used in PV applications.

This paper focuses on the analysis and investigation of the high-efficiency seven-level (7L) multilevel converter to be used in PV applications. The proposed converter topology, called symmetrical three-phase E-type inverter (S-3Φ7L E-type inverter), helps in optimising the required DC-bus voltage and the voltage rating of the power semiconductors, allowing to overcome the devices voltage stress in the PV applications at 1.5 kV DC-bus voltage. Starting from the basic seven voltage levels converters, such as neutral point-clamped (NPC) [24] and FC [24], other 7L converters have been proposed in the literature, such as active boost neutral-point-clamped (ABNPC) [25], 7L P2 inverter (P2-I) [26], and 7L hybrid converters [27–29]. A low number of power devices are offered by the ABNPC [25], hybrid NPC [27], and hybrid T-type [29] topologies. However, the proposed 7-L E-type inverter may
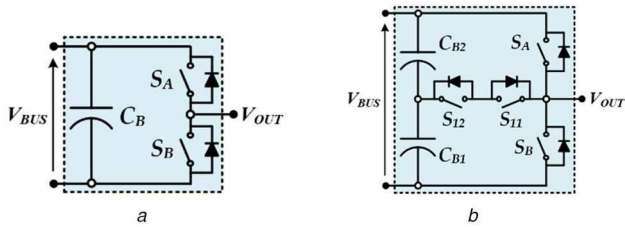
Fig. 1 *Single-phase topology*
(a) Single-phase leg inverter, *(b)* Single-phase T-type inverter
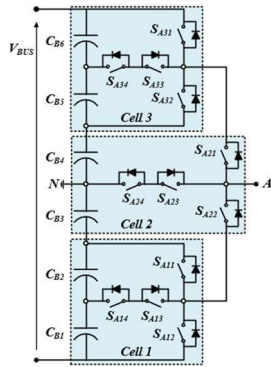

Fig. 2 *Circuit schematic of the S-3Φ7L E-type inverter*
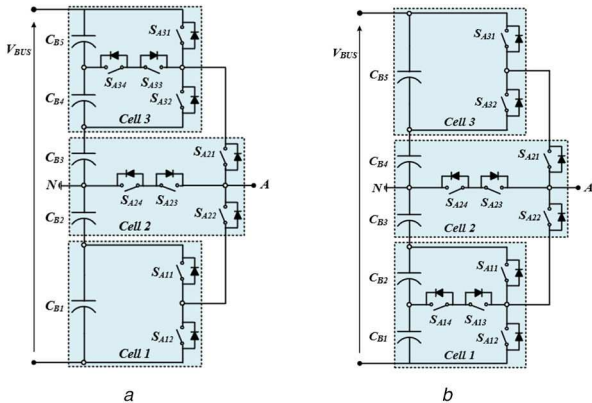

Fig. 3 *Circuit schematic of the A-3Φ7L E-type inverter*
(a) Type 1, the single-phase inverter is located to the bottom part, *(b)* Type 2, the single-phase inverter cell is located to the top part

have better conduction and switching losses compared to the other topologies, as will be explained later. The only drawback of the proposed topology, as well as the NPC, active neutral-point-clamped (ANPC), and FC topologies, compared to the hybrid topologies, is the voltage unbalancing across the DC-link capacitors. The main contribution of this paper is to propose, analyse, and implement a new 7L inverter topology for PV applications able to improve the efficiency and the quality of the output voltage thanks to the use of power semiconductors with low voltage and current stress.

The derivation of the topology, the general analysis, and the modulation scheme have been discussed in Section 2. A review of the S-3Φ7L E-type converter mode of operations is provided in Section 3. Section 4 shows the voltage and current stresses of the power semiconductors located in the proposed inverter. Power semiconductors selection and performance of the converter, heat-sink design, and DC-bus capacitors analysis are carefully addressed in Section 5. The experimental results of the converter prototype are discussed in Section 6 and finally, the conclusions of the paper are given in Section 7.

2 3Φ7L E-type topology derivation

Starting from the conventional single-phase inverter and single-phase T-type inverter shown in Fig. 1, it is possible to derive
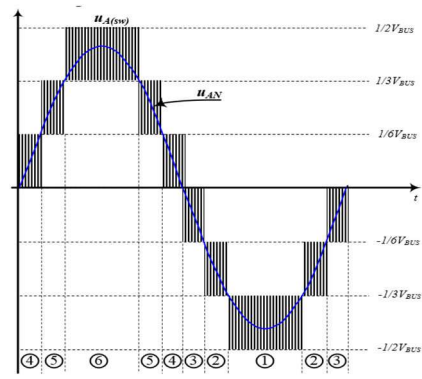
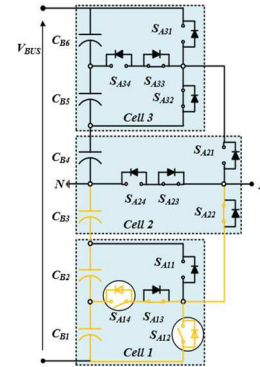**Fig. 4** *Line-to-neutral switching voltage $u_{A(sw)}$*

Fig. 5 *Inverter operating in sector 1*

different topologies. For instance, the converter illustrated in [11, 19] is composed of the combination of two basic single-phase inverters and one basic single-phase T-type converter. The proposed topology in this paper is based on the T-type topology. Particularly, each phase of the S-3Φ7L E-type inverter [20] consists of six series-connected DC-bus capacitors C_{B1}, C_{B2}, C_{B3}, C_{B4}, C_{B5}, and C_{B6}, and three single T-type cells, as shown in Fig. 2. This converter is called symmetrical three-phase E-type inverter (S-3Φ7L E-type inverter). Unlike the S-3Φ7L E-type, the asymmetrical three-phase E-type inverter (A-3Φ7L E-type inverter) can be realised using two basic single-phase T-type inverters and one basic single-phase inverter, as illustrated in Fig. 3.

In the A-3Φ7L E-type inverter of type 1, Fig. 3*a*, the single-phase inverter cell is located at the bottom part of the circuit, while in the A-3Φ7L E-type inverter of type 2, Fig. 3*b*, the single-phase inverter is placed at the top part of the circuit. In both cases, there are only five DC-bus capacitors and the phase-to-neutral switching voltage waveform shows six voltage levels.

3 Symmetrical 3Φ7L E-type inverter

In this section, the general analysis of the S-3Φ7L E-type inverter is proposed.

3.1 Inverter characteristics

The voltage across every single DC-side capacitor is $v_{CB1} = v_{CB2} = v_{CB3} = v_{CB4} = v_{CB5} = v_{CB6} = 1/6 V_{BUS}$. The line-to-neutral switching voltage $u_{x(sw)}$, with $x \in \{A, B, C\}$, shows seven voltage levels, as illustrated in Fig. 4. As can be seen from Fig. 4, the S-3Φ7L E-type inverter works in six different areas.

- Area 1. The first harmonic of the phase-to-neutral voltage u_{AN} is negative. According to the switches S_{x14} and S_{x12}, the line-to-neutral switching voltage $u_{A(sw)}$ is between two values $-1/2V_{BUS}$ and $-1/3V_{BUS}$. Fig. 5 shows the commutation path highlighted in orange and the switching devices involved in this sector.
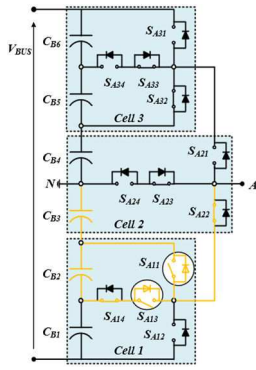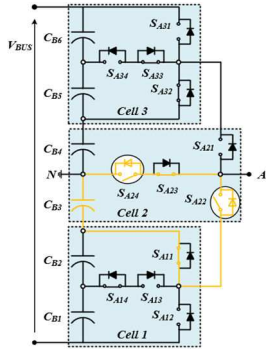
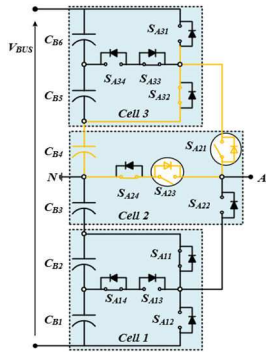**Fig. 6** *Inverter operating in sector 2*

Fig. 7 *Inverter operating in sector 3*

Fig. 8 *Inverter operating in sector 4*

Fig. 9 *Inverter operating in sector 5*

Fig. 10 *Inverter operating in sector 6*
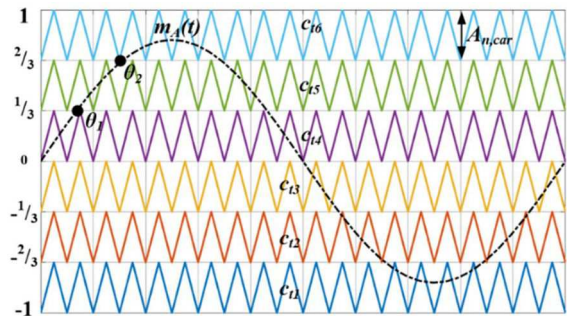
Fig. 11 *Modulation strategy of the single-phase S-1Φ7L E-type inverter*

- Area 2. The line-to-neutral switching voltage $u_{A(\text{sw})}$ can take on two discrete values $-1/3V_{\text{BUS}}$ and $-1/6V_{\text{BUS}}$ according to the states of the switches S_{x11} and S_{x13}. The commutation path and switching devices operating in sector 2 are illustrated in Fig. 6.
- Area 3. The switching voltage $u_{A(\text{sw})}$ is included between two discrete values $-1/6V_{\text{BUS}}$ and 0 according to the states of switches S_{x22} and S_{x24}. Fig. 7 shows both the switching devices and commutation operating in this sector.
- Area 4. In this area, the first harmonic of the voltage u_{AN} becomes positive. The line-to-neutral switching voltage $u_{A(\text{sw})}$ is included between 0 and $1/6V_{\text{BUS}}$ according to the states of the switches S_{x21} and S_{x23}. Fig. 8 shows both the switching devices and commutation operating in area 4.
- Area 5. The switching voltage $u_{A(\text{sw})}$ can take two values $1/6V_{\text{BUS}}$ and $1/3V_{\text{BUS}}$ according to the states of switches S_{x32} and S_{x34}. The commutation path and switching devices operating in sector 5 are illustrated in Fig. 9.
- Area 6. The line-to-neutral switching voltage $u_{A(\text{sw})}$ is included between $1/3V_{\text{BUS}}$ and $1/2V_{\text{BUS}}$ according to the states of switches S_{x31} and S_{x33}. The commutation path and switching devices operating in sector 5 are illustrated in Fig. 10.
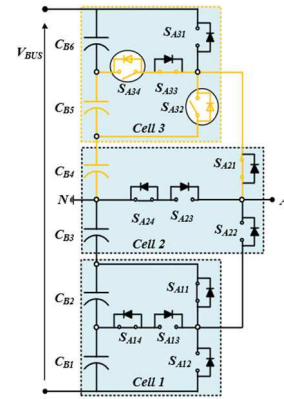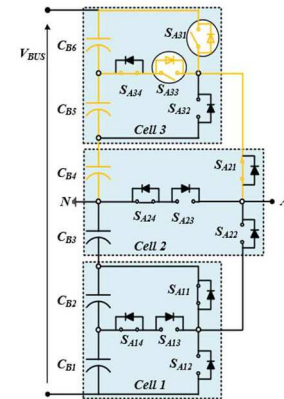
3.2 Modulation scheme and duty cycles

A phase disposition (PD) multilevel pulse width modulation (PWM) [30] has been implemented to control the proposed converter. Fig. 11 shows the modulation strategy associated with the single-phase converter, where the modulating signal of phase A is compared to the six carrier signals, c_{t1}, c_{t2}, c_{t3}, c_{t4}, c_{t5}, and c_{t6}. Modulating signals can be written as in (1), with $x \in \{A, B, C\}$ and $y \in \{0, 1, 2\}$, where M_0 is the inverter modulation depth, $-1 \le M_0 \le 1$ and ω_0 is the output frequency. Each carrier controls two different devices in opposite phase ($S_{x12} \leftrightarrow S_{x14}$, $S_{x11} \leftrightarrow S_{x13}$, $S_{x22} \leftrightarrow S_{x24}$, $S_{x21} \leftrightarrow S_{x23}$, $S_{x32} \leftrightarrow S_{x34}$, $S_{x31} \leftrightarrow S_{x33}$). The angles θ_1 and θ_2 between the control signals and the modulating signal are specified in (2)

$$m_x(t) = M_0\sin\left(\omega_0 t - y\frac{2\pi}{3}\right) \tag{1}$$

$$\begin{aligned}\theta_1 &= \omega_0 t_1 = \arcsin\left(\frac{1}{3M_0}\right) \\ \theta_2 &= \omega_0 t_2 = \arcsin\left(\frac{2}{3M_0}\right)\end{aligned} \tag{2}$$

Table 1 Duty cycles of the devices located into S-3Φ7L E-type inverter

$$d_{x11}(t) = \begin{cases} 2 + 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \begin{aligned} &\pi + \theta_1 \le \theta < \pi + \theta_2 \& \\ &2\pi - \theta_2 < \theta \le 2\pi - \theta_1 \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x12}(t) = \begin{cases} -\left[2 + 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right)\right] & \pi + \theta_2 \le \theta \le 2\pi - \theta_2 \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x13}(t) = \begin{cases} -1 - 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \begin{aligned} &\pi + \theta_1 \le \theta < \pi + \theta_2 \& \\ &2\pi - \theta_2 < \theta \le 2\pi - \theta_1 \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x14}(t) = \begin{cases} 3\left[1 + M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right)\right] & \pi + \theta_2 \le \theta \le 2\pi - \theta_2 \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x21}(t) = \begin{cases} 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \begin{aligned} &0 \le \theta < \theta_1 \& \\ &\pi - \theta_1 < \theta \le \pi \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x22}(t) = \begin{cases} -3M_0\sin\left(\omega_0 t - y\dfrac{2\pi}{3}\right) & \begin{aligned} &\pi \le \theta < \pi + \theta_1 \& \\ &2\pi - \theta_1 < \theta \le 2\pi \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x23}(t) = \begin{cases} 1 - 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \begin{aligned} &0 \le \theta < \theta_1 \& \\ &\pi - \theta_1 < \theta \le \pi \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x24}(t) = \begin{cases} 1 + 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \begin{aligned} &\pi \le \theta < \pi + \theta_1 \& \\ &2\pi - \theta_1 < \theta \le 2\pi \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x31}(t) = \begin{cases} -2 + 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \theta_2 \le \theta \le \pi - \theta_2 \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x32}(t) = \begin{cases} 2 - 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \begin{aligned} &\theta_1 \le \theta < \theta_2 \& \\ &\pi - \theta_2 < \theta \le \pi - \theta_1 \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x33}(t) = \begin{cases} 3\left[1 - M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right)\right] & \theta_2 \le \theta \le \pi - \theta_2 \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x34}(t) = \begin{cases} -1 + 3M_0\sin\left(\theta - y\dfrac{2\pi}{3}\right) & \begin{aligned} &\theta_1 \le \theta < \theta_2 \& \\ &\pi - \theta_2 < \theta \le \pi - \theta_1 \end{aligned} \\ 0 & \text{Otherwise} \end{cases}$$

$$d_{x,\text{switch}}(t) = \frac{1}{A_{n,\text{car}}}\left[\left(\frac{A_{n,\text{car}}}{2} - m_{n,\text{car}}\right) + m_x(t)\right] \quad (3)$$

The duty cycle of the devices can be obtained from (3), where $A_{n,\text{car}}$ is the amplitude of the carriers and $m_{n,\text{car}}$ is the offset of the carriers, with $n = 1, 2, 3, 4, 5,$ and 6. Replacing (1) into (3), the duty cycles for each power semiconductors have been obtained. Table 1 listed the duty cycles for each device.

4 Switch voltage and current stress

4.1 Switches configuration

The devices located in the middle leg of the converter, S_{x13}, S_{x14}, S_{x23}, S_{x24}, S_{x33}, and S_{x34}, are voltage and current bidirectional. The devices placed in the external leg of the single-cell T-type inverter, S_{x11}, S_{x12}, S_{x21}, S_{x22}, S_{x31}, and S_{x32} are voltage unidirectional and current bidirectional. The blocking voltage $V_{\text{BL(max)}}$ at a steady-state across the power semiconductors when $V_{\text{BUS}} = 1.5$ kV is shown in Figs. 12 and 13. Looking at Fig. 12a, the maximum blocking voltage across S_{x11}, S_{x12}, S_{x31}, and S_{x32} is $1/3 V_{\text{BUS}}$.

The blocking voltage is $1/6 V_{\text{BUS}}$ for the devices S_{x13}, S_{x14}, S_{x33}, and S_{x34}, as illustrated in Fig. 12b. The maximum blocking voltages across S_{x21}, S_{x22} and S_{x23}, S_{x24} are $2/3 V_{\text{BUS}}$ and $1/2 V_{\text{BUS}}$, respectively, as illustrated in Fig. 13. It is easy to understand from this analysis that the blocking voltage at a steady-state depends on
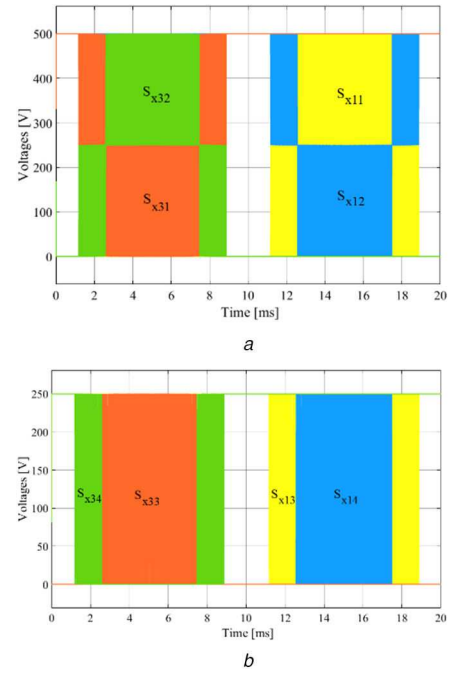

Fig. 12 *Blocking voltages of the switches in the S-3Φ7L E-type inverter at a steady-state*
(a) S_{x11}, S_{x12}, S_{x31}, S_{x32}, *(b)* S_{x13}, S_{x14}, S_{x33}, S_{x34}
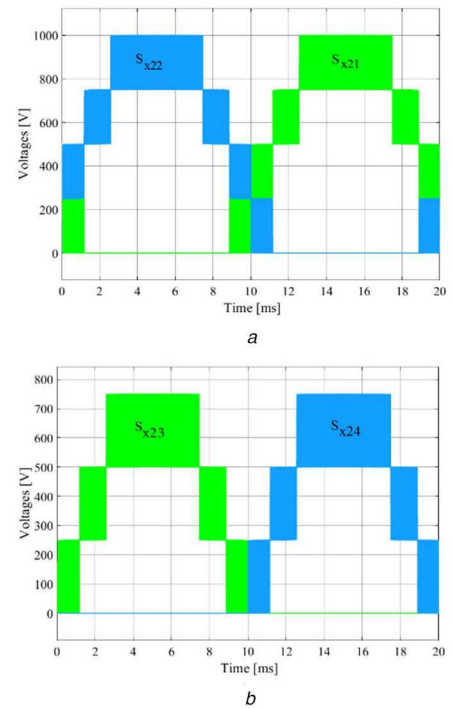

Fig. 13 *Blocking voltages of the switches in the S-3Φ7L E-type inverter at a steady-state*
(a) S_{x21}, S_{x22}, *(b)* S_{x23}, S_{x24}

the switches position into the converter arrangement. From blocking voltages, the technology of the power semiconductors can be selected. For example, the devices S_{x21}, S_{x22}, S_{x23}, and S_{x24} can be 1200 V silicon carbide metal–oxide–semiconductor field-effect transistor (SiC-MOSFET), the switches S_{x11}, S_{x12}, S_{x31}, and S_{x32} can be 650 V SiC-MOSFET and the devices S_{x13}, S_{x14}, S_{x33}, and S_{x34} can be 300 V SiC-MOSFET.

4.2 Device current stress

The average and root mean square (RMS) currents flowing in the devices of the converter have been estimated according to (4),

where $i_x(t)$ is the phase to neutral current, $d_{x,\text{switch}}$ is the duty cycle of the devices previously calculated and T_0 is the fundamental period

$$I_{\text{RMS}} = \sqrt{\frac{1}{T_0} \int_0^{T_0} \left[i_x^2(t) \cdot d_{x,\text{switch}}(t) \right] \mathrm{d}t}$$

$$I_{\text{AVG}} = \frac{1}{T_0} \int_0^{T_0} \left[i_x(t) \cdot d_{x,\text{switch}}(t) \right] \mathrm{d}t \qquad (4)$$

Table 2 Single-phase inverter parameters

phase-to-neutral RMS voltage u_{AN}	[V]	495
DC-bus voltage V_{BUS}	[kV]	1.5
switching frequency f_{sw}	[kHz]	20
output frequency f_0	[Hz]	50
power factor	—	1
rated power P_0	[kW]	13.34
RMS phase current I_0	[A]	26.26

Table 3 Average and RMS current coefficients of the power semiconductors

i	Devices	Coefficients
1	S_{x11}, S_{x32}	$a_i = 6(\theta_1 - \theta_2) - 3\sin(2\theta_1) + 3\sin(2\theta_2)$
		$b_i = 8[-\cos(\theta_1) + \cos(\theta_2)] - 4[\cos(\theta_1) - 1]$
		$c_i = \cos(\theta_1)\left(\cos(\theta_1)^2 - 3\right) - \cos(\theta_2)\left(\cos(\theta_2)^2 - 3\right)$
		$d_i = \theta_1 - \sin(2\theta_1) - 2(\theta_1 - \theta_2) + \sin(2\theta_2)$
2	S_{x12}, S_{x31}	$a_i = 3[\pi - 2\theta_2 + \sin(2\theta_2)]$
		$b_i = 8\cos(\theta_2)$
		$c_i = 2\cos(\theta_2)\left(3 - \cos(\theta_2)^2\right)$
		$d_i = 2\theta_2 - \pi + \sin(2\theta_2)$
3	S_{x21}, S_{x22}	$a_i = 2\theta_1 - 3\sin(2\theta_1)$
		$b_i = 1 - 4\cos(\theta_1)$
		$c_i = 2(\cos(\theta_1) + 2)\left(\cos(\theta_1)^2 - 1\right)$
		$d_i = \frac{1}{2}(1 - 2\theta_1 - \sin(2\theta_1))$
4	S_{x23}, S_{x24}	$a_i = 6\theta_1 - 3\sin(2\theta_1)$
		$b_i = -8\theta_2 - 12\theta_1 - 4\sin(2\theta_1) + 4\sin(2\theta_2)$
		$c_i = (\cos(\theta_1) - 1)^2\left(\cos(\theta_1)^2\right)$
		$d_i = 3\theta_1 + 2\sin(2\theta_1) - 1$
5	S_{x13}, S_{x14}, S_{x33} S_{x34}	$a_i = 6(\theta_1 + \theta_2) + 3\sin(2\theta_1) - 6\sin(2\theta_2)$
		$b_i = 8\cos(\theta_2) - 4\cos(\theta_1)$
		$c_i = (\theta_1 - \theta_2) - \sin(2\theta_1) + \sin(2\theta_2)$
		$\quad + 2\cos(\theta_1)\left(\cos(\theta_1)^2 - 3\right) - 2\cos(2\theta_2)\left(\cos(\theta_2)^2 - 3\right)$
		$d_i = 2\theta_2 - \sin(2\theta_2) + \cos(\theta_2)\left(\cos(\theta_2)^2 + 1\right)$

By replacing the duty cycle given in Table 1 into (4) and considering the parameters of the inverter listed in Table 2, the average and RMS currents in each switch have been obtained. The compact form of the analytical expressions of the average and RMS currents flowing in each power semiconductor and their coefficients are listed in Table 3 in the Appendix. The average and RMS current values as a function of the output power are given in Table 4.

4.3 Stress comparison of 7L topologies

In this section, a comparative analysis between different single-phase 7L topologies is carried out. The number of power devices, including switches (insulated-gate bipolar transistor/MOSFET and antiparallel diode), diodes, DC-bus capacitors, and flying capacitors for the different topologies is shown in Table 5. In the worst case, during the peak of the inverter modulation index, the current flows through three power devices in the proposed 7-L E-type inverter, while the phase current flows through six power devices in the 7L NPC and 7L FC inverters [24, 25]. The same also happens with the other types of inverters. During the peak of the modulation index, the current involves four power devices in the 7L hybrid NPC [27], five power semiconductors in the 7L hybrid T-type [29], and six power devices in the 7L hybrid ANPC [31]. Although in the worst case, the current loop involves three power semiconductors in the 7L ABNPC [25], 7L P2-I [26], and 7L hybrid T-type [29] inverters, the main issue in such inverters compared to the proposed 7L inverter is that the phase current flows through the FC, which can generate high losses. Consequently, it can be asserted that the commutation loop and the current path of the proposed 7L topology are better than the other 7L topology, thus a reduction in conduction losses can be achieved. Since the current path of the 7L E-type inverter is short, the commutation inductance L_ξ can be of low value, generating a reduced overvoltage. The over-voltage commutation Δv is defined as in (5), where k_R is the coefficient that takes into account the resonance of the DC-bus circuit, L_ξ is the commutation inductance, di_{sw}/dt is the device current slope, and V_{FR} is the forward recovery voltage of the complementary freewheeling diode

$$\Delta v = k_R L_\xi \frac{di_{\text{sw}}}{dt} + V_{\text{FR}} \qquad (5)$$

As it can be noticed, when the commutation inductance L_ξ is increased, keeping constant the other parameters, the resulting overvoltage increases too. This means that the switching losses of the proposed inverter can be lower than in the other 7L topologies. Additionally, as it can be easily understood from the analysis made in the previous section, the blocking voltage of all power semiconductors of the proposed topology is $1/6 V_{\text{BUS}}$ during the commutations. However, the maximum blocking voltage equal to $2/3 V_{\text{BUS}}$ happens across the devices S_{x23}, or S_{x24} during either the negative peak or the positive peak of the modulation index. Table 5 shows the maximum voltage stress across the power components, DC-bus capacitor, and flying capacitors for the different 7L

Table 4 RMS and average devices current

P_0 [kW]		S_{x31} S_{x12}	S_{x32} S_{x11}	S_{x33}, S_{x34}, S_{x13}, S_{x14}	S_{x24} S_{x23}	S_{x21} S_{x22}
1.6	I_{AVG}	0.58	0.21	0.7	0.0	1.5
	I_{RMS}	2.4	0.9	1.2	0.5	2.1
3.34	I_{AVG}	1.2	0.4	1.4	0.0	3.0
	I_{RMS}	4.4	1.9	2.2	0.77	5.1
6.67	I_{AVG}	2.4	0.8	2.8	0.01	6.0
	I_{RMS}	7.7	4.25	3.6	1.5	10.2
10	I_{AVG}	3.5	1.3	4.1	0.02	8.9
	I_{RMS}	12.3	5.8	5.9	2.1	15.1
13.34	I_{AVG}	4.7	1.7	5.4	0.1	11.8
	I_{RMS}	17.6	7.8	8.2	2.5	19.6

Table 5 Number of devices and maximum voltage stress in 7-level inverter topologies

	Number of power devices	Number of DC-bus capacitors	Number of Flying capacitors	DC-bus capacitors voltage stress	Flying capacitors voltage stress	Power devices voltage stress
E-type [20]	12	6	—	$1/6V_{BUS}$	—	$2/3V_{BUS}$
NPC [24]	22	6	—	$1/6V_{BUS}$	—	$1/6V_{BUS}$
FC [24, 25]	12	2	5	$1/2V_{BUS}$	$5/6V_{BUS}$	$5/6V_{BUS}$
ABNPC [25]	8	2	2	$1/4V_{BUS}$	$1/2V_{BUS}$	$1/2V_{BUS}$
P2-I [26]	12	3	3	$1/3V_{BUS}$	$1/3V_{BUS}$	$1/3V_{BUS}$
hybrid NPC [27]	10	2	2	$1/2V_{BUS}$	$1/3V_{BUS}$	$1/2V_{BUS}$
hybrid clamped (HC) [28]	12	3	2	$1/3V_{BUS}$	$1/6V_{BUS}$	$1/3V_{BUS}$
hybrid T-type [29]	8	2	1	$1/2V_{BUS}$	V_{BUS}	V_{BUS}
hybrid ANPC [31]	16	2	1	$1/2V_{BUS}$	V_{BUS}	V_{BUS}
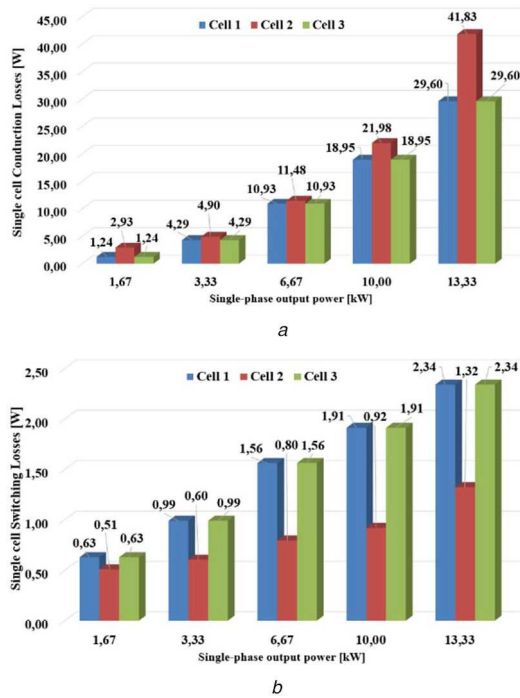
Fig. 14 *Single-phase power losses distribution of the devices located in a single cell*
(a) Conduction losses, *(b)* Switching losses

inverter topologies. The classical 7L NPC [24] has low-voltage stress across the devices, but the current can involve six power semiconductors in the worst case, which can generate high-conduction losses. The 7L P2-I [26] and 7L hybrid inverters [27, 28] show relatively low-voltage stress across the power semiconductors, however, the current path involves more than three devices. The 7L hybrid inverters in [29, 31] exhibit high-voltage stress across all the devices and the current path is very long since it involves five or even six power semiconductors. Finally, the 7L ABNPC inverter [25] shows good performance in terms of voltage and current stress compared to the 7L E-type inverter. Nevertheless, the 7L ABNPC inverter makes use of flying capacitors, which must be preloaded and can generate high losses. It is true that the maximum voltage stress across the power semiconductors in the 7L E-type inverter is equal to $2/3V_{BUS}$; however, when the devices must withstand that voltage the current through them is equal to zero. This means that the switching overvoltage Δv does not occur during the maximum voltage stress of the devices, but it occurs only during the commutations when the voltage across the semiconductors is equal to $1/6V_{BUS}$. According to this analysis, the proposed 7L E-type converter, even if it does not use a lower number of components, compared to the other 7L inverter topologies it presents lower voltage stress and good commutation loop, which can provide a better response in terms of efficiency.

5 Hardware design of the S-1Φ7L E-type inverter

This section focuses on the design procedure to realise the S-3Φ7L E-type converter. Particularly, the power losses are analytically evaluated to select suitable power components. After that, the design procedure to select the heat-sink is described and, finally, the DC-bus capacitors' analysis is addressed.

5.1 Power devices selection and efficiency

Based on the operating condition listed in Table 2, as well as the obtained voltage and current stress, the power devices have been selected. Particularly, the performance of the proposed converter has been carefully investigated by considering the SiC devices. The switches located in cell 1 and cell 3 of Fig. 2 are 650 V, 17 mΩ SiC-MOSFETs and 650 V, 40 A SiC diodes, while the devices located in cell 2 (see Fig. 2) are 1200 V, 22 mΩ SiC-MOSFETs and 1200 V, 40 A SiC diodes. The conduction and switching losses have been obtained by the analytical investigation. The conduction losses of power semiconductors are evaluated applying (6), where T_{sw} is the switching period, $V_{sw(0)}$ is the forward voltage drop, r_{sw} is the device ohmic resistance, and I_{AVG}, I_{RMS} are the previously achieved RMS and average currents

$$P_c \simeq V_{sw0}I_{AVG} + r_{sw}I_{RMS}^2 \tag{6}$$

The $V_{sw(0)}$ and r_{sw} values as a function of the junction temperature have been obtained from the MOSFETs and diodes datasheet. The switching losses have been achieved by applying (7), where $k_{1,on}$, $k_{2,on}$, $k_{1,off}$, and $k_{2,off}$ are the polynomial coefficients and V_{sw} is the voltage across the device during the switching action

$$P_{on} \simeq f_{sw}\overbrace{V_{sw}\left[k_{1,on}i_{sw}(t) + k_{2,on}i_{sw}^2(t)\right]}^{E_{on}}$$
$$P_{off} \simeq f_{sw}\overbrace{V_{sw}\left[k_{1,off}i_{sw}(t) + k_{2,off}i_{sw}^2(t)\right]}^{E_{off}} \tag{7}$$

Using the datasheet of the devices, the E_{on} and E_{off} values can be calculated performing a two-order polynomial approximation as in [32].

Losses of the power devices located in cell 1, cell 2, and cell 3 as a function of the output power are illustrated in Fig. 14. Fig. 14*a* shows that the conduction losses in cell 2 are higher than in cell 1 and cell 3. This happens because device S_{x21} is always in on state condition during the positive half-wave of the modulating signal and e device S_{x22} is always in on state condition during the negative half-wave of the modulating signal. Looking at Fig. 14*b* it is possible to notice that the switching losses in cell 1 and cell 3 are higher than the losses in cell 2 since the devices commutations located in cell 1 and cell 3 occur during the peak of the phase voltage waveform. Fig. 15 shows the efficiency and losses distributions related to the power devices as a function of modulation depth M_0 when the switching frequency f_{sw} is equal to 20 kHz. It can be seen from Fig. 15 that the efficiency shows an
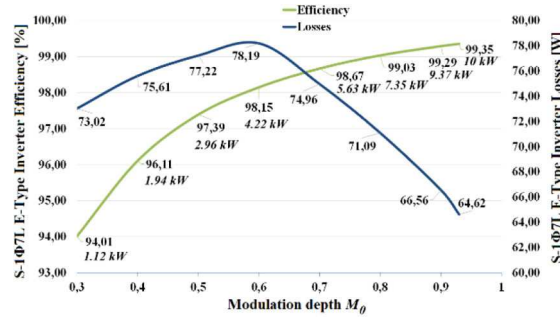
Fig. 15 *Losses and efficiency related to the power devices of the single-phase 7L E-type inverter versus modulation depth M_0 with f_{SW} = 20 kHz*

increasing trend when the modulation depth M_0 increases. Additionally, the losses exhibit an increasing trend when M_0 is <0.6 and a decreasing trend when M_0 is >0.6. The losses are significantly affected by the number of enabled voltage levels, the 7L E-type inverter works with five voltage levels when M_0 is <0.667 and it works with three voltage levels when M_0 is <0.337. A high value of the power losses occurs when M_0 is close to 0.66 because the devices S_{x13}, S_{x14}, S_{x33}, and S_{x34} are always closed since the inverter works with five voltage levels. In this condition, the current flows through three devices and the conduction losses of the devices S_{x13}, S_{x14}, S_{x33}, and S_{x34} are relatively high.

5.2 Heat-sink selection

According to the analysis obtained in the previous section, it can be calculated the thermal resistance between the heat sink and ambient $R_{th(s-a)}$ and then select the heatsink. The equivalent thermal circuit is considered as shown in Fig. 16, where T_j is the junction temperature, T_c is the case temperature, T_s is the heatsink temperature, and T_a is the ambient temperature. Moreover, $R_{th(j-c)}$ is the thermal resistance between the junction and the base-plate, $R_{th(c-s)}$ is the thermal resistance between the case and the heatsink, finally, $R_{th(s-a)}$ is the thermal resistance between the heatsink and the ambient. The maximum losses at rated power occur in cell 2. Particularly, the maximum power dissipated by a single MOSFET P_S (S_{A21} or S_{x22}) is about equal to 21 W, whereas the maximum power dissipated by a single diode is neglected in comparison with the losses in a single MOSFET due to the high-power factor operating point. Thus, considering a $R_{th(j-c)}$ equal to 0.65°C/W for the MOSFET, the maximum temperature range junction case is given by (8)

$$\Delta T_{jc} = R_{th(j-c)} P_{loss} \simeq 13.65°C \quad (8)$$

If the maximum junction temperature is set at 125°C, the maximum case temperature is obtained in (9)

$$T_{c,max} = T_{j,max} - \Delta T_{jc} = 111.35°C \quad (9)$$

Assuming the ambient temperature at 50°C, the thermal resistance $R_{th(j-c)}$ is given in (10), where P_T is the total losses of the single-phase E-type inverter versus about equal to 107 W at nominal power (see Fig. 14)

$$R_{th(c-a)} = \frac{T_{c,max} - T_a}{P_T} \simeq 0.57°C/W \quad (10)$$

The obtained resistance $R_{th(j-c)}$ value represents the maximum value that can be used for the heatsink to obtain the desired working temperature.

5.3 Switching frequency selection and output filters

The power losses and output filter design have a huge impact on the switching frequency f_{sw}. As can be noticed in (7) the switching losses are directly related to the switching frequency. Increasing f_{sw}
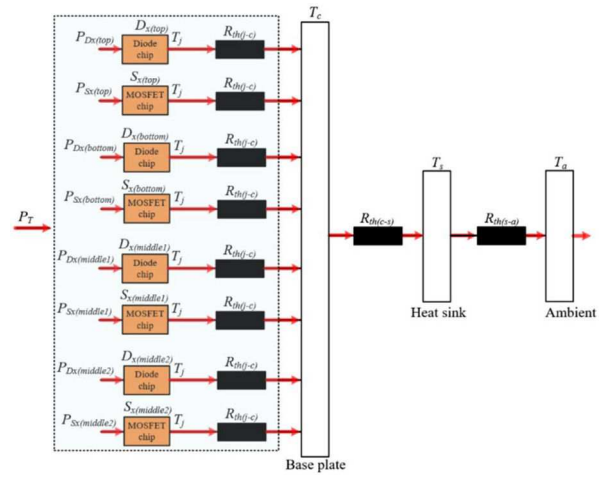

Fig. 16 *Equivalent thermal circuit of the single-cell T-type*
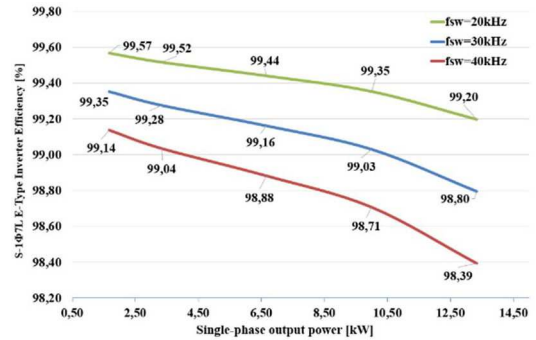

Fig. 17 *Efficiency of the single-phase 7L E-type inverter versus output power for different switching frequency values*

results in higher losses as shown in Fig. 17. On the other hand, increasing the switching frequency leads to small and cheap passive components. In fact, the variation of the flux density in the inductors is reduced when the frequency increases and, since the size and the volume of the core are reduced, the core losses are limited. Hence, the switching frequency can be selected according to the trade-off between power losses and the filter design. The inductors and capacitors of the output filters are designed according to the procedure proposed in [14]. Applying this method, the minimum capacitance and inductance values are about equal to 2 μF and 65 μH, respectively. Thus, the selected capacitance value is 7.2 μF and the selected inductance value is 80 μF. The filter board employed in [14] has been modified to be used in combination with the proposed converter.

5.4 DC-bus capacitor selection

The DC-bus capacitors are selected according to the DC-bus capacitor RMS current and DC-bus voltage ripple. The main problem of the proposed topology is the unbalancing voltage among the series-connected capacitors.
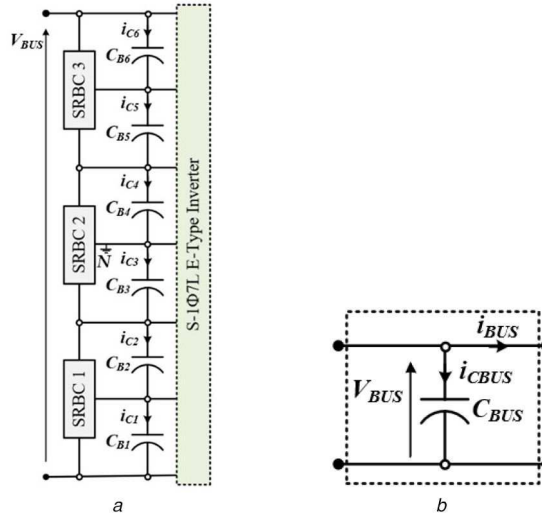
Fig. 18 *Model of the DC-bus capacitors*
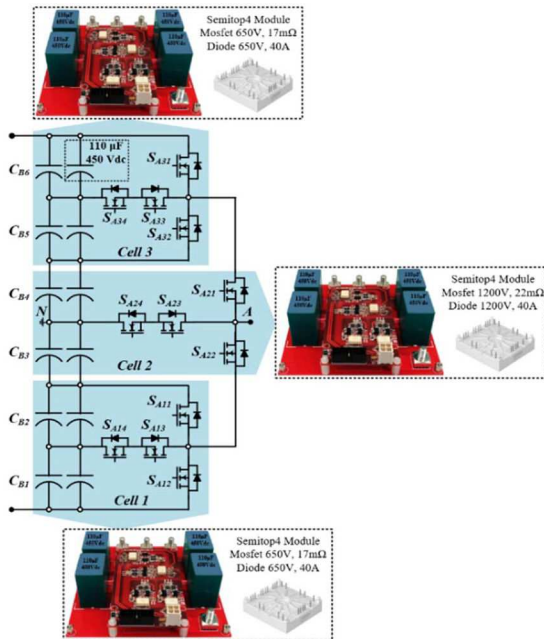*(a)* Equivalent circuit diagram, *(b)* Simplified circuit

Fig. 19 *S-1Φ7L E-type converter power modules*

The problem of the unbalancing voltages is not the focus of the present work. In this paper, it is assumed that three external series balancing circuits (SRBCs) [19] are used to balance the voltage across the capacitors in order to obtain six equal DC-bus current $i_{C1} = i_{C2} = i_{C3} = i_{C4} = i_{C5} = i_{C6} = i_{BUS}$, as shown in Fig. 18$a$. Fig. 18$b$ shows the equivalent DC-bus capacitor circuit. The instantaneous DC-bus current $i_{BUS}(t)$ over a fundamental period T_0 is composed of two terms: low-frequency current i_{LF}, related to the fundamental frequency and its harmonics, and high-frequency current i_{HF} linked to the switching frequency current and its harmonics. However, the low-frequency current has a strong impact on the capacitor losses, size, lifetime, and cost, thus the high-frequency current i_{HF} can be neglected. The low-frequency current can be found in case of the asymmetric condition in which the load current flows through one phase as in (11), where I_0 is the RMS load current, ω_0 is the fundamental frequency, and φ_0 is the phase displacement between the output voltage and the corresponding output current at the fundamental frequency

$$\begin{cases} i_A(t) = \sqrt{2}I_0 \sin(\omega_0 t - \varphi_0) \\ i_B(t) = 0 \\ i_C(t) = 0 \end{cases} \tag{11}$$

The relationship between the instantaneous DC-bus and the load power is given in

$$V_{BUS}i_{BUS}(t) = P_{out} = u_A(t)i_A(t) + u_B(t)i_B(t) + u_C(t)i_C(t) \tag{12}$$

Replacing (11) into (12), the low-frequency instantaneous DC-bus current is obtained as in (13), where V_0 and I_0 are the output RMS voltage and current

$$i_{LF}(t) = \frac{V_0 I_0}{V_{BUS}}[\cos \varphi_0 - \cos(2\omega_0 t)] \tag{13}$$

Looking at (13) it is possible to identify two main components: (i) the average component and (ii) the double fundamental frequency component. Assuming that the SRBCs compensate all the DC-bus current harmonics except the 100 Hz component, from (13) the RMS value of the double fundamental frequency can be written as in (14)

$$I_{CBUS}|_{100\,Hz} = \frac{V_0 I_0}{\sqrt{2}V_{BUS}} \tag{14}$$

Low-frequency voltage ripple is caused by the low-frequency capacitor current. The dominant low-frequency current is the second harmonic which flows to the DC-bus capacitors. Peak to peak voltage ripple can be approximated as in (15), where N_S is the number of the series capacitors and C_{BUS} is the partial DC-bus capacitor ($C_{BUS} = C_{B1} = C_{B2} = C_{B3} = C_{B4} = C_{B5} = C_{B6}$).

$$\Delta V_{BUS} = \frac{2\sqrt{2}}{(2\pi 100)C_{BUS}} N_S I_{CBUS} \tag{15}$$

Considering the peak-to-peak voltage ripple ΔV_{BUS}=300 V and according to (14) and (15), the required partial DC-bus capacitor value C_{BUS} is about 570 μF. Each phase leg of the 7L E-type converter requires a minimum capacitance of 190 μF; thus, it is possible to use two parallel and two series film capacitors for each cell of the single-phase inverter, as shown in Fig. 19. Hence, the 110 μF, 450 V_{dc} film capacitor (manufacturer EPCOS) has been selected.
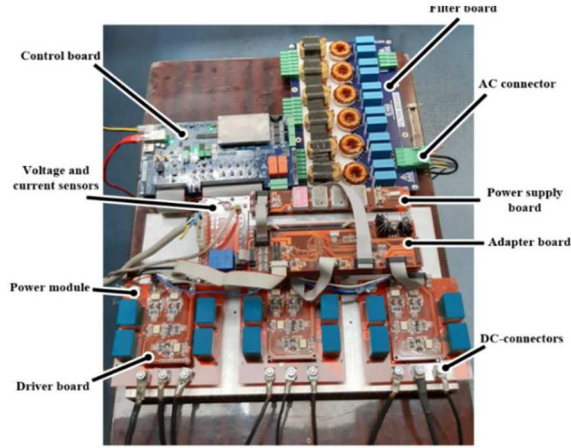
Fig. 20 *Single-phase 7L E-type converter prototype*

Table 6 List of the main components of the S-1Φ7L E-type inverter

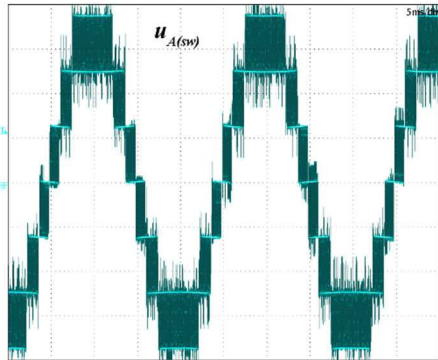|	
SiC-MOSFET	650 V, 17 mΩ, 1200 V, 22 mΩ
SiC diode	650 V, 40 A, 1200 V, 40 A
DC-link capacitor (each)	110 µF 450 Vdc
gate driver	ISO5452
custom filter inductor [14]	High Flux, CH330160
filter capacitor (each)	Kemet, 1.8 µF, 760 VAC
voltage sensor	AMC1200
current sensor	LAH25-NP
heat-sink	MeccAL

Fig. 21 *Phase-to-neutral switching voltage waveform of the phase A. 200 V/div, 5 ms/div*

# 6 Experimental verification

The symmetrical single phase 7L E-type inverter prototype is composed of three Semitop4 custom modules, as illustrated in Fig. 19. Cell 1 and cell 3 are realised using the 650 V, 17 mΩ SiC-MOSFETs (SCT3017AL) and 650 V, 40 A SiC diodes (SCS240AE2), whereas cell 2 is composed of 1200 V, 22 mΩ SiC-MOSFETs (SCT3030KL) and 1200 V, 40 A SiC diodes (SCS240KE2). The gate driver circuits are placed on the top side of the modules.

Experimental tests are performed according to Table 2 and considering six programmable DC power supply set at 250 V. The converter has been controlled using a dedicated control board, which uses the National Instruments System-on-Module (sbRIO-9651) [33].

Fig. 20 shows the prototype of the single-phase S-1Φ7L E-type converter with a filter board and control board. It is possible to see the DC-connectors, three power modules, driver circuits, power supply board, adapter board, voltage and sensors board (the current sensors are not visible in the picture because they are placed on the bottom side of the board), filter board (only one phase of the filter
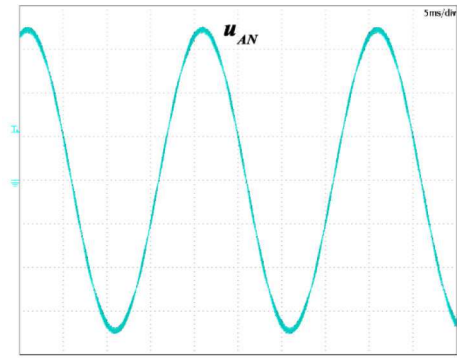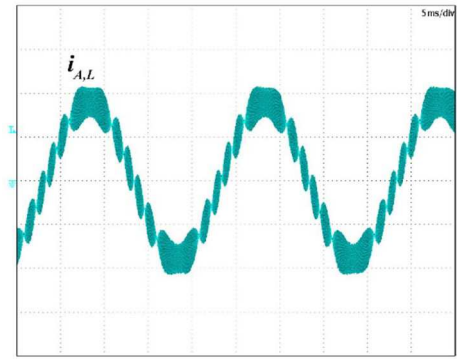
Fig. 22 *Voltage and current waveforms*
(a) Phase voltage waveform u_{AN}, *(b)* Phase current $i_{A,L}$. 200 V/div, 20 A/div, 5 ms/div

board is used), and control board. The list of the main components of the proposed converter is shown in Table 6.

6.1 Steady-state performance

Voltage and current waveforms are investigated using the Yokogawa DL9140 oscilloscope. The switching voltage waveform under a resistive load is illustrated in Fig. 21.

The phase voltage u_{AN} and inductor current $i_{A,L}$ waveforms at 40 kW output power condition are shown in Fig. 22. The previous figures (Figs. 21 and 22) are obtained when the modulation depth M_0 is close to 1. Based on the analysis proposed in [34], the Fourier series expansion of the phase-to-neutral output voltage using the PD PWM with reference to the DC-bus voltage V_{BUS} and to modulation depth M_0 is given in (16), where n is the harmonic order, m is the number of levels, ω_0 is the fundamental angular frequency, ω_s is the switching angular frequency, J_l is the lth order Bessel function of the first kind. The amplitude of the harmonics in the phase-to-neutral switching voltage strongly depends on the modulation depth and a number of levels.

Fig. 23 shows the normalised harmonic content before and after filtering the phase-to-neutral voltage u_{AN}, under resistive load

$$
\begin{aligned}
u_{AN(sw)}(t) = {} & \frac{V_{BUS}M_0}{2}\sin\omega_0 t + \left[\sum_{n=1}^{\infty}\left(\frac{4V_{BUS}}{n(m-1)\pi}\right)\right. \\
& \left[2\sum_{l=1}^{\infty}J_{2l-1}\left(\frac{M_0 n(m-1)\pi}{2}\right)\right]\sin[(2l-1)\omega_0 t] \\
& \cos\left(\frac{n(m-1)\pi}{2}\right) - \left\{J_0\left(\frac{M_0 n(m-1)\pi}{2}\right)\right. \\
& \left. + 2\sum_{l=1}^{\infty}J_{2l}\left(\frac{M_0 n(m-1)\pi}{2}\right)\right. \\
& \left.\left.\cos(2l\omega_0 t)\left(\frac{n(m-1)\pi}{2}\right)\right\}\right]\cos n(m-1)\omega_s t
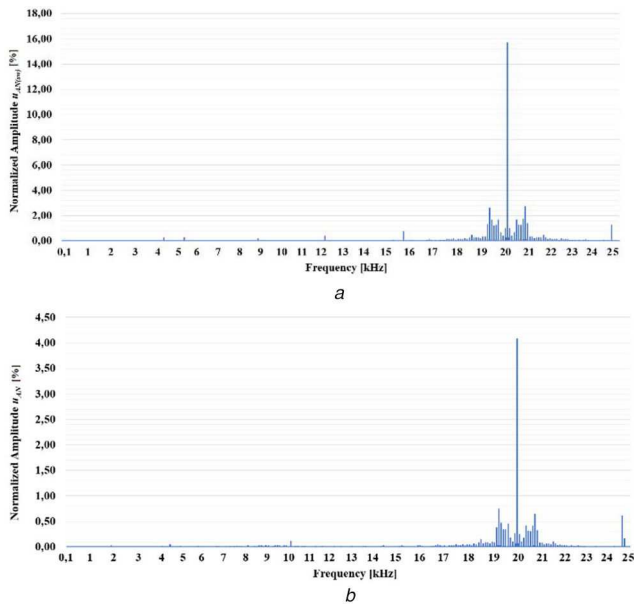\end{aligned} \tag{16}
$$

Fig. 23 *Normalised phase-to-neutral voltage harmonic content with $M_0 = 0.93$*
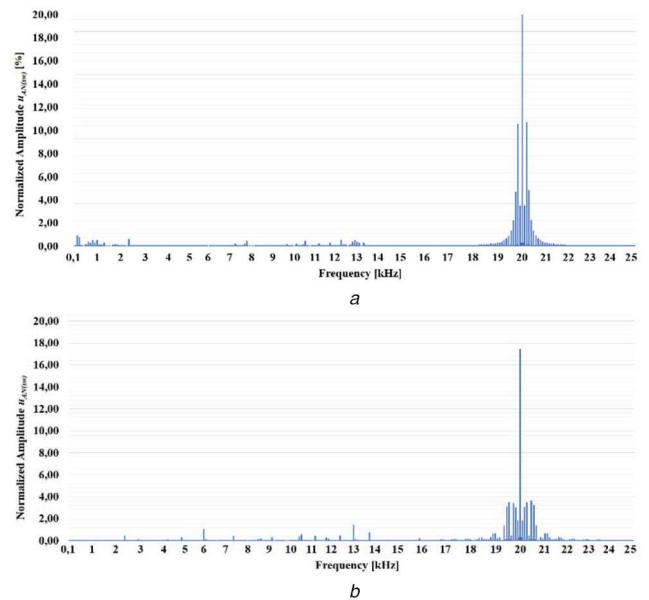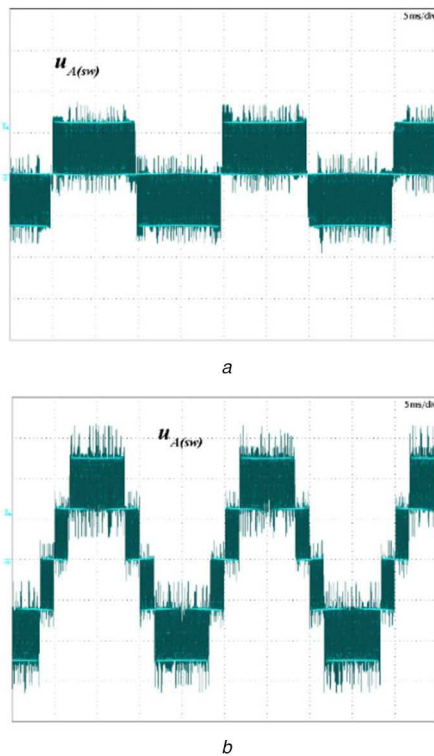*(a)* Before the filter $u_{AN(sw)}$, *(b)* After the filter u_{AN}

Fig. 24 *Phase-to-neutral switching voltage for different values of the modulation depth*
(a) $M_0 = 0.3$, *(b)* $M_0 = 0.65$. 200 V/div, 5 ms/div

Table 7 THD of the output voltage at the input and output of the line filter for different values of the modulation depth M_0

	$M_0 = 0.3$	$M_0 = 0.65$	$M_0 = 0.93$
THD at filter input	0.93	0.41	0.27
THD at filter output	0.44	0.21	0.09

The horizontal axis shows the frequency and the vertical axis illustrates the harmonic amplitudes normalised to the fundamental harmonic. It can be seen that the harmonic contents of the u_{AN} after the output filter is strongly reduced. The phase-to-neutral switching


Fig. 25 *Normalised phase-to-neutral switching voltage harmonic content*
(a) $M_0 = 0.3$, *(b)* $M_0 = 0.65$

voltage for different values of the modulation depth is shown in Fig. 24. When M_0 is set at 0.3, Fig. 24*a*, the converter shows three voltage levels and only the cell 2 is working and the switches S_{x11} and S_{x32} are always turned-on. The converter behaviour is reduced to the classic T-type inverter. When M_0 is set at 0.65, the converter displays five voltage levels, as illustrated in Fig. 24*b* and the switches S_{x12} and S_{x31} are always turned-off. Fig. 25 illustrates the normalised harmonic content of the phase-to-neutral switching voltage when the modulation depth M_0 is equal to 0.3 and 0.65, respectively. The vertical axis is normalised with respect to the fundamental harmonic. It can be noticed that when the modulation depth is reduced the harmonic content of the output voltage is degraded since the number of levels is reduced according to (16). Comparing Fig. 25 to the harmonic distribution of Fig. 23*a*, the amplitude of the peaks at the switching frequency is greater when the modulation depth is lower. Finally, the total harmonic distortion (THD) at the input and output of the line filter for different values of the modulation depth M_0 is listed in Table 7. The blocking voltage waveforms at steady state of the devices S_{x31}, S_{x32}, S_{x33}, S_{x34}, S_{x21}, and S_{x23} located in the top half circuit of the inverter are shown in Figs. 26–28.

The remaining power switches in the inverter have the complementary blocking voltage due to the symmetry of the converter. The illustrated experimental results confirm the theoretically evaluated voltage distribution across power components.

6.2 Performance evaluation

The efficiency of the S-1Φ7L E-type inverter is measured through the Voltech PM3000A power analyser. One channel of the power analyser is used to measure the input power at the DC-bus and two channels are used to measure the output power through Aron's insertion.

The efficiency as a function of the power has been obtained for different values of the switching frequency f_{sw}. After that, the measured efficiency curves are compared with the analytically calculated efficiency curves. Fig. 29 shows the total efficiency comparison between the experimental and analytical results including the power devices, the DC-bus capacitors, and the output filter for two values of the switching frequency, 20 kHz (green line) and 40 kHz (red line). The total efficiency as a function of the modulation index is shown in Fig. 30. The green line is related to efficiency at 20 kHz and the red line is related to the efficiency at 40 kHz. It can be seen the good matching between the theoretical results (solid line) and the experimental results (dashed line). The
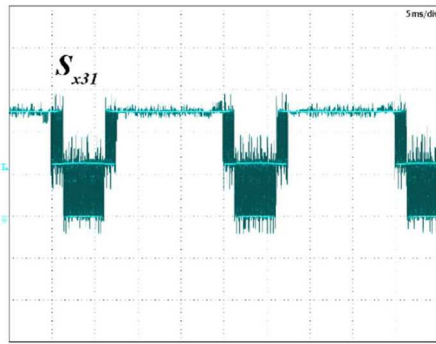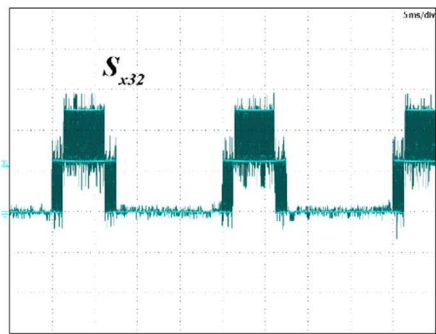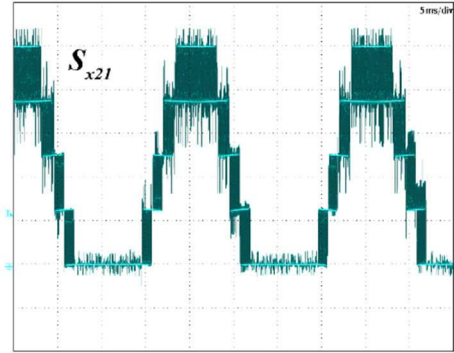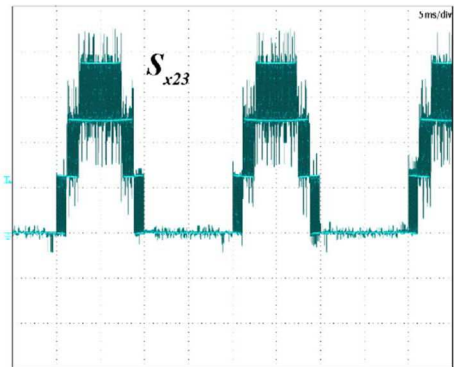
Fig. 26 *Steady-state blocking voltages of the switches in the S-1Φ7L E-type inverter*
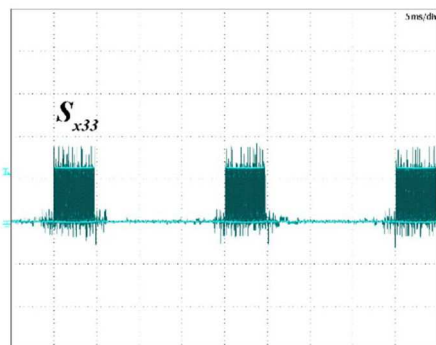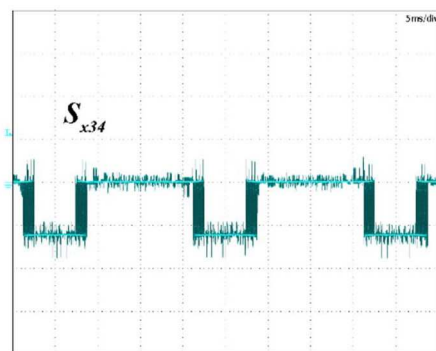*(a)* S_{x31}, *(b)* S_{x32}. 200 V/div, 5 ms/div

Fig. 27 *Steady-state blocking voltages of the switches*
(a) S_{x33}, *(b)* S_{x34}. 200 V/div, 5 ms/div

dashed line is the measured efficiency and the solid line is the calculated efficiency.

The peak efficiency for both measurements occurs close to the 6.5 kW. The measured efficiency is 98.83% at rated power and f_{sw} = 20 kHz. It is evident that the obtained experimental results do not match exactly with the analytical data; however, the theoretical curves are consistent with the experimental curves.
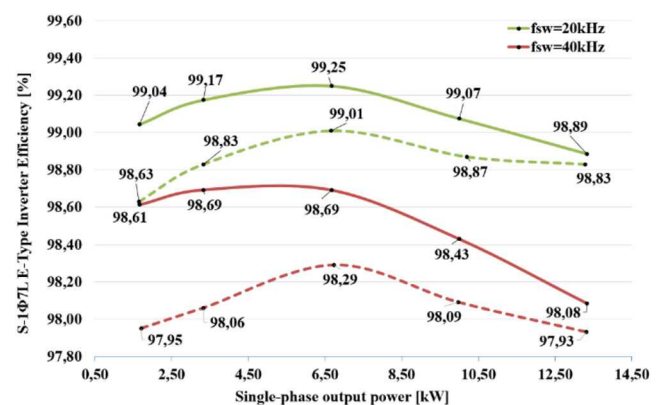

Fig. 28 *Steady-state blocking voltages of the switches*
(a) S_{x21}, *(b)* S_{x23}. 200 V/div, 5 ms/div

Fig. 29 *Total efficiency related to the single-phase 7L E-type inverter (including power semiconductors, DC-bus capacitor, and output filter) as a function of the output power at f_{sw} = 20 kHz (green line) and f_{sw} = 40 kHz (red line): experimental (dashed line) and analytical results (solid line)*

7 Conclusions

In this paper, the 3Φ7L E-type inverter has been analysed and designed to be used in PV applications. Thanks to the proposed topology it is possible to extend the DC-bus voltage range keeping low the power semiconductors voltage stress. The operating principle of the 3Φ7L E-type inverter has been explained and the analytical equations of the duty cycles, as well as the voltage and current stress for each power semiconductor located in the 3Φ7L E-type inverter have been obtained. The design procedure for the converter has been addressed. Particularly, the selection of the power devices and heatsink, as well as the DC-bus capacitor analysis, has been carried out in the paper. Afterwards, the efficiency and losses distribution as a function of the operating conditions have been estimated with respect to the 1200 and 650 V SiC-MOSFETs and diodes. The prototype of the single-phase 7L E-type inverter has been built and tested to demonstrate the operating principle of the converter. The experimental performance of the converter has been compared to the analytical results.
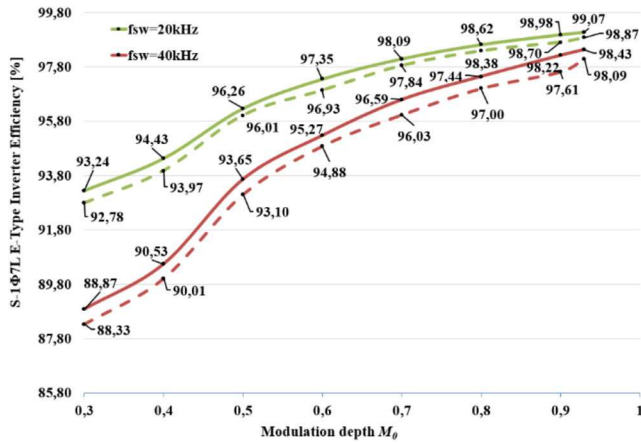
Fig. 30 *Total efficiency related to the single-phase 7L E-type inverter (including power semiconductors, DC-bus capacitor, and output filter) as a function of the modulation depth M_0 at f_{sw} = 20 kHz (green line) and f_{sw} = 40 kHz (red line): experimental (dashed line) and analytical results (solid line)*

According to the results, the newly conceived converter topology is capable of achieving a peak efficiency of 99%.

8 References

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9 Appendix

The average and RMS currents flowing through the power semiconductors are given in (17), where the coefficients a_i, b_i, c_i, and d_i are listed in Table 3

$$I_{\mathrm{AVG},i} = \frac{\sqrt{2}I_0 M_0}{4\pi}\left(a_i + \frac{b_i}{M_0}\right)$$

$$I_{\mathrm{RMS},i} = \sqrt{\frac{(\sqrt{2}I_0)^2 M_0}{2\pi}\left(c_i + \frac{d_i}{M_0}\right)} \tag{17}$$