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A Low-Power CMOS Bandgap Voltage Reference for Supply Voltages Down to 0.5 V

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Abstract: A voltage reference is strictly required for sensor interfaces that need to perform nonratiometric data acquisition. In this work, a voltage reference capable of working with supply voltages down to 0.5 V is presented. The voltage reference was based on a classic CMOS bandgap core, properly modified to be compatible with low-threshold or zero-threshold MOSFETs. The advantages of the proposed circuit are illustrated with theoretical analysis and supported by numerical simulations. The core was combined with a recently proposed switched capacitor, inverter-like integrator implementing offset cancellation and low-frequency noise reduction techniques. Experimental results performed on a prototype designed and fabricated using a commercial 0.18 µm CMOS process are presented. The prototype produces a reference voltage of 220 mV with a temperature sensitivity of 45 ppm/°C across a 10–50 °C temperature range. The proposed voltage reference can be used to source currents up to 100 µA with a quiescent current consumption of only 630 nA.

Keywords: voltage reference; CMOS bandgap; low-voltage; low-power; inverter-like

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1. Introduction

In the era of the Internet of Things (IoT), the development of nonintrusive wearable biomedical devices is stimulating research in many different fields, including that of integrated electronic circuits [1–4]. The need to monitor important vital parameters during the normal daily activities of humans has motivated the design of autonomous wearable devices capable of performing chemical–physical analysis of body fluids such as sweat, tears, and urine [5–7]. One of the main challenges posed by these devices is related to the availability of very low power budgets, typically provided by small batteries and/or energy harvesters. Among the latter, BioFuel Cells (BFCs) [8,9] and ThermoElectric Generators (TEGs) [10–12] have received considerable interest in the last few years for applications that include and go beyond wearable devices. TEGs and BFCs provide supply voltages that can drop well below 1 V depending on the environmental conditions, and depending on their size, their available power may be as small as a few hundred nanowatts [13]. Circuits designed to be directly powered by TEGs and BFCs must meet such extreme voltage and power constraints.

The same constraints apply also to the Voltage Reference (VR), which is a cell that must be present in integrated circuits to enable nonratiometric analog-to-digital signal conversion and sensor stimulation. The most popular VR is the bandgap circuit [14–16], where a Proportional-To-Absolute-Temperature (PTAT) voltage is added to a Complementary-To-Absolute-Temperature (CTAT) voltage in proportion to cancel the temperature coefficient of the resulting voltage. In the standard bandgap circuit, the CTAT component is the base-emitter voltage (V_{BE}) of a Bipolar Junction Transistor (BJT), while the PTAT term $\Delta V_{BE} = V_{BE1} - V_{BE2}$ is the difference of the V_{BE} of two BJTs with different current densities. Exploiting diodes and substrate BJTs, the bandgap voltage reference can be implemented using pure CMOS processes [17]. The value of the reference voltage produced by a standard bandgap (BG) circuit, around 1.2 V, makes it not suitable for ultralow-voltage applications.

The current-mode [18–20] and reverse [21,22] bandgap versions allow scaling down the reference voltage and then reducing the minimum supply voltage (V_{dd}). However, due to the necessity to forward-bias a p-n silicon junction, the minimum V_{dd} achievable with BJT-based voltage references cannot be reduced below around 0.7 V. Unfortunately, this value is still too high for circuits that have to be directly powered by BFCs and TEGs. The operation of BJT-based VRs can be extended to voltages well below 1 V using a charge pump to boost the V_{dd} just for the BJTs and their biasing circuits [23].

In order to reduce the minimum V_{dd} of voltage references, a popular strategy is replacing the BJTs with MOSFETs biased in the subthreshold region. A real advantage in terms of minimum V_{dd} can be obtained only by getting rid of all BJTs in a VR circuit. The first examples of CMOS-compatible VRs [24,25] used subthreshold-biased MOSFETs only to produce the PTAT component, while they still relied on a substrate BJT for the CTAT voltage. All-MOSFET VRs can be based on a large variety of principles. Several CMOS transpositions of BJT standard bandgap circuits have been proposed: in this case, the gate–source voltage (V_{GS}) replaces the V_{BE} in the CTAT term, while the ΔV_{BE} is replaced by a ΔV_{GS} in the PTAT source. In [26,27], different methods for summing a ΔV_{GS} and a V_{GS} term with arbitrary weights were proposed. More recently, all-MOSFET versions of the current mode bandgap have been proposed [28,29]. An alternative approach that turns out to be also effective against process variations consists of taking the difference of the threshold voltages of a depletion and an enhancement device [30]. The drawback of this kind of VR is that depletion MOSFETs are not available in most modern CMOS processes. Another popular approach is biasing a diode-connected MOSFET with a current that has a properly tailored temperature dependence such that the typical CTAT dependence of the threshold voltage is canceled [31]. MOSFET-based voltage dividers have been recently proposed in combination with extensive body bias to cancel the dependence of the output voltage from both V_{dd} and temperature [32,33].

In this work, we analyzed the suitability for ultralow supply voltage of the CMOS transposition of the popular BJT-based Kuijk bandgap core [15]. The main strength of this core is the low number of devices involved (two MOSFETs and three resistors), resulting in potential lower noise and design simplicity. To the best of our knowledge, this simple topology has received little attention in the literature in its BJT-free version. Using both analytical arguments and numerical simulations, we highlight the problems occurring when, pursuing low supply voltages, the original circuit is implemented using low-threshold MOSFETs. A slightly improved core that overcomes these issues is proposed, and its effectiveness is demonstrated by means of numerical calculations. The proposed topology maintains the simplicity of the design procedure that constitutes one of the attractive characteristics of Kuijk-like bandgap cores.

In order to give experimental support to the proposed core topology, we designed a prototype using a 0.18 µm CMOS process. The feedback connection required by this class of VRs is provided in the prototype by a recently introduced switched capacitor integrator, having an always-available output voltage and intrinsic offset and flicker noise cancellation [34]. This integrator was already used in the combination of a BJT bandgap core in a differential-output VR designed for the 1.4–3.3 V V_{dd} range [35]. In this work, we used an inverter-like version of the integrator, capable of working with V_{dd} down to 0.5 V [34]. It was already used in combination with an equivalent Kujik-like switched-capacitor core with a diode-connected MOSFET [36].

The results of the measurements performed on the prototype are described, demonstrating that a reference voltage with low sensitivity with respect to temperature and supply voltage can be obtained with the proposed approach.

2. LV Bandgap Voltage Reference

Figure 1a shows the Kujik BG BJT-based core [15], where $V_1 = V_2$ due to the virtual short-circuit at the amplifier input, resulting in the following ratio of $Q_1 - Q_2$ collector

currents: $I_{C2}/I_{C1} = R_1/R_2$. The reference voltage V_{ref}, in the case of $R_1 = R_2$ (i.e., $I_{C1} = I_{C2}$), is:

$$V_{ref} = V_{BE1} + \frac{R_1}{R_T}\Delta V_{BE} = V_{BE1} + \frac{R_1}{R_T}U_T ln(N), \quad (1)$$

where $U_T = kT/q$ is the equivalent thermal voltage (k is the Boltzmann constant, T the absolute temperature, and q the electron charge) and N is simply the ratio of the emitter areas of Q_2 and Q_1. A proper sizing of the resistive ratio R_1/R_T allows the temperature derivative compensation of V_{ref} at a target temperature, for instance room temperature ($T_0 = 27$ °C), obtaining the typical value of the reference voltage, close to 1.22 V, which practically sets the minimum supply voltage to around 1.4 V.

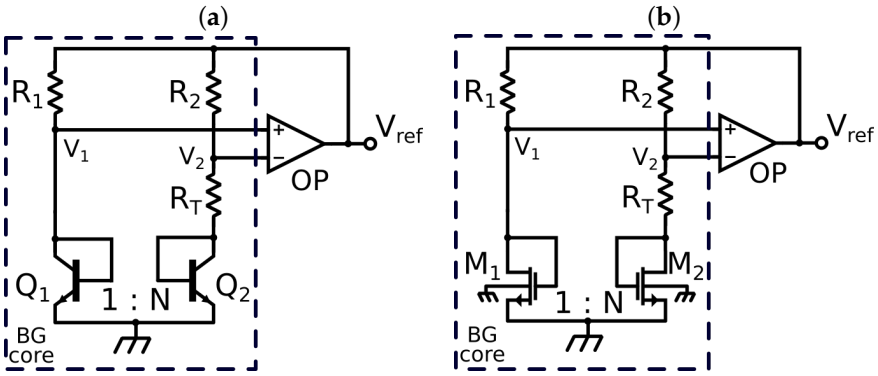

Figure 1. Schematic view of (**a**) the bandgap reference voltage proposed in [15] and (**b**) its all-MOSFET version.

2.1. MOSFET-Based Voltage Reference

In order to reduce the required supply voltage, the two BJTs in the Kujik BG core can be replaced with MOSFETs biased in weak inversion, obtaining the circuit in Figure 1b. The drain current of a MOSFET in weak inversion can be expressed as [37]:

$$I_D = I_S e^{\frac{V_{GS}-V_{th}}{nU_T}} e^{-\frac{V_{SB}(n-1)}{nU_T}} \left(1 - e^{-\frac{V_{DS}}{U_T}}\right) \quad (2)$$

where V_{th} is the threshold voltage, V_{DS} and V_{SB} are the drain–source and the source–body voltages, respectively, $I_S = 2n\mu C_{ox}U_T^2 W/L$ is the transistor-specific current [38], n is the slope factor, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, and W/L is the aspect ratio. By simple calculations, the reference voltage of the BG core in Figure 1b is:

$$V_{ref} = V_{GS1} + \frac{R_1}{R_T}\Delta V_{GS} = V_{GS1} + \frac{R_1}{R_T}nU_T ln(N), \quad (3)$$

where N is the ratio of the M_2 and M_1 aspect ratios, i.e., $N = (W_2/L_2)/(W_1/L_1)$. The PTAT term $\Delta V_{GS} = V_{GS1} - V_{GS2}$ is obtained by calculating V_{GS1} and V_{GS2} by means of Equation (2), where we supposed that both M_1 and M_2 work in the saturation region ($V_{DS} \gg U_T$).

We now briefly evaluate the temperature derivative of V_{GS1} around T_0, verifying its role in the CTAT term. Deriving the expression of V_{GS1} from Equation (2) and considering the expression of the M_1 drain current $I_{D1} = \Delta V_{GS}/R_T$:

$$\frac{\partial V_{GS1}}{\partial T} = G(T) = \alpha + n\frac{k}{q}\left[\frac{V_{od1}(T)}{nU_T} - (\alpha_R T + 1 + \gamma)\right], \quad (4)$$

where $\alpha = \partial V_{th}(T)/\partial T$ is the threshold voltage temperature derivative that we approximated as a temperature-independent term, $V_{od1} = (V_{GS1} - V_{th})$ is the overdrive voltage, α_R is the TCR of the resistors, and $\gamma < 0$ is the exponent of the temperature dependence of the electron mobility μ: $\mu(T) = \mu(T_0)(T/T_0)^\gamma$. The parameter α is negative and typically

represents the dominant contribution in Equation (4), making V_{GS1} the CTAT component, as anticipated.

Following the typical approach of nulling the temperature derivative of V_{ref} for $T = T_0$, we obtained the proper value of R_1/R_T that allows the first-order temperature compensation of the PTAT and the CTAT terms. Then, with simple calculations, the reference voltage at T_0 can be written as:

$$V_{ref}(T_0) = V_{GS1}(T_0) - G(T_0)T_0 = V_{th}(T_0) - \alpha T_0 + nU_T(T_0)(\alpha_R T_0 + 1 + \gamma). \quad (5)$$

It is worth mentioning that the reference voltage at $T = T_0$ does not depend on device bias, provided that $M_1 - M_2$ work in the weak inversion and saturation region. Assuming the parameter values from the device models of the technology used in this work (standard 0.18 µm CMOS process) and an overdrive voltage equal to 0 V, $G(T_0) \simeq -0.6$ mV/K and $V_{ref}(T_0) \simeq V_{th}(T_0) + 0.18$ V. With typical threshold voltages around 0.4 V, we obtained a reference voltage around 0.6 V. Considering that the margin of the Operational Amplifier (OP) output voltage to V_{dd} is, in the best case, equal to a saturation voltage V_{DSAT}, a minimum supply voltage of around 0.7 V can be estimated.

In order to scale down the reference voltage, it is possible to choose Low-Threshold-Voltage (LVT) or Zero-Threshold-Voltage (ZVT) devices, which are available in many current CMOS processes. However, we must guarantee the saturation region for $M_1 - M_2$, which are diode-connected and have $V_{DS} = V_{GS}$. In weak inversion, the saturation voltage V_{DSAT} is around $4U_T$. Regular MOSFET devices typically show $V_{th} \gg U_T$, and then, the saturation condition is ensured even when overdrive voltages are close to zero or negative. On the other hand, the threshold voltage of LVT devices can be on the order of the saturation voltage, so that $M_1 - M_2$ are biased at the boundary of the triode region and the effects of V_{DS1} and V_{DS2} cannot be neglected any more. Consequently, ΔV_{GS} could be no longer PTAT in the whole temperature range of interest. When V_{DS} cannot be neglected in Equation (2), an analytical solution cannot be found.

For this reason, we developed a numerical simulator, written using the Scipy scientific modules of the Python language, to solve the network of the BG core depicted in Figure 1b and to find ΔV_{GS} and V_{ref} in a temperature range from 0 °C to 80 °C. The drain currents of $M_1 - M_2$ were modeled according to Equation (2), tuned with the electrical parameters of a commercial 0.18 µm CMOS process. In order to highlight the role played by V_{DS}, we compared the results of simulations performed with and without the V_{DS}-dependent term of Equation (2). In the rest of the paper, we refer to the solution obtained neglecting the V_{DS} as the ideal case. OP was considered ideal with an infinite gain, thus ensuring the virtual short-circuit $V_1 = V_2$. R_T was sized to fix the MOSFET drain currents (here, around 200 nA), while $R_1 = R_2 = R$ was sized to obtain the first-order temperature compensation of the PTAT and the CTAT terms at $T = T_0 = 27$ °C in the ideal case. (W_1/L_1) and (W_2/L_2) were chosen as large as possible to guarantee the weak inversion biasing of both M_1 and M_2. The N factor is typically in the range from 2 (minimum area occupation) to 8 (compact common-centroid layouts). We adopted an intermediate value $N = 5$, but the following results did not vary significantly with this parameter, once R and R_T were properly resized accordingly. Finally, three different values of $V_{th}(T_0)$ were considered in the simulations: 0.11, 0.2, 0.3 V.

Figure 2a shows the temperature behavior of ΔV_{GS} for different $V_{th}(T_0)$ (simply expressed as V_{th} in the plot legends). The dashed curves represent the ideal ΔV_{GS}: notice that the curves are practically coincident, showing that there is no influence from the threshold voltage, in agreement with Equation (3). On the other hand, the ΔV_{GS} curves obtained by taking into account also the V_{DS} effect strongly depend on V_{th}. For $V_{th} = 0.3$ V, the effect of V_{DS} is almost negligible, as shown also in the inset of Figure 2a. For a lower value of V_{th} (0.2 V), ΔV_{GS} differs from the ideal curve especially for large temperatures, while for even lower values of V_{th} (e.g., 0.11 V), the temperature behavior of ΔV_{GS} is not PTAT any more in the whole temperature range. It was not possible to repeat the simulations for $V_{th} < 0.11$ V (corresponding to typical LVT or ZVT devices), because V_{GS2}

(and consequently V_{DS2}) became negative for a certain range of temperatures and the numerical solver failed to find the correct solution of the equation set. Figure 2b shows the temperature behavior of V_{ref} for the same V_{th} values as in Figure 2a. Failure in obtaining a correct PTAT voltage for low V_{th} is clearly reflected in the temperature stability of V_{ref}. A significant deviation from the ideal case can be observed for $V_{th} = 0.2$ V, while for $V_{th} = 0.11$ V, the effect of V_{DS} completely disrupts the temperature stabilization mechanism. For $V_{th} = 0.3$ V, instead, the temperature behavior is practically the same as in the ideal case; however, it is worth noting that the value of the obtained reference voltage is close to 0.5 V. Considering the minimum overhead required by the amplifier, this results in a reasonable minimum V_{dd} value of about 0.6 V. In the next section, we present a new BG topology where the use of LVT or ZVT devices did not incur the above-mentioned issue, thus allowing further scaling of the minimum supply voltage.

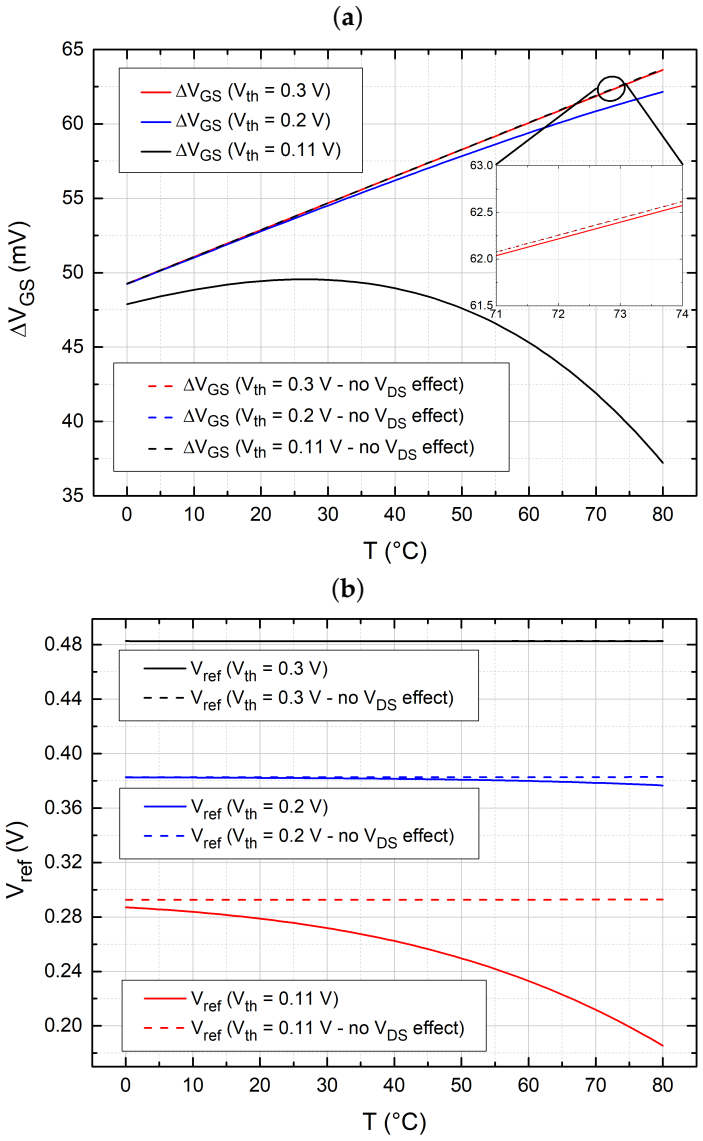

Figure 2. Temperature behavior of ΔV_{GS} (**a**) and V_{ref} (**b**) in the BG core of Figure 1b, for different values of V_{th}, considering or neglecting the V_{DS} effect on the drain current.

2.2. Proposed BG Core

Figure 3a shows the proposed BG core, where the diode connections of $M_1 - M_2$ were removed and the drain terminals were connected to the supply voltage, while the resistive network made by R_1, R_2, and R_T was shifted to the source side. In this way, V_{DS} can be

larger than V_{GS} and does not suffer from the small values assumed by the latter in LVT and ZVT devices. It is straightforward to verify that the working principle of the proposed core is identical to that of Figure 1b, with the only difference that V_{SB} of $M_1 - M_2$ is not zero. Thus, the reference voltage is then:

$$V_{ref} = V_{GS1} + \frac{R_1}{R_T}\Delta V_{GS} = V_{GS1} + \frac{R_1}{R_T}U_T ln(N), \quad (6)$$

which differs from Equation (3) only for the absence of the factor n in the PTAT term. In a triple-well process (or p-well), a source–body connection would be allowed, making the V_{ref} of the circuits in Figures 1b and 3a perfectly equivalent. This condition is clearly not essential, since the sum of a PTAT and a CTAT term is present in the expression of V_{ref} given in Equation (6). More interestingly, it is possible to demonstrate that, imposing an R_1/R_T ratio that nulls the V_{ref} temperature derivative at $T = T_0$, the expression of the reference voltage of the proposed BG core at $T = T_0$ is the same as Equation (5) regardless of the presence of a body–source connection. Thus, $V_{ref}(T_0) \simeq V_{th}(T_0) + 0.18$ V, as in the case of the standard core of Figure 1b. With the proposed core, the $V_{ref}(T_0)$ value can be lowered by means of employing LVT or ZVT devices, without incurring the problems that affect the standard core. The limiting condition on the minimum supply voltage is given by M_2 entering the triode region. The minimum V_{dd} value is determined by the following condition:

$$V_{DS2} = V_{dd} - V_{S2} > V_{DSAT} \quad (7)$$

Expanding the term V_{S2} by simple calculations based on the analysis performed above, the minimum V_{dd} at $T = T_0$ can be written as:

$$V_{dd-min} = |G(T_0)T_0| + U_{T0} ln(N) + V_{DSAT} \simeq 0.32\,\text{V} \quad (8)$$

In order to verify the correct behavior of the proposed core and find a more accurate value of V_{dd-min}, we performed numerical simulations also on the proposed BG core. The physical and geometrical parameters used in the simulation program were the same as the ones used for the standard core, except for R_T, which was slightly different to compensate the different slope of the PTAT term.

Figure 4a shows the temperature behavior of ΔV_{GS} and V_{ref} in the case of M_1 and M_2 with $V_{th} = 0.11$ V and $V_{dd} = 0.5$ V. As in the case of the standard core, simulations were performed with and without the V_{DS}-dependent term in Equation (2). Differently from Figure 2a, ΔV_{GS} is minimally affected by the V_{DS} effect, maintaining an excellent linear dependence from the temperature. Furthermore, also the temperature behavior of V_{ref} is very close to the ideal one. In Figure 4b, we performed the same simulations, but considering $V_{th} = 50$ mV, which is close to the actual value of the threshold voltage of an LVT device in the adopted technology. The temperature behavior for both ΔV_{GS} and V_{ref} is still quite close to the ideal case, but the absolute value of V_{ref} is obviously lower.

Figure 5 shows the variations of $V_{ref}(T_0)$ and the temperature coefficient (TC) as a function of the supply voltage. The temperature coefficient is defined as: $(V_{ref,max} - V_{ref,min})/(V_{ref}(T_0)\Delta T)$, where $V_{ref,max}$ and $V_{ref,min}$ are the maximum and the minimum values of V_{ref} over the investigated temperature interval and $\Delta T = 80$ °C is the total temperature excursion. In the case of neglecting the V_{DS} effect (dashed curves), no dependence on the supply voltage is present. Actually, appreciable variations of V_{ref} and TC are present only for values of V_{dd} lower than 0.4 V. This value is larger than the estimate given in Equation (8). This discrepancy derives from considering an abrupt transition between saturation and triode region. In practice, the V_{DS} effects start being non-negligible for V_{DS} values higher than the V_{DSAT} value (100 mV) used in Equation (8).

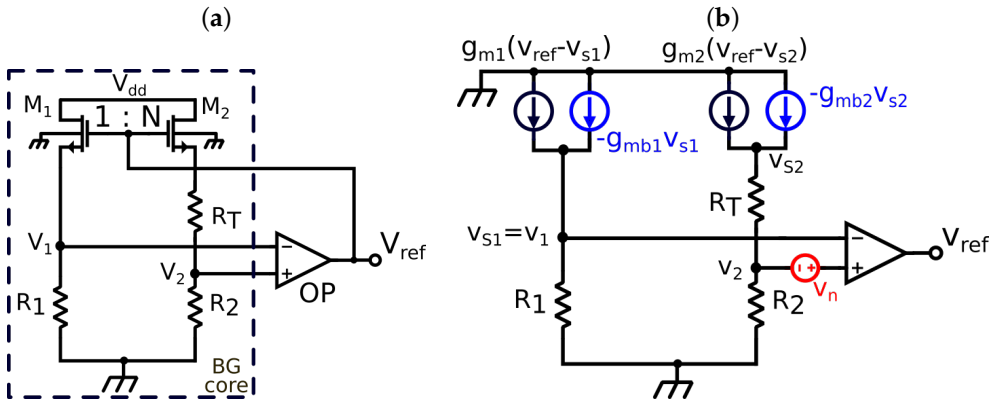

Figure 3. Schematic view of (**a**) the proposed bandgap reference voltage and (**b**) its equivalent small signal circuit.

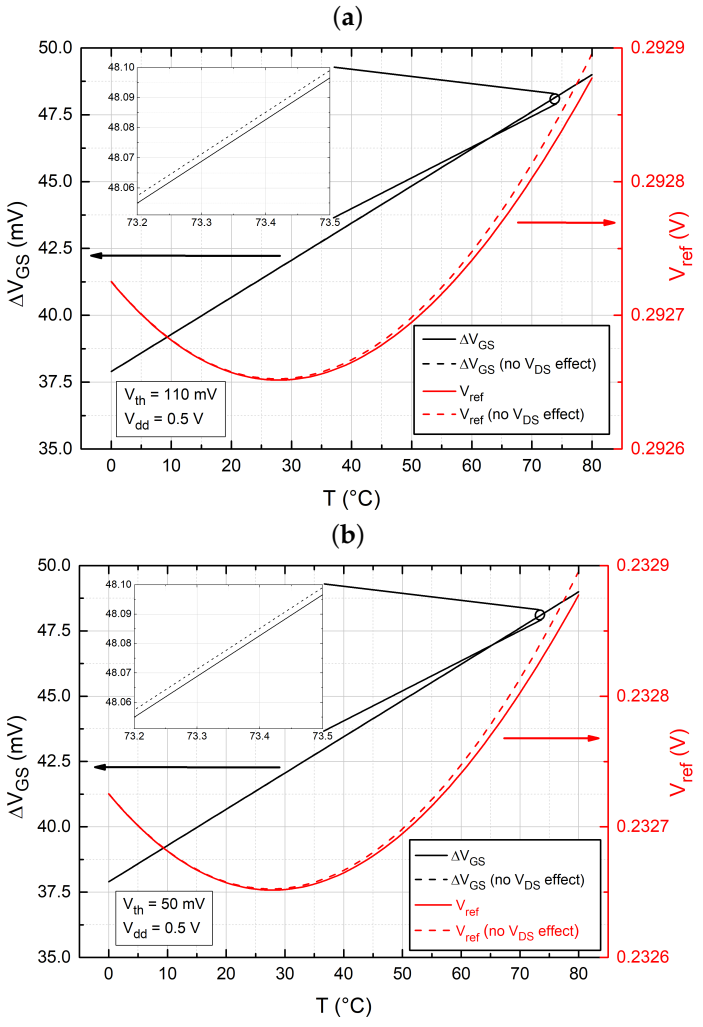

Figure 4. Temperature behavior of V_{ref} and ΔV_{GS} in the BG core of Figure 3a, for $V_{dd} = 0.5$ V, considering or neglecting the V_{DS} effect on the drain current, for $V_{th} = 110$ mV (**a**) and $V_{th} = 50$ mV (**b**).

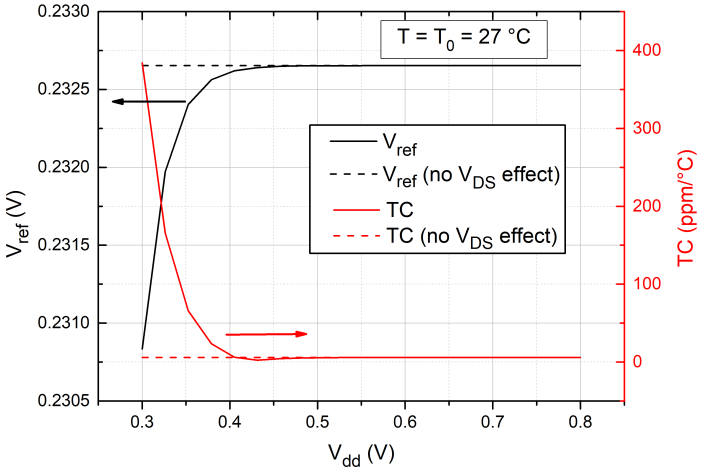

Figure 5. Supply voltage dependence of V_{ref} (at $T = T_0$) and the Temperature Coefficient (TC), considering or neglecting the V_{DS} effect on the drain current.

2.3. Offset and Noise Contribution of the Amplifier

Bandgap topologies that employ an operational amplifier to ensure equal currents in the two branches of the core necessarily suffer from the effect of offset and noise introduced by the op amp [35]. The Referred-To-Input (RTI) error voltage of OP, indicated in Figure 3b as v_n, gives a contribution to the reference voltage equal to v_{n-out}:

$$v_{n-out} \simeq \frac{v_n}{\beta}, \tag{9}$$

where β is a small signal transfer function defined as follows:

$$\beta = \frac{v_1 - v_2}{v_{ref}}. \tag{10}$$

From the equivalent small signal circuit of the proposed BG core depicted in Figure 3b, considering that $n = 1 + g_{mb}/g_m$, it is straightforward to evaluate β:

$$\beta = \frac{g_{m1}R_1 - g_{m_2}R_2 + g_{m1}g_{m2}R_1R_Tn}{(1 + g_{m1}nR_1)(1 + g_{m2}n(R_2 + R_T))} \tag{11}$$

Because of the design choice $R_1 = R_2$ and consequently $I_{D1} = I_{D2}$, the transconductance of $M_1 - M_2$ biased in weak inversion is equal to $g_{m1} = g_{m2} = ln(N)/(nR_T)$. By nulling the temperature derivative of V_{ref} expressed in Equation (6) around T_0, we derive $R_1 = -G(T_0)R_Tq/(ln(N)k)$. Finally, we can express β as:

$$\beta = \frac{-\frac{G(T_0)q}{kn}}{1 - \frac{G(T_0)q}{k}} \frac{ln(N)}{1 - \frac{G(T_0)q}{k} + ln(N)}. \tag{12}$$

Considering a typical range of N from 2 to 8, β varies from 0.05 to 0.15. As a result, according to Equation (9), v_{n-out} can be from 7- to 20-times v_n. For this reason, the input voltage noise and offset of the amplifier can significantly degrade the reference voltage accuracy. As shown in the next section, the proposed core was combined with an amplifier performing Correlated Double Sampling (CDS) to reduce its offset and low-frequency noise.

3. Prototype Design

The proposed LV-VR, shown in Figure 6, was implemented using a 0.18 µm CMOS process from UMC. The LV-BG core was the same as just described in the previous section where transistors $M_1 - M_2$ are LVT devices, having threshold voltages (V_{th0}) lower than 100 mV. The amplifier OP was replaced by a Discrete Time (DT) Switched Capacitor (SC)

integrator (DTI), enclosed inside the blue dotted polygon in Figure 6. The integrator was presented for the first time in [34] and was selected for the proposed LV-VR since it offers the following unique combination of properties: (i) it operates CDS, reducing the input-referred offset voltage and low frequency noise; (ii) its output voltage is valid across the whole clock cycle, making it equivalent to a continuous-time integrator; (iii) it ideally does not draw current from the inputs as soon as the virtual short-circuit is established; (iv) it provides a high DC gain. The integrator is formed by two stages, built around amplifiers A_1 and A_2. In turn, A_1 and A_2 are based on gain stages (I_1 and I_2), consisting of standard CMOS inverters. In A_2, the inverter is followed by a source-follower stage (devices $M_3 - M_4$), introduced to allow driving resistive loads with reduced gain loss. In order to maintain an acceptable output range, a ZVT device (native n-MOSFET) was used for M_3. The circuit operates with a two-phase clock. Switches are labeled with numbers that indicate the clock phase where they are closed (on state). The detailed operating principle of the SC integrator was analyzed in [34]. Briefly, in the transition between Phase 2 to Phase 1, a charge proportional to the input differential voltage ($V_d = V_2 - V_1$) is injected from capacitor C_S into capacitor C_T. In the transition between Phase 1 and the following Phase 2, this charge is transferred to C_F, which produces a voltage increment equal to $\Delta V_{out} = V_d C_S / C_F$, proving that the circuit operates as a DT integrator. It can be easily verified that the voltages at the input of A_1 and A_2 contribute to all charge transfers only in the form of the differences of samples taken at different instants of the clock cycle. This proves that CDS is actually applied to A_1 and A_2 input offset and low-frequency noise voltages. Capacitor C_H is used to maintain negative feedback in Phase 2, when C_T is transferring charge to C_F. The use of C_H instead of a direct input–output connection reduces the output swing of the A_1 output voltage across phase transitions, increasing the equivalent DC gain of the integrator. For this mechanism to be effective, in Phase 1, C_H must be connected to a voltage as close as possible to the closed-loop A_1 input voltage. This voltage, indicated with V_{inv}, is produced by inverter I_3 closed in unity gain configuration. The DC gain of the integrator can be shown to be in the order of $A_1^2 A_2$. As a result, even with the typically small gains of inverter-like amplifiers (order of tens, at ultralow supply voltages), DC gains of several thousands are guaranteed using the adopted two-stage integrator.

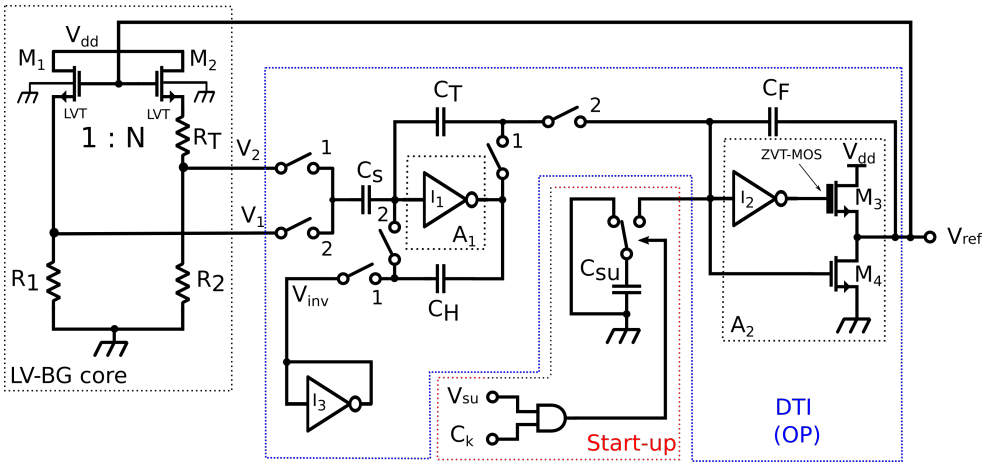

Figure 6. Schematic view of the proposed LV-VR.

3.1. Start-Up Circuit

As in traditional bandgap-like structures, the proposed circuit suffers from the presence of an unwanted all-zero stable solution. To prevent the circuit from being trapped, a start-up architecture is mandatory. The start-up circuit adopted in this work is shown in the red dashed box in Figure 6: C_k is the clock signal, while V_{su} is the output voltage of the low-voltage comparator shown in Figure 7. The comparator is composed by a cascade of three inverters: the first one, M_5 and M_6, sets the threshold voltage, and the other two inverters make the transition sharper. The threshold voltage is reached when the input

voltage of the comparator (i.e., V_{ref}) is such that the current in M_6 equals the constant current provided by M_5. By proper sizing of M_5 and M_6, the threshold voltage was set to a value slightly lower than the steady-state value of V_{ref}, even considering the spread due to the process variations. When voltage V_{ref} is lower than the comparator threshold voltage, the charge pump formed by capacitor C_{SU} pumps charges into C_F, allowing V_{ref} to increase to a voltage large enough to enable the circuit to start its autonomous evolution towards the correct steady-state solution. Since the steady-state value of V_{ref} is larger than the comparator threshold voltage, the start-up circuit is normally powered off.

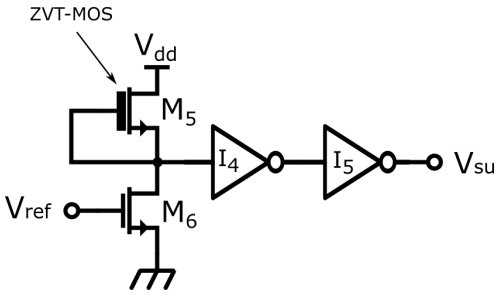

Figure 7. Schematic view of the auxiliary LV-comparator.

3.2. Device Sizing

As shown in Figure 6, the proposed prototype is formed by two main blocks, namely the bandgap core and the amplifier (SC integrator). The procedure used to design the core is very simple, and this is a clear advantage of Kujik-like solutions. M_1 and M_2 are LVT devices, characterized by a threshold voltage around 50 mV. The value of N, which is not critical, sets the voltage across resistor R_T (PTAT voltage). In turn, R_T sets the bias current through M_1 and M_2, i.e., the power consumption of the core. Once the magnitude of the current is established, M_1's aspect ratio must be chosen large enough to keep the MOSFET in weak inversion. This step sets M_1's overdrive voltage, which is not critical, since it does not affect the value of V_{ref}, according to Equation (5). Finally, the R/R_T ratio is set to the value that nulls the derivative of V_{ref} with respect to temperature. This last step can be simply accomplished by means of a single parametric sweep, performed using the electrical simulator. We chose a value of N equal to 5, which was obtained by connecting five M_1 replicas in parallel to form M_2. In practice, this corresponded to setting the multiplicity factor (m) of M_2 to 5. The value of R_T was chosen to set the core current consumption to a few hundred nA. Clearly, larger resistance values can be adopted to reduce the current consumption, at the cost of a larger area occupation. As far as the SC integrator is concerned, transistors M_3 and M_4 are ZVT MOSFETs, and the remaining transistors are Regular Threshold Voltage (RVT) devices. Complementary transmission gates employing regular threshold devices were used for all switches.

Tables 1 and 2 summarize the sizes of the active and passive components, respectively. As far as passive components are concerned, resistors R_1, R_2, and R_T are high-resistivity polysilicon resistors, and all capacitors are metal–insulator–metal devices.

Table 1. Sizing of LV-VR transistors.

Device	Type	W (μm)	L (μm)	m
M_1	LVT	3	3	1
M_2	LVT	3	3	5
M_3	ZVT	3.5	0.35	4
M_4	RVT	1.8	0.18	2
M_5	ZVT	0.5	0.5	1
M_6	RVT	3	3	10
M_{I1n}	RVT	2	2	1
M_{I1p}	RVT	2	2	4
M_{I2n}	RVT	2	2	1
M_{I2p}	RVT	2	2	4
M_{I3n}	RVT	2	2	1
M_{I3p}	RVT	2	2	4
M_{I4n}	RVT	0.28	0.18	1
M_{I4p}	RVT	0.28	0.18	4
M_{I5n}	RVT	0.28	0.18	1
M_{I5p}	RVT	0.28	0.18	4

Table 2. Sizing of LV-VR passive components.

Device	Value	Device	Value
R_1	616 kΩ	C_T	1 pF
R_2	616 kΩ	C_F	1 pF
R_T	154 kΩ	C_H	1 pF
C_S	1 pF	C_{SU}	200 fF

4. Results

The proposed LV-VR was designed with the Cadence Virtuoso Platform for Custom IC design, electrically verified by means of the Spectre simulator and fabricated with the UMC 0.18 μm CMOS process. An optical micrograph of the proposed voltage reference is shown in Figure 8, where the layout is superimposed on the picture. The total area consumption was close to 0.015 mm^2. All tests were performed with V_{dd} = 0.5 V, T = 27 °C, and f_{clk} = 100 kHz, unless otherwise specified.

The dependence of V_{ref} on the supply voltage V_{dd} was measured over a set of ten chips. Figure 9 shows the highest (dots) and the lowest (triangle) V_{ref} vs. V_{dd} characteristics. The spread between the two curves is 71.5 mV. Since the main contribution of the reference voltage is represented by the threshold voltage, it can be argued that this uncertainty is mainly due to the V_{th} spread. Corner process simulations confirmed that the variation of the M_1 and M_2 threshold voltages was actually close to the reference voltage spread. The circuit started working properly with V_{dd} = 0.5 V and in the supply voltage range from 0.5 V to 1.3 V the V_{ref} variation was close to 2 mV for both characteristics. Note that the lower V_{dd} limit was higher than the 0.4 V prediction derived from the numerical simulations of Figure 5. This could be due to additional constraints on V_{dd} imposed by the SC integrator.

The V_{ref} temperature dependence is shown in Figure 10 for a sample that exhibits an intermediate V_{ref} value with respect to the extremes shown in Figure 9. Measurements were performed using a Peltier-cell cryostat sweeping the temperature in the range 10 °C to 80 °C. A maximum variation of 6.7 mV can be observed in the whole temperature range. If we focus on the temperature range generally considered for wearable applications [39] (i.e., from 10 °C up to 50 °C), the variation was close to 1 mV, with an average TC of 45 ppm/°C.

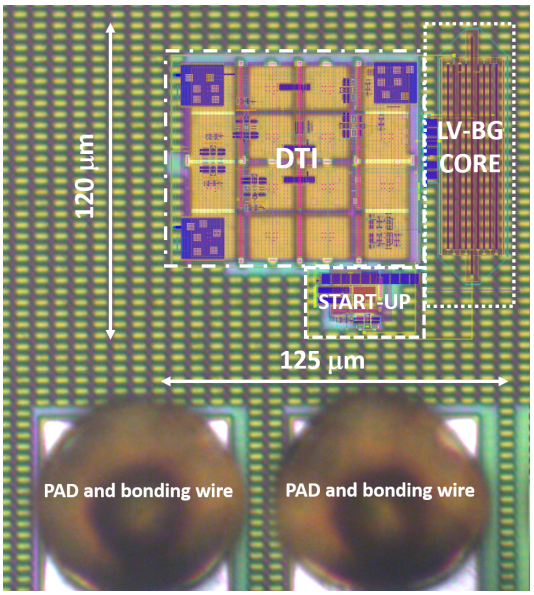

Figure 8. Micrograph of the proposed voltage reference with the layout aligned and superimposed in order to show the devices and interconnections that would be otherwise hidden below the planarization dummies. The dimensions and the main blocks are indicated.

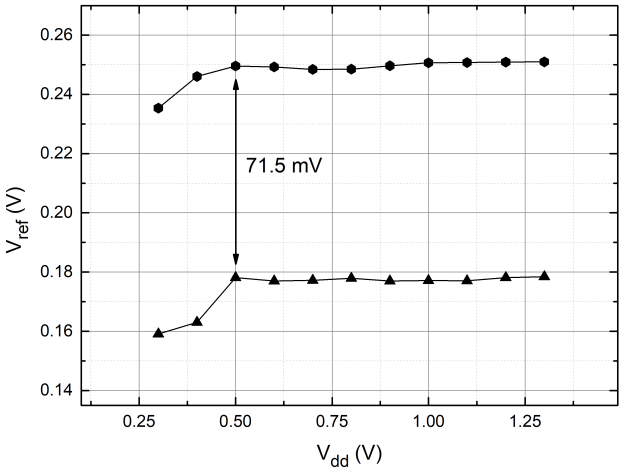

Figure 9. Measured output voltage, V_{ref}, as a function of the power supply at room temperature.

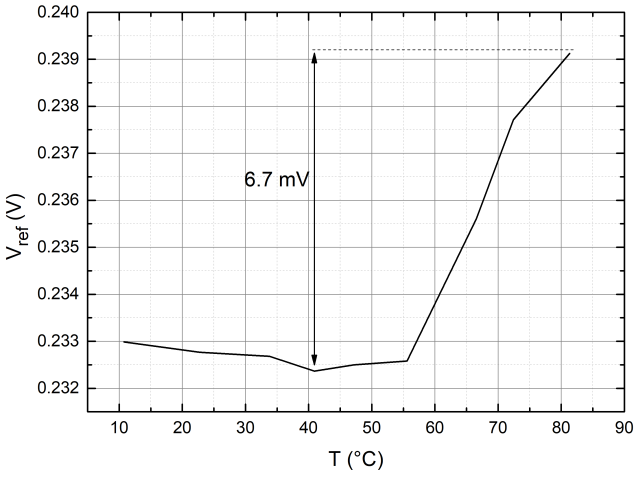

Figure 10. Measured temperature dependence of the output voltage in the range 10 °C to 80 °C .

In Figure 11, the output reference voltage is plotted as a function of the output current. It is possible to observe that V_{ref} undergoes very small variations for sourced current up to 104 µA. The bias current of the proposed bandgap was around 630 nA, and thus, the maximum sourced current was 165-times larger than the bias one.

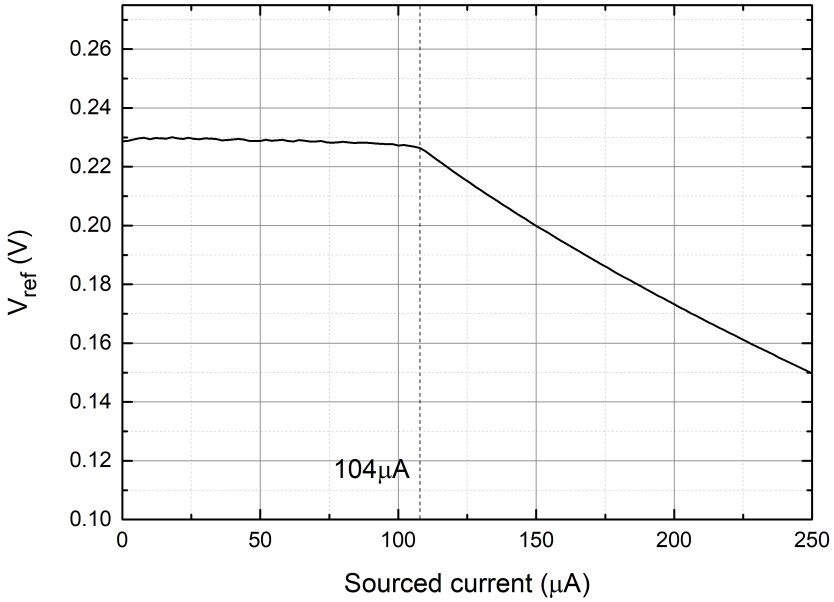

Figure 11. Measured output reference voltage vs. sourced output current.

Finally, the unfiltered output noise density is depicted in Figure 12. The noise density decrease for frequencies higher than 2 kHz was due to the intrinsic DT transfer function of the feedback loop [35]. A typical flicker noise component can be observed at low frequencies. This can be ascribed to contributions from $M_1 - M_2$, which differently from the input noise of the amplifier, are not subjected to correlated-double sampling. The root-mean-squared voltage noise in the bandwidth from 0.2 Hz to 10 kHz was around 330 µV.

The performance of the VR prototype described in this paper is summarized in Table 3, where the data extracted by recent works on Sub-1 V references are also reported. The proposed solution is lines up with most of the state-of-the-art designs included in the comparison. A point of weakness is represented by the power consumption, which could be simply overcome by scaling up the values of all resistors by the same factor, obviously at the cost of increased area occupation. Furthermore, it should be noted that, differently from the proposed circuit, all the VRs reported in Table 3 have no capability of sourcing significant output currents, with the exception of Reference [22]. The impressively low supply voltage reported in [33] was obtained by applying active body biasing to n-MOSFETs, which is not compatible with inexpensive n-well CMOS processes. The other work in the table that exhibits a supply voltage below 0.3 V [29] actually used a charge pump to double the value of V_{dd}, providing the headroom required to bias a current mode bandgap core.

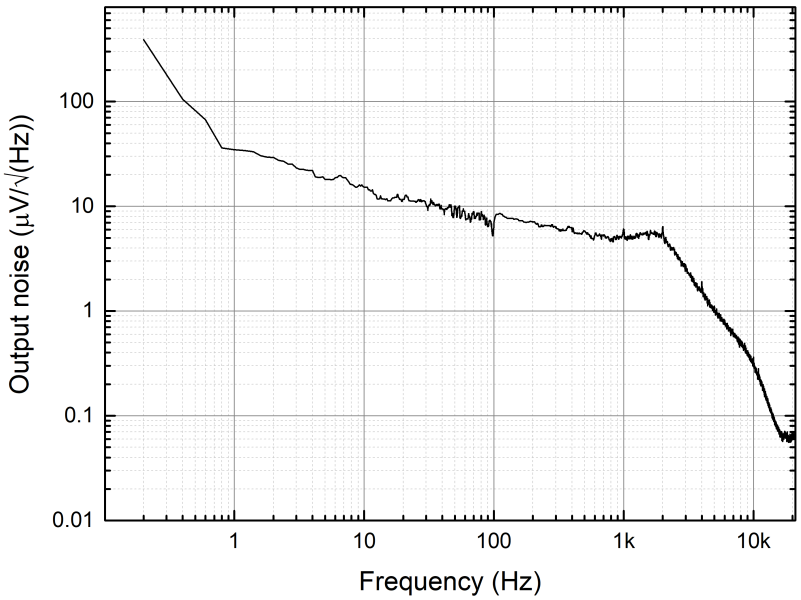

Figure 12. Output noise spectral density. Noise density in the flat region is indicated.

Table 3. Performance summary and comparison of state-of-the-art LV VRs.

	This Work	[22]	[40]	[23]	[41]	[29]	[33]	[27]
Technology (nm)	180	130	180	65	180	110	180	180
Power (nW)	315	170	2.6	38	14	5.35×10^3	5.4×10^{-3}	19
V_{dd-min} (V)	0.5	0.75	0.45	0.5	0.45	0.242	0.25	0.7
V_{ref} (V)	0.233	0.256	263.5	0.495	0.118	0.195	0.091	0.438
PSRR (dB)	−44@100 Hz	N.A	−40@30 Hz	−50@DC	−40@100 Hz	N.A.	−70@100 Hz	N.A.
Temperature range (°C)	10–50	−20–85	0–125	−40–120	−40–125	N.A.	0–120	−25–85
TC (ppm/°C)	45	40	165	42	63.6	134	265	22.1
Trimmed	NO	YES	NO	YES	YES	YES	NO	YES
LR (mV/V)	1.44	0.013	1.16	3.2	1.2	8	0.145	0.571
Area (mm^2)	0.015	0.055	0.043	0.0522	0.012	0.013	0.0022	0.041

5. Conclusions

It was shown that direct replacement of the BJTs with low-threshold MOSFETs in the popular Kuijk bandgap core [15] is not a viable solution to obtain VRs compatible with ultralow supply voltages. The weakness was found to be the diode connection of the MOSFETs, which results in an insufficient V_{DS} when the devices are biased in the deep subthreshold region. The main effect is a failure in the PTAT voltage/current generation, which occurs independently of the V_{dd} value. It is worth noting that the observed problem should affect in the same way different architectures where a mesh of diode-connected MOSFETs is used to obtain a PTAT current [28,29]. The proposed improvement was demonstrated to be suitable for the design of Kuijk-like cores with very low-threshold-voltage MOSFETs. The principle, which was illustrated with analytical arguments, was also supported by experimental results obtained from the proposed prototype, designed using a standard CMOS n-well technology. Another merit of the prototype was the use of a recently introduced SC integrator, which, differently from other alternative designs operating CDS for offset and noise reduction, produced a really time-continuous output, which was valid across the whole clock cycle. Thanks to the inverter-like implementation of the integrator, the correct operation of the prototype was enabled down to 0.5 V. Note that the described prototype represents only one of the possible implementations of voltage references based on the proposed core. Different solutions where the resistor values are

increased to reduce power consumption or alternative amplifier topologies are employed can be envisioned.

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