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A Three Phase Photovoltaic Power System Connected to the MV Network: Behaviour during Voltage Dips

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Abstract The presence of Distributed Generation (DG) in the distribution network is increasing and represents one of the most important research areas. Several reasons have forced this increase like the possibility to use renewable resources reducing the fossil fuels use with environmental and energy benefits.

The paper deals with the results of a study performed by RSE, in the frame of the Research Fund for the Italian Electrical System, focused on the behaviour during voltage dips of a "DG system", consisting in a Photovoltaic generator (PV) connected to the network with three phase Voltage Source Inverter (VSI).

Key words

Distributed Generation (DG), Photovoltaic power system (PV), Voltage Source Inverters (VSI), Fault Ride Through (FRT), Voltage Dips.

1. Introduction

Several reasons have forced the Distributed Generation (DG) presence increase in the distribution network, among them the possibility to use renewable resources reducing the fossil fuels use with environmental and energy benefits has a particular importance. Moreover this issue represents one of the most important research areas.

Among renewable resources Photovoltaic arrays are one of the DG sources that have shown a continuous growing trend in the last few years. Distributed Generation is typically connected to the AC distribution network using power electronic devices like Voltage Source Inverters (VSI).

With this increase of DG and the consequent evolution of the distribution network from a passive to an active system new issues, relevant to the Distributed Generation impact in the network, have to be considered during steady state and transient conditions.

In this contest, the paper deals with the results of a study performed by RSE, in the frame of the Research Fund for the Italian Electrical System, focused on a "DG system", with a Photovoltaic generator (PV) interfaced to the network with three phase VSI.

The main issue of the study is to investigate possible control methodologies for interconnecting PV arrays to the distribution power system, taking into account also the new proposals for the Fault Ride Through (FRT) during the voltage dips occurrence.

2. Three Phase MV Network Connected to a Photovoltaic Power System

The study has been focused on the Medium Voltage (MV) network and performed with digital simulations in ATPdraw (Alternative Transient Program) with the main goals of analyzing and understanding:

- the PV plant design;
- the behaviour of the system during voltage dips in the MV network;
- the possible control methodologies for the Fault Ride Through capability [1] ÷ [3].

The structure of the simulated system consists of (Fig. 1):

- a PV array;
- a DC/DC BOOST converter to extract the Maximum Power Point Tracking (MPPT) from the PV array and to increase the output voltage to a level suitable for the inverter;
- a two level three phase VSI to connect the DG to the MV network through a MV/LV transformer.

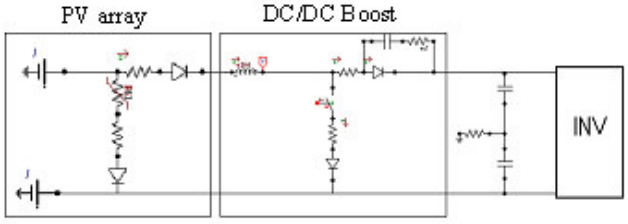

Fig. 1: Simulated system: simplified structure

A MV bus-bar with its feeders and HV/MV transformer has been implemented in the digital model together with an equivalent for the HV network.

A. *Photovoltaic equivalent model*

A PV array consists of solar cells, each generating a certain voltage and current; by connecting these cells in series and in shunt, the required current and voltage can be generated.

The photovoltaic equivalent system has been represented by the following equivalent model shown in Fig. 2.

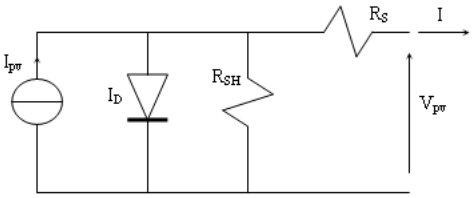

Fig. 2: PV cell circuit model

The simple electric equivalent model of a solar cell is made by a photovoltaic current source I_{pv}, a diode, a shunt resistor (R_{sh}), that takes into account the current to earth under normal operation conditions, and a series resistor (R_s), that represents the internal resistance to the flow of generated current and depends on the thick of the junction P-N, on the present impurities and on the contact resistances.

The current-voltage (I-V) characteristic is given by:

$$I = I_{pv} - I_D - \frac{V_{PV} + I R_s}{R_{sh}}$$
$$I_D = I_0 \left[\exp \frac{q\left(V_{PV} + I R_s\right)}{AkT} - 1 \right] \quad (1)$$

where in Fig. 2 and in the equation (1):

- I is the current injected by the PV system;
- I_{pv} represent the current generated by the cell that is a constant for a given temperature (T) and Solar irradiation (G);
- I_D the current flowing through the diode that depend from its reverse saturation current I_0;
- A is the identity factor of the diode and depends on the recombination factors inside the diode itself (for crystalline silicon is about 2);
- q is the electron charge (1.60217646E-19 C);
- k is the Boltzmann constant (1.3806503E-23 J/K);
- T is the absolute temperature in K degree.

In the usual cells, the leakage current to earth, flowing through R_{sh}, is negligible with respect to the other two currents. As a consequence, the saturation current of the diode can be experimentally determined by applying the no-load voltage V_{oc} to a not-illuminated cell and measuring the current flowing inside the cell.

In this study the output I(V) and P(V) characteristics has been calculated for the following PV system features:

P_{MPPT}	580 kW
V_{MPPT}	610 V
I_{MPPT}	950 A
T	25°C
G	1000 W/m^2

In particular in Fig. 3 it's possible to evaluate that under short-circuit conditions the generated current is at the highest (I_{sc}), whereas with the circuit open the voltage (V_{OC}) is at the highest. Under the two above mentioned conditions the electric power produced in the cell is null (green line), whereas starting from the short-circuit condition, when the voltage increases, the produced power rises too: after reaching the maximum power point (P_m), the power falls suddenly near to the no-load voltage value.

At first the MPPT algorithm has not been implemented, in the study, setting the MPPT current on a constant value equal to the MPP current in the assumption of a MPPT dynamic slower than those of the power electronic components and of the system itself. In the same way, constant solar irradiation and temperature assumption has been done.

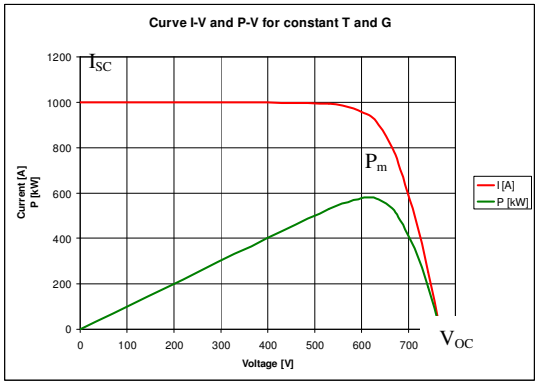

Fig. 3: Curve I-V and P-V for constant Temperature (T) and Solar Irradiation (G)

B. *DC/DC BOOST converter*

The converter placed between the photovoltaic generator and DC bus is a unidirectional chopper. The need for raising or lowering converter derives from the relationship between the DC voltage and PV generator working, considering the variations in relation to different environmental conditions (sunlight and temperature). For the photovoltaic generator the MPP voltage value is 610 V. In particular, in the case under consideration, assuming an inverter DC bus voltage of 800 V, the chopper implemented in the study is a DC/DC BOOST converter.

The PV generator interface converter must ensure the operation at the point voltage - current that corresponds to the maximum output power to ensure the provision of all the available power. A schematic diagram of the DC/DC converter is shown in Fig. 4.

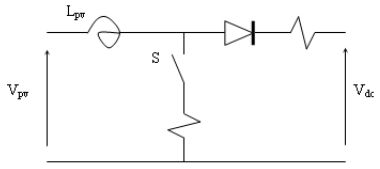

Fig. 4: DC/DC boost converter schematic diagram

The chopper is modulated with a fixed band width current modulation where the current reference is the I_{MPPT} (Fig. 5). The error signal, obtained as the difference between I_{MPPT} and the actual current generated by PV, is compared with the thresholds (±5% I_{MPPT}) and:

- if the PV current (red line) is greater than the superior limit (green line), the valve S is open (brown line lower level) so that the current can flow to the network decreasing and returning to the reference band;
- if the current is less than the lower limit (blue line), S valve is closed (brown line upper level), the voltage V_{pv} is applied to the inductor L_{pv} and the current increases energizing the inductor.

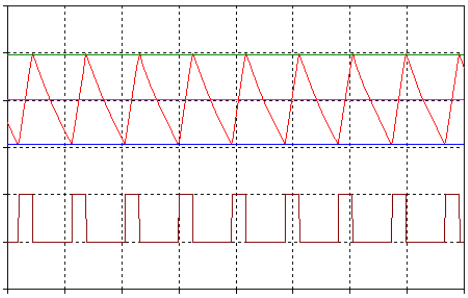

Fig. 5: Chopper modulation: PV current and switching signal

C. *Voltage Source Inverter (VSI)*

To connect the PV system to the network a Voltage Source Inverter has been considered, in particular a two level three phase inverter configuration (Fig. 6) and a fixed band width modulation have been studied.

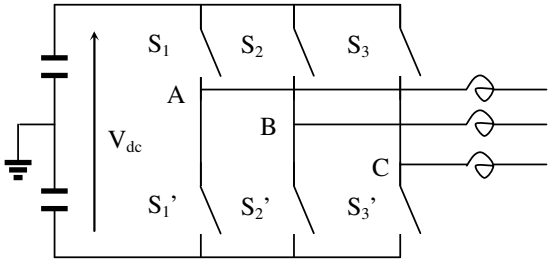

Fig. 6: Two level three phase inverter configuration scheme

The inverter behaves as a current source with respect to the network: in particular its control logic is based on a current control loop to inject an active AC current, whose reference comes from a DC voltage control loop (Fig. 7) to exchange the active power generated by the PV system at its MPP value [4].

The currents reference (I_{ref_a}, I_{ref_b}, I_{ref_c}), in phase with the three phase network voltage (V_a, V_b, V_c), are obtained multiplying these voltages with a gain G that represent the Proportional-Integral regulator output. An easy first order Proportional-Integral (PI) controller has been adopted and the PI regulator parameters have been calculated considering the performance in term of bandwidth (10Hz) and phase margin (75°). In Fig. 8 is shown the PI regulator step response.

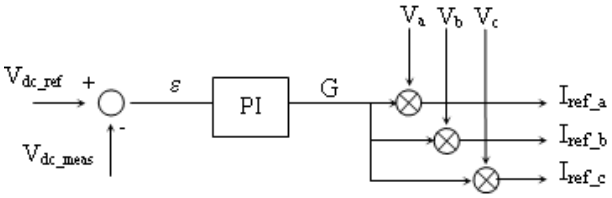

Fig. 7: Inverter DC voltage control loop

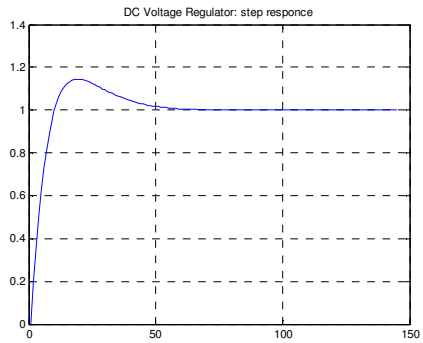

Fig. 8: DC voltage regulator: step response

The inverter currents are modulated with a fixed band width modulation and in particular a band of 10% has been considered. The error signal is obtained from the difference between the actual inverter currents and the reference ones and compared with the thresholds and the switching signals for the IGBT are obtained (Fig. 9 and Fig. 10).

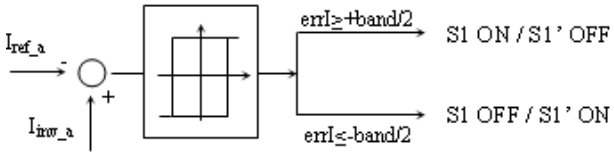

Fig. 9: Inverter current modulation scheme: fixed band width modulation

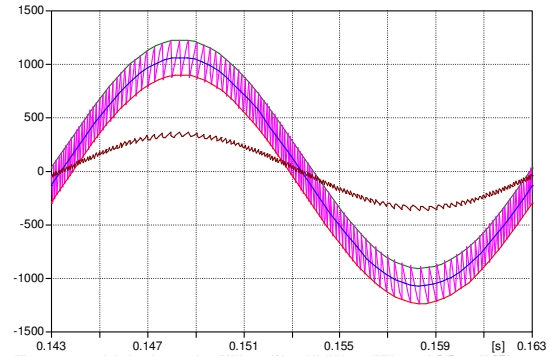

Fig. 10: Maximum (green line) and minimum (red line) band limits, reference (blue line) and inverter (magenta curve) current and network voltage (brown line) waveforms for one phase.

3. Simulations and results

To study the PV power plant behaviour, different kind of three phase voltage dips (different depth, inductive or resistive fault impedance) and different system configuration have been considered.

In particular, the following two configurations have been taken into account:

- without any "external" device or control logic;
- with an "external" device or/and control logic acting during the voltage dip.

In the second configuration, the "external" device is a chopper introduced to limit the DC voltage, since this voltage increases during the dip as a consequence of the active power unbalance between the PV generation and the actual active power exchange with the AC network.

As "external" control logic, the voltage dip detection has been developed to regulate the DG active power flow. In this case, some proposals for the Fault Ride Through have been investigated. Among them the request to avoid any active power flow with the AC network has been implemented [3].

In these studies, it's important first to consider the V_{dc} reaction to the voltage dip. Every voltage dips induces an oscillation in the V_{dc} [5]. During a voltage dip, the PV array inject the same current as before, since the MPPT dynamic is slower and the DC/DC BOOST converter decouples the PV array from the network. In this condition the network voltage is less and so there is an excess of PV active power injected that can't flow to the network and it's absorbed by the buffer capacitor resulting in an instantaneous increase of the DC voltage. The magnitude of this increase depends on the dip depth and the fault impedance type.

Simulations, for different fault types occurring in the MV network, have been performed to illustrate the different behaviours of the two undertaken configurations.

In particular three phase faults have been simulated in the MV network to realize different dip depths (30-60 % V_n) and different network voltage phase shifts (by means of inductive or resistive fault impedance). In the following simulations the "user convention" has been taken into account.

A. Without any "external" devices or control logic

These simulations have the main goal to understand what happen to the inverter during a voltage dip if it remains connected to network without any "external" protection device or control logic.

In particular, in the following, the presented results are relevant to:

1. a three phase fault, with a voltage reduction of 30% and inductive impedance fault;
2. a three phase very deep voltage dip with voltage reduction of 60% and resistive impedance fault causing a voltage phase shift.

Inductive fault with a voltage reduction of 30%V_n

In the first simulation (Fig. 11, Fig. 12, Fig. 13 and Fig. 14), since the fault is not so deep and there isn't any voltage phase shift, the V_{dc} regulator is able to respond to a voltage step quickly and without any drawback to the inverter (Fig. 12).

The inverter output current increase (Fig. 13) to keep the inverter DC voltage at its reference, compensating the active power unbalance between the PV generator and the network. In Fig. 14 the active power magnitude is shown.

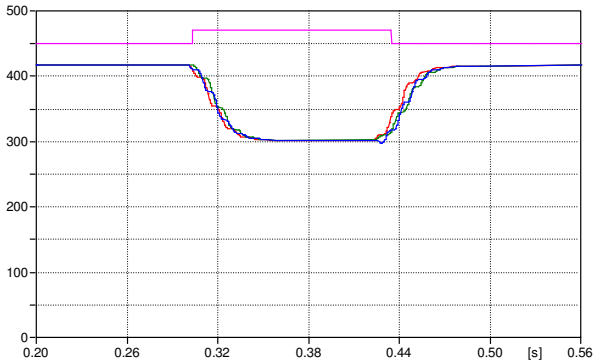

Fig. 11: BT voltage Magnitude with the voltage dip identification signal (magenta line)

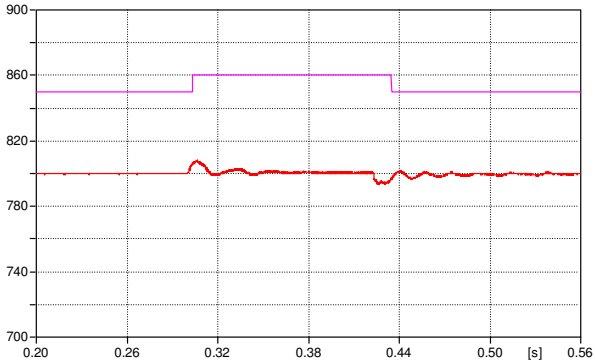

Fig. 12: DC voltage magnitude with the voltage dip identification signal (magenta line)

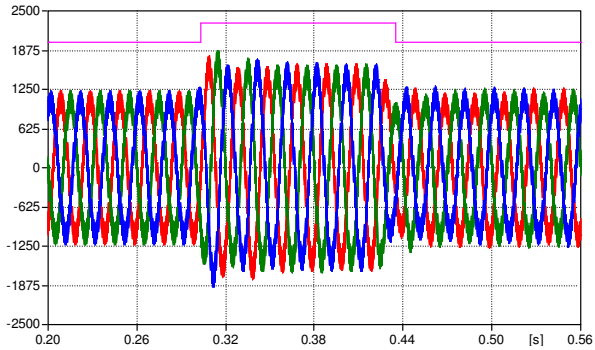

Fig. 13: Inverter Currents waveform generated with the voltage dip identification signal (magenta line)

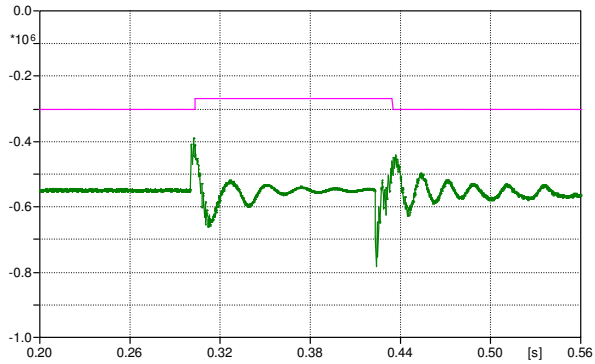

Fig. 14: Magnitude of the active power injected in the network by the PV array + inverter with the voltage dip identification signal (magenta line)

In the simulation of an inductive fault with a voltage reduction of 30%V_n it seems not necessary to apply any

external device or control logic to modify the inverter behaviour during the voltage dip.

Resistive fault with a voltage reduction of 60%V_n

On the contrary, the second simulation shows that during a deep voltage dip the active power injected by PV can't flow to the network and so it's determine the instantaneous increase of the DC voltage. In the extreme hypothesis without any protection devices or logic to limit the maximum V_{dc} and the maximum current that can flow thought the inverter IGBT, the simulation results are shown in Fig. 15, Fig. 16 and Fig. 17.

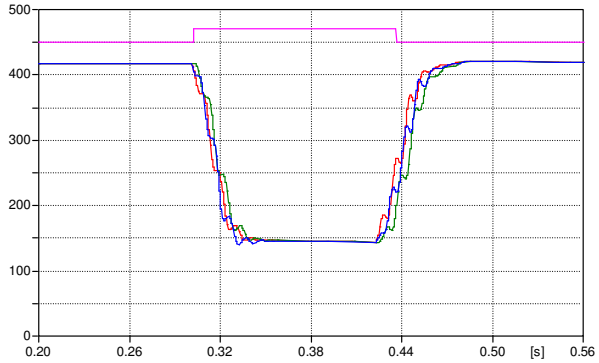

Fig. 15: Magnitude of BT voltages

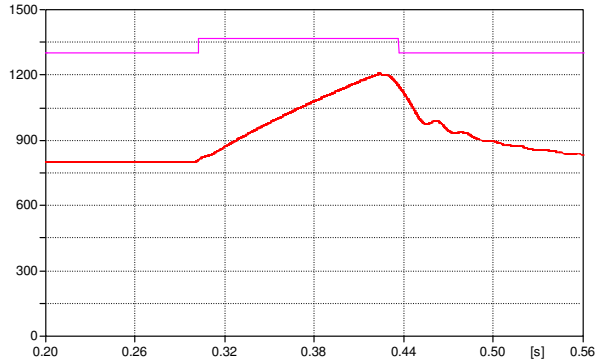

Fig. 16: DC voltage magnitude with the voltage dip identification signal (magenta line)

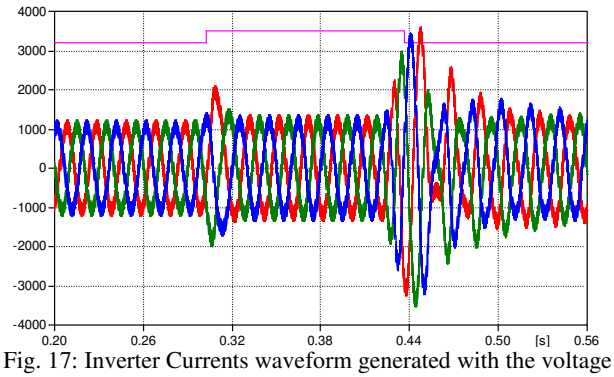

Fig. 17: Inverter Currents waveform generated with the voltage dip identification signal (magenta line)

B. With "external" devices and control logic

Nowadays, new proposals for the Fault Ride Through (FRT) are arising based on the request of maintaining the DG connected to the network during the voltage dip.

Considering the V_{dc} magnitude shown in Fig. 16, it's evident that to fulfil the new requirements it's necessary to provide any "external" device and/or control logic to protect the inverter.

Since the three phase very deep voltage dips with a voltage reduction of 60% in case of resistive impedance, are the heaviest in term of voltage phase shift, only these simulations, to evaluate the external device and the external control logic, have been presented in the following.

In particular, the simulations results are relevant to the presence during the voltage dip of:

- only an "external" device;
- an "external" device and a control logic.

With an "external" device

The "external" device used is a chopper that limits the DC voltage when the inverter design upper limit is exceeded. The simulation results are presented in Fig. 18 ÷ Fig. 21.

The DC magnitude is shown in Fig. 18 with the voltage dip identification signal (magenta line): the V_{dc} variation at the end of the voltage dip depends on the system parameters, in particular the RC damping effect of the circuit involved in the transient.

The V_{dc} regulator output G, during this transient, reaches its threshold value (Fig. 20), limiting the active power flow (Fig. 21) to the network avoiding the balance with the PV generation.

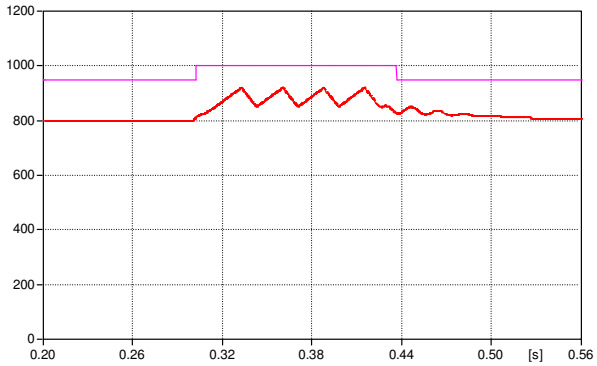

Fig. 18: DC voltage magnitude with the voltage dip identification signal (magenta line)

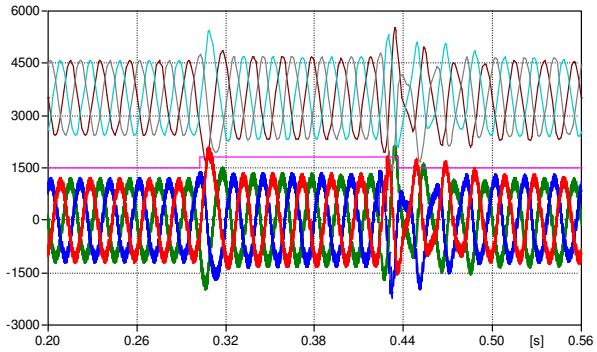

Fig. 19: Inverter current reference waveform (upper curves) and currents generated (lower curves) with the voltage dip identification signal (magenta line)

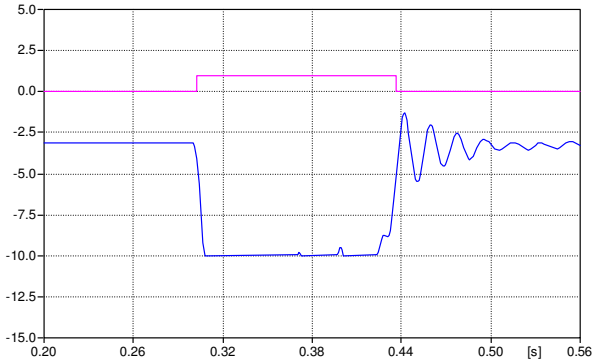

Fig. 20: Magnitude of G with the voltage dip identification signal (magenta line)

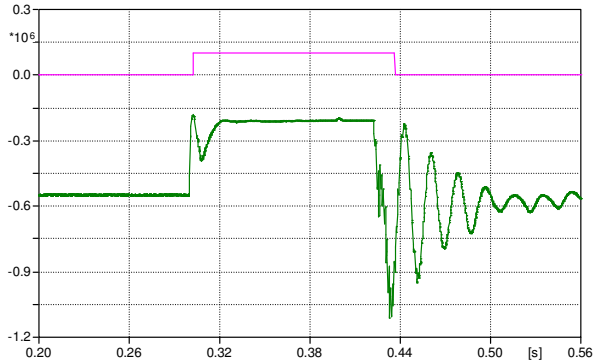

Fig. 21: Magnitude of the active power injected in the network by the PV array + inverter with the voltage dip identification signal (magenta line)

With an "external" device and control logic

The Italian FRT new proposals foreseen that during a voltage dip the DG system has to remain connected to the network without injecting any active power [3]. The control logic to fulfil this condition is to force the V_{dc} regulator output to zero (G=0).

As in the previous case, the chopper acts until the V_{dc} exceeds the upper limit. In this case, through the logic signal that recognize the voltage dip occurs (magenta line), the regulator behaviour has been modified imposing G=0 (Fig. 22). In this way the active power injected in the network and the inverter currents are zero (Fig. 23).

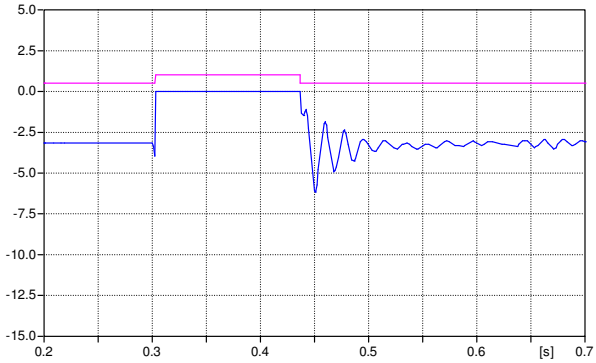

Fig. 22: Magnitude of G with the voltage dip identification signal (magenta line)

4. Conclusion

The developed model done by RSE provided an adequate basis for a general methodology to study different control logics to connect Distributed Generation to the network. In particular new proposals for Fault Ride Through (FRT) have been considered. The aim of these proposals is to avoid the DG system disconnection during voltage dips in the network.

The simulation results have shown that if the PV generator is connected to the network via VSI and DC/DC chopper, the PV array is decoupled from the network and so to avoid the DG system disconnection and to fulfil the FRT requests it's necessary to limit the DC voltage increase due to the active power unbalance between the PV generator and the network. The use of an external device and/or control logic has been studied and simulated put in evidence their effectiveness in achieving the FRT requirements.

Further deeper analysis of these issues will be done in the future to investigate other FRT constrains and different solutions to the possible DG disconnection.

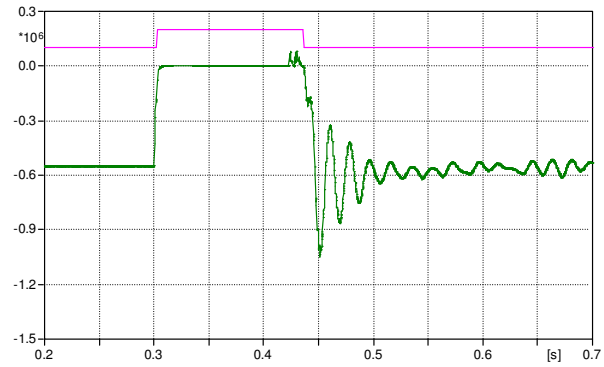

Fig. 23: Magnitude of the active power injected in the network by the PV array + inverter with the voltage dip identification signal (magenta line)

Acknowledgement

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